



# V386

## 8-BIT LVDS RECEIVER FOR VIDEO

### General Description

The V386 is an ideal LVDS receiver that converts 4-pair LVDS data streams into parallel 28 bits of CMOS/TTL data with bandwidth up to 2.38 Gbps throughput or 297.5 Mbytes per second.

This chip is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces through very low-swing LVDS signals.

ICS manufactures a large variety of video application devices. Consult ICS for all of your video application requirements.

### Pin Assignments

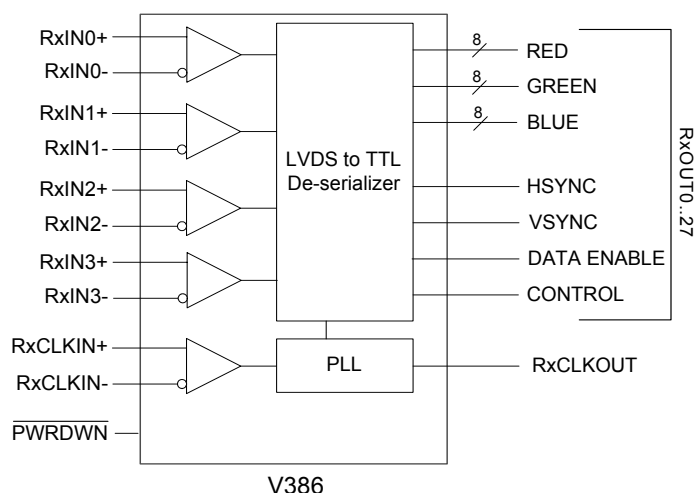
|          |    |    |         |
|----------|----|----|---------|
| RxOUT22  | 1  | 56 | VCC     |
| RxOUT23  | 2  | 55 | RxOUT21 |
| RxOUT24  | 3  | 54 | RxOUT20 |
| GND      | 4  | 53 | RxOUT19 |
| RxOUT25  | 5  | 52 | GND     |
| RxOUT26  | 6  | 51 | RxOUT18 |
| RxOUT27  | 7  | 50 | RxOUT17 |
| LVDS_GND | 8  | 49 | RxOUT16 |
| RxIN0-   | 9  | 48 | VCC     |
| RxIN0+   | 10 | 47 | RxOUT15 |
| RxIN1-   | 11 | 46 | RxOUT14 |
| RxIN1+   | 12 | 45 | RxOUT13 |
| LVDS_VCC | 13 | 44 | GND     |
| LVDS_GND | 14 | 43 | RxOUT12 |
| RxIN2-   | 15 | 42 | RxOUT11 |
| RxIN2+   | 16 | 41 | RxOUT10 |
| RxCLKIN- | 17 | 40 | VCC     |
| RxCLKIN+ | 18 | 39 | RxOUT9  |
| RxIN3-   | 19 | 38 | RxOUT8  |
| RxIN3+   | 20 | 37 | RxOUT7  |
| LVDS_GND | 21 | 36 | GND     |
| PLL_GND  | 22 | 35 | RxOUT6  |
| PLL_VCC  | 23 | 34 | RxOUT5  |
| PLL_GND  | 24 | 33 | RxOUT4  |
| PWRDWN   | 25 | 32 | RxOUT3  |
| RxCLKOUT | 26 | 31 | VCC     |
| RxOUT0   | 27 | 30 | RxOUT2  |
| GND      | 28 | 29 | RxOUT1  |

56-pin TSSOP  
V386

### Features

- Pin and function compatible with the National DS90CF386, Thine THC63LVDF84, TI SN65LVDS94
- Converts 4-pair LVDS data streams into parallel 28 bits of CMOS/TTL data
- Fully spread spectrum compatible
- Wide clock frequency range from 20 MHz to 85 MHz
- Supports VGA, SVGA, XGA, and SXGA
- LVDS voltage swing of 350 mV for low EMI
- On-chip PLL requires no external components
- Low-power CMOS design
- Falling edge clock triggered outputs
- Power-down control function
- Compatible with TIA/EIA-644 LVDS standards
- Packaged in a 56-pin TSSOP (Pb free available)

### Block Diagram





## Pin Descriptions

| Pin | Pin name | Type    | Description                                                                          |
|-----|----------|---------|--------------------------------------------------------------------------------------|
| 1   | RxOUT22  | OUT     | Data outputs on pins (RxOUT0..27)                                                    |
| 2   | RxOUT23  | OUT     | Data outputs on pins (RxOUT0..27)                                                    |
| 3   | RxOUT24  | OUT     | Data outputs on pins (RxOUT0..27)                                                    |
| 4   | GND      | Ground  | Digital ground                                                                       |
| 5   | RxOUT25  | OUT     | Data outputs on pins (RxOUT0..27)                                                    |
| 6   | RxOUT26  | OUT     | Data outputs on pins (RxOUT0..27)                                                    |
| 7   | RxOUT27  | OUT     | Data outputs on pins (RxOUT0..27)                                                    |
| 8   | LVDS_GND | Ground  | Analog ground                                                                        |
| 9   | RxIN0-   | LVDS IN | LVDS input (-)                                                                       |
| 10  | RxIN0+   | LVDS IN | LVDS input (+)                                                                       |
| 11  | RxIN1-   | LVDS IN | LVDS input (-)                                                                       |
| 12  | RxIN1+   | LVDS IN | LVDS input (+)                                                                       |
| 13  | LVDS_VCC | Power   | Analog power                                                                         |
| 14  | LVDS_GND | Ground  | Analog ground                                                                        |
| 15  | RxIN2-   | LVDS IN | LVDS input (-)                                                                       |
| 16  | RxIN2+   | LVDS IN | LVDS input (+)                                                                       |
| 17  | RxCLKIN- | LVDS IN | LVDS input (-)                                                                       |
| 18  | RxCLKIN+ | LVDS IN | LVDS input (+)                                                                       |
| 19  | RxIN3-   | LVDS IN | LVDS input (-)                                                                       |
| 20  | RxIN3+   | LVDS IN | LVDS input (+)                                                                       |
| 21  | LVDS_GND | Ground  | Analog ground                                                                        |
| 22  | PLL_GND  | Ground  | PLL ground                                                                           |
| 23  | PLL_VCC  | Power   | PLL power                                                                            |
| 24  | PLL_GND  | Ground  | PLL ground                                                                           |
| 25  | PWRDWN   | IN      | Power-down control input.<br>H: Normal<br>L: Power down, all outputs are pulled low. |
| 26  | RxCLKOUT | OUT     | Clock output                                                                         |
| 27  | RxOUT0   | OUT     | Data outputs on pins (RxOUT0..27)                                                    |
| 28  | GND      | Ground  | Digital ground                                                                       |
| 29  | RxOUT1   | OUT     | Data outputs on pins (RxOUT0..27)                                                    |
| 30  | RxOUT2   | OUT     | Data outputs on pins (RxOUT0..27)                                                    |
| 31  | VCC      | Power   | Digital power                                                                        |
| 32  | RxOUT3   | OUT     | Data outputs on pins (RxOUT0..27)                                                    |
| 33  | RxOUT4   | OUT     | Data outputs on pins (RxOUT0..27)                                                    |





## V386

### 8-BIT LVDS RECEIVER FOR VIDEO

| Pin | Pin name | Type   | Description                       |
|-----|----------|--------|-----------------------------------|
| 34  | RxOUT5   | OUT    | Data outputs on pins (RxOUT0..27) |
| 35  | RxOUT6   | OUT    | Data outputs on pins (RxOUT0..27) |
| 36  | GND      | Ground | Digital ground                    |
| 37  | RxOUT7   | OUT    | Data outputs on pins (RxOUT0..27) |
| 38  | RxOUT8   | OUT    | Data outputs on pins (RxOUT0..27) |
| 39  | RxOUT9   | OUT    | Data outputs on pins (RxOUT0..27) |
| 40  | VCC      | Power  | Digital power                     |
| 41  | RxOUT10  | OUT    | Data outputs on pins (RxOUT0..27) |
| 42  | RxOUT11  | OUT    | Data outputs on pins (RxOUT0..27) |
| 43  | RxOUT12  | OUT    | Data outputs on pins (RxOUT0..27) |
| 44  | GND      | Ground | Digital ground                    |
| 45  | RxOUT13  | OUT    | Data outputs on pins (RxOUT0..27) |
| 46  | RxOUT14  | OUT    | Data outputs on pins (RxOUT0..27) |
| 47  | RxOUT15  | OUT    | Data outputs on pins (RxOUT0..27) |
| 48  | VCC      | Power  | Digital power                     |
| 49  | RxOUT16  | OUT    | Data outputs on pins (RxOUT0..27) |
| 50  | RxOUT17  | OUT    | Data outputs on pins (RxOUT0..27) |
| 51  | RxOUT18  | OUT    | Data outputs on pins (RxOUT0..27) |
| 52  | GND      | Ground | Digital ground                    |
| 53  | RxOUT19  | OUT    | Data outputs on pins (RxOUT0..27) |
| 54  | RxOUT20  | OUT    | Data outputs on pins (RxOUT0..27) |
| 55  | RxOUT21  | OUT    | Data outputs on pins (RxOUT0..27) |
| 56  | VCC      | Power  | Digital power                     |





## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the V386. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item                                    | Rating                                         |
|-----------------------------------------|------------------------------------------------|
| Supply Voltage, VCC                     | -0.3 V to +4 V                                 |
| CMOS/TTL Output Voltage                 | -0.3 V to (VCC+0.3 V)                          |
| LVDS Receiver Input Voltage             | -0.3 V to (VCC+0.3 V)                          |
| Ambient Operating Temperature           | 0 to +70°C                                     |
| Storage Temperature                     | -65 to +150°C                                  |
| Junction Temperature                    | 150°C                                          |
| Soldering Temperature (10 seconds max.) | 260°C                                          |
| Maximum Package Power                   | 1.61 W (V386)                                  |
| Package Derating                        | 12.4 mW/°C above +25°C<br>15 mW/°C above +25°C |

## Recommended Operation Conditions

| Parameter                               | Min. | Typ. | Max. | Units |
|-----------------------------------------|------|------|------|-------|
| Ambient Operating Temperature (Ta)      | 0    | 25   | 70   | °C    |
| 3.3 V Supply Voltage (VCC)              | 3    | 3.3  | 3.6  | V     |
| Receiver Input Range (V <sub>IN</sub> ) | 0    |      | 2.4  | V     |
| Supply Noise Voltage (V <sub>N</sub> )  |      |      | 100  | mVpp  |

## Electrical Characteristics

VDD=3.3 V ±10%, Ambient temperature 0 to 70°C

| Parameter                         | Symbol          | Conditions                | Min. | Typ.  | Max. | Units |
|-----------------------------------|-----------------|---------------------------|------|-------|------|-------|
| <b>CMOS/TTL DC Specifications</b> |                 |                           |      |       |      |       |
| Input High Voltage                | V <sub>IH</sub> |                           | 2.0  |       | VCC  | V     |
| Input Low Voltage                 | V <sub>IL</sub> |                           | GND  |       | 0.8  | V     |
| Output High Voltage               | V <sub>OH</sub> | I <sub>OH</sub> = -0.4 mA | 2.7  | 3.3   | VCC  | V     |
| Output Low Voltage                | V <sub>OL</sub> | I <sub>OL</sub> = 2 mA    |      | 0.06  | 0.3  | V     |
| Input Clamp Voltage               | V <sub>CL</sub> | I <sub>CL</sub> = -18mA   |      | -0.79 | -1.5 | V     |
| Input Current                     | I <sub>IN</sub> | VCC                       |      |       | ±15  | μA    |





| Parameter                               | Symbol            | Conditions                                                         | Min.  | Typ. | Max. | Units |
|-----------------------------------------|-------------------|--------------------------------------------------------------------|-------|------|------|-------|
|                                         |                   | 0V                                                                 |       |      | ±10  |       |
| Output Short Circuit Current            | I <sub>OS</sub>   | V <sub>OUT</sub> = 0V                                              |       |      | -60  | mA    |
| LVDS Receiver DC Specifications         |                   |                                                                    |       |      |      |       |
| Differential Input High Threshold       | V <sub>TH</sub>   | V <sub>CM</sub> = +1.2 V                                           |       |      | +100 | mV    |
| Differential Input Low Threshold        | V <sub>TL</sub>   |                                                                    | -100  |      |      | mV    |
| Input Current                           | I <sub>IN</sub>   | V <sub>IN</sub> = +2.4 V, VCC = 3.6 V                              |       |      | ±10  | μA    |
|                                         |                   | V <sub>IN</sub> = 0V, VCC = 3.6 V                                  |       |      | ±15  | μA    |
| Receiver Supply Current                 |                   |                                                                    |       |      |      |       |
| Receiver Supply Current (worst case)    | I <sub>CCRW</sub> | C <sub>L</sub> = 8 pF, f = 65 MHz, worst case pattern              |       |      | 220  | mA    |
|                                         |                   | C <sub>L</sub> = 8 pF, f = 85 MHz, worst case pattern              |       |      | 240  | mA    |
| Receiver Supply Current (16 Grayscale)  | I <sub>CCRG</sub> | C <sub>L</sub> = 8 pF, f = 65 MHz, 16 Grayscale pattern            |       |      | 125  | mA    |
|                                         |                   | C <sub>L</sub> = 8 pF, f = 85 MHz, 16 Grayscale pattern            |       |      | 140  | mA    |
| Receiver Supply Current (Power Down)    | I <sub>CCRZ</sub> | Power_Down = Low, Receiver outputs stay low during Power-down mode |       | 140  | 400  | μA    |
| Receiver Switching Characteristics      |                   |                                                                    |       |      |      |       |
| CMOS/TTL Low-to-High Transition Time    | CLHT              | 20% to 80% VCC, C <sub>L</sub> = 8 pF                              |       | 2    | 3.5  | ns    |
| CMOS/TTL High-to-Low Transition Time    | CHLT              | 80% to 20% VCC, C <sub>L</sub> = 8 pF                              |       | 1.8  | 3.5  | ns    |
| CLKOUT period                           | RCOP              |                                                                    | 11.76 | T    | 50   | ns    |
| CLKOUT High Time                        | RCOH              | f = 85 MHz                                                         | 4.5   | 5    | 7    | ns    |
| CLKOUT Low Time                         | RCOL              | f = 85 MHz                                                         | 4     | 5    | 6.5  | ns    |
| Data Setup to CLKOUT                    | RSRC              | f = 85 MHz                                                         | 2.0   |      |      | ns    |
| Data Hold to CLKOUT                     | RHRC              | f = 85 MHz                                                         | 3.5   |      |      | ns    |
| RCK+/- to CLKOUT Delay                  | RCCD              | 25°C / 3.3 V                                                       | 8     | 14   | 20   | ns    |
| Receiver PLL Setup Time                 | RPLLS             |                                                                    |       |      | 10   | ms    |
| Receiver Power Down Delay               | RPDD              |                                                                    |       |      | 1    | μs    |
| Receiver Input Strobe Position for Bit0 | RSPos0            | f = 85 MHz, T = 11.76 ns                                           | 0.49  | 0.84 | 1.19 | ns    |
| Receiver Input Strobe Position for Bit1 | RSPos1            | f = 85 MHz, T = 11.76 ns                                           | 2.17  | 2.52 | 2.87 | ns    |
| Receiver Input Strobe Position for Bit2 | RSPos2            | f = 85 MHz, T = 11.76 ns                                           | 3.85  | 4.2  | 4.55 | ns    |
| Receiver Input Strobe Position for Bit3 | RSPos3            | f = 85 MHz, T = 11.76 ns                                           | 5.53  | 5.88 | 6.23 | ns    |
| Receiver Input Strobe Position for Bit4 | RSPos4            | f = 85 MHz, T = 11.76 ns                                           | 7.21  | 7.56 | 7.91 | ns    |





| Parameter                                | Symbol | Conditions               | Min.  | Typ.  | Max.  | Units |
|------------------------------------------|--------|--------------------------|-------|-------|-------|-------|
| Receiver Input Strobe Position for Bit5  | RSPos5 | f = 85 MHz, T = 11.76 ns | 8.89  | 9.24  | 9.59  | ns    |
| Receiver Input Strobe Position for Bit6  | RSPos6 | f = 85 MHz, T = 11.76 ns | 10.57 | 10.92 | 11.27 | ns    |
| RxIn Skew Margin (see note and Figure 8) | Rskm   | f = 85 MHz, T = 11.76 ns | 300   |       |       | ps    |
|                                          |        | f = 65 MHz, T = 15.38 ns | 500   |       |       | ps    |

Note: The skew margins mean the maximum timing tolerance between the clock and data channel when the receiver still works well. This margin takes into account the receiver input setup and hold time, and internal clock jitter (i.e., internal data sampling window - RSPos). This margin allows for LVDS transmitter pulse position, interconnect skew, inter-symbol interference and intrinsic channel mismatch which will cause the skew between clock (RC+ and RCK-) and data (RX[n]+ and RX[n]- ; n = 0, 1, 2, 3) channels.

## Thermal Characteristics

| Parameter                              | Symbol        | Conditions     | Min. | Typ. | Max. | Units |
|----------------------------------------|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air      |      | 84   |      | °C/W  |
|                                        | $\theta_{JA}$ | 1 m/s air flow |      | 76   |      | °C/W  |
|                                        | $\theta_{JA}$ | 3 m/s air flow |      | 67   |      | °C/W  |
| Thermal Resistance Junction to Case    | $\theta_{JC}$ |                |      | 50   |      | °C/W  |





## Timing Diagrams

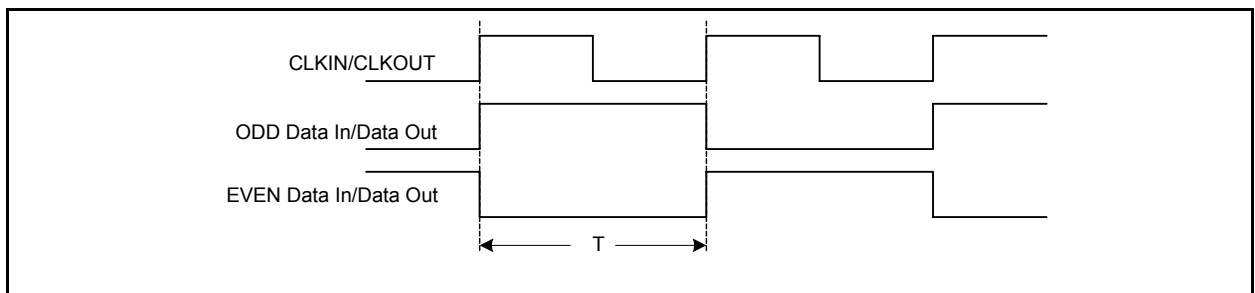


Figure 1a. "Worst Case" Test Pattern

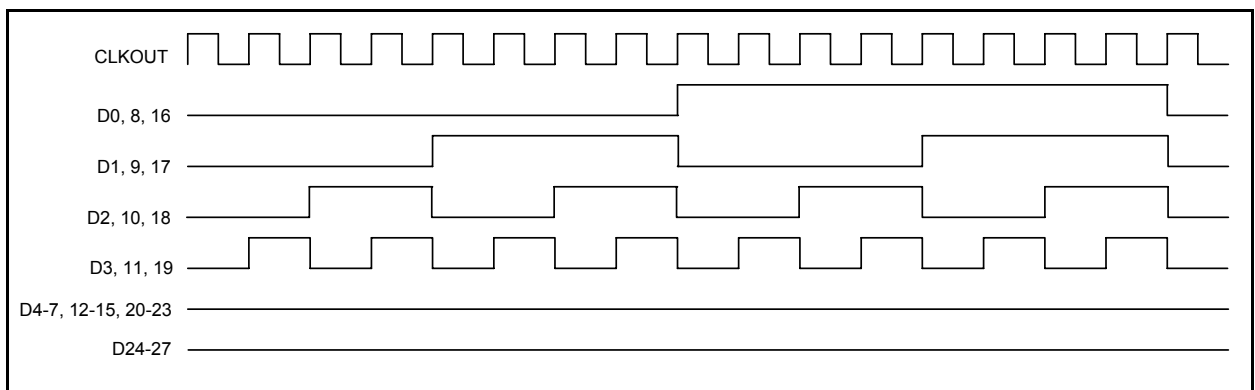


Figure 1b. 16-Grayscale Test-Pattern Waveforms

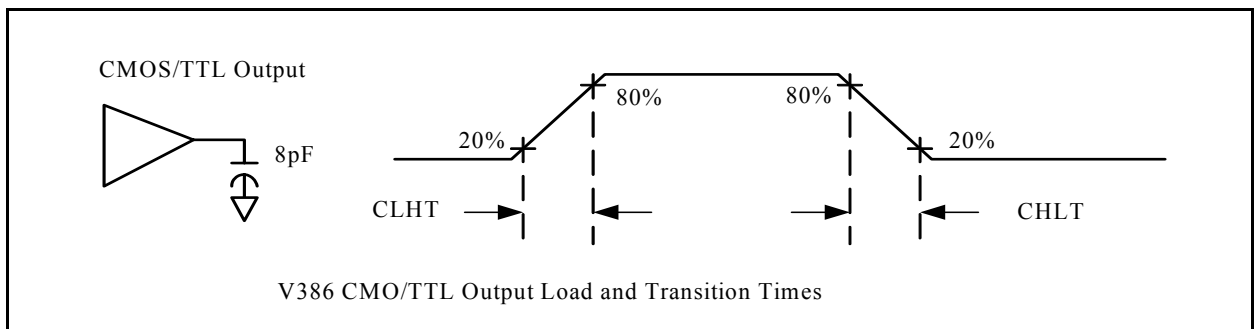


Figure 2. V386 CMOS/TTL Output Load and Transition Time



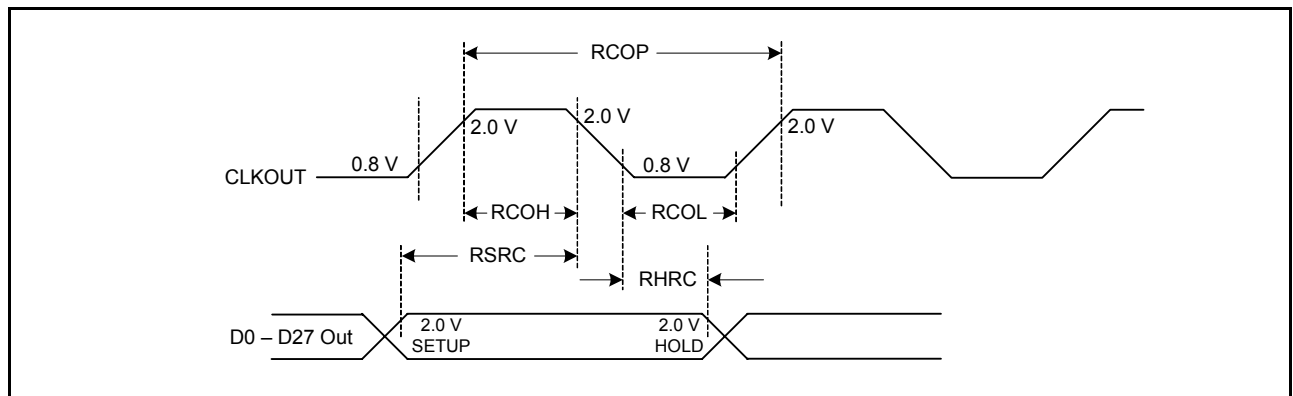


Figure 3. V386 SETUP/HOLD and High/Low Times

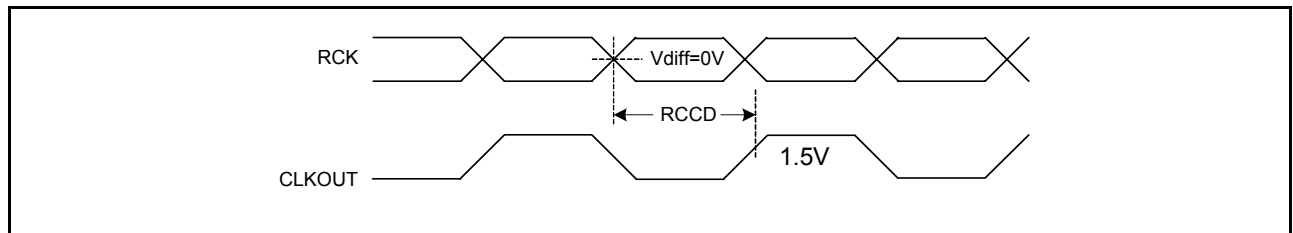


Figure 4. V386 Clock In to Clock Out Delay

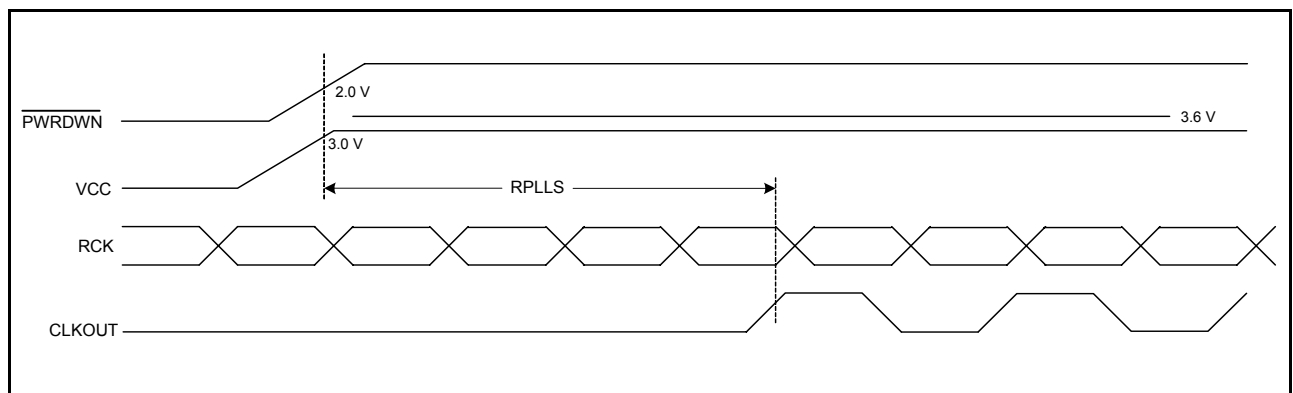


Figure 5. V386 Phase Lock Loop Set Time

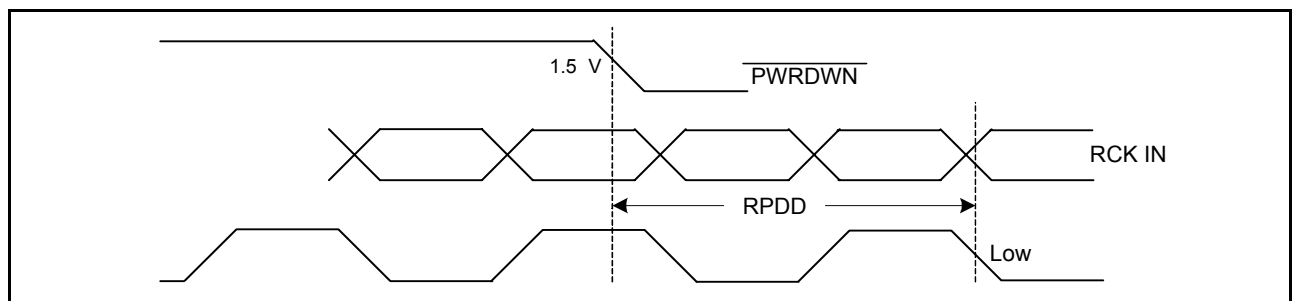


Figure 6. V386 Power Down Delay



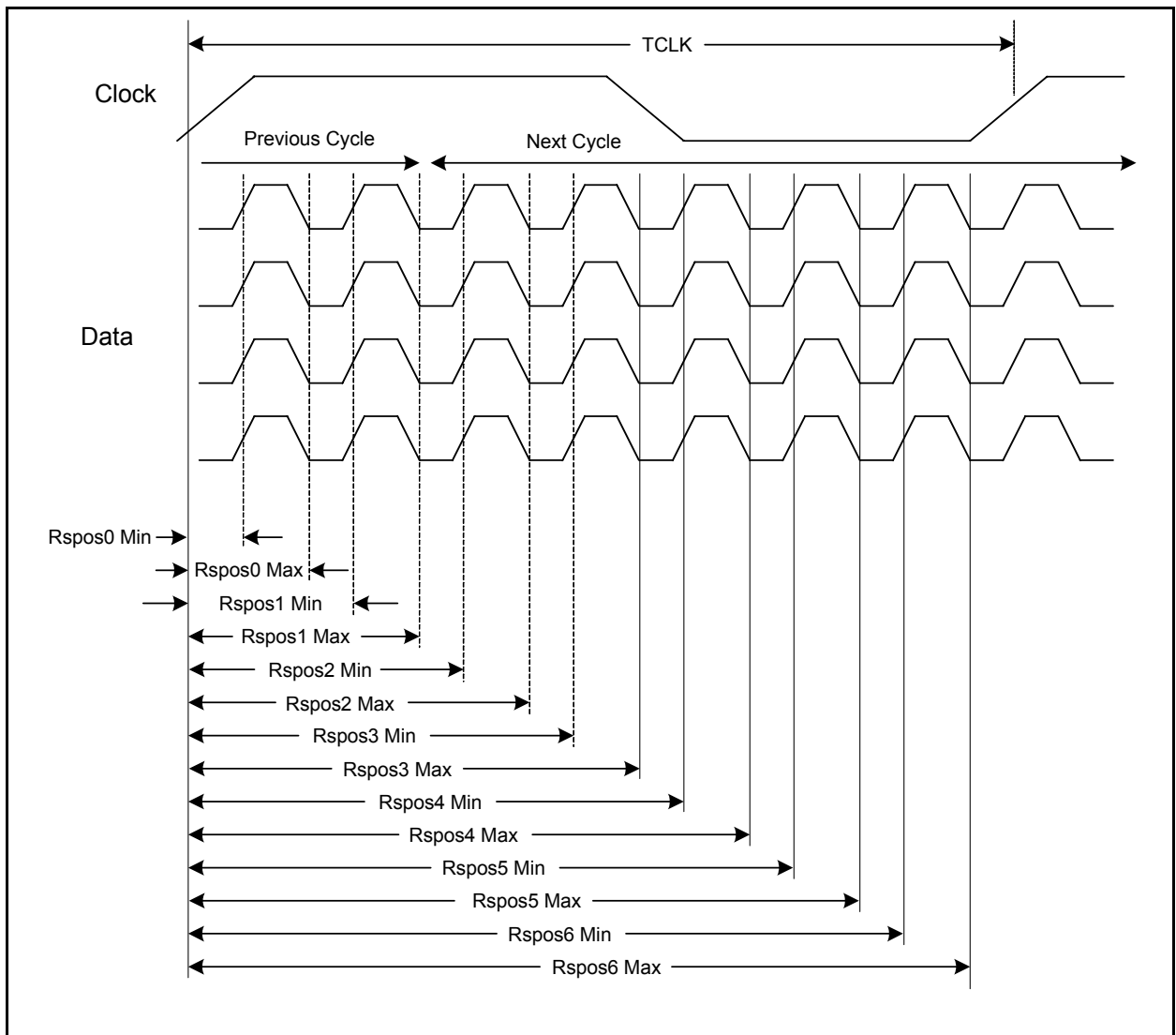


Figure 7. V386 LVDS Input Strobe Position

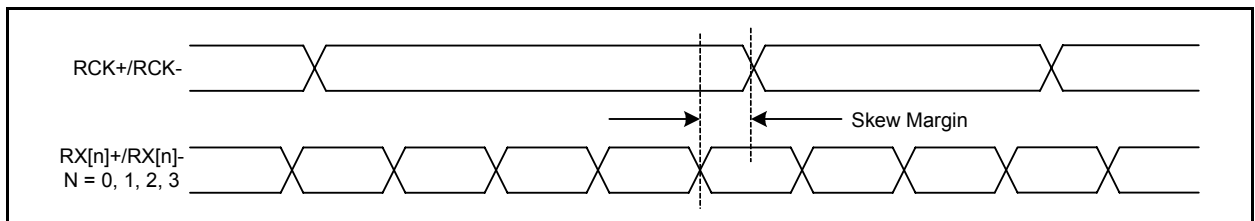


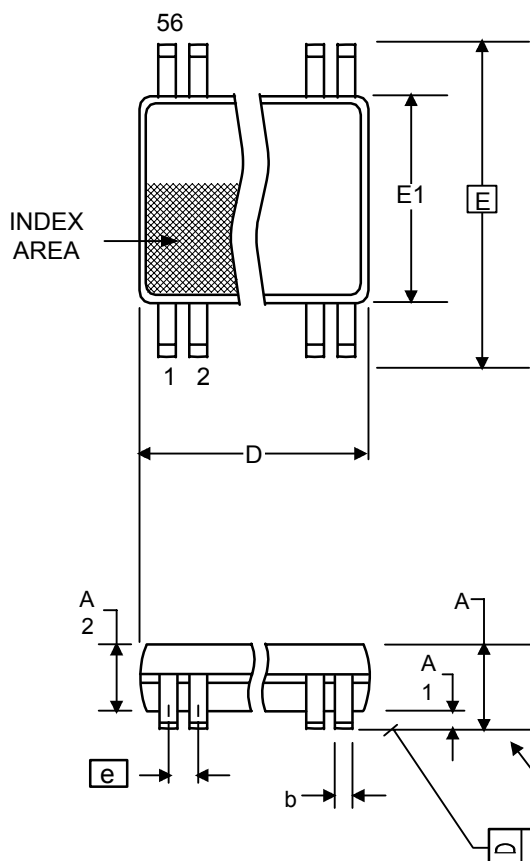
Figure 8. Receiver Input Skew Margin





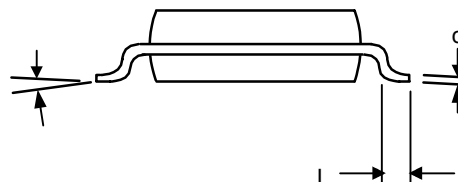
## Package Outline and Package Dimensions (56-pin TSSOP)

Package dimensions are kept current with JEDEC Publication No. 95



|        | Millimeters |       | Inches*     |       |
|--------|-------------|-------|-------------|-------|
| Symbol | Min         | Max   | Min         | Max   |
| A      | —           | 1.20  | —           | 0.047 |
| A1     | 0.05        | 0.15  | 0.002       | 0.006 |
| A2     | 0.80        | 1.05  | 0.032       | 0.041 |
| b      | 0.17        | 0.27  | 0.007       | 0.011 |
| C      | 0.09        | 0.20  | 0.0035      | 0.008 |
| D      | 13.90       | 14.10 | 0.547       | 0.555 |
| E      | 8.10 BASIC  |       | 0.319 BASIC |       |
| E1     | 6.00        | 6.20  | 0.236       | 0.244 |
| e      | 0.50 BASIC  |       | 0.020 BASIC |       |
| L      | 0.45        | 0.75  | 0.018       | 0.030 |
| a      | 0°          | 8°    | 0°          | 8°    |
| aaa    | —           | 0.10  | —           | 0.004 |

\* For reference only. Controlling dimensions in mm.



## Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package      | Temperature |
|---------------------|---------|--------------------|--------------|-------------|
| V386G               | V386G   | Tubes              | 56-pin TSSOP | 0 to +70°C  |
| V386GT              | V386G   | Tape and Reel      | 56-pin TSSOP | 0 to +70°C  |
| V386GLF             | V386GLF | Tubes              | 56-pin TSSOP | 0 to +70°C  |
| V386GLFT            | V386GLF | Tape and Reel      | 56-pin TSSOP | 0 to +70°C  |

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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