iPOWIR™ TECHNOLOGY

Synchronous Buck Multiphase Optimized BGA Power Block

Integrated Power Semiconductors, Drivers & Passives

Features:

- Output current 30A continuous with no derating up to T_{PCB} = 90°C and T_{CASE} = 90°C
- Operating frequency up to 1MHz
- Dual sided heatsink capable
- Very small 11mm x 11mm x 2.6mm profile
- iP2001 footprint compatible
- Internal features minimize layout sensitivity *
- Optimized for very low power losses

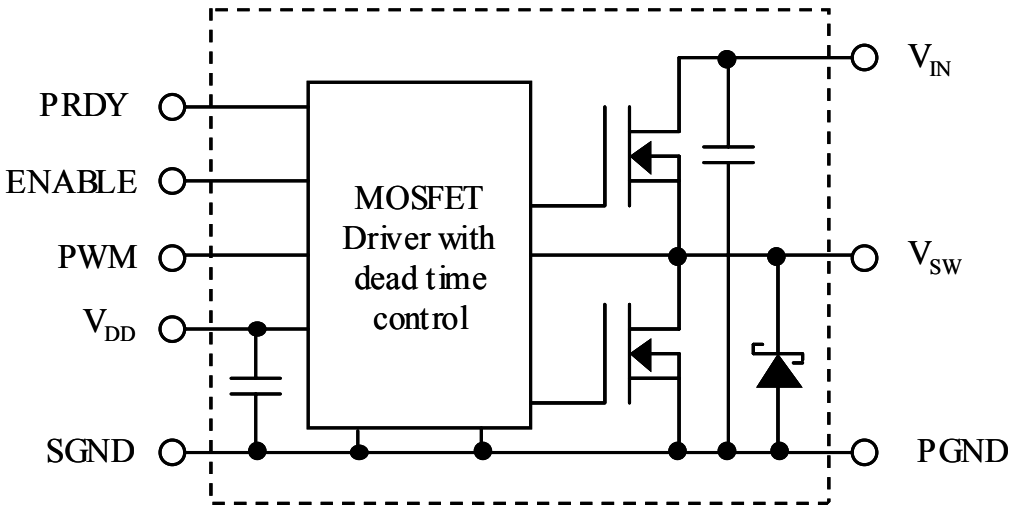
iP2002 Power Block

Description

The iP2002 is a fully optimized solution for high current synchronous buck multiphase applications. Board space and design time are greatly reduced because most of the components required for each phase of a typical discrete-based multiphase circuit are integrated into a single 11mm x 11mm x 2.6mm BGA power block. The only additional components required for a complete multiphase converter are a PWM IC, the external inductors, and the input and output capacitors.

iPOWIR technology offers designers an innovative board space saving solution for applications requiring high power densities. iPOWIR technology eases design for applications where component integration offers benefits in performance and functionality. iPOWIR technology solutions are also optimized internally for layout, heat transfer and component selection.

iP2002 Internal Block Diagram



* All of the difficult PCB layout and bypassing issues have been addressed with the internal design of the iPOWIR Block. There are no concerns about double pulsing, unwanted shutdown, or other malfunctions which often occur in switching power supplies. The iPOWIR Block will function normally without any additional input power supply bypass capacitors. However, for reliable long term operation it is recommended that at least four 10uF ceramic input decoupling capacitors are provided to the V_{IN} pin of each power block. No additional bypassing is required on the V_{DD} pin.

Absolute Maximum Ratings :

Parameter	Min	Typ	Max	Units	Conditions
V_{IN} to PGND	-	-	16	V	
V_{DD} to SGND	-	-	6.0	V	
PWM to SGND	-0.3	-	V_{DD}+0.3	V	not to exceed 6.0V
Enable to SGND	-0.3	-	V_{DD}+0.3	V	not to exceed 6.0V
Output RMS Current	-	-	30	A	
Block Temperature	-40	-	125	°C	

Recommended Operating Conditions :

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	4.6	5.0	5.5	V	
Input Voltage Range	V_{IN}	3.0	-	13.2	V	see Figs. 2 & 3
Output Voltage Range	V_{OUT}	0.9	-	3.3	V	see Figs. 2, 4 & 8
Output Current Range	I_{OUT}	-	-	30	A	see Fig. 2
Operating Frequency	fsw	150	-	1000	kHz	see Figs. 2 & 5
Operating Duty Cycle	D	-	-	85	%	

Electrical Specifications @ V_{DD} = 5V (unless otherwise specified) :

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Block Power Loss ①	P_{BLK}	-	7.2	8.9	W	V_{IN} = 12V, V_{OUT} = 1.3V,
Turn On Delay ②	$t_{d(on)}$	-	63	-	ns	I_{OUT} = 30A, f_{SW} = 1MHz
Turn Off Delay ②	$t_{d(off)}$	-	26	-		
V_{IN} Quiescent Current	I_{Q-VIN}	-	-	1.0	mA	Enable = 0V, V_{IN} = 12V
V_{DD} Quiescent Current	I_{Q-VDD}	-	-	10	µA	Enable = 0V, V_{DD} = 5V
Under-Voltage Lockout	UVLO					
Start Threshold	V_{START}	4.2	4.4	4.5	V	
Hysteresis	$V_{Hys-UVLO}$	-	.05	-		
Enable	Enable					
Input Voltage High	V_{IH}	2.0	-	-	V	
Input Voltage Low	V_{IL}	-	-	0.8		
Power Ready	PRDY					
Logic Level High	V_{OH}	4.5	4.6	-	V	V_{DD} = 4.6V, I_{Load} = 10mA
Logic Level Low	V_{OL}	-	0.1	0.2		V_{DD} < UVLO Threshold, I_{Load} = 1mA
PWM Input	PWM					
Logic Level High	V_{OH}	2.0	-	-	V	
Logic Level Low	V_{OL}	-	-	0.8		

① Measurement were made using four 10uF (TDK C3225X7R1C106M or equiv.) capacitors across the input (see Fig. 8).

② Not associated with the rise and fall times. Does not affect Power Loss (see Fig. 9).