

Data Sheet June 5, 2006 FN662.5

High Frequency NPN Transistor Array

The CA3127 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1GHz, making the CA3127 useful from DC to 500MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127 provides close electrical and thermal matching of the five transistors.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG.#
CA3127M	CA3127	-55 to 125	16 Ld SOIC	M16.15
CA3127MZ (Note)	CA3127MZ	-55 to 125	16 Ld SOIC (Pb-free)	M16.15

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

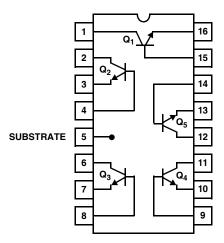
- Gain Bandwidth Product (f_T)>1GHz
 Power Gain30dB (Typ) at 100MHz
- Noise Figure 3.5dB (Typ) at 100MHz
- Five Independent Transistors on a Common Substrate
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- VHF Amplifiers
- Multifunction Combinations RF/Mixer/Oscillator
- · Sense Amplifiers
- Synchronous Detectors
- VHF Mixers
- IF Converter
- IF Amplifiers
- · Synthesizers
- · Cascade Amplifiers

Pinout

CA3127 (SOIC) TOP VIEW



Absolute Maximum Ratings

The following ratings apply for each transistor in the device	
Collector-to-Emitter Voltage, V _{CEO} 15	δ۷
Collector-to-Base Voltage, V _{CBO}	J۷
Collector-to-Substrate Voltage, V _{CIO} (Note 1)	J۷
Collector Current Io 20m	ıA

Operating Conditions

Temperature Range.....-55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ _{JA} (°C/W)
SOIC Package	120
Maximum Power Dissipation, P _D (Any One Transistor).	
Maximum Junction Temperature (Die)	175°C
Maximum Junction Temperature (Plastic Packages)	150°C
Maximum Storage Temperature Range65	5°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC - Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- 1. The collector of each transistor of the CA3127 is isolated from the substrate by an integral diode. The substrate (Terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
- 2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25$ °C

PARAMETER	TEST	TEST CONDITIONS		TYP	MAX	UNITS
DC CHARACTERISTICS (For Each Transistor)	<u>.</u>					
Collector-to-Base Breakdown Voltage	$I_C = 10\mu A, I_E = 0$	$I_{C} = 10\mu A, I_{E} = 0$		32	-	V
Collector-to-Emitter Breakdown Voltage	$I_C = 1mA$, $I_B = 0$		15	24	-	V
Collector-to-Substrate Breakdown-Voltage	$I_{C1} = 10\mu A, I_B = 0$, I _E = 0	20	60	-	V
Emitter-to-Base Breakdown Voltage (Note 3)	$I_E = 10\mu A, I_C = 0$		4	5.7	-	V
Collector-Cutoff-Current	V _{CE} = 10V I _B = 0		-	-	0.5	μА
Collector-Cutoff-Current	V _{CB} = 10V, I _E = 0		-	-	40	nA
DC Forward-Current Transfer Ratio	V _{CE} = 6V	$I_C = 5mA$	35	88	-	
		I _C = 1mA	40	90	-	
		$I_C = 0.1 \text{mA}$	35	85	-	
Base-to-Emitter Voltage	V _{CE} = 6V	$I_C = 5mA$	0.71	0.81	0.91	V
		I _C = 1mA	0.66	0.76	0.86	V
		$I_C = 0.1 \text{mA}$	0.60	0.70	0.80	V
Collector-to-Emitter Saturation Voltage	I _C = 10mA, I _B = 1	I _C = 10mA, I _B = 1mA		0.26	0.50	V
Magnitude of Difference in V _{BE}		Q_1 and Q_2 Matched $V_{CE} = 6V$, $I_C = 1mA$		0.5	5	mV
Magnitude of Difference in I _B	$V_{CE} = 6V, I_C = 1m$			0.2	3	μА
DYNAMIC CHARACTERISTICS	1					
Noise Figure	f = 100kHz, R _S =	f = 100kHz, $R_S = 500Ω$, $I_C = 1mA$		2.2	-	dB
Gain-Bandwidth Product	$V_{CE} = 6V, I_{C} = 5m$	$V_{CE} = 6V$, $I_C = 5mA$		1.15	-	GHz
Collector-to-Base Capacitance	V _{CB} = 6V, f = 1MH	$V_{CB} = 6V, f = 1MHz$		See Fig.	-	pF
Collector-to-Substrate Capacitance	V _{CI} = 6V, f = 1MH	V _{CI} = 6V, f = 1MHz			-	pF
Emitter-to-Base Capacitance	V _{BE} = 4V, f = 1MHz		-	_	-	pF
Voltage Gain	V _{CE} = 6V, f = 10M	$V_{CE} = 6V$, $f = 10MHz$, $R_L = 1k\Omega$, $I_C = 1mA$		28	-	dB
Power Gain		Cascode Configuration		30	-	dB
Noise Figure	$f = 100MHz, V+ = 12V, I_C = 1mA$		-	3.5	-	dB

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Electrical Specifications T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Resistance	Common-Emitter Configuration	-	400	-	Ω
Output Resistance	$V_{CE} = 6V$, $I_{C} = 1mA$, $f = 200 \text{ MHz}$	-	4.6	-	kΩ
Input Capacitance		-	3.7	=	pF
Output Capacitance		-	2	-	pF
Magnitude of Forward Transadmittance		-	24	-	mS

NOTE:

3. When used as a zener for reference voltage, the device must not be subjected to more than 0.1mJ of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10mA.

Test Circuits

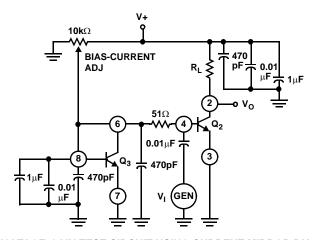


FIGURE 1. VOLTAGE-GAIN TEST CIRCUIT USING CURRENT-MIRROR BIASING FOR $\mathbf{Q}_{\mathbf{2}}$

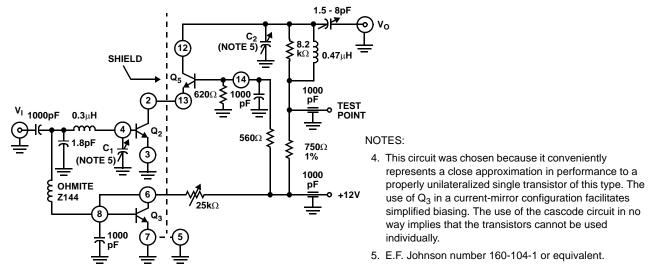


FIGURE 2. 100MHz POWER-GAIN AND NOISE-FIGURE TEST CIRCUIT

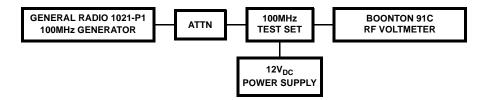


FIGURE 3A. POWER GAIN SET-UP

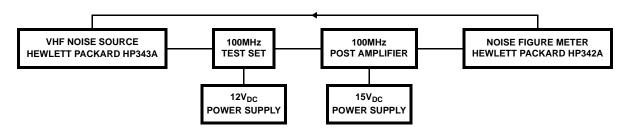


FIGURE 3B. NOISE FIGURE SET-UP
FIGURE 3. BLOCK DIAGRAMS OF POWER-GAIN AND NOISE-FIGURE TEST SET-UPS

Typical Performance Curves

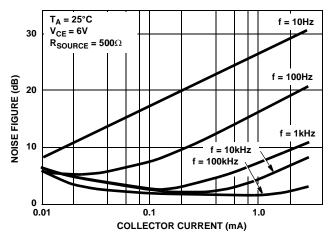


FIGURE 4. NOISE FIGURE vs COLLECTOR CURRENT

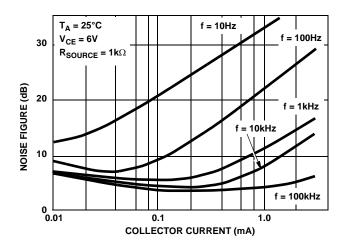


FIGURE 5. NOISE FIGURE vs COLLECTOR CURRENT

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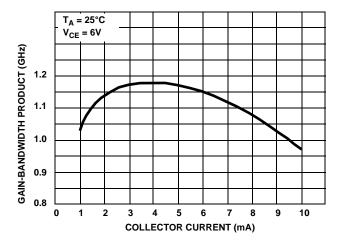


FIGURE 6. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT

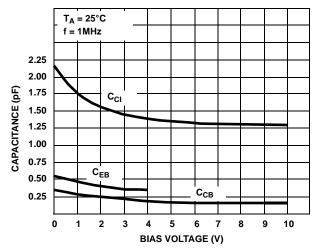


FIGURE 8A. CAPACITANCE vs BIAS VOLTAGE FOR Q2

5

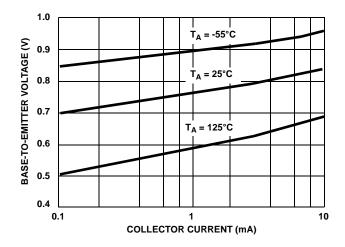


FIGURE 7. BASE-TO-EMITTER VOLTAGE vs COLLECTOR CURRENT

	CAPACITANCE (pF)							
	C	СВ	B C _{CE}		C _{EB}		C _{CI}	
TRAN- SISTOR	PKG	TOTAL	PKG	TOTAL	PKG	TOTAL	PKG	TOTAL
BIAS (V)	-	6V	-	6V	-	4V	-	6V
Q ₁	0.025	0.190	0.090	0.125	0.365	0.610	0.475	1.65
Q ₂	0.015	0.170	0.225	0.265	0.130	0.360	0.085	1.35
Q_3	0.040	0.200	0.215	0.240	0.360	0.625	0.210	1.40
Q ₄	0.040	0.190	0.225	0.270	0.365	0.610	0.085	1.25
Q ₅	0.010	0.165	0.095	0.115	0.140	0.365	0.090	1.35

FIGURE 8B. TYPICAL CAPACITANCE VALUES AT f = 1MHz.
THREE TERMINAL MEASUREMENT. GUARD ALL
TERMINALS EXCEPT THOSE UNDER TEST.

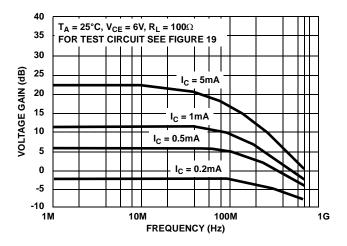


FIGURE 9. VOLTAGE GAIN vs FREQUENCY

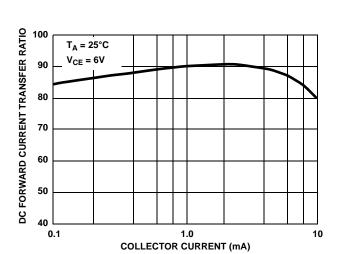


FIGURE 11. DC FORWARD-CURRENT TRANSFER RATIO (h_{FE}) vs COLLECTOR CURRENT

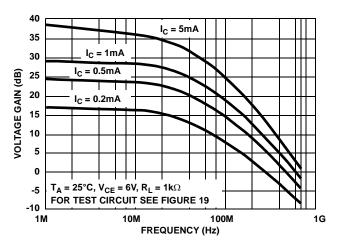


FIGURE 10. VOLTAGE GAIN vs FREQUENCY

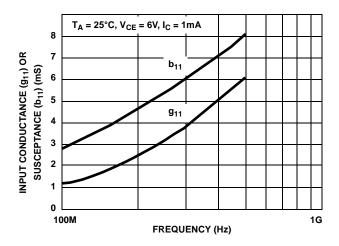


FIGURE 12. INPUT ADMITTANCE (Y₁₁) vs FREQUENCY

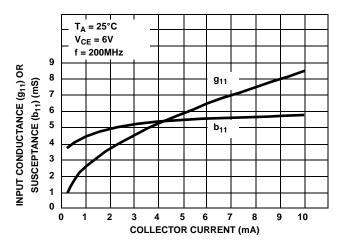


FIGURE 13. INPUT ADMITTANCE (Y₁₁) vs COLLECTOR CURRENT

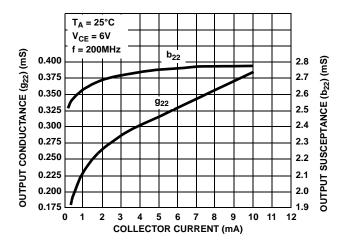


FIGURE 15. OUTPUT ADMITTANCE (Y₂₂) vs COLLECTOR CURRENT

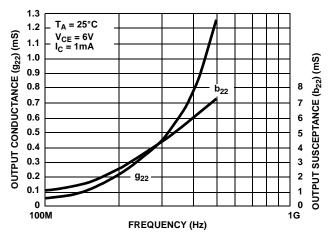


FIGURE 14. OUTPUT ADMITTANCE (Y22) vs FREQUENCY

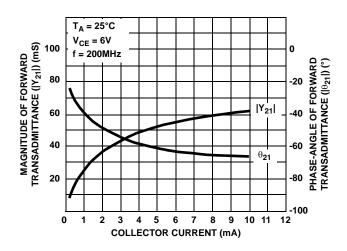


FIGURE 16. FORWARD TRANSADMITTANCE (Y₂₁) vs COLLECTOR CURRENT

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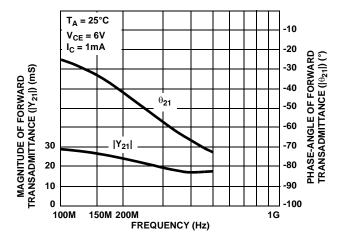


FIGURE 17. FORWARD TRANSADMITTANCE (Y_{21}) vs FREQUENCY

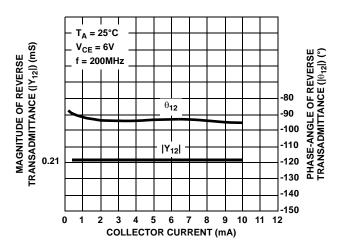


FIGURE 18. REVERSE TRANSADMITTANCE (Y_{12}) vs COLLECTOR CURRENT

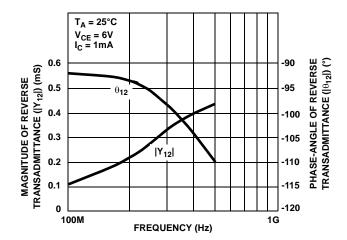
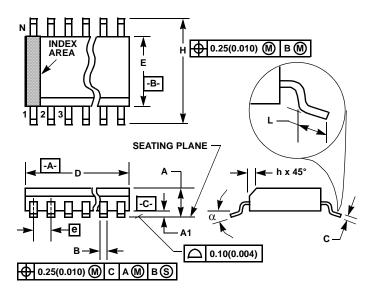


FIGURE 19. REVERSE TRANSADMITTANCE (Y₁₂) vs FREQUENCY

Small Outline Plastic Packages (SOIC)



NOTES:

- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
- 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- 4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
- 5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- 6. "L" is the length of terminal for soldering to a substrate.
- 7. "N" is the number of terminal positions.
- 8. Terminal numbers are shown for reference only.
- The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
- Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

	INCHES		MILLIN		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
В	0.013	0.020	0.33	0.51	9
С	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
Е	0.1497	0.1574	3.80	4.00	4
е	0.050 BSC		1.27 BSC		-
Н	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		1	6	7
α	0°	8°	0°	8°	-

Rev. 1 6/05

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