Proximity Sensor with Intelligent Interrupt and Sleep Modes

ISL29027

The ISL29027 is an integrated infrared light-to-digital converter with a built-in IR LED driver and I^2C Interface (SMBus Compatible). The flexible interrupt scheme is designed for minimal microcontroller utilization.

For proximity sensor (Prox) data conversions, the built-in driver turns on an external infrared LED and the proximity sensor ADC converts the reflected IR intensity to digital. This ADC rejects ambient IR noise (such as sunlight) and has a 540µs conversion time.

The ISL29027 provides proximity sensing with a typical 138µA normal operation current (110µA for sensors and internal circuitry, ~28µA for external LED) with 220mA current pulses for a net 100µs, repeating every 800ms (or under).

The ISL29027 uses both a hardware pin and software bits to indicate an interrupt event has occurred. A proximity interrupt is defined as a measurement over a threshold limit. The user may also require that proximity interrupts occur at once, up to 16 times in a row before activating the interrupt pin.

The ISL29027 is designed to operate from 2.25V to 3.63V over the -40°C to +85°C ambient temperature range. It is packaged in a clear, lead-free 8 lead ODFN package.

Applications

- Mobile Devices: Smart Phone, PDA, GPS
- Computing Devices: Laptop PC, Netbook
- Consumer Devices: LCD-TV, Digital Picture Frame, Digital Camera

Features

- Works Under All Light Sources Including Sunlight
- Intelligent Interrupt Scheme Simplifies µC Code

Proximity Sensing

- Proximity Sensor with Broad IR Spectrum
  - Can Use 850nm and 950nm External IR LEDs
- IR LED Driver with I^2C Programmable Sink Currents
  - Net 100µs Pulse with 110mA or 220mA Amplitudes
  - Periodic Sleep Time up to 800ms Between Pulses
- Ambient IR Noise Cancellation (Including Sunlight)

Intelligent and Flexible Interrupts

- Proximity Interrupt Thresholds
- Adjustable Interrupt Persistency
  - 1/4/8/16 Consecutive Triggers Required Before Interrupt

Ultra Low Power

- 138µA DC Typical Supply Current for Prox Sensing
  - 110µA for Sensors and Internal Circuitry
  - 28µA Typical Current for External IR LED (Assuming 220mA for 100µs Every 800ms)
- <1.0µA Supply Current When Powered Down

Easy to Use

- Set Registers; Wait for Interrupt
- I^2C (SMBus Compatible) Output
- Temperature Compensated
- Tiny ODFN8 2.0x2.1x0.7 (mm) Package

Additional Features

- 1.7V to 3.63V Supply for I^2C Interface
- 2.25V to 3.63V Sensor Power Supply
- Pb-Free (RoHS Compliant)
- I^2C Address Selection Pin

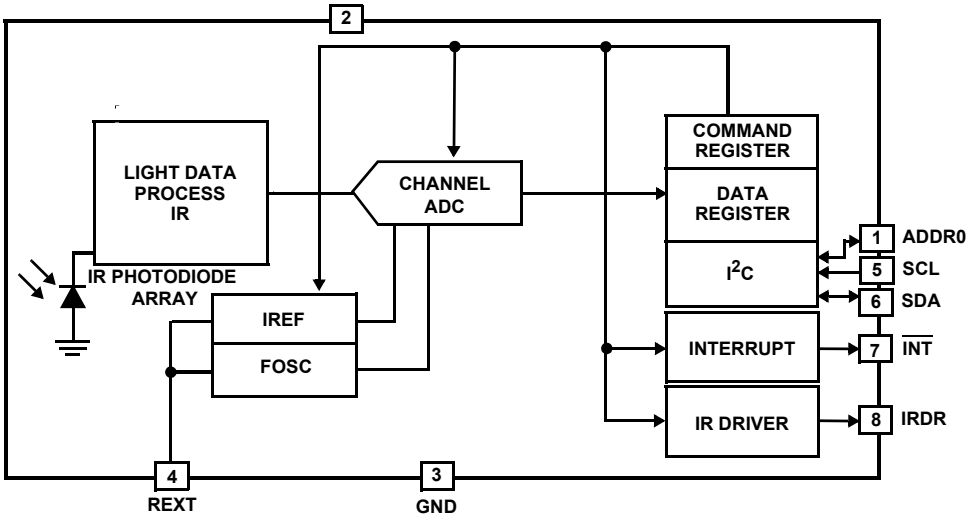

FIGURE 1. BLOCK DIAGRAM

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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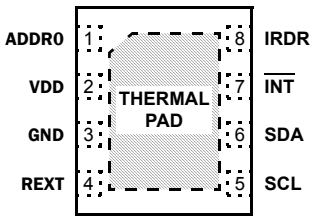
Pin Configuration

ISL29027
8 LD ODFN (2.0mmx2.1mmx0.7mm)
TOP VIEW



*THERMAL PAD CAN BE CONNECTED TO GND OR ELECTRICALLY ISOLATED

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION	
0	T.PAD	Thermal Pad (connect to GND or float)	
1	ADDR0	I^2C address pin - pull high or low (do not float)	
2	VDD	Positive supply: 2.25V to 3.63V	
3	GND	Ground	
4	REXT	External resistor (499kΩ; 1%) connects this pin to ground	
5	SCL	I^2C clock line	The I^2C bus lines can be pulled from 1.7V to above V_{DD}, 3.63V max
6	SDA	I^2C data line	
7	$\overline{INT}$	$\overline{Interrupt}$ pin; Logic output (open-drain) for interrupt	
8	IRDR	IR LED driver pin - current flows into ISL29027 from LED cathode	

Ordering Information

PART NUMBER (Notes 1, 2, 3)	TEMP. RANGE (°C)	PACKAGE Tape & Reel (Pb-free)	PKG. DWG. #
ISL29027IR0Z-T7	-40 to +85	8 Ld ODFN	L8.2.1x2.0

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL29027. For more information on MSL, please see Technical Brief TB477.

Absolute Maximum Ratings (T_A = +25°C)

V_{DD} Supply Voltage between V_{DD} and GND 4.0V
I^2C Bus Pin Voltage (SCL, SDA) . . . . . -0.5V to 4.0V
I^2C Bus Pin Current (SCL, SDA) . . . . . <10mA
R_{EXT} Pin Voltage . . . . . -0.5V to VDD + 0.5V
IRDR Pin Voltage 5.5V
ADDR0 Pin Voltage . . . . . -0.5V to VDD + 0.5V
INT Pin Voltage . . . . . -0.5V to 4.0V
INT Pin Current . . . . . <10mA
ESD Rating
Human Body Model (Note 6) 2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld ODFN Package (Notes 4, 5)	88	10

Maximum Die Temperature . . . . . +90°C
Storage Temperature . . . . . -40°C to +100°C
Operating Temperature . . . . . -40°C to +85°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. ESD on all pins is 2kV except for IRDR, which is 1.5kV.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications V_{DD} = 3.0V, T_A = +25°C, R_{EXT} = 499kΩ 1% tolerance.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
V_{DD}	Power Supply Range		2.25	3.0	3.63	V
SR_V_{DD}	Input Power-up Slew Rate	V_{DD} Rising Edge between 0.4V and 2.25V	0.5			V/ms
I_{DD_OFF}	Supply Current when Powered Down	PROX_EN = 0		0.1	0.8	µA
$I_{DD\_PRX\_SLP}$	Supply Current for Prox in Sleep Time	PROX_EN = 1		80		µA
f_{OSC}	Internal Oscillator Frequency			5.25		MHz
t_{INTGR_PROX}	8-bit Prox Integration/Conversion Time			0.54		ms
$DATA_{PROX\_0}$	Prox Measurement w/o Object in Path			1	2	Counts
$DATA_{PROX\_F}$	Full Scale Prox ADC Code				255	Counts
$DATA_{PROX\_1}$	Prox Measurement Result	(Note 7)	36	46	56	Counts
t_r	Rise Time for IRDR Sink Current	R_{LOAD} = 15Ω at IRDR pin, 20% to 80%		500		ns
t_f	Fall time for IRDR Sink Current	R_{LOAD} = 15Ω at IRDR pin, 80% to 20%		500		ns
I_{IRDR_0}	IRDR Sink Current	PROX_DR = 0; V_{IRDR} = 0.5V	95	110	125	mA
I_{IRDR_1}	IRDR Sink Current	PROX_DR = 1; V_{IRDR} = 0.5V		220		mA
I_{IRDR_LEAK}	IRDR Leakage Current	PROX_EN = 0; V_{DD} = 3.63V (Note 8)		0.001	1	µA
V_{IRDR}	Acceptable Voltage Range on IRDR Pin	Register bit PROX_DR = 0	0.5		4.3	V
t_{PULSE}	Net I_{IRDR} On Time Per PROX Reading			100		µs
V_{REF}	Voltage of R_{EXT} Pin			0.51		V
F_{I2C}	I^2C Clock Rate Range				400	kHz
V_{I2C}	Supply Voltage Range for I^2C Interface		1.7		3.63	V
V_{IL}	SCL and SDA Input Low Voltage				0.55	V
V_{IH}	SCL and SDA Input High Voltage		1.25			V
I_{SDA}	SDA Current Sinking Capability	V_{OL} = 0.4V	3	5		mA
$I_{\overline{INT}}$	$\overline{INT}$ Current Sinking Capability	V_{OL} = 0.4V	3	5		mA

Electrical Specifications V_{DD} = 3.0V, T_A = +25°C, R_{EXT} = 499kΩ 1% tolerance. (Continued)

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
$PSRR_{IRDR}$	$(\Delta I_{IRDR})/(\Delta V_{IRDR})$	PROX_DR = 0; V_{IRDR} = 0.5V to 4.3V		4		mA/V

NOTES:

7. An 850nm infrared LED is used to test PROX/IR sensitivity in an internal test mode.
8. Ability to guarantee I_{IRDR} leakage of ~1nA is limited by test hardware..
9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

I^2C Electrical Specifications For SCL and SDA unless otherwise noted, V_{DD} = 3V, T_A = +25°C, R_{EXT} = 499kΩ 1% tolerance (Note 10).

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V_{I2C}	Supply Voltage Range for I^2C Interface		1.7		3.63	V
f_{SCL}	SCL Clock Frequency				400	kHz
V_{IL}	SCL and SDA Input Low Voltage				0.55	V
V_{IH}	SCL and SDA Input High Voltage		1.25			V
V_{hys}	Hysteresis of Schmitt Trigger Input		$0.05V_{DD}$			V
V_{OL}	Low-level Output Voltage (Open-drain) at 4mA Sink Current				0.4	V
I_i	Input Leakage for each SDA, SCL Pin		-10		10	µA
t_{SP}	Pulse Width of Spikes that must be Suppressed by the Input Filter				50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid				900	ns
C_i	Capacitance for each SDA and SCL Pin				10	pF
$t_{HD:STA}$	Hold Time (Repeated) START Condition	After this period, the first clock pulse is generated	600			ns
t_{LOW}	LOW Period of the SCL Clock	Measured at the 30% of VDD crossing	1300			ns
t_{HIGH}	HIGH period of the SCL Clock		600			ns
$t_{SU:STA}$	Set-up Time for a Repeated START Condition		600			ns
$t_{HD:DAT}$	Data Hold Time		30			ns
$t_{SU:DAT}$	Data Set-up Time		100			ns
t_R	Rise Time of both SDA and SCL Signals	(Note 11)	$20 + 0.1xC_b$			ns
t_F	Fall Time of both SDA and SCL Signals	(Note 11)	$20 + 0.1xC_b$			ns
$t_{SU:STO}$	Set-up Time for STOP Condition		600			ns
t_{BUF}	Bus Free Time Between a STOP and START Condition		1300			ns
C_b	Capacitive Load for Each Bus Line				400	pF
$R_{pull-up}$	SDA and SCL System Bus Pull-up Resistor	Maximum is determined by t_R and t_F	1			kΩ
$t_{VD;DAT}$	Data Valid Time				0.9	µs
$t_{VD:ACK}$	Data Valid Acknowledge Time				0.9	µs
V_{nL}	Noise Margin at the LOW Level		0.1VDD			V
V_{nH}	Noise Margin at the HIGH Level		0.2VDD			V

NOTES:

10. All parameters in I^2C Electrical Specifications table are guaranteed by design and simulation.
11. Cb is the capacitance of the bus in pF.

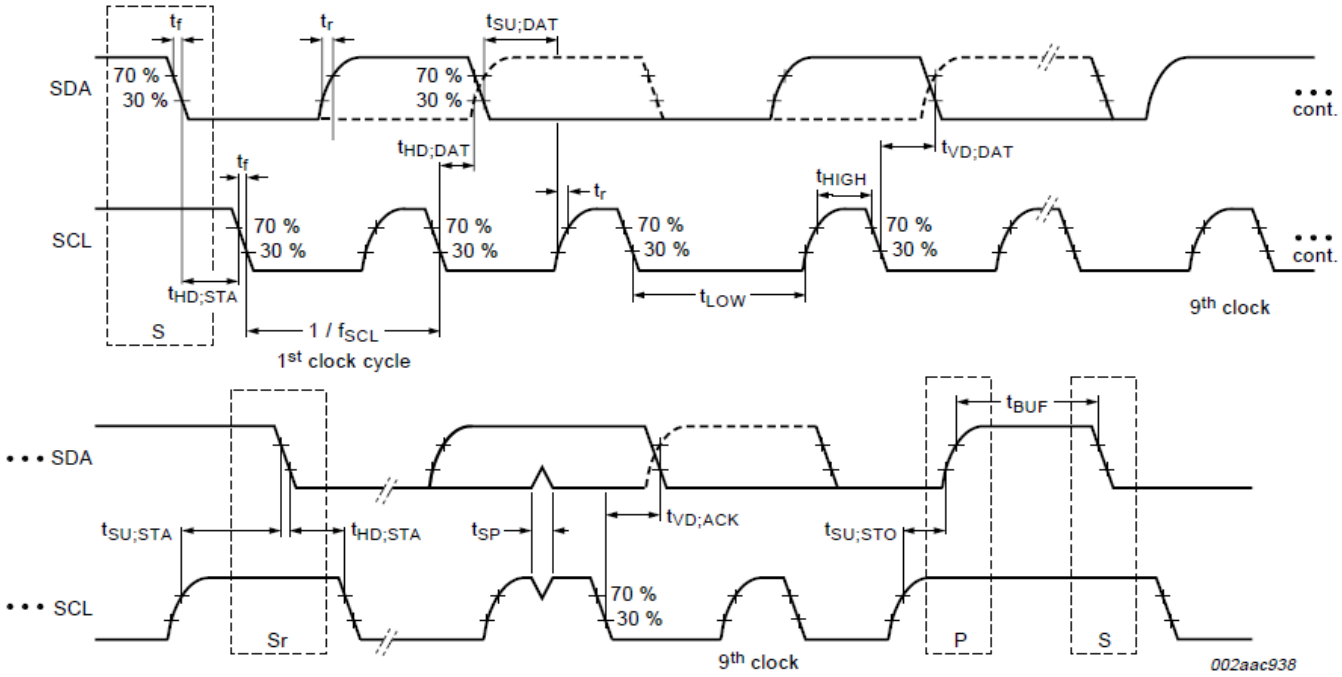


FIGURE 2. I²C TIMING DIAGRAM

Register Map

There are ten 8-bit registers accessible via I²C. Registers 0x1 and 0x2 define the operation mode of the device. Registers 0x3 and 0x4 store the various Prox thresholds which trigger interrupt events. Registers 0x8 store the results of Prox ADC conversions.

TABLE 1. ISL29028A REGISTERS AND REGISTER BITS

		BIT								
ADDR	REG NAME	7	6	5	4	3	2	1	0	DEFAULT
0x00	(n/a)	*(Reserved)*								(n/a)
0x01	CONFIGURE	PROX EN	PROX_SLP[2:0]			PROX_DR	(Write 0)	(Write0)	(Write0)	0x00
0x02	INTERRUPT	PROX_FLAG	PROX_PRST[1:0]		*(Write 0)*	(Write0)	(Write 0)		(Write 0)	0x00
0x03	PROX_LT	PROX_LT[7:0]								0x00
0x04	PROX_HT	PROX_HT[7:0]								0xFF
0x05	(n/a)	(Reserved)								(n/a)
0x06	(n/a)	*(Reserved)*								(n/a)
0x07	(n/a)	*(Reserved)*								(n/a)
0x08	PROX_DATA	PROX_DATA[7:0]								0x00
0x09	(n/a)	*(Reserved)*								(n/a)
0x0A	(n/a)	*(Reserved)*								(n/a)
0x0E	TEST1	*(Write as 0x00)*								0x00
0x0F	TEST2	*(Write as 0x00)*								0x00

Register Descriptions

TABLE 2. REGISTER 0x00 (RESERVED)

BIT #	ACCESS	DEFAULT	NAME	FUNCTION/OPERATION
7:0	RO	(n/a)	(n/a)	Reserved - no need to read or write

TABLE 3. REGISTER 0x01 (CONFIGURE) - PROX CONFIGURATION

BIT #	ACCESS	DEFAULT	NAME	FUNCTION/OPERATION
7	RW	0x00	PROX_EN (Prox Enable)	When = 0, proximity sensing is disabled When = 1, continuous proximity sensing is enabled. Prox data will be ready 0.54ms after this bit is set high
6:4	RW	0x00	PROX_SLP (Prox Sleep)	For bits 6:4 = (see the following) 111; sleep time between prox IR LED pulses is 0.0ms (run continuously) 110; sleep time between prox IR LED pulses is 12.5ms 101; sleep time between prox IR LED pulses is 50ms 100; sleep time between prox IR LED pulses is 75ms 011; sleep time between prox IR LED pulses is 100ms 010; sleep time between prox IR LED pulses is 200ms 001; sleep time between prox IR LED pulses is 400ms 000; sleep time between prox IR LED pulses is 800ms
3	RW	0x00	PROX_DR (Prox Drive)	When = 0, IRDR behaves as a pulsed 110mA current sink When = 1, IRDR behaves as a pulsed 220mA current sink
2	RW	0x00	Unused (Write 0)	Unused register bit (write 0)
1	RW	0x00	Unused (Write 0)	Unused register bit (write 0)
0	RW	0x00	Unused (Write 0)	Unused register bit (write 0)

TABLE 4. REGISTER 0x02 (INTERRUPT) - PROX INTERRUPT CONTROL

BIT #	ACCESS	DEFAULT	BIT NAME	FUNCTION/OPERATION
7	FLAG	0x00	PROX_FLAG (Prox Flag)	When = 0, no Prox interrupt event has occurred since power-on or last “clear” When = 1, a Prox interrupt event occurred. Clearable by writing “0”
6:5	RW	0x00	PROX_PRST (Prox Persist)	For bits 6:5 = (see the following) 00; set PROX_FLAG if 1 conversion result trips the threshold value 01; set PROX_FLAG if 4 conversion results trip the threshold value 10; set PROX_FLAG if 8 conversion results trip the threshold value 11; set PROX_FLAG if 16 conversion results trip the threshold value
4	RW	0x00	*Unused* *(Write 0)*	Unused register bit - write 0
3	RW	0x00	*Unused* *(Write 0)*	Unused register bit - write 0
2:1	RW	0x00	*Unused* *(Write 0)*	Unused register bit - write 0
0	RW	0x00	*Unused* *(Write 0)*	Unused register bit - write 0

TABLE 5. REGISTER 0x03 (PROX_LT) - INTERRUPT LOW THRESHOLD FOR PROXIMITY SENSOR

BIT #	ACCESS	DEFAULT	BIT NAME	FUNCTION/OPERATION
7:0	RW	0x00	PROX_LT (Prox Threshold)	8-bit interrupt low threshold for proximity sensing

TABLE 6. REGISTER 0x04 (PROX_HT) - INTERRUPT HIGH THRESHOLD FOR PROXIMITY SENSOR

BIT #	ACCESS	DEFAULT	BIT NAME	FUNCTION/OPERATION
7:0	RW	0xFF	PROX_HT (Prox Threshold)	8-bit interrupt high threshold for proximity sensing

TABLE 7. REGISTER 0x08 (PROX_DATA) - PROXIMITY SENSOR DATA

BIT #	ACCESS	DEFAULT	BIT NAME	FUNCTION/OPERATION
7:0	RO	0x00	PROX_DATA (Proximity Data)	Results of 8-bit proximity sensor ADC conversion

TABLE 8. REGISTER 0x0E (TEST1) - TEST MODE

BIT #	ACCESS	DEFAULT	BIT NAME	FUNCTION/OPERATION
7:0	RW	0x00	*(Write as 0x00)*	Test mode register. When 0x00, in normal operation

TABLE 9. REGISTER 0x0F (TEST2) - TEST MODE 2

BIT #	ACCESS	DEFAULT	BIT NAME	FUNCTION/OPERATION
7:0	RW	0x00	*(Write as 0x00)*	Test mode register. When 0x00, in normal operation

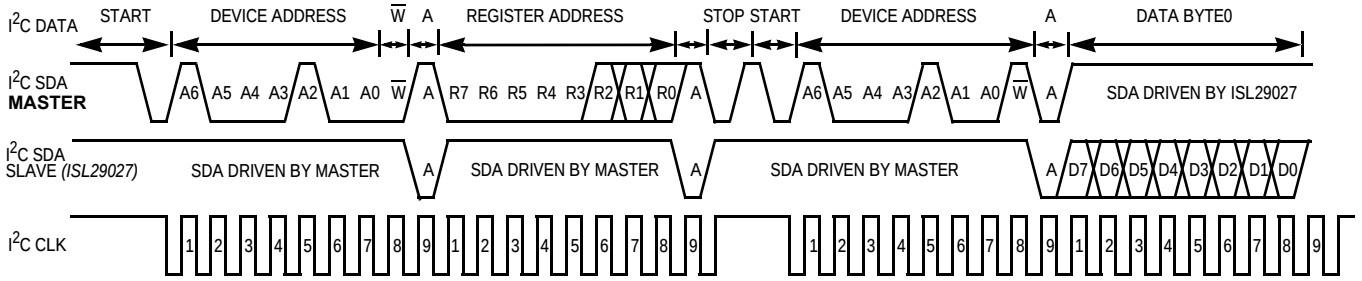


FIGURE 3. I2C DRIVER TIMING DIAGRAM FOR MASTER AND SLAVE CONNECTED TO COMMON BUS

Principles of Operation

I2C Interface

The ISL29027's I2C interface slave address is internally hardwired as 0b100010<x>, where "0b" signifies binary notation and x represents the logic level on pin ADDR0.

Figure 3 shows a sample one-byte read. The I2C bus master always drives the SCL (clock) line, while either the master or the slave can drive the SDA (data) line. Every I2C transaction begins with the master asserting a start condition (SDA falling while SCL remains high). The first transmitted byte is initiated by the master and includes 7 address bits and a R/$\overline{W}$ bit. The slave is responsible for pulling SDA low during the ACK bit after every transmitted byte.

Each I2C transaction ends with the master asserting a stop condition (SDA rising while SCL remains high).

For more information about the I2C standard, please consult the Philips™ I2C specification documents.

Photodiodes and ADCs

The ISL29027 contains photodiode arrays which convert photons (light) into current. The proximity sensor is an 8-bit ADC. When proximity sensing is enabled, the IRDR pin will drive a user-supplied infrared LED, the emitted IR reflects off an object (i.e., a human head) back into the ISL29027, and a sensor converts the reflected IR wave to a current signal in 0.54ms. The ADC subtracts the IR reading before and after the LED is driven (to remove ambient IR such as sunlight), and converts this value to a digital count stored in Register 0x8. Because of the conversion times, the user must let the ADCs perform one full conversion first before reading from I2C Registers PROX_DATA (wait 0.54ms). The proximity sensor runs continuously with a time between conversions decided by PROX_SLP (Register 1 Bits [6:4]).(as shown in Figure 4).

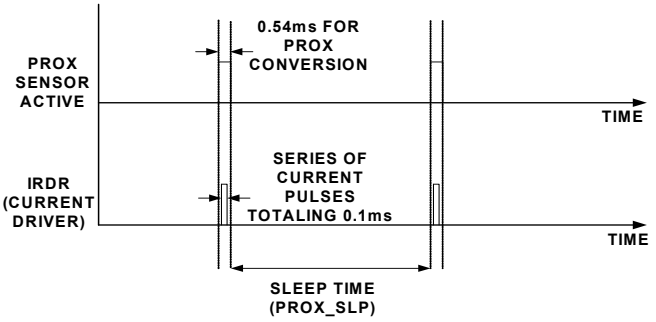


FIGURE 4. CURRENT DRIVE MODE OPTIONS

Proximity Sensing

When proximity sensing is enabled (PROX_EN = 1), the external IR LED is driven for 0.1ms by the built-in IR LED driver through the IRDR pin. The amplitude of the IR LED current depends on Register 1 bit 3: PROX_DR. If this bit is low, the load will see a

fixed 110mA current pulse. If this bit is high, the load on IRDR will see a fixed 220mA current pulse as seen in Figure 5.

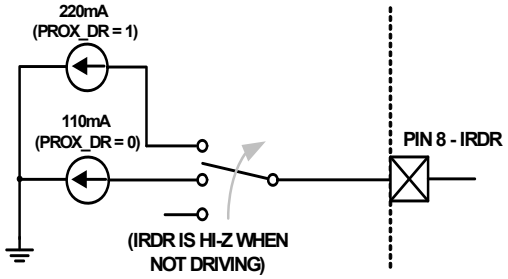


FIGURE 5. CURRENT DRIVE MODE OPTIONS

When the IR from the LED reaches an object and gets reflected back into the ISL29027, the reflected IR light is converted into current as per the IR spectral response shown in Figure 7. One entire proximity measurement takes 0.54ms for one conversion (which includes 0.1ms spent driving the LED), and the period between proximity measurements is decided by PROX_SLP (sleep time) in (Register 1 Bits 6:4).

Average LED driving current consumption is given by Equation 1.

$$I_{IRDR;AVE} = \frac{I_{IRDR;PEAK} \times 100\mu s}{T_{SLEEP}} \quad \text{(EQ. 1)}$$

A typical IRDR scheme is 220mA amplitude pulses every 800ms, which yields 28µA DC.

Total Current Consumption

Total current consumption is the sum of IDD and IIRDR. The IRDR pin sinks current (as shown in Figure 5) and the average IRDR current can be calculated using Equation 1. IDD depends on voltage and the mode-of-operation, as seen in Figure 9.

Interrupt Function

The ISL29027 has an intelligent interrupt scheme designed to shift some logic processing away from intensive microcontroller I^2C polling routines (which consume power) and towards a more independent light sensor, which can instruct a system to “wake up” or “go to sleep”.

A proximity interrupt event (PROX_FLAG) is governed by the high and low thresholds in registers 3 and 4 (PROX_LT and PROX_HT). PROX_FLAG is set when the measured proximity data is more than the higher threshold X-times-in-a-row (X is set by user; see next paragraph). The proximity interrupt flag is cleared when the prox data is lower than the low proximity threshold X-times-in-a-row, or when the user writes “0” to PROX_FLAG.

Interrupt persistency is another useful option available for proximity measurements. Persistency requires X-in-a-row interrupt flags before the INT pin is driven low. Prox have their own independent interrupt persistency options. See PROX_PRST bits in Register 2.

VDD Power-up and Power Supply Considerations

Upon power-up, please ensure a VDD slew rate of 0.5V/ms or greater. After power-up, or if the user’s power supply temporarily deviates from our specification (2.25V to 3.63V), Intersil recommends the user write the following: write 0x00 to register 0x01, write 0x29 to register 0x0F, write 0x00 to register 0x0E, and write 0x00 to register 0x0F. The user should then wait ~1ms or more and then rewrite all registers to the desired values. If the user prefers a hardware reset method instead of writing to test registers: set VDD = 0V for 1 second or more, power back up at the required slew rate, and write registers to the desired values.

Power-Down

To put the ISL29027 into a power-down state, the user can set PROX_EN bits to 0 in Register 1. Or more simply, set all of Register 1 to 0x00.

Noise Rejection

Charge balancing ADC’s have excellent noise-rejection characteristics for periodic noise sources whose frequency is an integer multiple of the conversion rate. For instance, a 60Hz AC unwanted signal’s sum from 0ms to k*16.66ms (k = 1,2...ki) is zero. Similarly, setting the device’s integration time to be an integer multiple of the periodic noise signal greatly improves the light sensor output signal in the presence of noise. Since wall sockets may output at 60Hz or 50Hz, our integration time is 0.54ms: the lowest common integer number of cycles for both frequencies.

Proximity Detection of Various Objects

Proximity sensing relies on the amount of IR reflected back from objects. A perfectly black object would absorb all light and reflect no photons. The ISL29027 is sensitive enough to detect black ESD foam which reflects only 1% of IR. For biological objects, blonde hair reflects more than brown hair and customers may notice that skin tissue is much more reflective than hair. IR penetrates into the skin and is reflected or scattered back from within. As a result, the proximity count peaks at contact and monotonically decreases as skin moves away. The reflective characteristics of skin are very different from that of paper.

Typical Circuit

A typical application for the ISL29027 is shown in Figure 6. The ISL29027's I^2C address is internally hardwired as 0b100010<x>, with x representing the logic state of input I^2C address pin ADDR0. The device can be tied onto a system's I^2C bus together with other I^2C compliant devices.

Soldering Considerations

Convection heating is recommended for reflow soldering; direct-infrared heating is not recommended. The plastic ODFN package does not require a custom reflow soldering profile, and is qualified to +260°C. A standard reflow soldering profile with a +260°C maximum is recommended.

Suggested PCB Footprint

It is important that users check the "Surface Mount Assembly Guidelines for Optical Dual FlatPack No Lead (ODFN) Package" before starting ODFN product board mounting.

http://www.intersil.com/data/tb/TB477.pdf

Layout Considerations

The ISL29027 is relatively insensitive to layout. Like other I2C devices, it is intended to provide excellent performance even in significantly noisy environments. There are only a few considerations that will ensure best performance.

Route the supply and I^2C traces as far as possible from all sources of noise. 0.1µF and 1µF power supply decoupling capacitors need to be placed close to the device.

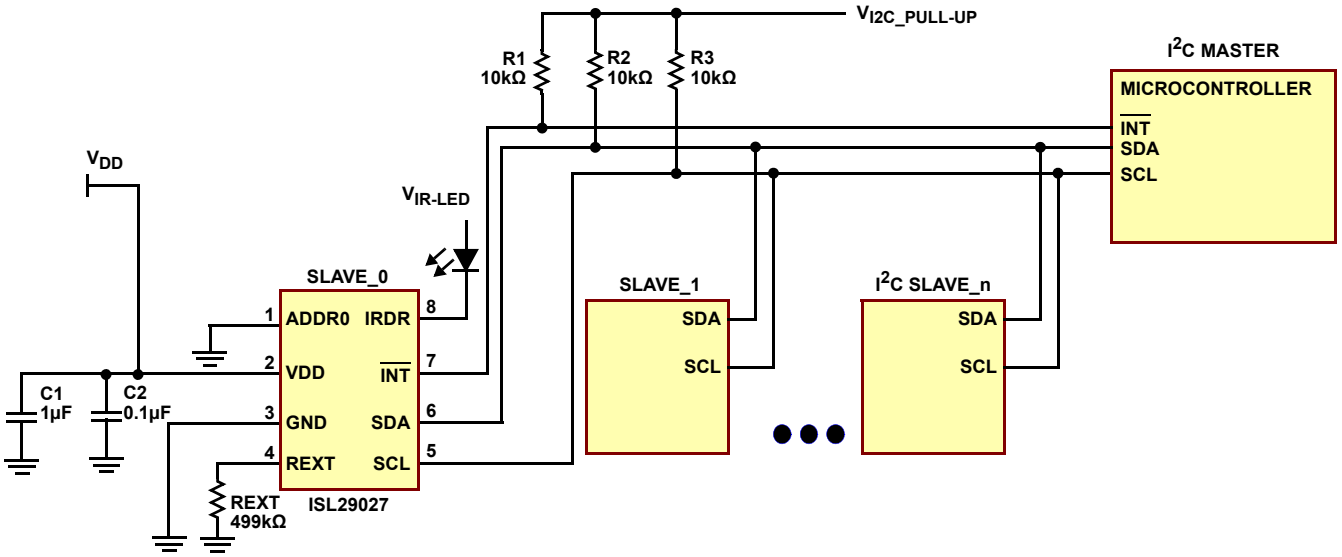


FIGURE 6. ISL29027 TYPICAL CIRCUIT

Typical Performance Curves V_{DD} = 3.0V, R_{EXT} = 499kΩ

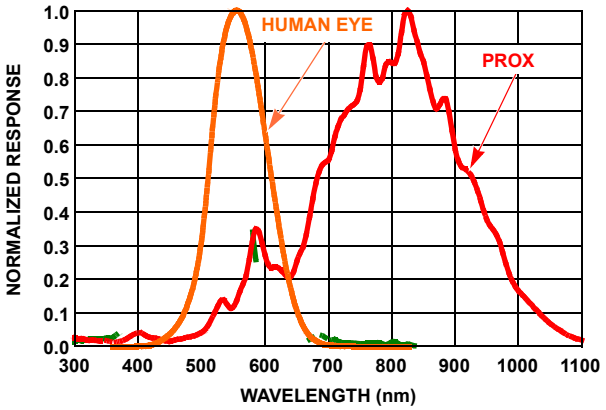


FIGURE 7. ISL29027 SENSITIVITY TO DIFFERENT WAVELENGTHS

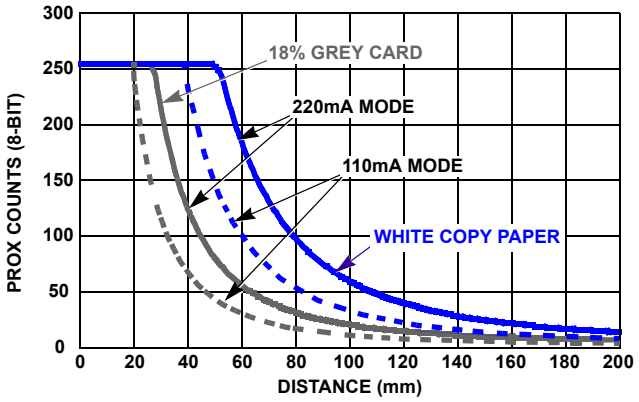


FIGURE 8. PROX COUNTS vs DISTANCE WITH 10CM x 10CM REFLECTOR

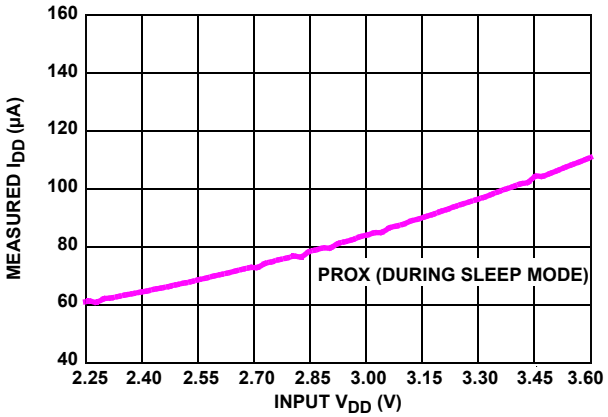


FIGURE 9. V_{DD} vs I_{DD} FOR VARIOUS MODES OF OPERATION

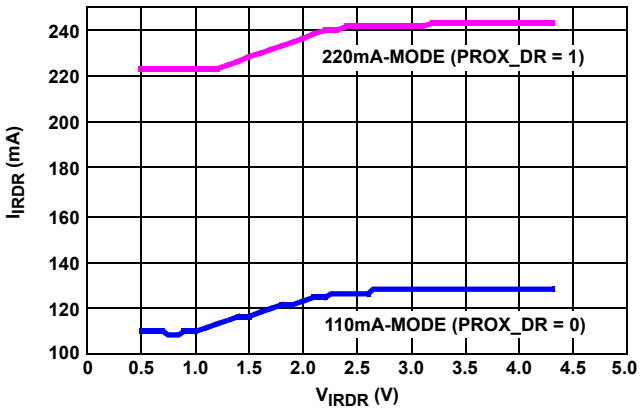


FIGURE 10. IRDR PULSE AMPLITUDE vs V_{IRDR}

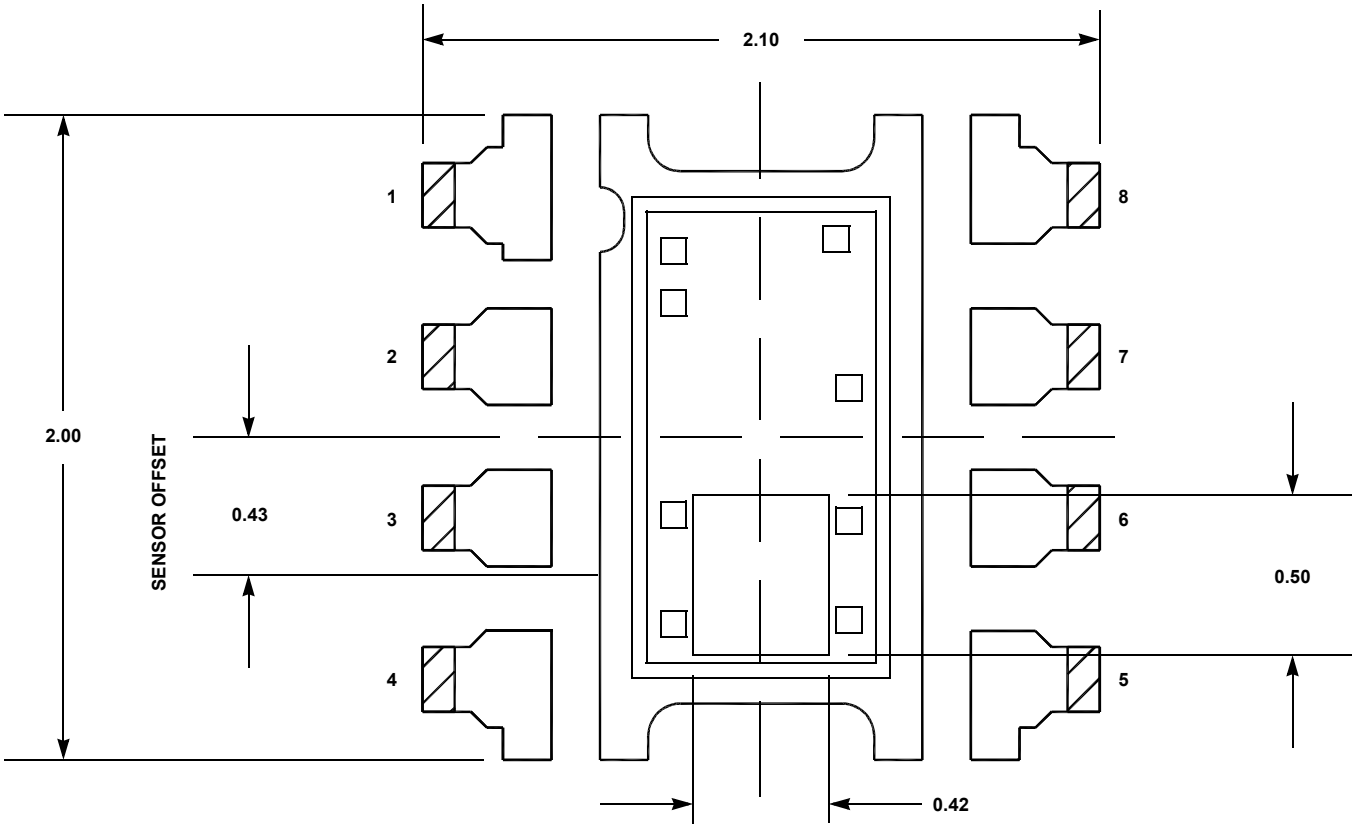


FIGURE 11. 8 LD ODFN SENSOR LOCATION OUTLINE - DIMENSIONS IN mm

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
2/7/11	FN7815.0	Initial Release.
7/14/11	FN7815.1	Page 1: Corrected "Light Data Process ALS and IR" to "Light Data Process IR" Page 2: Corrected Technical Brief reference in Note 3 from TB363 to TB477 Page 10: Removed "(USING ISL29028 EVALUATION BOARD)" from Figure 8 caption Page 13: Updated L8.2.1x2.0 as follows: Changed the drawing in the bottom view to show the new look of the pin#1 indicator Corrected note 4 from "Dimension b applies.." to "Dimension applies..." Added note 4 callout to bottom view Enclosed Note #'s 4, 5, 6 in triangles

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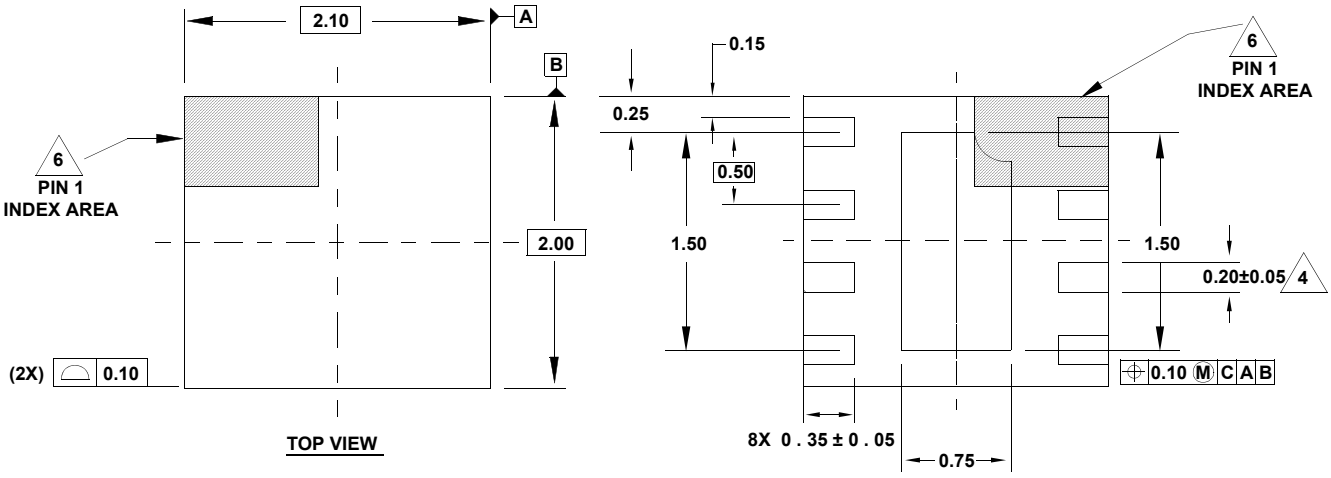
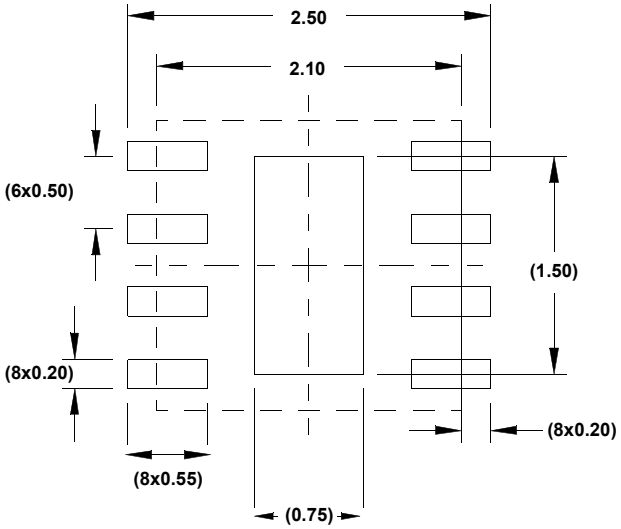
Package Outline Drawing

L8.2.1x2.0

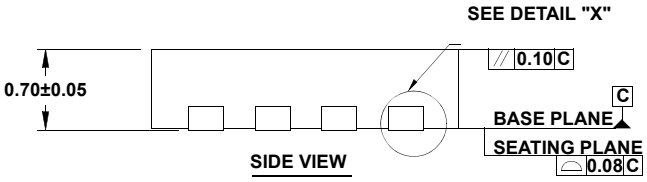
8 LEAD OPTICAL DUAL FLAT NO-LEAD PLASTIC PACKAGE (ODFN)

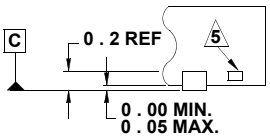
Rev 3, 1/11





TYPICAL RECOMMENDED LAND PATTERN





NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.25mm and 0.35mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

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