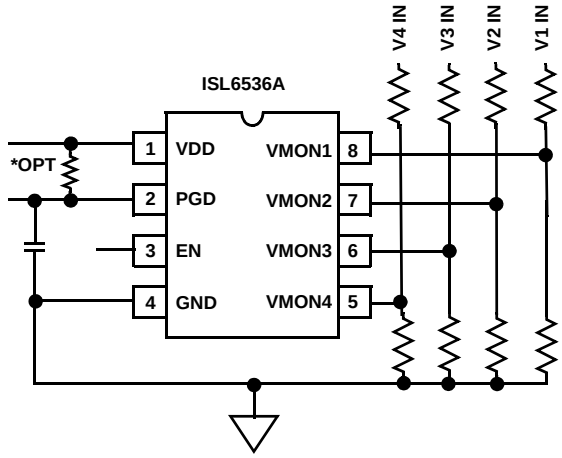
Data Sheet | May 2004 | FN9136.1

## Four Channel Supervisory IC

The ISL6536A is a four channel supervisory IC designed to monitor voltages >, = 0.7V. This IC bias range is from 2.7V to 5V but can supervise any positive voltage using an external resistor divider to translate to a lower voltage for comparison to the internal 0.63V reference.

Once properly biased and enabled when all four voltage monitor (VMON) inputs are satisfied the PGOOD output will be immediately released to go high to signal that voltage is valid on all four rails. Subsequently when the monitored voltage on any rail drops below its user defined threshold point, the PGOOD output is pulled low. Each rail's VMON point is independently adjustable with a resistor divider. The PGOOD output is guaranteed to be valid with IC bias lower than 1V. The VMON inputs will ignore 30µs transients on the monitored supplies. The PGOOD output is an open-drain to allow ORing of multiple signals and interfacing to a range of logic levels. The ENABLE input provides for a reset of the PGOOD output when it is pulled down below 0.5V. With an internal 10uA pull-up to VDD it can be signalled with common logic or pulled to ground with a push button switch.

## Typical Application Schematic




## Features

- 1% VMON Threshold accuracy
- Adjustable undervoltage lockout for each supply
- Active high PGOOD Output
- Guaranteed PGOOD Valid to Falling VDD < 1V
- VMON Glitch Immunity
- Pb-free Available as an Option

## Applications

- Graphics Cards
- Multi voltage DSPs and Processors
- µP Voltage Monitoring
- Embedded Control Systems
- Intelligent Instruments
- Medical Equipment
- Network Routers
- Portable Battery-Powered Equipment
- Set-Top Boxes
- Telecommunications Systems

## Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|
| ISL6536AIB | -40 to +85 | 8 Lead SOIC | M8.15 |
| ISL6536AIBZ (See Note) | -40 to +85 | 8 Lead SOIC (Pb-free) | M8.15 |
| ISL6536AIB-T | 8 Lead SOIC Tape and Reel | | |
| ISL6536AIBZ-T (See Note) | 8 Lead SOIC Tape and Reel (Pb-free) | | |

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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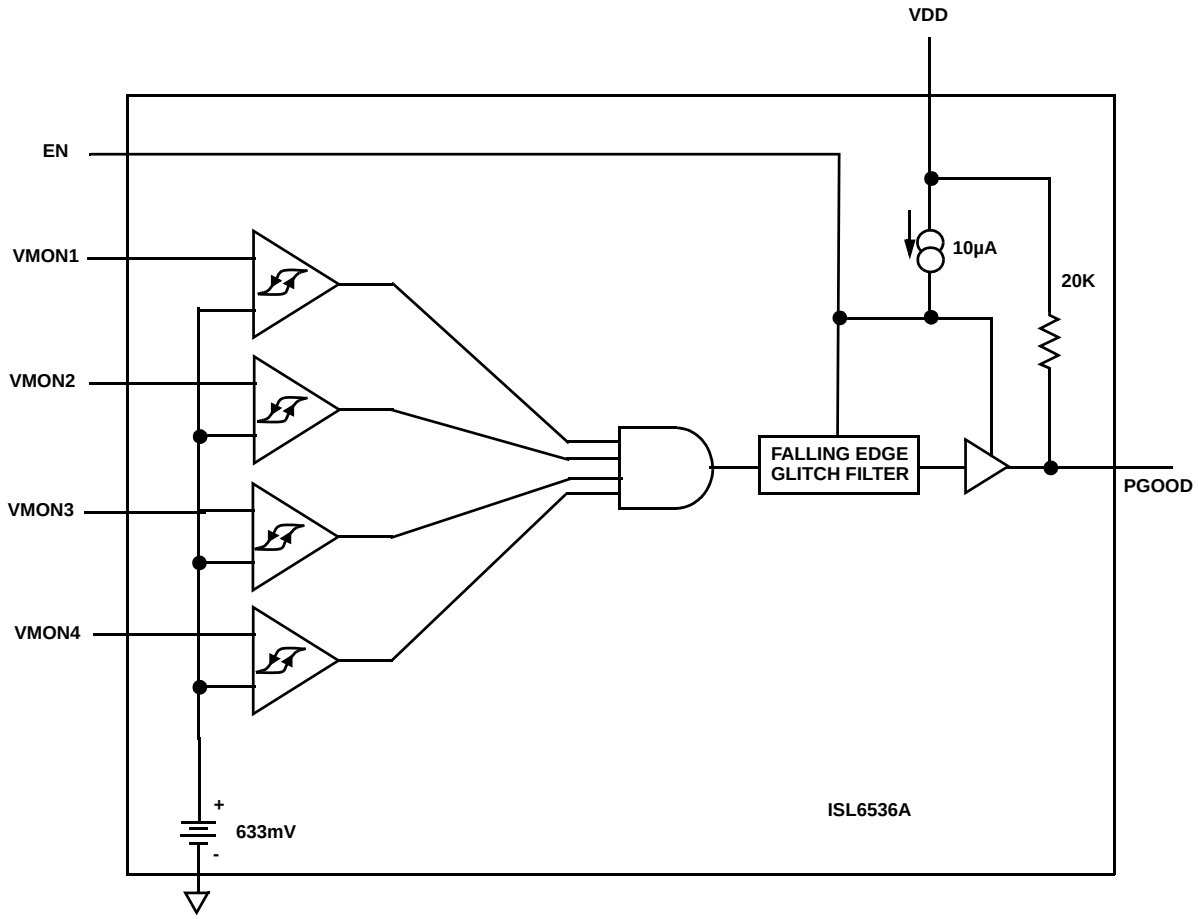
## Pin Descriptions

| ISL6536A | PIN NAME | FUNCTION DESCRIPTION |
|---|---|---|
| 1 | VDD | Bias IC from nominal 2.7V to 5V |
| 2 | PGOOD | PGOOD is the boolean AND function of all the UV inputs being satisfied. This is an open drain output and can be pulled high to the appropriate level with an external resistor. Additionally a 20kΩ pull up to VDD is provided internally. |
| 3 | ENABLE | Enabling input for supervisory function. Has a 10µA pull-up to VDD |
| 4 | GND | IC ground |
| 5-8 | VMON1<br>VMON2<br>VMON3<br>VMON4 | These inputs provide for a programmable monitored voltage threshold referenced to an internal 0.633V reference with 1% accuracy. These inputs have a 30µs glitch filter to prevent transient upsets from being recognized by PGOOD. |



## Absolute Maximum Ratings

VDD . . . . . +6V
VMON, PGOOD, ENABLE. . . . . -0.3V to VDD+0.3V
ESD Classification . . . . . 4kV (HBM)

## Operating Conditions

VDD Supply Voltage Range. . . . . +2.7V to +5.5V
Temperature Range ($T_A$) . . . . . -40°C to 85°C

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ (°C/W) |
|---|---|
| SOIC Package . . . . . | 108 |

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board. See Tech Brief TB379 for details.
2. 2. All voltages are relative to GND, unless otherwise specified.

## Electrical Specifications

Nominal VDD = 3.3V, $T_A = T_J$ = -40°C - 85°C, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **BIAS** | | | | | | |
| IC Supply Current | $I_{VDD}$ | VMON > VMON_L2H | - | 165 | 1000 | µA |
| VDD Power On | VDD_L2H | VDD low to high | - | 2.6 | - | V |
| VDD Power On Reset | VDD_POR | VDD high to low | - | 2.4 | - | V |
| **PGOOD** | | | | | | |
| Pull-Down Current | $_{PG}$pd | VPGOOD = 0.5V | - | 2 | - | mA |
| Pull-Up Resistance | $_{PG}$pu | | - | 20 | - | kΩ |
| Output Low | $V_{PGl}$ | VDD= 1V | - | 0.05 | 0.1 | V |
| Delay from VMON Rising | $T_{PG}$delVMON | Last valid input = Vth to PG release | - | 2 | - | µs |
| Delay from EN Rising | $T_{PG}$delENR | EN high to PG release | - | 0.05 | - | µs |
| Delay from EN Falling | $T_{PG}$delENF | EN low to PG pulling low | - | 0.015 | - | µs |
| **ENABLE** | | | | | | |
| Rising Threshold | $V_{EN}$ | ENABLE Low to High Threshold | 0.4VDD | 0.5VDD | 0.6VDD | V |
| Threshold Hysteresis | $V_{EN\_HYS}$ | | - | 0.065 | - | V |
| Pull-up Current | $I_{ENpu}$ | VEN = 0.5V | - | 10 | - | µA |
| **VMON INPUT** | | | | | | |
| Falling Threshold | 3.3VMON_H2L | Tj=+25c | 0.627 | 0.633 | 0.639 | V |
| Falling Threshold Temp Coefficient | 3.3VMON_TC | | - | 33 | - | µV/°C |
| Hysteresis | VVMON_HYS | | - | 10 | - | mV |
| Range | VMON_RNG | | - | 1 | - | mV |
| Glitch Filter Duration | TFIL | VMON glitch to PGOOD low Filter | - | 30 | - | µs |

## ISL6536A Description and Operation

The ISL6536A is a four channel supervisory IC with industry leading 1% tolerance and 1mV range between channels. This IC is designed to monitor multiple voltages greater than 0.7V and is suitable for both microprocessors or industrial system applications.

Upon VDD bias power up the PGOOD output is held low with VDD as low as 0V. Once biased to 2.7V and enabled the IC continuously monitors from one to four voltages independently through external resistor dividers comparing each VMON pin voltage to an internal 0.63V reference.

Once all VMON input voltages rise above 0.63V the PGOOD (power good) output signal is released and is pulled high via an external pull resistor to indicate that the power conditions have been met. The PGOOD output is an open-drain to allow ORing of the signals and interfacing to a wide range of logic levels.

Once any VMON input falls below 0.63V the PGOOD output is pulled low, the VMON inputs are designed to reject fast transients (30µs).

If less than four voltages are being monitored, connect the unused VMON pins to VDD.

The PGOOD pin has an internal 20kΩ pull-up to VDD making an external pull-up resistor unnecessary.

Figure 1 illustrates the operational timing diagram.

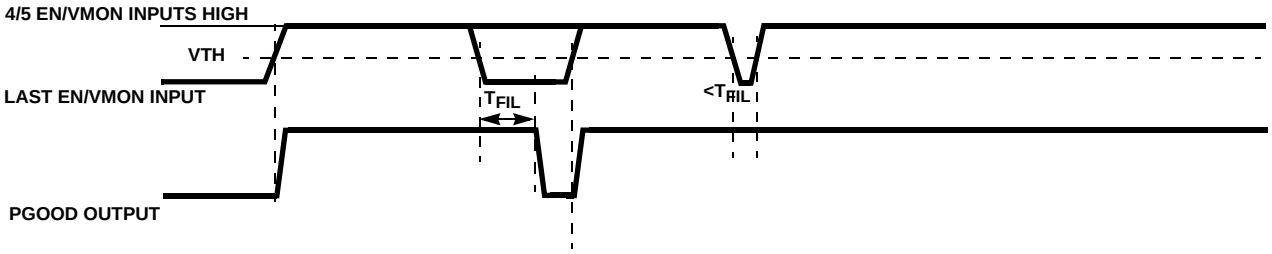



**FIGURE 1. ISL6536A OPERATIONAL TIMING DIAGRAM**

## Typical Performance Curves

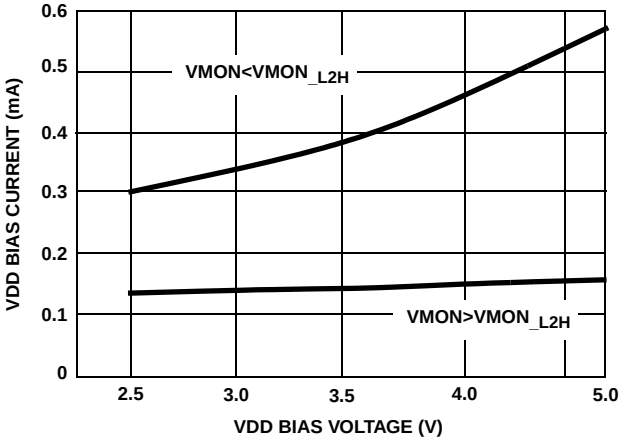



**FIGURE 2. VDD CURRENT vs VDD VOLTAGE**

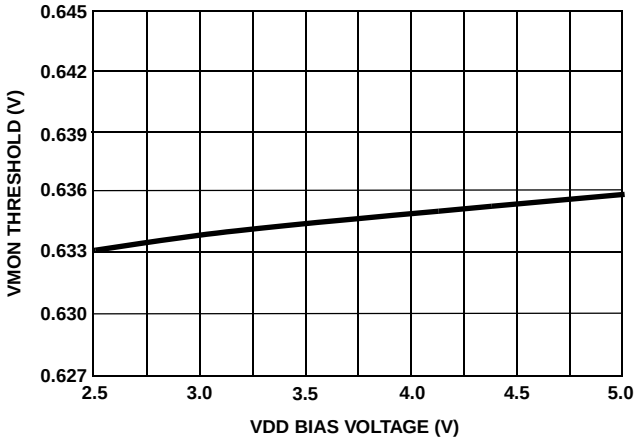
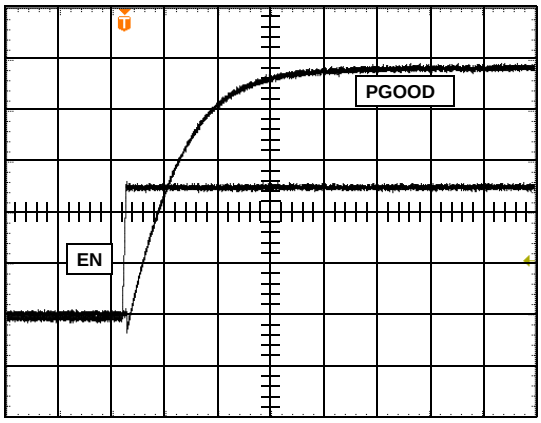


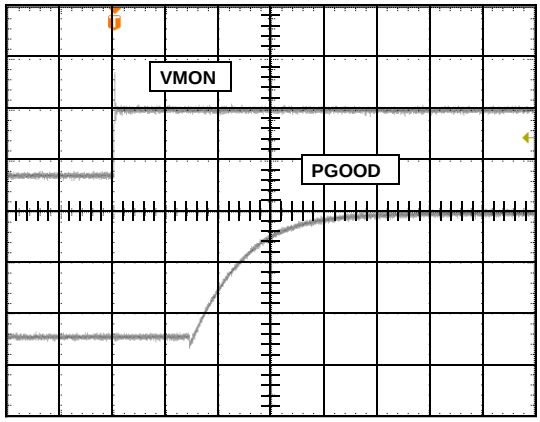

**FIGURE 3. VMON THRESHOLD vs VDD VOLTAGE**

## Typical Performance Curves (Continued)



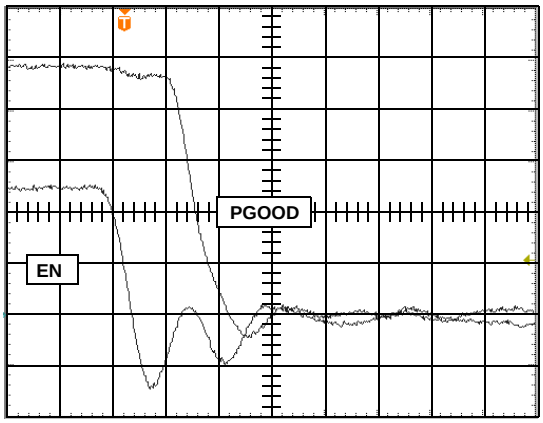

PG = 1V/DIV
EN = 1V/DIV
1µs/DIV

FIGURE 4. EN HIGH TO PGOOD



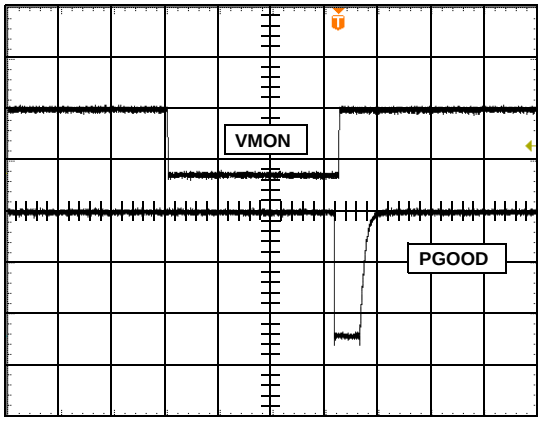

PG = 2V/DIV
VMON = 1V/DIV
1µs/DIV

FIGURE 5. VMON HIGH TO PGOOD



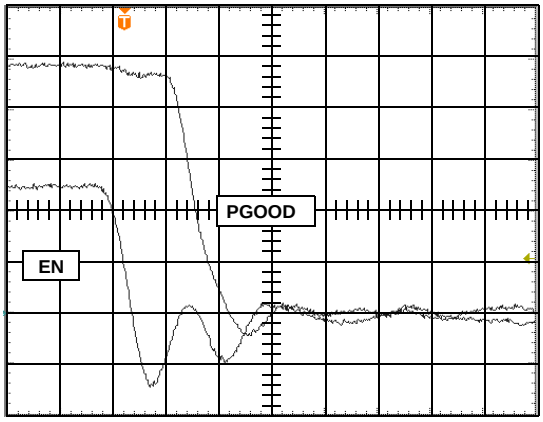

EN = 1V/DIV
PG = 1V/DIV
10nS/DIV

FIGURE 6. EN LOW TO PGOOD



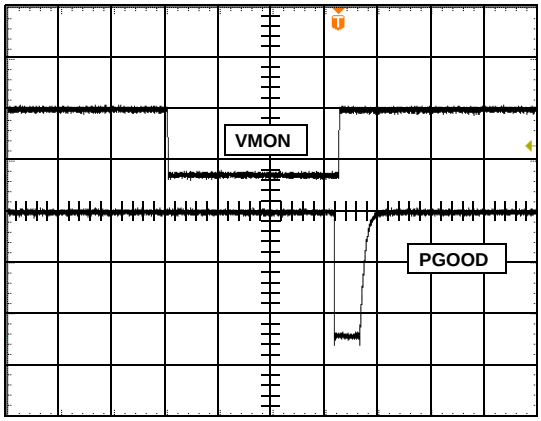

PGOOD = 2V/DIV
VMON = 1V/DIV
10µs/DIV

FIGURE 7. VMON LOW TO PGOOD




EN = 1V/DIV
PG = 1V/DIV
10nS/DIV

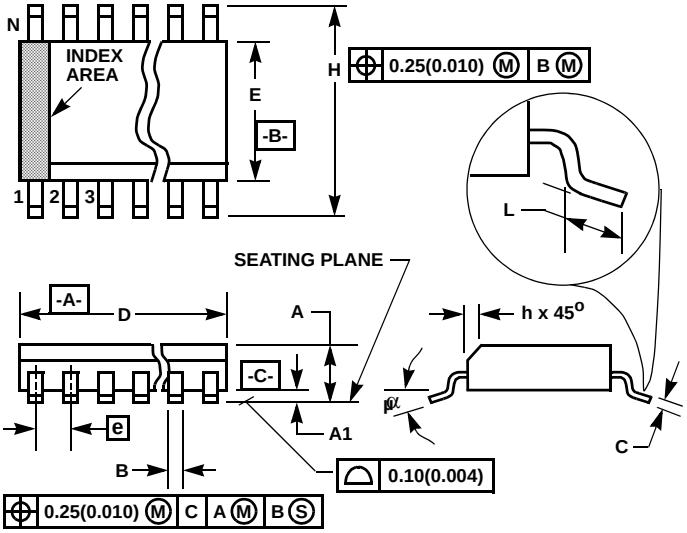
FIGURE 8. EN LOW TO PGOOD




PGOOD = 2V/DIV
VMON = 1V/DIV
10µs/DIV

FIGURE 9. VMON LOW TO PGOOD

## Small Outline Plastic Packages (SOIC)




NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

**M8.15 (JEDEC MS-012-AA ISSUE C)**
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| $\alpha$ | $0^o$ | $8^o$ | $0^o$ | $8^o$ | - |

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