



## Features

- Excellent common-mode rejection ratio (CMRR)
- Application circuits can meet isolation requirements of worldwide telephony standards
- Small 8-pin SOIC
- Worldwide telephone network compatibility
- Full-wave ringing level detector comparator with internal threshold, large hysteresis, and logic-level output
- 3.3V or 5V operation
- High differential input impedance
- Very low common-mode input impedance
- Fixed gain
- Differential or single-ended linear output
- TTL logic level input
- CMOS logic level output (TTL compatible)
- Virtually non-detectable in voice monitoring applications

## Description

The Clare CPC5710N is a selectable dual function CMOS special purpose integrated high-impedance input, fixed-gain amplifier and an internally set voltage level comparator for telephone line monitoring. The high (>40dB) common-mode rejection ratio makes the CPC5710N an excellent choice for signaling detection, line condition monitoring, discrete voice recording and CID buffering applications. In addition to voice applications, the CPC5710N is ideal for data applications such as embedded modem designs utilized in broadband set-top boxes.

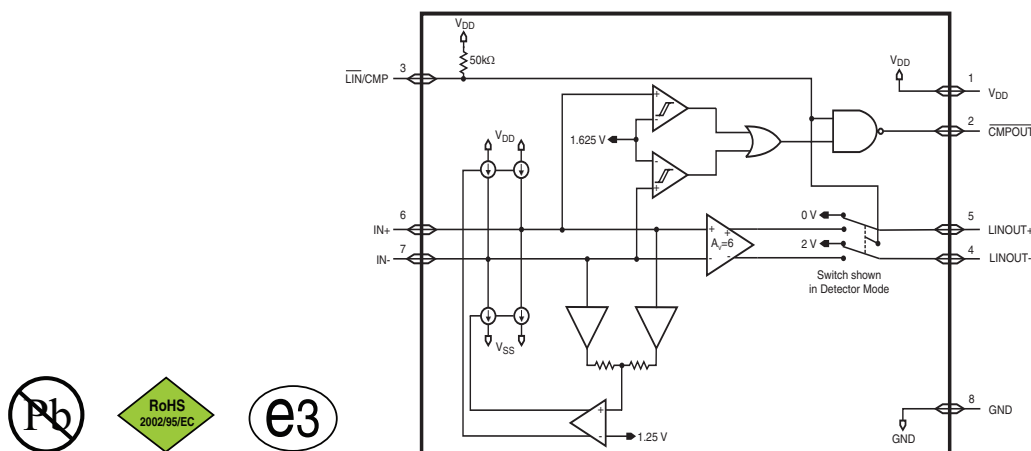
## Ordering Information

| Part Number | Description                    |
|-------------|--------------------------------|
| CPC5710N    | PLM IC, Tubed, 100/Tube        |
| CPC5710NTR  | PLM IC, Tape & Reel, 2000/Reel |

## Applications

- The CPC5710N can be used for line monitoring or detection of signaling states and loop conditions such as:
  - Display feature (caller ID) signal buffering
  - Line-In-Use (LIU) detection
  - Ringing signal with adjustable detection level
  - Battery presence monitoring
  - Tip to ring line voltage monitoring
  - Line polarity
  - Imperceptible voice recording

**Figure 1. CPC5710N Block Diagram**

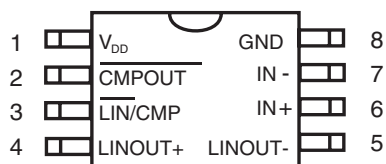


## CPC5710N

|                                                                                                                    |          |
|--------------------------------------------------------------------------------------------------------------------|----------|
| <b>1. Specifications</b>                                                                                           | <b>3</b> |
| 1.1 Package Pinout                                                                                                 | 3        |
| 1.2 Pin Description                                                                                                | 3        |
| 1.3 Absolute Maximum Ratings                                                                                       | 3        |
| 1.4 Recommended Operating Environment                                                                              | 3        |
| 1.5 Electrical Characteristics                                                                                     | 4        |
| 1.5.1 AC Characteristics                                                                                           | 4        |
| 1.5.2 Detector Threshold Characteristics                                                                           | 4        |
| 1.5.3 $\overline{\text{LIN}}$ /CMP Input Characteristics                                                           | 4        |
| 1.5.4 Power Characteristics                                                                                        | 4        |
| <b>2. Using CPC5710N</b>                                                                                           | <b>5</b> |
| 2.1 $\overline{\text{LIN}}$ /CMP Input                                                                             | 5        |
| 2.2 Amplifier Design Considerations                                                                                | 5        |
| 2.2.1 Linear Amplifier Gain                                                                                        | 5        |
| 2.3 Detector Considerations                                                                                        | 5        |
| 2.3.1 Ringing Signal Detection                                                                                     | 5        |
| 2.3.2 Setting Ringing Detection Threshold                                                                          | 5        |
| 2.4 Power Quality                                                                                                  | 6        |
| <b>3. Applications</b>                                                                                             | <b>7</b> |
| 3.1 Line-In-Use (LIU) and Line Polarity Detector                                                                   | 7        |
| 3.2 Non-Intrusive Line Monitoring, Display Feature (Caller ID) Signal Reception, and Ringing Detection Application | 8        |
| 3.2.1 Frequency Response                                                                                           | 8        |
| 3.3 Regulatory Issues                                                                                              | 8        |
| <b>4. Manufacturing Information</b>                                                                                | <b>9</b> |
| 4.1 Mechanical Dimensions                                                                                          | 9        |
| 4.1.1 8-Pin SOIC Package                                                                                           | 9        |
| 4.1.2 Tape and Reel Specifications                                                                                 | 9        |
| 4.2 Soldering                                                                                                      | 10       |
| 4.3 Washing                                                                                                        | 10       |

## 1. Specifications

### 1.1 Package Pinout



### 1.2 Pin Description

| Pin | Name            | Description                                            |
|-----|-----------------|--------------------------------------------------------|
| 1   | V <sub>DD</sub> | Power supply                                           |
| 2   | CMPOUT          | Detector output                                        |
| 3   | LIN/CMP         | Comparator Enable - disables linear amplifier outputs. |
| 4   | LINOUT-         | Linear amplifier inverting output                      |
| 5   | LINOUT+         | Linear amplifier non-inverting output                  |
| 6   | IN+             | Non-inverting differential input                       |
| 7   | IN-             | Inverting differential input                           |
| 8   | GND             | Ground                                                 |

### 1.3 Absolute Maximum Ratings

| Parameter                       | Minimum | Maximum               | Unit |
|---------------------------------|---------|-----------------------|------|
| V <sub>DD</sub>                 | -0.3    | 6                     | V    |
| Storage temperature             | -40     | +125                  | °C   |
| Total package power dissipation |         | 300                   | mW   |
| Logic input voltage             | -0.3    | V <sub>DD</sub> + 0.3 | V    |

*Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.*

### 1.4 Recommended Operating Environment

| Parameter   | Conditions     | Minimum | Typical | Maximum | Unit |
|-------------|----------------|---------|---------|---------|------|
| Temperature |                | -40     | -       | +85     | °C   |
| Humidity    | Non-condensing | 5       | -       | 95      | %    |

## 1.5 Electrical Characteristics

Unless otherwise specified, minimum and maximum values are guaranteed by production testing requirements. Typical values, the result of engineering evaluations, are characteristic of the device and are

provided for informational purposes only. They are not however, a part of the production testing requirements. Unless otherwise indicated:

$V_{DD} = 5V$ , Temperature = 25°C

### 1.5.1 AC Characteristics

| Parameter                      | Symbol        | Conditions                                              | Minimum | Typical | Maximum | Unit   |
|--------------------------------|---------------|---------------------------------------------------------|---------|---------|---------|--------|
| Input Impedance                | $Z_{IN}$      |                                                         | 10      | -       | -       | MΩ     |
| Input offset voltage           | $V_{IO}$      |                                                         | -       | -       | 40      | mV     |
| Input offset current           | $I_{IO}$      | $I_{CM} = 0$ , No common-mode signal applied.           | -       | -       | 35      | nA     |
|                                |               | $I_{CM} = 12\mu A$ (per lead) signal applied.           | -       | -       | 125     | nA     |
| Output DC bias level           | $V_{OUT\_DC}$ | At LINOUT+ or LINOUT-, $I_O = 0.5mA$                    | 0.9     | 1.0     | 1.1     | V      |
| Output Low Voltage             | $V_{OUT}$     | $I_O = 0.5mA$                                           | -       | -       | 50      | mV     |
| Gain                           | $A_V$         | 0 to 20kHz                                              | 5.88    | 6       | 6.12    | -      |
| Common-mode rejection ratio    | CMRR          | Common-mode current $\leq 12\mu A$ per lead, 0 to 120Hz | 40      | -       | -       | dB     |
| Equivalent input noise voltage | $V_N$         |                                                         | -       | -90     | -       | dBm/Hz |

### 1.5.2 Detector Threshold Characteristics

| Parameter           | Symbol         | Conditions             | Minimum | Typical | Maximum | Unit |
|---------------------|----------------|------------------------|---------|---------|---------|------|
| Detection threshold | $V_{IN\_DET}$  | $I_{CM} = 0$           | 675     | 750     | 850     | mV   |
|                     |                | $I_{CM} = \pm 12\mu A$ | 488     | 750     | 1012    | mV   |
| Detector hysteresis | $V_{IN\_HYST}$ | $I_{CM} = 0$           | 300     | 375     | 450     | mV   |

### 1.5.3 LIN/CMP Input Characteristics

| Parameter                  | Symbol   | Conditions      | Minimum | Typical | Maximum | Unit    |
|----------------------------|----------|-----------------|---------|---------|---------|---------|
| Input low voltage          | $V_{IL}$ |                 | -       | -       | 0.8     | V       |
| Input high voltage         | $V_{IH}$ |                 | 2.0     | -       | -       | V       |
| Input low leakage current  | $I_{IL}$ | $V_{IL} = 0.4V$ | -       | -       | -120    | $\mu A$ |
| Input high leakage current | $I_{IH}$ | $V_{IH} = 2.4V$ | -       | -       | -120    | $\mu A$ |

### 1.5.4 Power Characteristics

| Parameter      | Symbol   | Conditions                  | Minimum | Typical | Maximum | Unit |
|----------------|----------|-----------------------------|---------|---------|---------|------|
| Supply voltage | $V_{DD}$ |                             | 3.0     | -       | 5.5     | V    |
| Supply current | $I_{DD}$ | All inputs and outputs open | -       | -       | 10      | mA   |

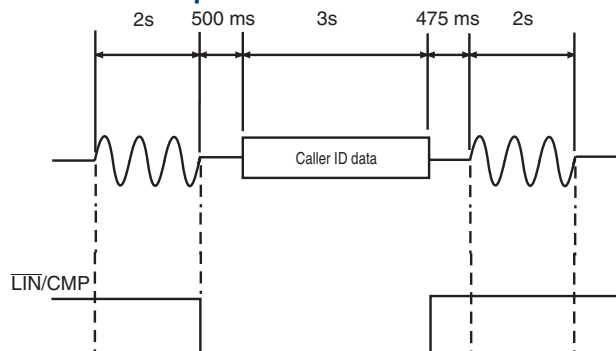
## 2. Using CPC5710N

### 2.1 $\overline{\text{LIN}}/\text{CMP}$ Input

The  $\overline{\text{LIN}}/\text{CMP}$  input selects the active output, either the detector output  $\overline{\text{CMPOUT}}$  or the linear outputs,  $\text{LINOUT-}$  and  $\text{LINOUT+}$ . Set  $\overline{\text{LIN}}/\text{CMP}$  low for linear output and high for comparator output. Note that both outputs cannot be used at once.

With  $\overline{\text{LIN}}/\text{CMP}$  at logic low ( $\overline{\text{LIN}}/\text{CMP} = 0$ ), the amplifier outputs are biased at a nominal  $1V_{\text{DC}}$  and  $\overline{\text{CMPOUT}}$  is held high. With  $\overline{\text{LIN}}/\text{CMP}$  at logic high ( $\overline{\text{LIN}}/\text{CMP} = 1$ ),  $\text{LINOUT+}$  is 0V and  $\text{LINOUT-}$  is 2V.

Figure 2.  $\overline{\text{LIN}}/\text{CMP}$  Timing for Caller-ID Signal Reception



Signal levels not to scale

### 2.2 Amplifier Design Considerations

Amplifier inputs are biased at a nominal  $1.25V_{\text{DC}}$ , the internal voltage reference. The internal common-mode circuitry maintains the average of the inputs at  $1.25V_{\text{DC}}$ . For example, if one input reaches 1.3V, the common-mode circuit drives the other input to 1.2V.

#### 2.2.1 Linear Amplifier Gain

Display feature information (caller ID) and voice signals are coupled through the linear amplifier. In North America, CID data signals are typically sent between the first and second ringing signal burst.

Referring to **Figure 6.**, signal gain from tip and ring to  $\text{LINOUT+}$  and  $\text{LINOUT-}$  is determined by:

$$GAIN_{CID}(dB) = 20\log \left[ \frac{6R_{SNPD}}{\sqrt{(4R_{SNP} + R_{SNPD})^2 + \frac{1}{(\pi f C_{SNP})^2}}} \right]$$

where  $f$  is the frequency of the signal.

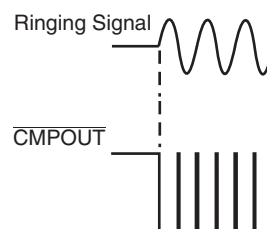
Clare Application Note AN-117 **Customize Caller ID Gain and Ringing Detect Voltage Threshold** is a spreadsheet for trying different component values in this type of circuit.

### 2.3 Detector Considerations

#### 2.3.1 Ringing Signal Detection

The CPC5710N detector is a full-wave configuration. Ringing signals will assert the output on both positive and negative parts of the ringing waveform. Hysteresis is employed by the internal comparator circuit to provide noise immunity. The set-up of the detector causes  $\overline{\text{CMPOUT}}$  output pulses to remain low for most of the ringing signal positive and negative half-cycles.  $\overline{\text{CMPOUT}}$  returns high when the ringing signal is near the zero-voltage crossing.

Figure 3.  $\overline{\text{CMPOUT}}$  Relative to Input



#### 2.3.2 Setting Ringing Detection Threshold

The ringing detection threshold depends on the component values of the input network. The values for these components shown in the application circuit are recommended for typical operation. Referring to **Figure 6.**, the ringing detection threshold can be changed according to the following formula:

$$V_{RINGPK} = \left( \frac{750mV}{R_{SNPD}} \right) \sqrt{(4R_{SNP} + R_{SNPD})^2 + \frac{1}{(\pi f_{RING} C_{SNP})^2}}$$

## CPC5710N

With the application circuit in **Figure 6.**, the series capacitors serve to reduce the magnitude of the high-amplitude, low-frequency ringing signals, while making the ringing detection threshold of the CPC5710N variable with the frequency of the ringing signal. With the circuit as given,  $\overline{\text{CMPOUT}}$  will change states with a 15Hz ringing signal at approximately 48V<sub>PEAK</sub>. For a 68Hz ringing signal,  $\overline{\text{CMPOUT}}$  will change states with a ringing signal amplitude of approximately 11.5V<sub>PEAK</sub>.

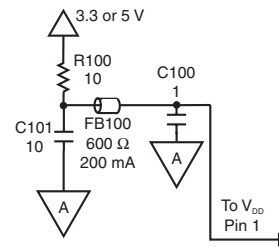
In applications where CPC5710N will be used only as a ringing level detector, or if significant attenuation of the amplified signal can be tolerated, the frequency variability of the ringing detection threshold can be reduced by increasing the value of the resistors and capacitors in series with the input.

Clare Application Note AN-117 **Customize Caller ID Gain and Ringing Detect Voltage Threshold** is a spreadsheet for trying different component values in this circuit for LITELINK snoop circuit applications.

## 2.4 Power Quality

CPC5710N works best with a clean power supply. To clean up power supply noise, Clare, Inc., recommends using a pi network on the V<sub>DD</sub> pin as shown in **Figure 4.**, if needed.

**Figure 4. Optional Power Supply pi Network**



Note: For lower-frequency noise, use a 220  $\mu\text{H}$  inductor in series with R100.

## 3. Applications

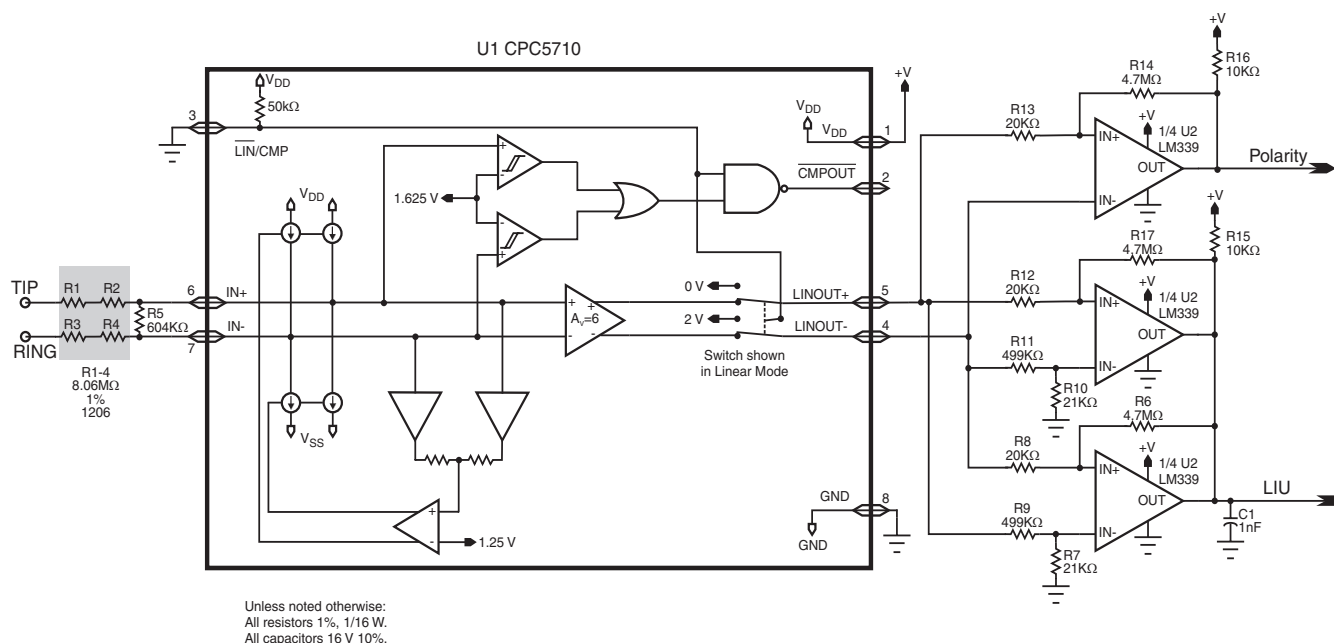
### 3.1 Line-In-Use (LIU) and Line Polarity Detector

This circuit performs two phone line interface functions, LIU and line polarity detection. The LIU output is logic high if the tip to ring voltage is less than approximately 17V. This will occur whenever a parallel device on the line such as a telephone or FAX is taken

off hook. This circuit can also be used to detect for the presence or loss of battery.

The Polarity output indicates the polarity of the phone line. Whenever tip is positive with respect to ring, Polarity out will be a logic high.

**Figure 5. LIU and Polarity Detection Application Circuit**



### 3.2 Non-Intrusive Line Monitoring, Display Feature (Caller ID) Signal Reception, and Ringing Detection Application

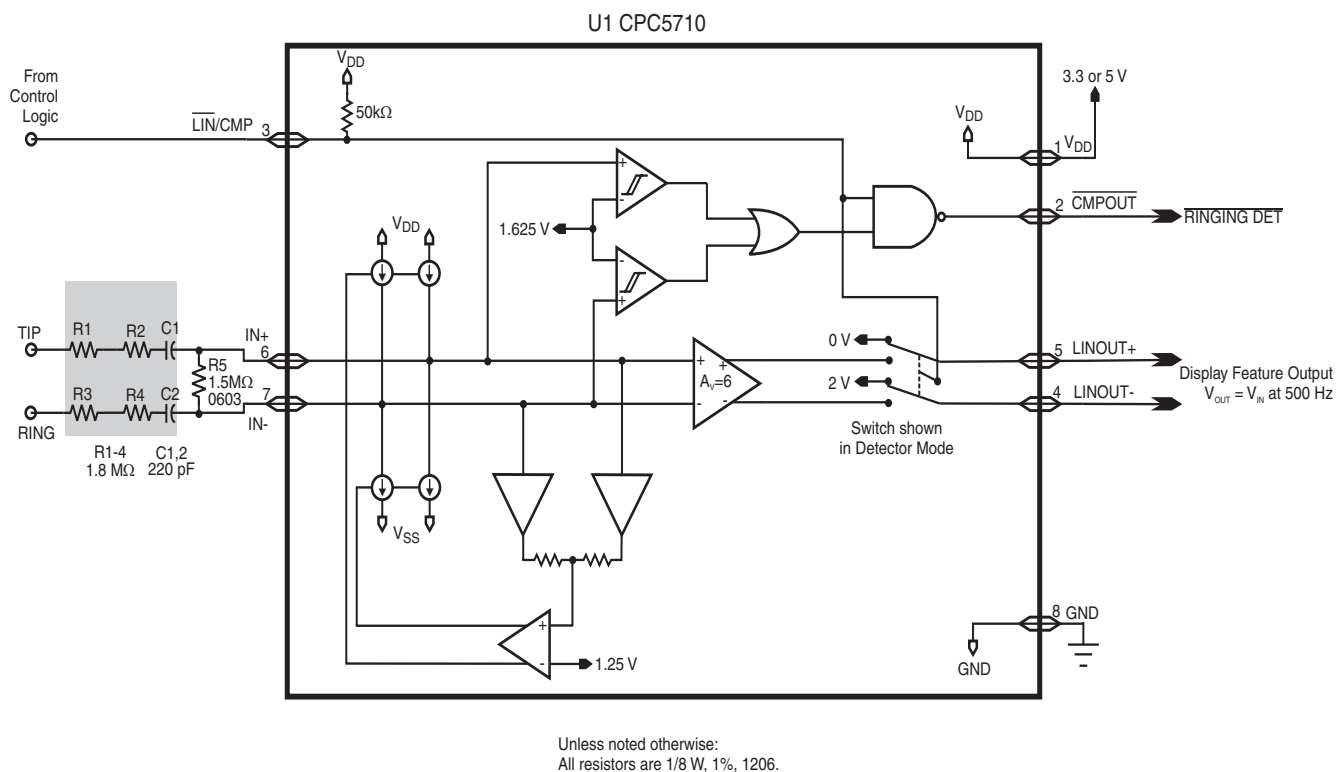
This application uses the logic input  $\overline{\text{LIN}}/\text{CMP}$  to select between ringing detection or buffering display feature (caller-ID) and voice signals. Note the AC coupling of the tip and ring signals.

With this circuit, setting  $\overline{\text{LIN}}/\text{CMP}$  to a logic high enables the ringing detector.

period, configure  $\overline{\text{LIN}}/\text{CMP}$  with a logic low to couple the audio frequency signal to the output pins.

Please see “Detector Considerations” on page 5 for more information on ringing detection.

**Figure 6. Non-Intrusive Line Monitoring, Display Feature (Caller ID) Signal Reception, and Ringing Detection Application Circuit**



#### 3.2.1 Frequency Response

The blocking capacitors used in this application circuit affect the frequency response of the system. With the components shown, response rolls off 3dB @ 166Hz. Other values can be used for different response characteristics.

### 3.3 Regulatory Issues

Component sizing and value recommendations shown in the application circuits above will need to be reviewed with regard to the regulatory and safety requirements for each particular application.

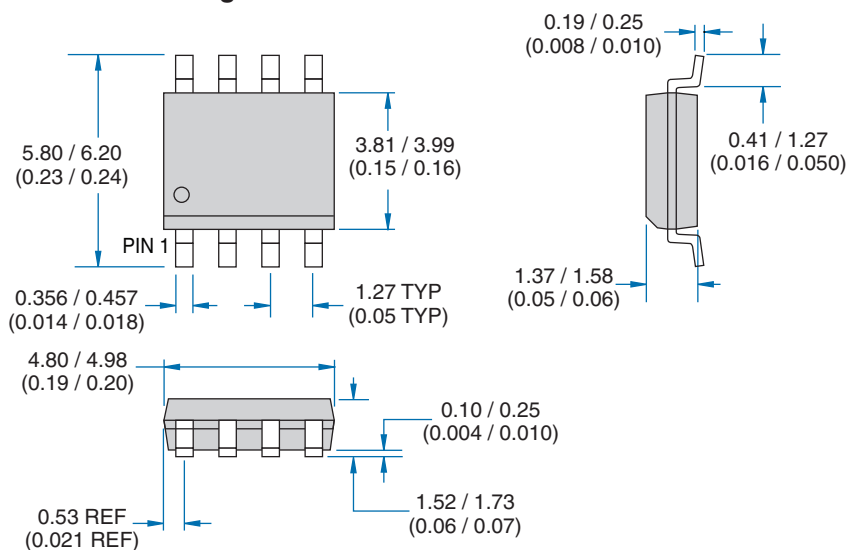
## 4. Manufacturing Information

Note that the CPC5710N branding (package imprinting) leaves off the last character of the part number, the letter "N," due to package space limitations.

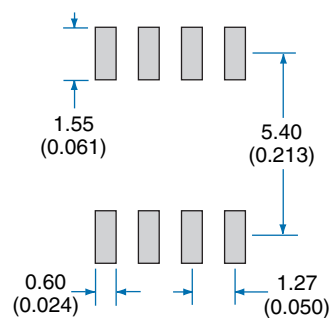
### 4.1 Mechanical Dimensions

#### 4.1.1 8-Pin SOIC Package

##### 8-Pin SOIC Package



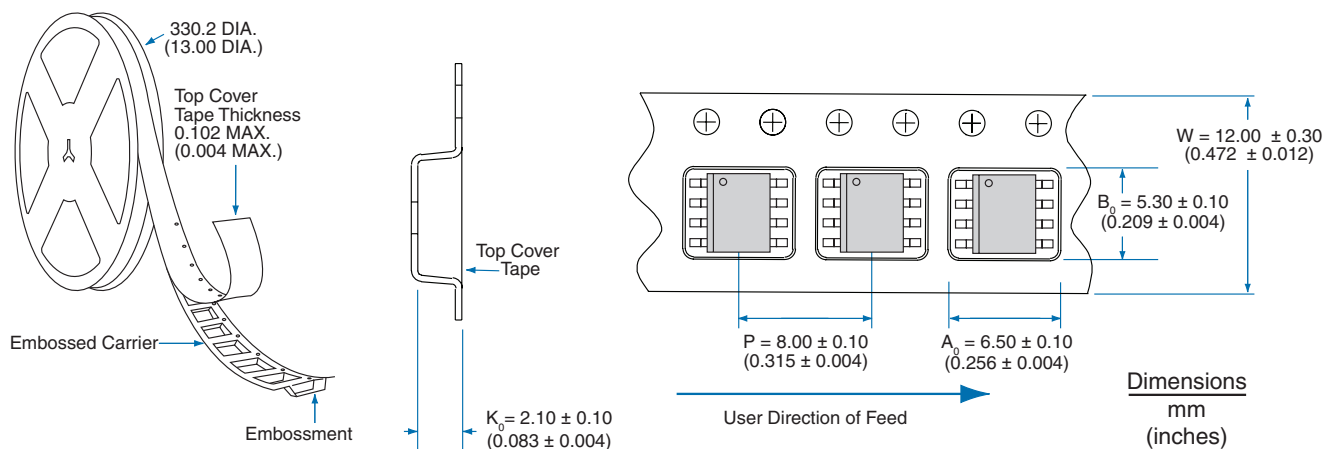
##### Recommended PCB Land Pattern



Dimensions  
mm  
(inches)

#### 4.1.2 Tape and Reel Specifications

##### Tape and Reel Packaging for 8-Pin SOIC Package



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

## 4.2 Soldering

For proper assembly, the component must be processed in accordance with the current revision of IPC/JEDEC standard J-STD-020. Failure to follow the recommended guidelines may cause permanent damage to the device resulting in impaired performance and/or a reduced lifetime expectancy.

## 4.3 Washing

Clare does not recommend ultrasonic cleaning of this part.



For additional information please visit [www.clare.com](http://www.clare.com)

*Clare, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. Neither circuit patent licenses or indemnity are expressed or implied. Except as set forth in Clare's Standard Terms and Conditions of Sale, Clare, Inc. assumes no liability whatsoever, and disclaims any express or implied warranty relating to its products, including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.*

*The products described in this document are not designed, intended, authorized, or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or where malfunction of Clare's product may result in direct physical harm, injury, or death to a person or severe property or environmental damage. Clare, Inc. reserves the right to discontinue or make changes to its products at any time without notice.*

Specification: DS-CPC5710 - R02  
© Copyright 2008, Clare, Inc.  
All rights reserved. Printed in USA.  
8/7/08