Replacing Spansion S25FL512S with Macronix MX66L51235F

1. Introduction

This application note compares the Macronix MX66L51235F and Spansion S25FL512S serial flash devices. This document does not provide detailed information on each individual device, but highlights the similarities and differences between them. The comparison covers the general features, performance, packaging, command set, and other parameters.

The information in this document is based on datasheets listed in Section 9. Newer versions of the datasheets may override the contents of this document.

2. Feature Comparison

Both flash device families have similar features and functions as shown in Table 2-1. Significant differences are highlighted in blue.

Table 2-1: Features

Feature	Macronix MX66L51235F	Spansion S25FL512S
Supply Voltage Range	2.7V ~ 3.6V	2.7V~3.6V / 1.65~3.6V VIO(4)
READ (1-1-1) (1)	Yes	Yes
FAST_READ (1-1-1)(1)	Yes	Yes
DREAD/DOR (1-1-2)(1)	Yes	Yes
2READ/DIOR (1-2-2)(1)	Yes	Yes
QREAD/QOR (1-1-4)(1)	Yes	Yes
4READ/QIOR (1-4-4)(1)	Yes	Yes
QPI (4-4-4)(1)	Yes	-
DDR (Double Data Rate)	-	Yes
Page Program Size	256B	512B
Sector Size	4KB	-
Block Size	32KB and 64KB	256KB
Security OTP Size	512B	1024B
Program/Erase Suspend & Resume	Yes	Yes
Read Burst Mode	Yes	-
Adjustable Output Driver	Yes	-
FastBoot/AutoBoot Mode	Yes	Yes
Configurable Dummy Cycles	Yes	Yes
S/W Reset Command	Yes	Yes
HOLD# Pin	-	Yes
RESET# Pin	Yes	Yes(2)
Advanced Sector Protection	Yes	Yes
Manufacturer ID	C2h	01h
Device ID	20h/1Ah	02h/20h
Package(3)	16-SOP (300mil) 8-WSON (8x6mm) 24-BGA (5x5 ball)	16-PIN SOP (300mil) - 24-BGA (5x5 ball)

Note:

1. x-y-z in I/O mode indicates the number of active pins used for op-code(x), address(y) and data(z).

2. Macronix offers the RESET# pin in all packages, but Spansion only offers the RESET# pin in 16-SOP and 24-BGA packages.
3. See datasheet for full list of packages available.
4. VIO support not offered in all package options. See datasheet ordering information.

3. Performance Comparison

Tables 3-1 and 3-2 show MX66L51235F and S25FL512S AC performance.

Table 3-1: Read Performance

Parameter		Macronix MX66L51235F	Spansion S25FL512S
Normal Read		50MHz	50MHz
Fast Read	1-1-1	104MHz(1)	133MHz
DREAD	1-1-2	104MHz	104MHz
2READ	1-2-2	84MHz(2)	104MHz
QREAD	1-1-4	104MHz	104MHz
4READ	1-4-4	84MHz(2)	104MHz
tCLQV / tV	15pf	7ns	6.5ns(3.0V-3.6V)
	30pf	9ns	8ns

Note:
1. *MX66L51235F Fast Read runs up to 104MHz with default dummy cycles and 133MHz with 10 dummy cycles.*
2. *MX66L51235F Multi I/O runs up to 104MHz with 8 dummy cycles and 133MHz with 10 dummy cycles.*
3. *All values in Table 3-1 are maximum.*

Table 3-2: Write Performance

Parameter		Macronix MX66L51235F	Spansion S25FL512S
Erase	4KB	43ms	-
	32KB	190ms	-
	64KB	340ms	-
	256KB	-	520ms
Chip Erase / Bulk Erase		120s	103s
Program	Byte	12us	-
	Page	600us (256B)	340us(512B)
Program/Erase Cycles (Endurance)		100,000	100,000

Note: All values in Table 3-2 are typical.

4. DC Characteristics

Both flash series characteristics are similar in primary features and functions. However, there are minor differences in DC characteristics which should be evaluated to determine their significance.

Table 4-1: Read / Write Current

Parameter	Macronix MX66L51235F	Spansion S25FL512S
Read Current @ 1xI/O	30mA @ 84MHz	16mA @ 50MHz
Standby Current	200uA	100uA
Deep Power Down Current	40uA	N/A
Write Current	50mA	100mA

Note: All values in Table 4-1 are maximum.

Table 4-2 compares I/O voltage levels between the two families. Spansion supports a Versatile I/O Voltage on some package options while Macronix does not.

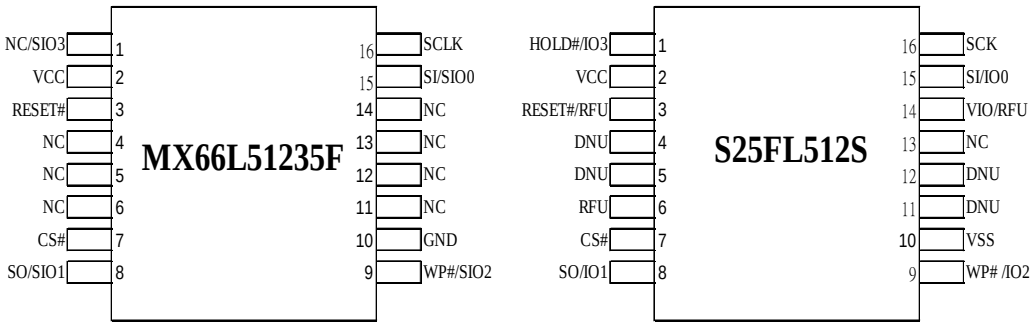
Table 4-2: Input / Output Voltage

Parameter	Macronix MX66L51235F	Spansion S25FL512S
VIO Voltage	-	1.65V ~ VCC+200mV
Input Low Voltage	-0.5V (min.) / 0.8 (max.)	-0.5V (min.) / 0.2VIO(max.)
Input High Voltage	0.7VCC (min.) / VCC+0.4V (max.)	0.7VIO (min.) / VIO+0.4V (max.)
Output Low Voltage	0.2V (max.)	0.15VIO (max.)
Output High Voltage	VCC-0.2 (min.)	0.85VIO (min.)

5. Hardware Consideration

The pin assignments of the 16-SOP and 24-BGA packages are identical, with the exception of the VIO and HOLD# pin functions which are unavailable on the Macronix chips. The figures below show the common packages and the pin assignments for the Macronix and Spansion devices.

16-SOP (300mil)

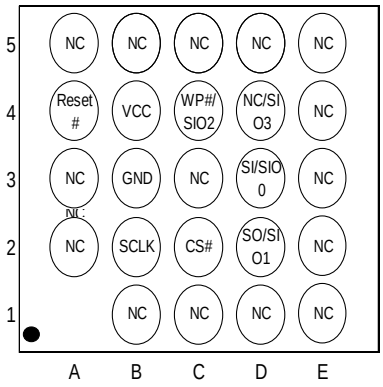


Reset# signal is internal pull high

DNU means Do Not Use
RFU means Reserve for Future Use
Reset# and Hold# signals are internal pull high

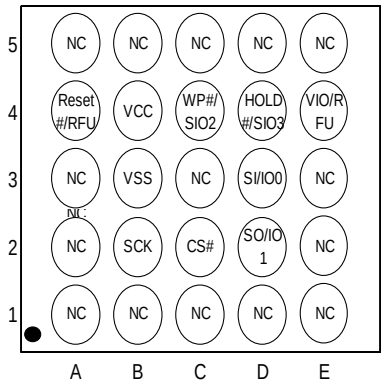
24-BGA (5x5 ball)

MX66L51235F



Reset# signal is internal pull high

S25FL512S



Reset# and Hold# signals are internal pull high

6. Software Considerations

Basic command set and 4-Byte command set of both flash families are similar. Status Register and Configuration Register definitions are slightly different. Minor algorithm modifications may be necessary depending on your application. The most common commands are the same as shown in Tables 6-1 and 6-2. Notable differences are highlighted in blue in Table 6-3.

Table 6-1: Core Command Set Comparison

Instruction Type	Instruction		Description	Op-code	
	Macronix MX66L51235F	Spansion S25FL512S		Macronix MX66L51235F	Spansion S25FL512S
Read	READ	READ	Normal Read	03h	03h
	FAST_READ	FAST_READ	Fast Read (1-1-1)	0Bh	0Bh
	DREAD	DOR	1I/2O Read (1-1-2)	3Bh	3Bh
	2READ	DIOR	2xI/O Read (1-2-2)	BBh	BBh
	QREAD	QOR	1I/4O Read (1-1-4)	6Bh	6Bh
	4READ	QIOR	4xI/O Read (1-4-4)	EBh	EBh
Write	WREN	WREN	Write Enable	06h	06h
	WRDI	WRDI	Write Disable	04h	04h
	PP	PP	Page Program	02h	02h
	SE 4K	P4E	Sector Erase	20h	20h
	BE	SE	Block Erase 64KB/256KB(1)	D8h (64KB)	D8h (256KB)
	CE	BE	Chip Erase / Bulk Erase	60h or C7h	60h or C7h
Read ID	RDID	RDID	Read Identification	9Fh	9Fh
Register	RDSR	RDSR1	Read Status Register	05h	05h
	WRSR	WRR	Write Status & Configuration Registers	01h	01h

Notes:

1. *Block Erase command D8h erases 64KBytes on the MX66L51235F, but erases 256KBytes on the S25FL512S.*

Table 6-2: 4-Byte Command Set Comparison

Instruction Type	Instruction		Description	Op-code	
	Macronix MX66L51235F	Spansion S25FL512S		Macronix MX66L51235F	Spansion S25FL512S
Write	READ4B	4READ	Normal Read	13h	13h
	Fast Read4B	4FAST_READ	Fast Read (1-1-1)	0Ch	0Ch
	DREAD4B	4DOR	1I/2O Read (1-1-2)	3Ch	3Ch
	2READ4B	4DIOR	2xI/O Read (1-2-2)	BCh	BCh
	QREAD4B	4QOR	1I/4O Read (1-1-4)	6Ch	6Ch
	4READ4B	4QIOR	4xI/O Read (1-4-4)	ECh	ECh
	PP4B	4PP	Page Program (1-1-1)	12h	12h
	-	QPP4B	Quad Page Program (1-1-4)	-	34h
	4PP4B	-	Quad Input Page Program (1-4-4)	3Eh	-
	SE4B	4P4E	Sector Erase	21h	21h
	BE4B	4SE	Block Erase 64KB	DCh	DCh

Notes: Address fields are 4-Bytes.

Table 6-3: Command Comparison

Instruction Type	Instruction		Description	Op-code	
	Macronix MX66L51235F	Spansion S25FL512S		Macronix MX66L51235F	Spansion S25FL512S
Other	EN4B	-	Enter 4-Byte Mode	B7h	-
	EX4B	-	Exit 4-Byte Mode	E9h(2)	-
	RSTEN	-	Reset Enable	66h	-
	RST	RESET	Software Reset Memory	99h	F0h
	-	MBR	Mode Bit Reset	FFh	FFh
	EQIO	-	Enable QPI	35h(2)	-
	-	CLSR(1)	Clear Status Register Fail Flags	-	30h(2)
	PGM/ERS Suspend	PGSP	Program Suspend	B0h	85h
	PGM/ERS Resume	PGRS	Program Resume	30h(2)	8Ah
	PGM/ERS Suspend	ERSP	Erase Suspend	B0h	75h
	PGM/ERS Resume	ERRS	Erase Resume	30h(2)	7Ah
	RDSFDP	-	Read SFDP	5Ah	5Ah
	REMS	REMS	Read Electronic Manufacturer Signature	90h	90h
	RES	RES	Read Electronic ID	ABh	ABh
Write	-	QPP	Quad Page Program (1-1-4)	-	32h or 38h(2)
	4PP	-	Quad Page Program (1-4-4)	38h(2)	-
		OTPP	OTP Program	-	42h
		OTPR	OTP Read	-	4Bh
	ENSO	-	Enter Secured OTP	B1h	-
	EXSO	-	Exit Secured OTP	C1h	-
Register	-	RDSR2	Read Status Register-2	-	07h
	RDCR	RDCR	Read Configuration Register	15h(2)	35h(2)
	RDSCUR	-	Read Security Register	2Bh(2)	-
	WRSCUR	-	Write Security Register	2Fh(2)	-
	ESFBR	-	Erase Fast Boot Register	18h	-
	RDFBR	ABRD	Read FastBoot/AutoBoot Register	16h(2)	14h
	WRFBR	ABWR	Write FastBoot/AutoBoot Register	17h(2)	15h(2)
Advanced Sector Protection	RDDPB	DYBRD	Read DPB (DYB) Register	E0h	E0h
	WRDPB	DYBWR	Write DPB (DYB) Register	E1h	E1h
	RDSPB	PPBRD	Read SPB (PPB) Status	E2h	E2h
	WRSPB	PPBP	SPB (PPB) Bit Program	E3h	E3h
	ESSPB	PPBE	Erase All SPB (PPB)	E4h	E4h
	RDDPB	DYBRD	Read DPB (DYB) Register	E0h	E0h
	WRLR	ASPP	Write Lock Register (Advanced Sector Protection Register)	2Ch	2Fh(2)
	RDLR	ASPRD	Read Lock Register (Advanced Sector Protection Register)	2Dh	2Bh(2)
	RDPASS	PASSRD	Read Password Register	27h	E7h
	WRPASS	PASSP	Write Password Register	28h	E8h
	PASSULK	PASSU	Password Unlock	29h	E9h(2)
	WPSEL	-	Write Protect Selection	68h	-

1. *MX66L51235F devices automatically clear the program or erase fail flags and do not have an explicit command to do so.*
2. *MX66L51235F and S25FL512S devices share the same command opcode, but the command function is different.*

6-1. Page Program Length Alignment

Page program maximum lengths are different between the MX66L51235F and the S25FL512S. Software modification is necessary if the longer page program length is being used. The Page Program length should be set to a maximum of 256 bytes and the 1 to 256 bytes to be programmed must fall within the same 256-Byte page boundary.

6-2. Sector Sizes

The MX66L51235F has uniform 64KB blocks that are each subdivided into two 32KB blocks and sixteen 4KB sectors. The S25FL512S has uniform 256KB blocks. Software adjustments are needed to accommodate the smaller blocks provided by the MX66L51235F. Please refer to the datasheets listed in Section 9 for memory organization details.

6-3. Secure OTP Differences

Both device families provide a secure One Time Programmable (OTP) area outside of the main memory array for user defined storage. The sizes, features, and access methods are different.

The S25FL512S has commands to directly read (OTPR) and program (OTPW) the OTP area and does not need to explicitly open this area for read and write operations.

The MX66L51235F operates in the OTP area using normal read and program instructions after explicitly opening the OTP area with the Enter Secured OTP (ENSO) command. While the OTP area is open, the main array is not accessible. When finished in the OTP area, the Exit Secure OTP (EXSO) command must be issued to return to the Read Main Array mode. The MX66L51235F OTP area has 512 bytes available for user data. The user may permanently lock the whole OTP area to prevent new data from being stored there. This area can optionally be programmed with user supplied data and factory locked by Macronix.

6-4. Block Protection Mode

The S25FL512S and the MX66L51235F use Status Register BP (Block Protect) bits to software write protect areas of memory. The S25FL512S only has three BP bits (BP2-BP0) and the granularity of the protected areas is very large. The MX66L51235F uses four BP bits (BP3-BP0) and provides a finer protection area granularity.

6-5. Advanced Sector Protection Mode

Both device families offer an Advanced Sector Protection mode used to provide volatile and nonvolatile individual sector (or block) protection and an optional password protection mode, but there are differences that need to be accommodated if this feature is used.

6-6 Status Register, Configuration Register, and Security Register

Both devices use registers to configure the flash for operation modes, but there are some differences that designers need to be aware of as software modifications may be needed. A detailed register comparison is shown in Table 6-4, Table 6-5, and Table 6-6. If a detailed functional description of register bits is required, please refer to the datasheets listed in Section 9.

Table 6-4: Status Register

Register Bit	Macronix MX66L51235F	Spansion S25FL512S
Bit0	WIP; 1=write operation	WIP; 1=write operation
Bit1	WEL; 1=write enable	WEL; 1=write enable
Bit2	BP0; BP protection	BP0; BP protection
Bit3	BP1; BP protection	BP1; BP protection
Bit4	BP2; BP protection	BP2; BP protection
Bit5	BP3; BP protection	E_ERR; 1=erase fail[*1]
Bit6	QE; 1=Quad mode enable	P_ERR; 1=program fail[*1]
Bit7	SRWD; 1=SR write disable	SRWD; 1=SR write disable

Note:
1. Macronix MX66L51235F Program and Erase Error bits are located in bits 5 and 6 of its Security Register.

Table 6-5: Configuration Register

Register Bit	Macronix MX66L51235F	Spansion S25FL512S
Bit0	ODS0; Output driver strength	FREEZE; 1=BPx write disable
Bit1	ODS1; Output driver strength	QUAD; 1=Quad mode enable
Bit2	ODS2; Output driver strength	RFU
Bit3	TB; 1=Bottom area protect	BPNV; 1=BPx is Volatile
Bit4	Reserved	RFU
Bit5	4 BYTE; 1=4byte address	TBPROT; 1=boot array protect
Bit6	DC0; Dummy cycle	LC0; Latency cycle
Bit7	DC1; Dummy cycle	LC1; Latency cycle

Table 6-6: Security Register

Register Bit	Macronix MX66L51235F	Spansion S25FL512S
Bit0	4Kb Secured OTP; 1=factory lock	PS; 1=Program suspend
Bit1	LDSO; 1=OTP lock down	ES; 1=Erase suspend
Bit2	PSB; 1=Program suspend	RFU
Bit3	ESB; 1=Erase suspend	RFU
Bit4	Reserved	RFU
Bit5	P_FAIL; 1=Program fail	RFU
Bit6	E_FAIL; 1=Erase fail	RFU
Bit7	WPSEL; 1=Individual WP	RFU

6-7. Manufacturer and Device Identification Numbers

Table 6-7 compares the Manufacturer and Device IDs returned by the RDID and REMS commands.

Table 6-7: Manufacturer and Device ID

Command Type	Macronix MX66L51235F	Spansion S25FL512S
RDID 9Fh	C2h/20h/1Ah	01h/02h/20h
REMS 90h	C2h/19h	01h/19h

7. Address Protocol Support

7-1. Addressing Memory Beyond 16MBytes

Both devices support various methods to address memory beyond 128Mb (16MBytes). Some of the methods employed are different, but the concepts are the same. Depending on the application, the software may require minor modifications. Please refer to the datasheets listed in Section 9 for more details.

7-1-1. 4-Byte Address Mode

4-Byte Address mode uses the legacy command set but the address field is 4-Bytes instead of 3-Bytes. The Macronix device uses the EN4B and EX4B commands to enter and exit 4-Byte address mode. On the Spansion device, 4-Byte address mode is entered or exited by setting or clearing bit-7 in the Bank Address Register (BAR). After making the mode selection, the appropriate number of address bytes (3-Byte or 4-Byte) must be used for all commands that require an address argument (with the exception of the Read SFDP command (5Ah), which always uses 3-Byte addressing).

7-1-2. Bank Address Mode

Bank Address Mode uses one or more of the low-order bits of a bank address register to supply address bits A24 and above for legacy read, program, and erase commands that use 3-Byte addressing. The serial flash internally appends the low-order bits from the bank address to the 3-Byte address to form an extended address. This allows access to addresses beyond 128Mb while still using the legacy command set and 3-Byte addressing. In Spansion devices the bank register is the BAR. In Macronix devices the bank address register is the Extended Address Register (EAR).

7-1-3. 4-Byte Address Command Set

Both Macronix and Spansion devices support a 4-Byte Address Command Set which always uses 4-Bytes of address, eliminating the need to enter or exit 4-Byte Address mode. The 4-Byte Address Command Set (see Table 6-2) supplements the legacy 3-Byte command set.

8. Summary

The Macronix MX66L51235F and Spansion S25FL512S have similar commands, functions, and features. Additionally, the supported package types have identical footprints and nearly identical pin out definitions. Software modification may be needed to accommodate to differences in the page program size and the block erase size. Additional software modification may be needed due to differences in status and configuration register bit assignments and the commands used to access them. A more detailed analysis should be done if functions such as Advanced Sector Protection, HOLD# pin, VIO voltage, DDR, or AutoBoot are used.

9. References

Table 9-1 shows the datasheet versions used for comparison in this application note. For the most current, detailed specification, please refer to the Macronix Website at http://www.macronix.com

Table 9-1: Datasheet Version

Datasheet	Location	Data Issued	Version
MX66L51235F	Website	AUG. 08, 2012	Rev. 0.00
S25FL512S	Website	MAR. 2, 2012	Rev. 02

10. Appendix

Table 10-1 shows the basic part number and package information cross reference between Macronix MX66L51235F and Spansion S25FL512S parts.

Table 10-1: Part Number Cross Reference

Density	Macronix Part No.	Spansion Part No.	Package	Dimension
512Mb(1)	MX66L51235FMI-10G	S25FL512SAGMFI/01/G1/R1(1)/(2) S25FL512SDPMFIG1(1)/(2)	16-SOP	300 mil
	MX66L51235FZ2I-10G	-	8-WSON	8x6mm
	MX66L51235FXDI-10G	S25FL512SAGBHI/21/A1/C1(1)/(3) S25FL512SDPMFIC1(1)/(3)	24-BGA	5x5 ball

Note:

1. *AG: 133MHz; DP: DTR 66MHz;*
2. *01: 16-SOP/8-WSON with 256KB sector; G1: 16-SOP with RESET# & 256KB sector; R1: 16-SOP with RESET#, VIO & 256KB sector.*
3. *21: 24-BGA with 256KB sector; A1: 24-BGA with RESET# & 256KB sector; C1: 24-BGA with RESET#, VIO & 256KB sector.*

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