POWER
MANAGEMENT

Marvell Solutions

88PG877 Family
Field Programmable DSP Switcher™

1 MHz, 7.5A Peak Current-Limit Step-Down Regulator with AnyVoltage™ Technology

Advance Datasheet, Patent Pending

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Document Status	
Advance Information	This document contains design specifications for initial product development. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
Preliminary Information	This document contains preliminary data, and a revision of this document will be published at a later date. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
Final Information	This document contains specifications on a product that is in final release. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
Revision Code: Rev. B	
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Overview

The 88PG877 device intelligent digital synchronous Step-Down (Buck) switching regulator housed in a 4 X 3 mm QFN-18 package. Internally self-compensated, these step-down regulators require no external compensation and work with low-ESR output capacitors to simplify the design, minimize board space, and reduce the amount of external components. The switching frequency for the step-down regulator is 1 MHz, allowing the use of low profile surface mount inductors and low value capacitors. The step-down regulator includes programmable output voltage to provide the user the ability to easily set the output voltage with external resistors, logic control, or serial data interface. The output voltage range is 0.72V to 3.63V.

Other key features of the 88PG877 family include soft start, an internal current limit, an undervoltage lockout, thermal shutdown, over voltage protection, and a Power-On Reset (POR) signal.

Features

- Tiny 4 X 3 mm QFN-18 package
- 1 MHz Switching frequency
- Low quiescent current of mA (typ.)
- Stable with ceramic output capacitors
- No external compensation required
- Over 95% efficiency
- Peak switch current limit up to 7.5A
- Input voltage range: 3.0V to 5.5V
- Serial / Logic Programmability
- Any Voltage™ Technology provides 64 output voltage selections to provide flexibility
- Programmable output voltage range:
  - 0.72V to 3.63V
- Built-in undervoltage lockout
- Over voltage protection
- Thermal shutdown protection
-
- Output voltage margining capability

Application

- Portable computing
- Disk drive power supplies
-

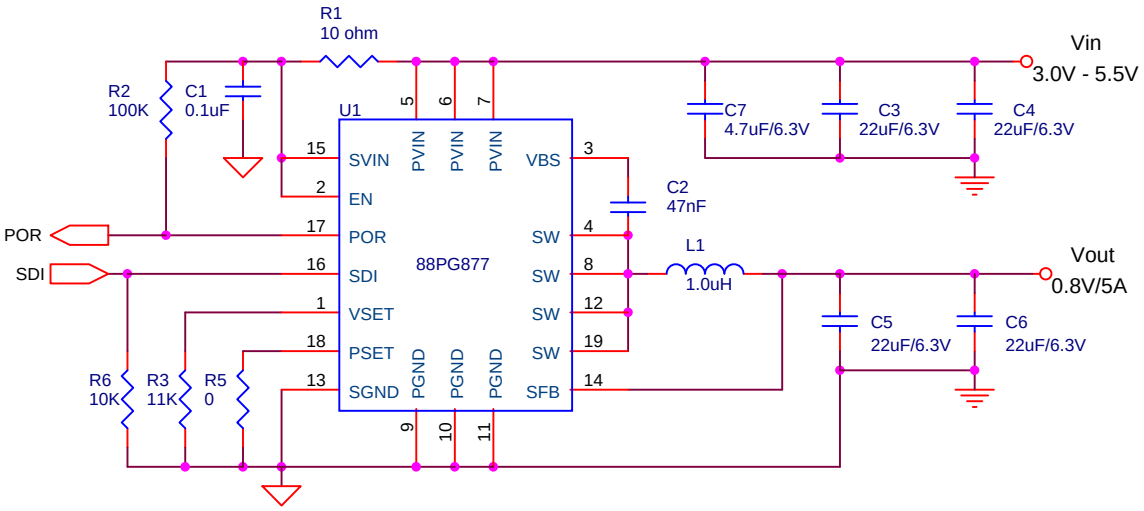

Figure 1: Typical High Efficiency 5V to 0.8V/5A Step-Down Regulator

Caution

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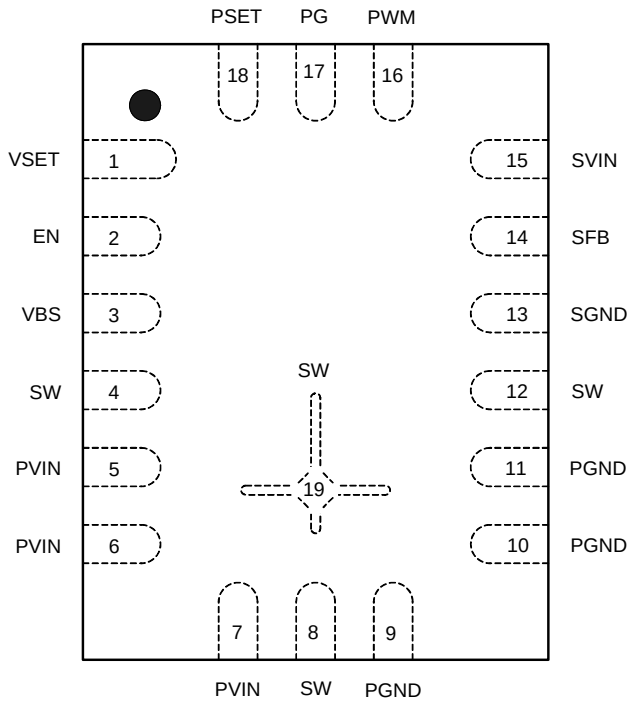
1.1 Pin Configuration

Figure 2: 88PG877 Family 4X3 mm QFN-18 Package - Top View



1.2 Pin Type Definitions

Table 1: Pin Type Definitions

Pin Type	Definitions
I	Input only
O	Output only
S	Supply
NC	Not Connected
GND	Ground

1.3 Pin Description

Table 2 provides pin descriptions for the 88PG877.

Table 2: Pin Description

Pin #	Pin Name	Pin Type	Pin Function
1	VSET	I	Voltage Set 1) This is used for selecting the output voltage level, when it is connected to SGND or SVIN in conjunction with PSET connection to SGND or SVIN. 2) Connect to an external resistor to ground to set the output voltage of the step-down switching regulator. See the “Electrical Characteristics” table for resistor values and Output Voltage Setting section. The total capacitance across this pin and SGND should be equal to 25 pF or less. Use resistors with tolerance
2	EN	I	
3	VBS	O	Bootstrap Voltage. Connect a 47 nF capacitor from this pin to SW.
4,8,12,	SW	O	Switch Node. Internal power MOSFET . This pin must connect to an external inductor.
5,6,7	PVIN	S	Power Input Voltage. Internal power MOSFET . Connect the decoupling capacitors between PVIN and PGND and position it as close as possible to the IC.
9,10,11	PGND	GND	Power Ground. The power ground must connect to the negative terminal of the input and output capacitors.
13	SGND	GND	Signal ground. This pin must connect to the power ground.
14	SFB	I	Switching Regulator Feedback. Senses the output voltage of the switching regulator.

Table 2: Pin Description (Continued)

Pin #	Pin Name	Pin Type	Pin Function
15	SVIN	S	Signal Input Voltage. The input voltage is V to 5.5V for internal circuitry. Connect a 0.1 µF decoupling capacitor between SVIN and SGND and position it as close as possible to the IC.
16	SDI	I	Serial Data Input: The input data into this pin is used to program the output voltage (see section 3.2). This pin must be connected to ground if not used.
17	P	O	Power-On Reset. Power-On Reset is an open drain output to indicate the status of the output voltage. The output pin goes high 40 ms after the output voltage is within the specified tolerance.
18	PSET	I	Percent Set 1) This is used for selecting the output voltage level when it is connected to SGND or SVIN in conjunction with VSET connection to SGND or SVIN. 2) Connect an external resistor to ground to set the output voltage of the step-down switching regulator. See the “Electrical Characteristics” table for resistor values and Output Voltage Setting section. Use resistor value with tolerance

Section 2. Electrical Specifications

2.1 Absolute Maximum Ratings[1]

Parameter	Symbol	Range	Units
Signal Input Voltage	S_{VIN}	-0.3 to 6.0	V
Power Input Voltage	P_{VIN}	-0.3 to 6.0	V
Switch Voltage	V_{SW}	-0.6 to (S_{VIN} +0.3)	V
			V
Switching Regulator Feedback Voltage	V_{SFB}	-0.6 to (S_{VIN} +0.3)	V
Voltage Set	V_{VSET}	-0.6 to (S_{VIN} +0.3)	V
Percentage Set Voltage	V_{PSET}	-0.6 to (S_{VIN} +0.3)	V
Shutdown Voltage	V	-0.6 to (S_{VIN} +0.3)	V
P Voltage	V_P	-0.6 to (S_{VIN} +0.3)	V
SDI Voltage	V_{SDI}	-0.6 to (S_{VIN} +0.3)	V
Operating Temperature Range[2]	T_{OP}	-40 to 85	°C
Maximum Junction Temperature	T_{JMAX}	125	°C
Storage Temperature Range	T_{STOR}	-65 to 150	°C
ESD Rating[3]		2	kV

1. Exceeding the absolute the maximum rating may damage the device.
2. Specifications over the –40 °C to 85 °C operating temperature ranges are assured by design, characterization and correlation with statistical process controls.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

2.2 Recommended Operating Conditions[1]

Parameter	Symbol	Range	Units
Signal Input Voltage	S_{VIN}	3.0 to 5.5	V
Power Input Voltage	P_{VIN}	3.0 to 5.5	V
Package Thermal Resistance[2]	θ_{JA}		°C/W
	θ_{JC}		°C/W

1. This device is not guaranteed to function outside the specified operating range.
2. Test on 3"x 4.5" 4-layer .

2.3 Electrical Characteristics

The following applies unless otherwise noted: S_{VIN} = P_{VIN} = V_{EN}= V_{VSET} = V_{PSET} = 5.0V, V_{OUT} = 1.5V, V_{SDI} = SGND = PGND, $L_{(BUCK)}$ = 1.0 µH, $C_{OUT\ (BUCK)}$ = 2 x 22 µF (Ceramic), T_A = 25 °C. **Bold values indicate -40 °C ≤ T_A ≤ 85 °C.**

Parameter	Symbol	Conditions	Min	Type	Max	Units
Signal Input Voltage Range	S_{VIN}	S_{VIN} = P_{VIN}	**3.0**		**5.5**	V
Power Input Voltage Range	P_{VIN}		**3.0**		**5.5**	V
Total Quiescent Current		No load				mA
Shutdown Supply Current	I_{SVIN}	V_{EN} = 0V		1	50	µA
Undervoltage Lockout	V_{UVLO}	High threshold, SV_{IN} increasing		2.85	3.00	V
		Low threshold, SV_{IN} decreasing				V
Over-voltage Protection	V_{OVP}	High threshold, SV_{IN} increasing		5.7		V
		Low threshold, SV_{IN} decreasing		5.6		V
Enable Threshold Voltage	V_{EN}	Enable regulators		P_{VIN}/2		V
Enable Hysteresis	V	Disable regulators				mV
Enable Pin Input Current	I_{EN}	V = 5.0V			5.0	µA
		V = 0V			5.0	µA
Over-temperature Thermal Shutdown	T_{OTS}	T_J increasing (Disable regulators)		150		°C
		T_J decreasing (Enable regulators)		120		°C

2.4 Switching Step-down Regulator

The following applies unless otherwise noted: S_{VIN} = P_{VIN} = V_{EN} =V_{VSET} = V_{PSET} = 5.0V, V_{OUT} = 1.5V, V_{SDI} = SGND = PGND, L = 1.0 µH, C_{OUT} = 2 x 22 µF (Ceramic), T_A = 25 °C. **Bold values indicate -40 °C ≤ T_A ≤ 85 °C**.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage	V_{OUT}	R_{VSET} = 11K, PWM mode		0.8		V
		R_{VSET} = 18.7K, PWM mode		1.0		
		R_{VSET} = 31.6K, PWM mode		1.2		
		R_{VSET} = 53.6K, PWM mode		1.5		
		R_{VSET} = 97.6K, PWM mode		1.8		
		R_{VSET} = 165K, PWM mode		2.5		
		R_{VSET} = 280K, PWM mode		3.0		
		R_{VSET} = 475K, PWM mode		3.3		
Percentage Set		R_{PSET} = 11K		-10		%
		R_{PSET} = 18.7K		-7.5		
		R_{PSET} = 31.6K		-5		
		R_{PSET} = 53.6K		-2.5		
		R_{PSET} = 97.6K		2.5		
		R_{PSET} = 165K		5		
		R_{PSET} = 280K		7.5		
		R_{PSET} = 475K		10		
Output Voltage Line Regulation	V_{LNREG}	P_{VIN} = 3.0V to 5.0V V_{OUT} = 1.5V I_{LOAD} = A		0.10		%
Output Voltage Load Regulation	V_{LDREG}	P_{VIN} = 5.0V V_{OUT} = 1.5V I_{LOAD} =		0.10		%
Switching Frequency	f_{SW}	I_{LOAD} = 2.5A		1.0		MHz
Minimum Peak Switch Current Limit	I_{LIM}			7.5		A
Output Current	I_{OUT}	L = 1.0 µH		5.0		A
Switch Leakage Current	I_{LSW}	P_{VIN} = V_{EN} = 0V		1	50	µA
		P_{VIN} = V_{EN} = 0V V_{SW} =		1		

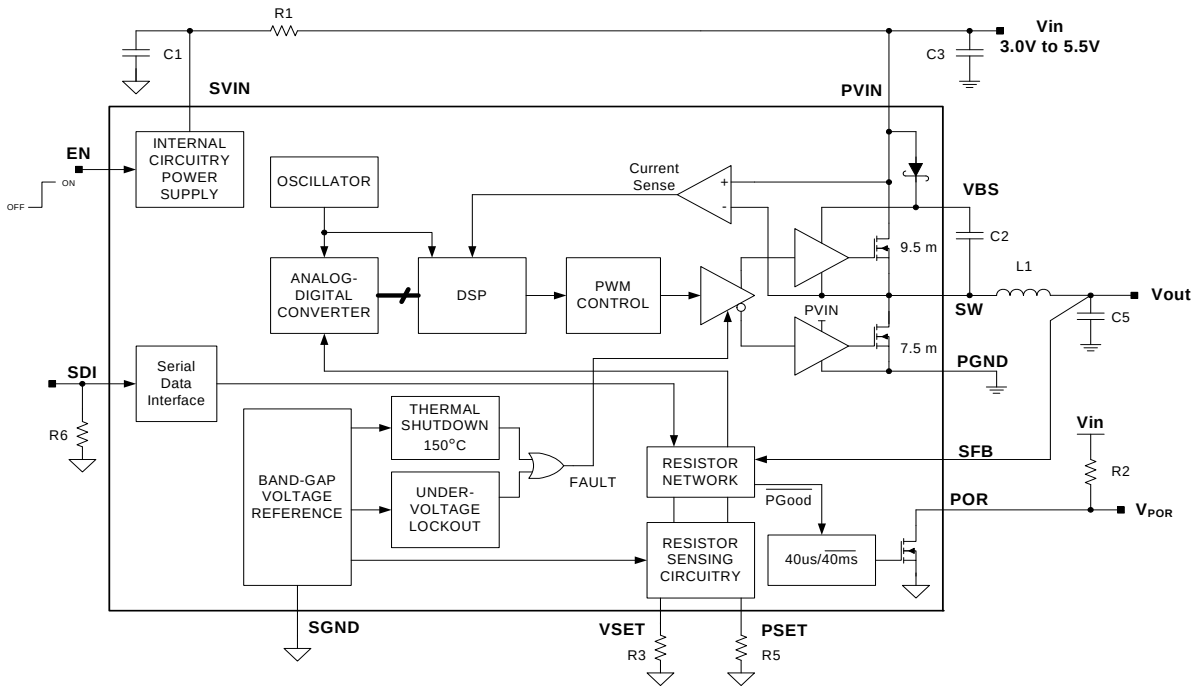
2.4 Switching Step-down Regulator

The following applies unless otherwise noted: S_{VIN} = P_{VIN} = V_{EN} =V_{VSET} = V_{PSET} = 5.0V, V_{OUT} = 1.5V, V_{SDI} = SGND = PGND, L = 1.0 µH, C_{OUT} = 2 x 22 µF (Ceramic), T_A = 25 °C. **Bold values indicate -40 °C ≤ T_A ≤ 85 °C**.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power-On Reset Threshold Voltage	V_{PORTH}	V_{OUT} ≥ 1.35V		V_{OUT}* 90%		V
		V_{OUT} < 1.32V		V_{OUT}- 130 mV		
Power-On Reset Output Low Voltage	V_{PORL}	I_{SINK} = 2 mA, V_{EN} = SGND = PGND			0.4	V
Power-On Reset Leakage Current	I_{POR}	V_{EN} = 0V		1		µA
Power-On Reset Delay	t_{RESET}			40		ms

Section 3. Functional Description

Figure 3: 88PG877 Block Diagram

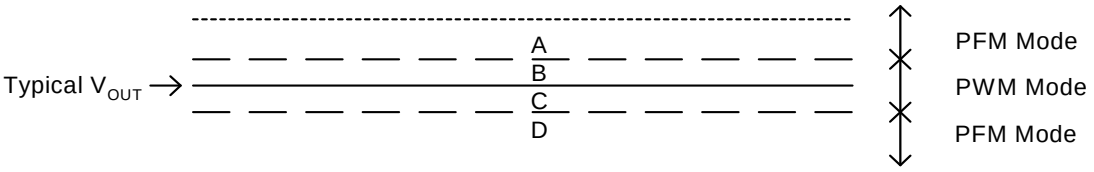


3.1 Regulation and Start-up

The step-down switching regulator uses Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM) modes to regulate the output voltage using digital control. The mode of operation depends on the level of output current and the output voltage.

In steady states, the step-down switching regulator monitors the current flowing through the inductor to determine if the regulator is handling heavy or light load applications. For heavy load applications, the step-down regulator operates in the PWM mode (B and C Figure 4) to minimize the ripple current for optimum efficiency and to minimize the ripple output voltage. The step-down regulator operates in the PFM and Discontinuous Conduction Mode (DCM) (A Figure 4) to limit the switching actions for optimum efficiency in light load applications. In this mode, the average output voltage is slightly higher than the average output voltage for heavy transient load applications.

Figure 4: Output Voltage Window



3.1.1 Digital Soft Start

During start-up, the 88PG877 provides a soft start function. Soft start reduces surge currents from input voltage and provides well-controlled output voltage rise characteristics. Figure 5 shows that the rise time for a 88PG877 increases from 20 µs at for a 0.8V output to 70 µs for a 3.3V output with a 20 mA load. Higher load current or larger output capacitance will increase the rise time. The load current is increased to 5A in Figure 6. The 3.3V output rise time nearly doubles to 130 µs with this load.

The 88PG877 has an internal switch current limit that operates on a cycle-by-cycle basis and limits the peak switch current. During soft start, the current limit threshold begins at approximately 34% of the peak current limit threshold and ramps to 100% in 7 steps at 25 µs per step (see Figure 7). During the switch first cycle, the high-side switch stays on until the switch current reaches the first current limit threshold (see Figure 8) which takes less than 1 µs. The high-side switch will then turn off for a fixed off-time. If the output voltage is still low in 25 µs, the current limit threshold increases to the next level. As can be seen from Figure 5, only 25 µs or 1 current step is required for the output to reach 0.8V and 75 µs or 3 current steps for 3.3V.

During soft start, the 88PG877 feeds a relatively constant current to the output capacitor in the first two steps. The average switch current during this period is approximately 2A. If more than 2 steps are required, then the switch current limit (I_{LIM}) will need to increase. The output voltage rise time is dependent on the value of the output capacitor, the output voltage, the load current (I_{OUT}), and the internal switch current limit circuitry and can be calculated using the following equation.

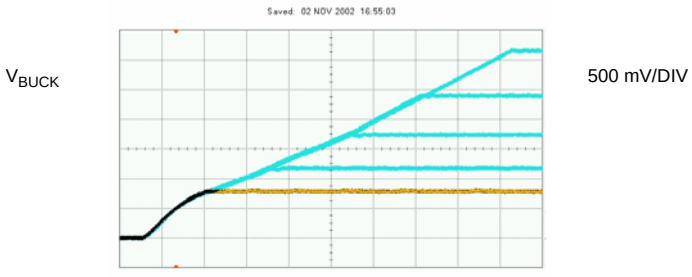
$$\text{RiseTime} = \frac{(C_{OUT} \bullet V_{OUT})}{(I_{LIM} - I_{OUT})}$$

$$= \frac{2 \bullet 22\mu F \bullet 3.3V}{2.0A - 0A}$$

$$= 72.6\mu S$$

Figure 5: Soft Startup

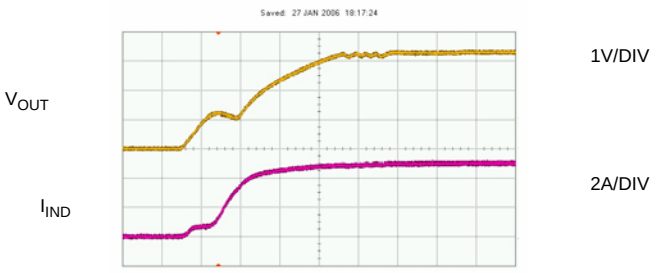
(0.8V, 1.2V, 1.8V, 2.5V, 3.3V)



I_{LOAD} = 20 mA

C_{OUT} = 2 x 22 µF

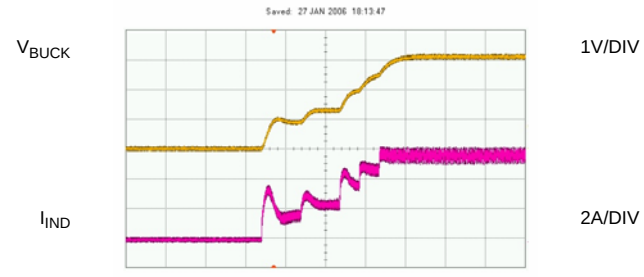
Figure 6: Soft Startup



V_{OUT} = 3.3V

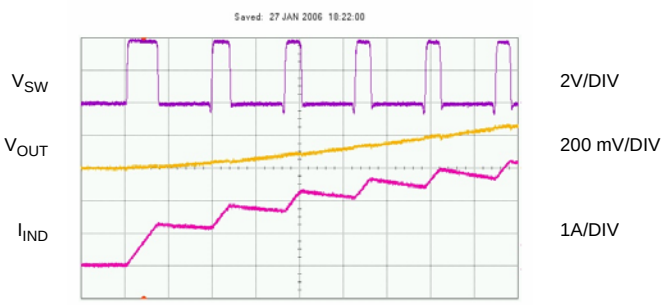
I_{LOAD} =

Figure 7: Inductor Current Steps at Startup



I_{LOAD} = Heavy Load

Figure 8: First Switching Cycle

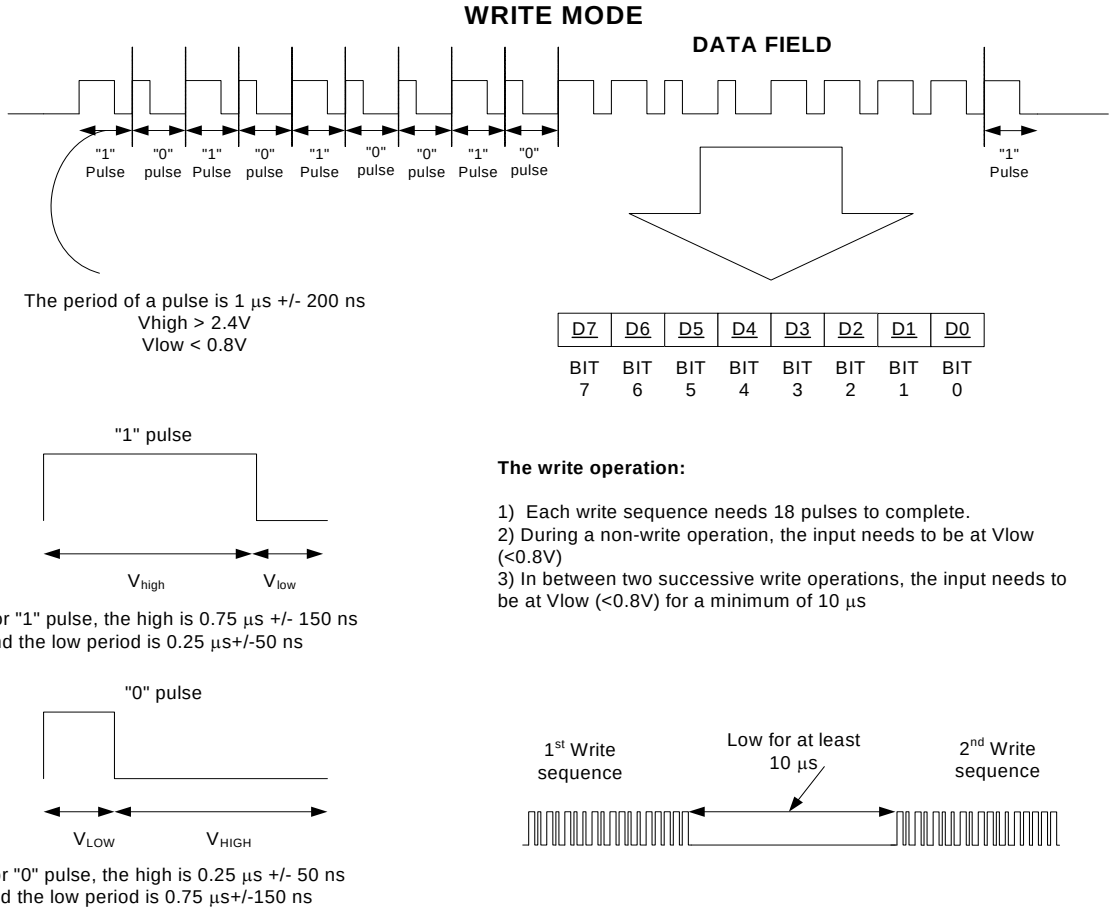


3.2 Output Voltage Setting

3.2.1 Serial Programmability

The output voltage of the step-down switching regulator can also be programmed by using 18-bit serial data into the SDI pin.

Figure 9: Serial Programmability



The first 4 bits (MSB-bits) of the data field are used to select the output voltage where the second 4 bits (LSB-bits) of the data field are used to trim the output voltage (percent of output voltage). The default value for the data field is as follows:

Table 3: Default Value of Data Field

	Data Field							
Description	Voltage Set				Percent Set			
Bits	7	6	5	4	3	2	1	0
Default Value	0	0	1	0	0	1	0	0

On power up, the output voltage is set according to R_{PSET} and R_{VSET}. The output voltage can then be field programmed by setting bit 3 and bit 7 to “1”. The output voltage and percent set are selected according to Table 4.

Table 4: Voltage and Percentage Set

	Data Field				V_{OUT} (V)	Data Field				Percent Set
Bits	7	6	5	4		3	2	1	0	
Value	1	0	0	0	0.8	1	0	0	0	-10%
	1	0	0	1	1.0	1	0	0	1	-7.5%
	1	0	1	0	1.2	1	0	1	0	-5.0%
	1	0	1	1	1.5	1	0	1	1	-2.5%
	1	1	0	0	1.8	1	1	0	0	+2.5%
	1	1	0	1	2.5	1	1	0	1	+5.0%
	1	1	1	0	3.0	1	1	1	0	+7.5%
	1	1	1	1	3.3	1	1	1	1	+10%

3.2.2 Logic Programmability

The output voltage of the step-down switching regulator can be programmed by connecting the VSET and PSET pins to SGND and/or SVIN. This can be very useful for standard output voltages. This method will eliminate the use of an external resistor to set the output voltage.

Table 5: Output Voltage Setting

V_{VSET}	V_{PSET}	V_{OUT}
SGND	SGND	0.8V
SGND	SVIN	1.0V
SVIN	SGND	1.2V
SVIN	SVIN	1.5V
SGND	11 kΩ ≤ R_{PSET} ≤ 475 kΩ	Hi-Z

3.2.3 Output Voltage – AnyVoltage™ Technology

The output voltage of the step-down switching regulator is programmed by using Table 6 or Table 7 to select resistor values for VSET and PSET pin. The VSET pin sets the output voltage and the PSET pin trims the set voltage to a percentage value. For example, to program 2.25V output, a 165 kΩ resistor is selected for the VSET pin, and an 11 kΩ resistor is selected for the PSET pin. The 165 kΩ resistor sets the output voltage to 2.5V and the 11 kΩ resistor trims the set voltage by -10%.

Using the VSET resistor's value greater than 619 kΩ or less than 7.68 kΩ disables the step-down switching regulator and sets the SW pin to high impedance. If the VSET resistor's value is outside the % tolerance, the output can be either higher or lower than the set voltage.

Using resistor values greater than 619 kΩ or less than 7.68 kΩ for the PSET pin does not affect the set voltage. When the PSET pin is not used, it must be connected to ground. Like the VSET resistor, the percent value can be either higher or lower if the PSET resistor's value is outside the % tolerance.

Table 6: Any Voltage Programming Table

		PSET								
		-10.0%	–7.5%	–5.0%	–2.5%	0%	2.5%	5.0%	7.5%	10.0%
		11k	18.7k	31.6k	53.6k	GND	97.6k	165k	280k	475k
VSET	11k	0.720	0.740	0.760	0.780	0.800	0.820	0.840	0.860	0.880
	18.7k	0.900	0.925	0.950	0.975	1.000	1.025	1.050	1.075	1.100
	31.6k	1.080	1.110	1.140	1.170	1.200	1.230	1.260	1.290	1.320
	53.6k	1.350	1.388	1.425	1.463	1.500	1.538	1.575	1.613	1.650
	97.6k	1.620	1.665	1.710	1.755	1.800	1.845	1.890	1.935	1.980
	165k	2.250	2.313	2.375	2.438	2.500	2.563	2.625	2.688	2.750
	280k	2.700	2.775	2.850	2.925	3.000	3.075	3.150	3.225	3.300
	475k	2.970	3.053	3.135	3.218	3.300	3.383	3.465	3.548	3.630

Table 7: Any Voltage Programming Table for 5% Resistors

		PSET								
		-10.0%	–7.5%	–5.0%	–2.5%	0%	2.5%	5.0%	7.5%	10.0%
		11k				GND				
VSET	11k	0.720	0.740	0.760	0.780	0.800	0.820	0.840	0.860	0.880
		0.900	0.925	0.950	0.975	1.000	1.025	1.050	1.075	1.100
		1.080	1.110	1.140	1.170	1.200	1.230	1.260	1.290	1.320
		1.350	1.388	1.425	1.463	1.500	1.538	1.575	1.613	1.650
		1.620	1.665	1.710	1.755	1.800	1.845	1.890	1.935	1.980
		2.250	2.313	2.375	2.438	2.500	2.563	2.625	2.688	2.750
		2.700	2.775	2.850	2.925	3.000	3.075	3.150	3.225	3.300
		2.970	3.053	3.135	3.218	3.300	3.383	3.465	3.548	3.630

The VSET and PSET resistors are read once during start-up before the output voltage is turned on. After the output voltage is turned on, the output voltage can change to different values using serial programming interface. Otherwise to configure the output to a different voltage, power has to recycle or the 88PG877 has to turn OFF and back ON using the EN pin.

Figure 10 shows the startup waveforms of the 88PG877. Once the input voltage (V_{IN}) is above the under voltage lockout (UVLO) upper threshold (UTH), the VSET and PSET pin becomes active. Current is first sourced out of PSET pin and then the VSET pin, in exponentially increasing steps. After each step there is a blanking time before the VSET voltage is compared to an internal 1.2V reference. If the VSET voltage is below internal reference voltage, the current source proceeds to the next step. Once the VSET voltage is above the internal reference voltage the sequence stops and the output voltage (VOUT) is allowed to turn on. Figure 11 shows the VSET waveform for VSET = 2.5V and PSET = –5% output. The 88PG877 keeps track of how many steps are required to determine the appropriate output voltage. Table 8 provides the number of steps necessary for each output voltage option. Using a VSET resistor of 165 kΩ requires the current source to step 4 times, and a PSET resistor of 31.6 kΩ requires 7 steps.

Figure 10: Startup Sequence

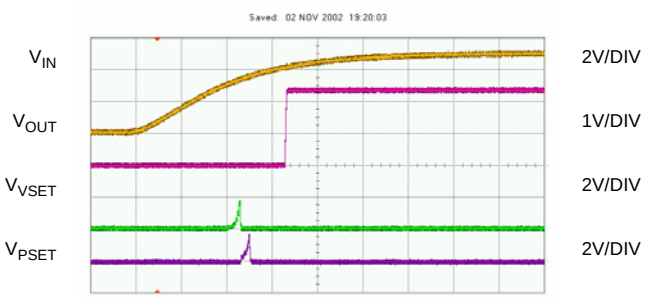


Figure 11:

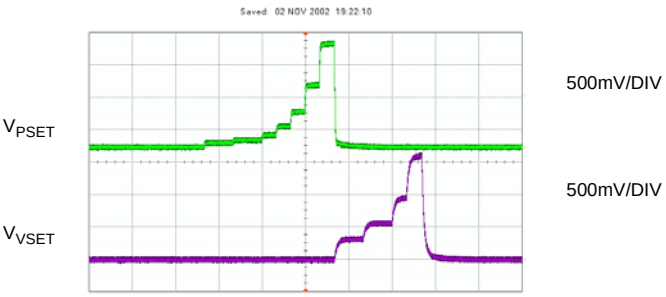


Table 8: Output Voltage Option Steps

Step	VOUT (V)	R_{VSET} (kΩ)
1	0	>619K[1]
2	3.3	475
3	3.0	280
4	2.5	165
5	1.8	97.6
6	1.5	53.6
7	1.2	31.6
8	1.0	18.7
9	0.8	11

Step	PSET (%)	R_{PSET} (kΩ)
1	0	>619K[1]
2	+10	475
3	+7.5	280
4	+5.0	165
5	+2.5	97.6
6	-2.5	53.6
7	-5.0	31.6
8	-7.5	18.7
9	-10	11

1. 619K or 0V tied to $SV_{IN.}$

The 88PG877 provides an innovative technique to set the output voltage. During start-up it reads the value of external resistors, which are located outside the regulator's feedback loop to program the output voltage. By placing the output voltage programming resistor outside the regulator's feedback loop, its tolerance does not affect the accuracy of the output voltage. Normally, adjustable regulators use 1% resistors to set the output voltage. However, these resistors are located inside the feedback loop, introducing as much as 2% of initial accuracy error to the output voltage, resulting in an overall initial accuracy of 3%. Whereas, the 88PG877 initial accuracy is 2% for any of the eight output voltages.

The VSET and PSET pins are sensitive to excessive leakage currents and stray capacitance. The output voltage can potentially be programmed to the lower output voltage if there is contamination, which introduces excessive leakage current on the VSET and PSET pin, especially for the 3.3V output or +10%. The parasitic resistance on these nodes must be greater than 3 MΩ and the stray capacitance must be less than 25 pF; otherwise, a 3.3V output can potentially end up at 3V.

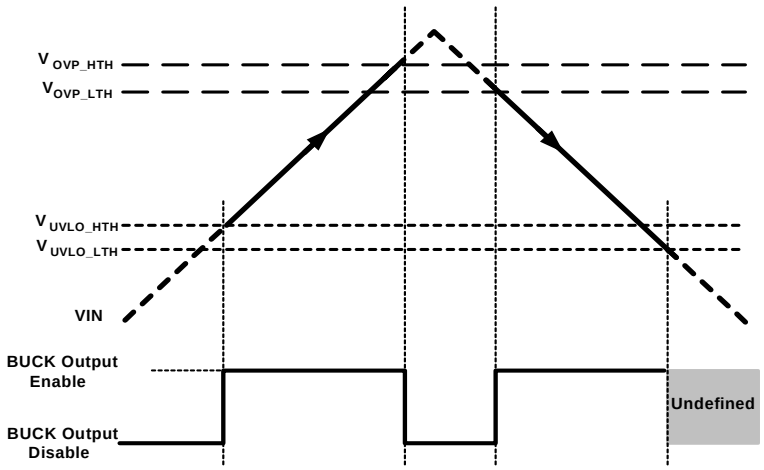
3.3 Undervoltage Lockout (UVLO)

At start-up, the 88PG877 incorporates undervoltage-lockout circuitry to enable the step-down switching regulator when the input voltage is above (typical). After the 88PG877 is enabled and the input voltage is lowered, the highest value of the minimum input voltage for both regulators to remain enabled is (typical).

3.4 Over Voltage Protection (OVP)

The 88PG877 incorporates an over voltage protection circuitry to disable the step-down switching regulator when the input voltage is above 5.7V (typical). The step-down switching regulator is enabled when the input voltage is below 5.6V (typical).

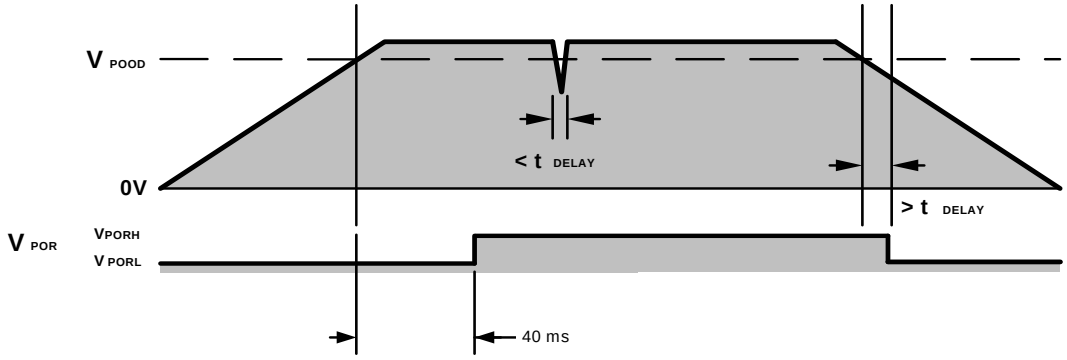
Figure 12: UVLO and OVP Waveforms



3.5 Power-On Reset (POR)

The Power-On Reset pin is an active-high, open-drain output pin. This output is held low when the output voltage of the step-down regulator is below the threshold. When the output voltage is above the threshold, the Power-On Reset pin goes high 40 ms later. Setting the output voltage greater than 1.35V, the threshold voltage is 0.9% * $V_{OUT\ (typical)}$. Setting the output voltage less than 1.32V, the threshold voltage is V_{OUT} – 130 mV (typical). A built-in 25 µs (t_{DELAY}) delay is incorporated to prevent nuisance tripping.

Figure 13: Power-On Reset Waveforms



3.6 Thermal Shutdown

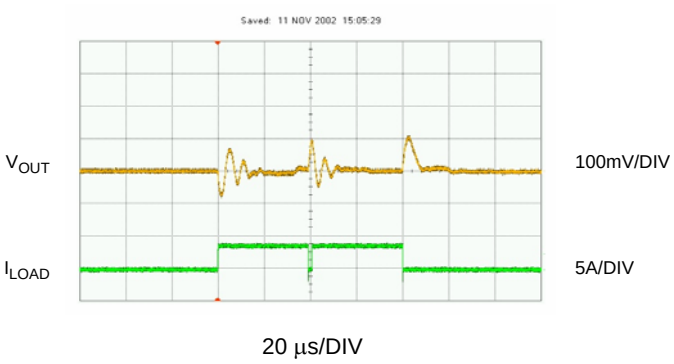
When the junction temperature of the 88PG877 exceeds 150 °C (typical), the thermal shutdown circuitry disables the step-down regulator. The step-down switching regulator is enabled when the junction temperature is decreased to 120 °C (typical).

3.7 Adaptive Transient Response

The 88PG877 device's Smart Technology allows the step-down switching regulator to quickly respond to the multiple step loads and maintain stability over a wide range of applications. Figure 14 shows an example of a second step-load applied while the output voltage of the step-down switching regulator increased due to the inductive kick from the first step-load.

Condition: V_{IN} = 5.0V, R_{SVIN} = 10Ω, C_{SVIN} = 0.1 µF, C_{PVIN} = µF, L = 1.0 µH, C_{OUT} = 2 x 22 µF, V_{OUT} = 1.V, I_{LOAD} = 1A to 5A.

Figure 14: Adaptive Transient Response



The worst case overshoot (V_{SOAR}) during a full-load to light-load transient due to stored inductor energy (Figure 14) can be calculated as:

$$V_{SOAR} = \frac{\Delta I_{LOAD(MAX)}^{2} \bullet L}{2 \bullet C_{OUT} \bullet V_{OUT}}$$

Although the V_{SOAR} cannot be eliminated, its amplitude can be controlled based on the C_{OUT} capacitor value. The appropriate C_{OUT} value can easily be calculated for the acceptable V_{SOAR} level for each specific application.

$$C_{OUT} = \frac{\Delta I_{LOAD(MAX)}^{2} \bullet L}{2 \bullet V_{SOAR} \bullet V_{OUT}}$$

Section 4. Functional Characteristics

The following applies unless otherwise noted: T_A = 25°C, R_{SVIN} = 10Ω, C_{SVIN} = 0.1 µF, C_{PVIN} = 2 x 22 µF, L = 1.0 µH, $C_{OUT\ (BUCK)}$ = 2 X 22 µF.

4.1 Start-up Waveforms

NOTE: When the input voltage rises above the UVLO's upper threshold, then there is a delay (4 ms typ) before the step-down regulator's output voltage turns on.

Figure 15: Startup Using the Enable Pin

10 ms/DIV

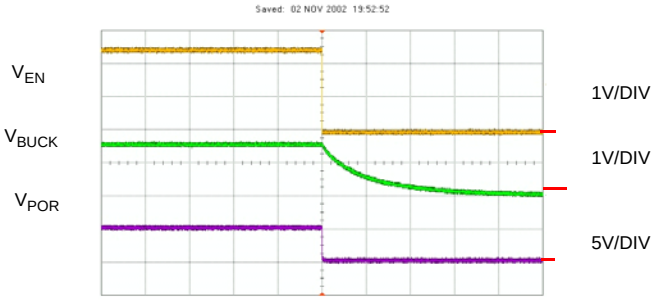
V_{IN} = 5.0V

V_{BUCK}= 1.2V

I_{LOAD} = No Load

t_{DLY}= 4.0 ms

Figure 16: Turn Off Using the Enable Pin

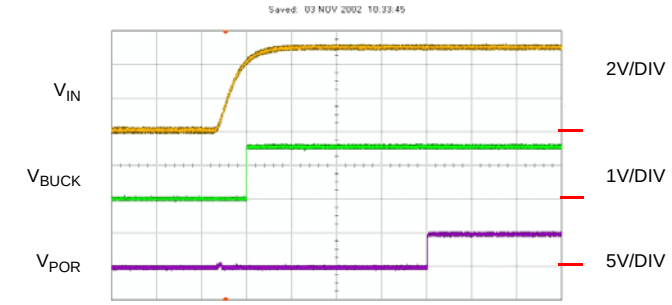


2.0 ms/DIV

V_{IN} = 5.0V

V_{BUCK}= 1.2V

Figure 17: Soft Start



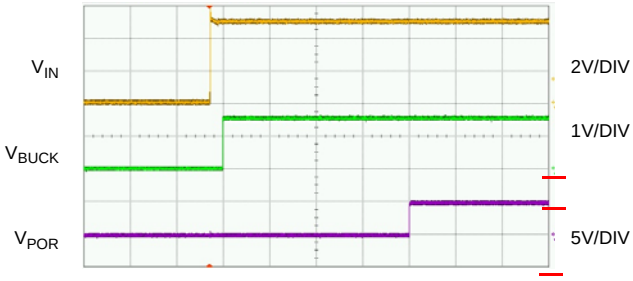
10 ms/DIV

V_{IN} = 5.0V

V_{BUCK}= 1.2V

I_{LOAD} = No Load

Figure 18: Hot Plug



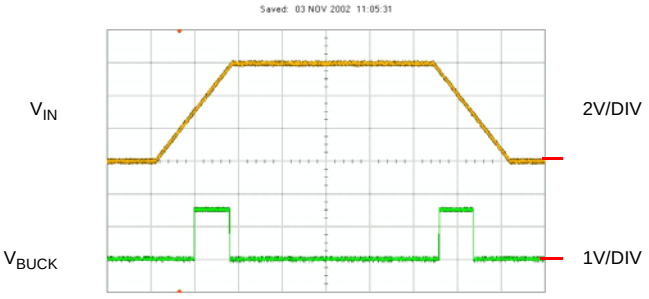
10 ms/DIV

V_{IN} = 5.0V

V_{BUCK}= 1.2V

I_{LOAD} = No Load

Figure 19: UVLO and OVP Thresholds



V_{IN} = 0 to 6.0V

V_{BUCK}= 1.5V

$I_{LOAD(BUCK)}$ = 1A

$V_{UVLO(HTH)}$ = 2.93V

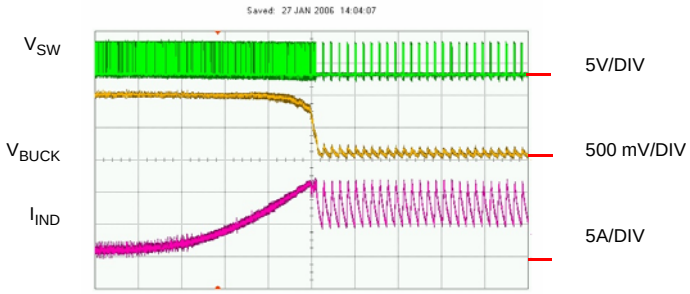
$V_{UVLO(LTH)}$= 2.87V

$V_{OVP(HTH)}$ = 5.74V

$V_{OVP(LTH)}$ = 5.53V

4.2 Short-Circuit Waveforms

Figure 20: Step-Down Short-Circuit Response



4.3 Switching Waveforms

NOTE: For repeatability of measuring output ripple ($V_{BUCK\ (P-P)}$) for the BUCK regulator, the standard test procedure limits the scope bandwidth to 20 MHz and uses a coax cable with very short leads terminated into 50Ω. The coax leads must be routed away from the switching node as much as possible.

Figure 21: Switching Waveforms - PWM mode

C_{IN} = 2x22 µF

V_{IN} = 5.0V

V_{BUCK}= 1.5V

I_{OUT} = 5.0A

$V_{OUT(P-P)}$ = 7.3 mV (Note)

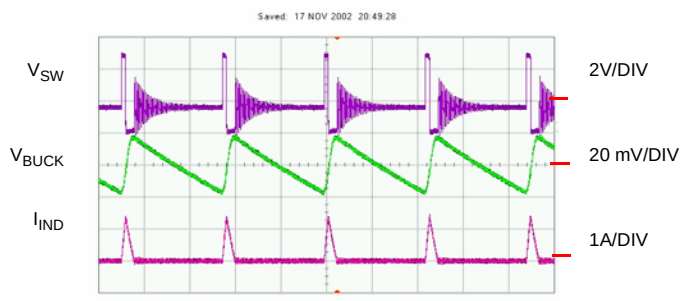
$V_{IN(P-P)}$ = 101 mV

$I_{IND(P-P)}$ = 1.2A

$I_{IND(PK)}$ = 5.4A

Freq = 964 kHz

Figure 22: Switching Waveforms - DCM Mode



V_{IN} = 5.0V

V_{BUCK}= 1.5V

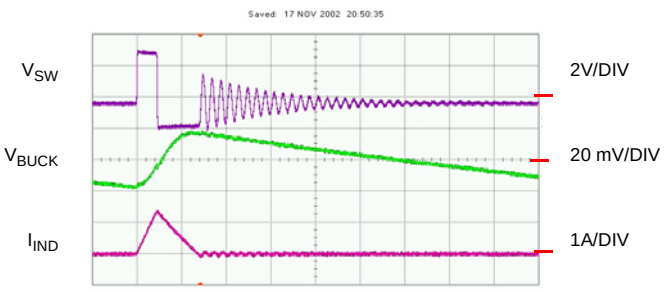
I_{OUT} = 50 mA

$V_{OUT(P-P)}$ = 37 mV (Note)

$I_{IND(PK)}$ = 1.42A

Freq = 89 kHz

Figure 23: Switching Waveforms - DCM Mode-Zoom



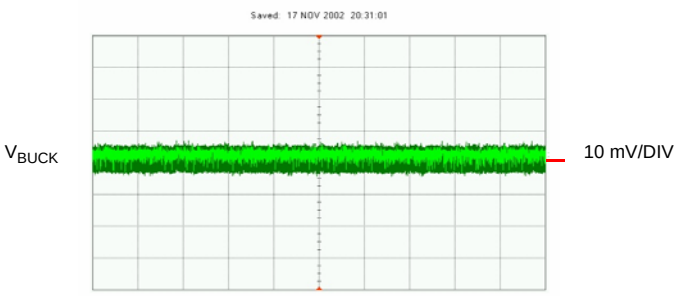
V_{IN} = 5.0V

V_{BUCK}= 1.5V

I_{OUT} = 50 mA

Ringing Freq = 5 MHz

Figure 24: PWM Output Ripple Voltage



V_{IN} = 5.0V

V_{BUCK}= 1.5V

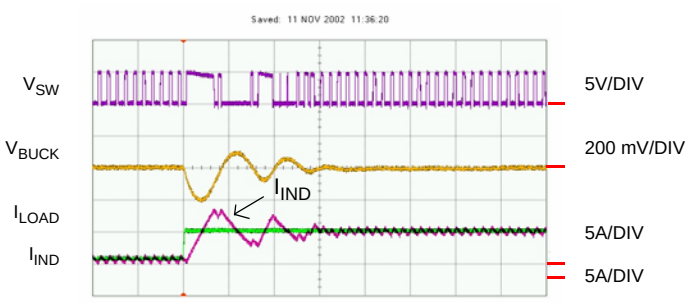
I_{OUT} = 5.0A

$V_{OUT(P-P)}$ = 11.2 mV (Note)

4.4 Load Transient Waveforms

4.4.1 Step-Down Regulator

Figure 25: Fast Load Rise Time

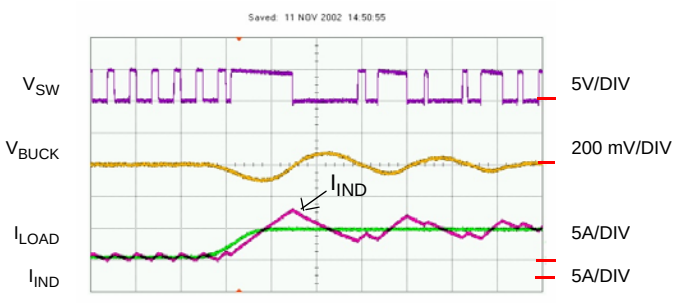


2.0 µs/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.5V
I_{OUT} = 1 A to 5A

C_{OUT} = **2 x 22 µF**
t_{RISE} = 27 A/µs

Figure 26: Slow Load Rise Time

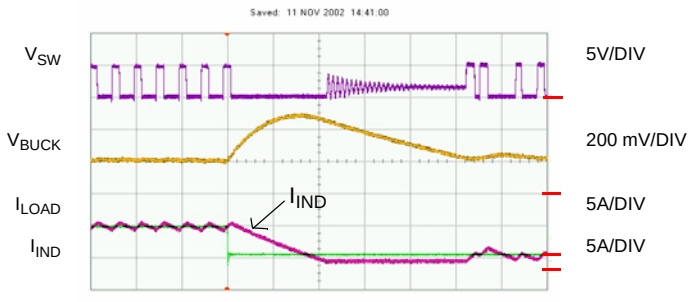


2.0 µs/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.5V
I_{OUT} = 1 A to 5A

C_{OUT} = **2 x 22 µF**
t_{RISE} = 2.4 A/µs

Figure 27: Fast Load Fall Time

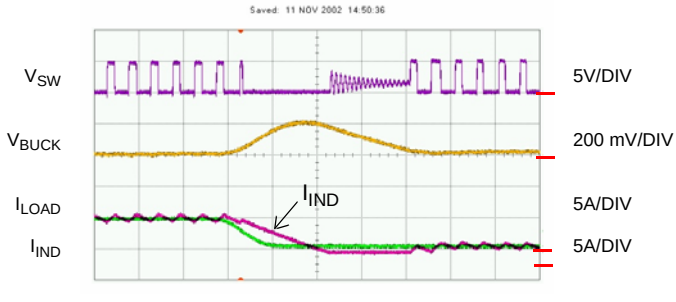


2.0 µs/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.5V
I_{OUT} = A to A

C_{OUT} = **2 x 22 µF**
t_{FALL} = 190 A/µs

Figure 28: Slow Load Fall Time

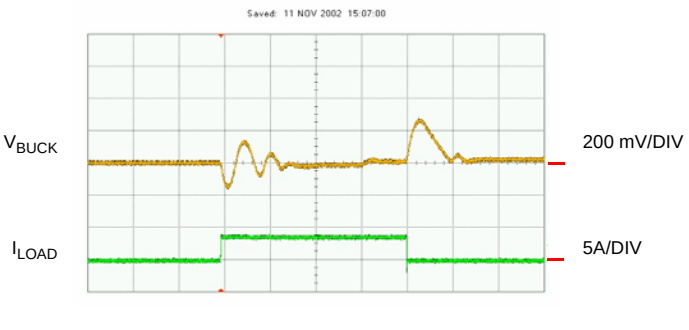


2.0 µs/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.5V
I_{OUT} = A to A

C_{OUT} = **2 x 22 µF**
t_{FALL} = 2.5 A/µs

Figure 29: Load Transient Response



10 µs/DIV

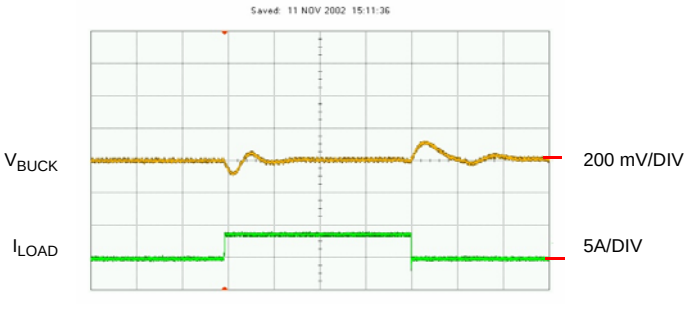
V_{IN} = 5.0V
V_{BUCK}= 1.5V
C_{OUT} = 2 x 22 µF
I_{LOAD} = 1A to 5A
t_{RISE} = 27 A/µs
t_{FALL} = 190 A/µs

Figure 30: Double-Pulsed Load Response

20 µs/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.5V
C_{OUT} = 2 x 22 µF
I_{LOAD} = 1A to 5A
t_{RISE} = 27 A/µs
t_{FALL} = 190 A/µs

Figure 31: Load Transient Response



10 µs/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.5V
C_{OUT} = 4 x 22 µF
V_{CG} = GND
I_{LOAD} = 1A to 5A
t_{RISE} = 27 A/µs
t_{FALL} = 190 A/µs

Figure 32: Double-Pulsed Load Response

20 µs/DIV

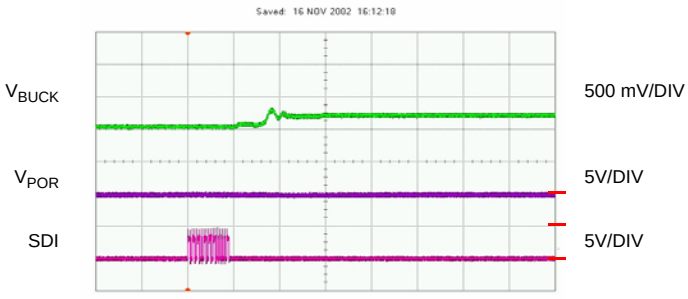
V_{IN} = 5.0V
V_{BUCK}= 1.5V
C_{OUT} = 4 x 22 µF
V_{CG} = GND
I_{LOAD} = 1A to 5A
t_{RISE} = 27 A/µs
t_{FALL} = 190 A/µs

4.5 Output Voltage Transient Waveforms

The following graphs show the effect of changing the step-down regulator's output voltage using the serial interface. Depending on the change in the step-size of the output voltage, the output load, and the output capacitance, the power-on reset pin de-asserts when the changes of the output voltage occur beyond the 25 µs (typical) delay.

4.5.1 Step-Down Regulator

Figure 33: V_{OUT} = 1.0V to 1.2V with No Load

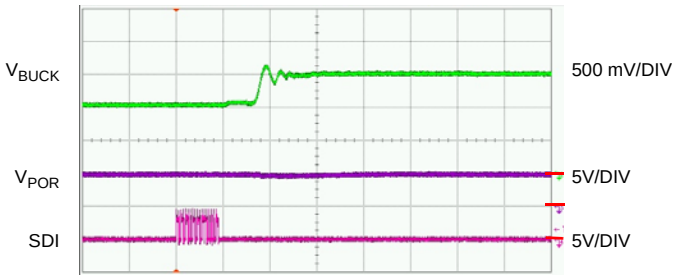


20 µs/DIV

V_{IN} = 5.0V

C_{OUT}= (2 x 22) + 1000 µF

Figure 34: V_{OUT} = 1.0V to 1.5V with No Load

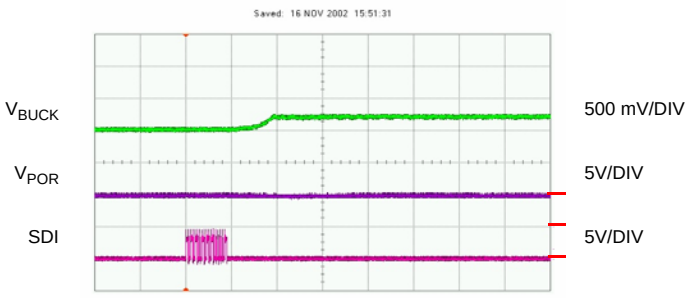


20 µs/DIV

V_{IN} = 5.0V

C_{OUT}= (2 x 22) +1000 µF

Figure 35: V_{OUT} = 1.0V to 1.2V with I_{LOAD} = 5A



20 µs/DIV

V_{IN} = 5.0V

C_{OUT}= (2 x 22) + 1000 µF

Figure 36: V_{OUT} = 1.0V to 1.5V with I_{LOAD} = 5A

20 µs/DIV

V_{IN} = 5.0V

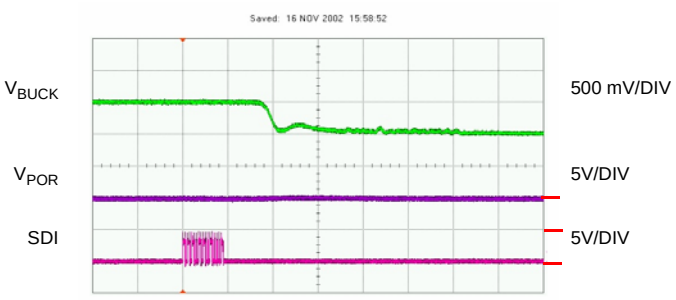
C_{OUT}= (2 x 22) +1000 µF

Figure 37: V_{OUT} = 1.2V to 1.0V with I_{LOAD} = 5A

V_{IN} = 5.0V

C_{OUT}= (2 x 22)+1000 µF

Figure 38: V_{OUT} = 1.5V to 1.0V with I_{LOAD} = 5A

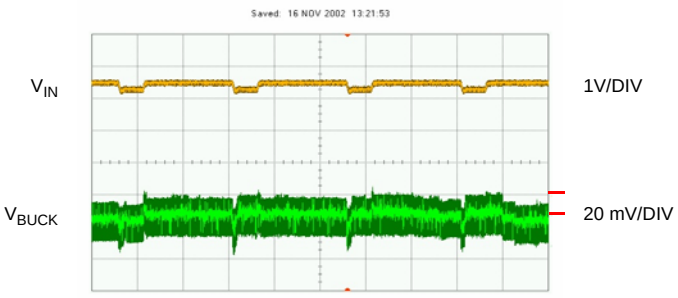


V_{IN} = 5.0V

C_{OUT}= (2 x 22)+1000 µF

4.6 Line Transient Waveforms

Figure 39: Line Transient @ V_{IN} = 3.2V to 3.6V



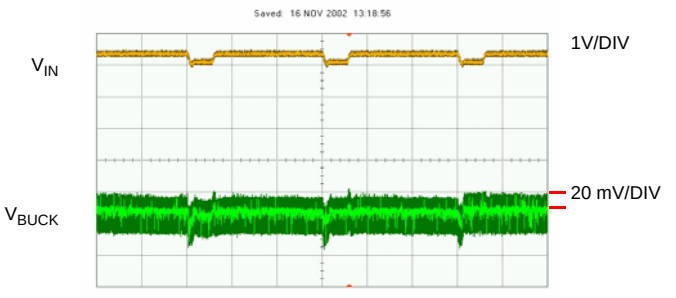
V_{IN} = 3.6V

C_{IN}= 22 µF

V_{BUCK} = 1.2V

I_{LOAD} = 5A

Figure 40: Line Transient @ V_{IN} = 4.1V to 4.5V



V_{IN} = 4.5V

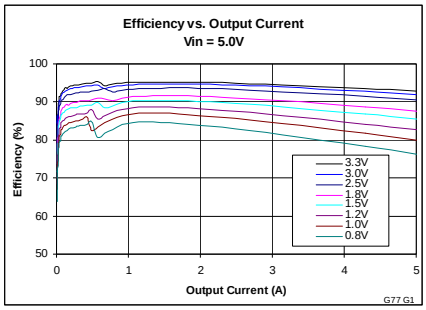
C_{IN}= 22 µF

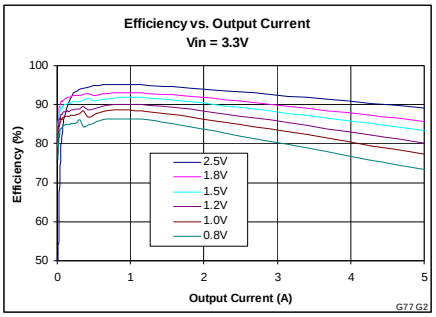
V_{BUCK} = 1.2V

I_{LOAD} = 5A

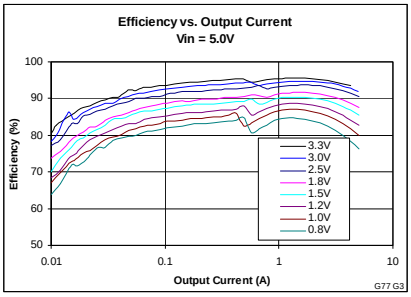
Section 5. Typical Characteristics

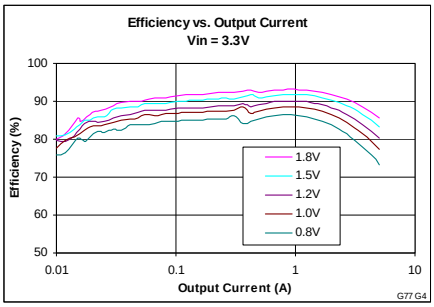
5.1 Efficiency Graphs



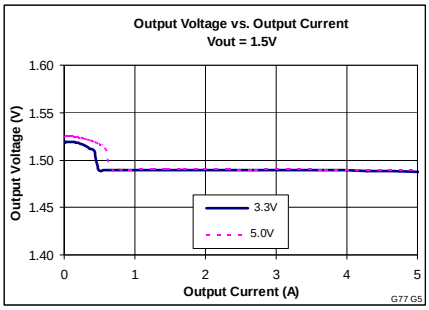


5.1.1 Efficiency Graphs in log scale

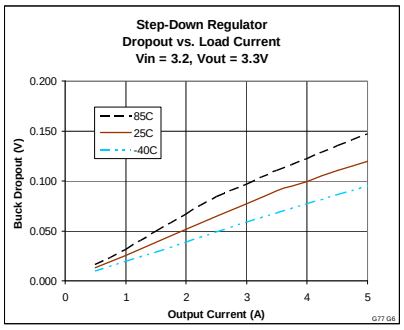




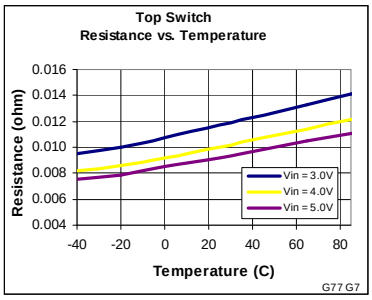
5.2 Load Regulation

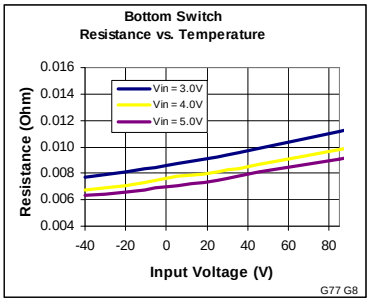


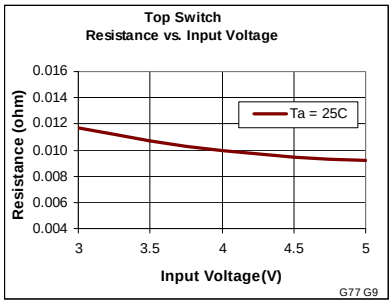
5.3 Dropout Voltage

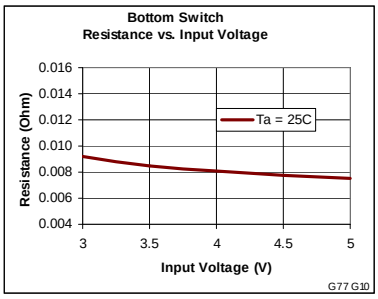


5.4 RDS (ON) Resistance



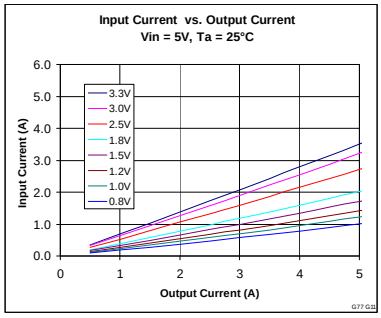


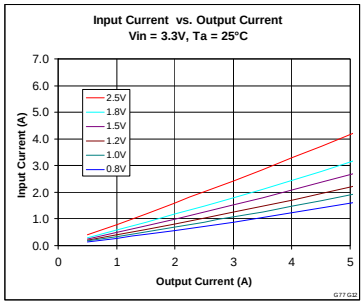


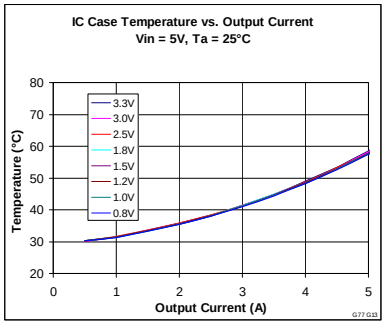


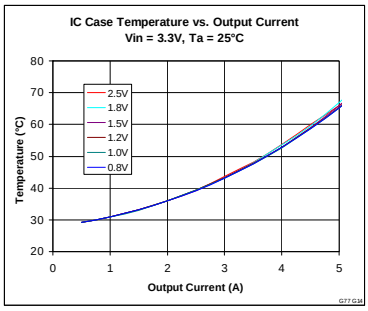
5.5 IC Case and Inductor Temperature

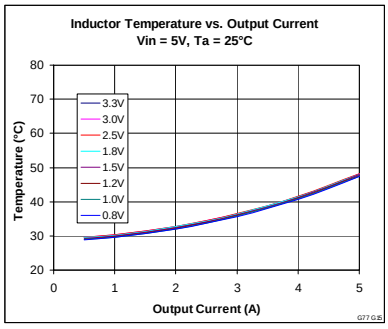
The following data was taken using a 1.4 square inch PCB 1 oz. copper and L = 1.2 µH. Actual results depend upon the size of the PCB proximity to other heat emitting components.

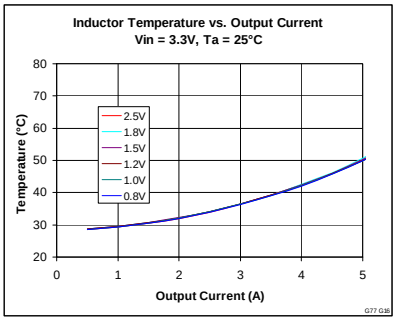




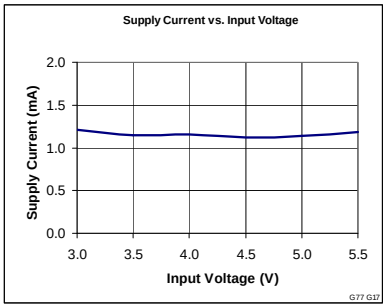




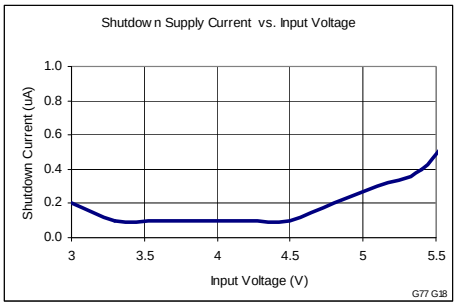




5.6 Input Voltage Graphs

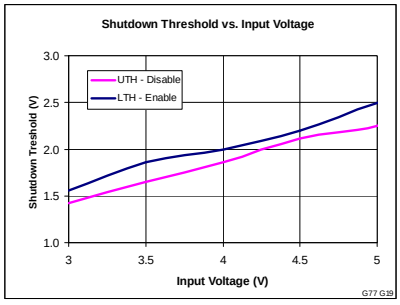


Load = No Load

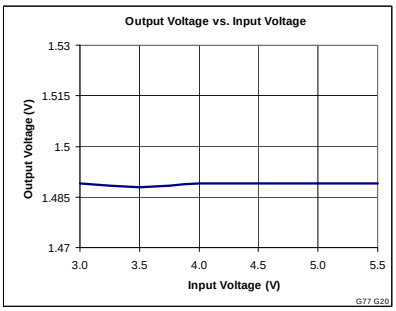


V_{IN} = 5.0V

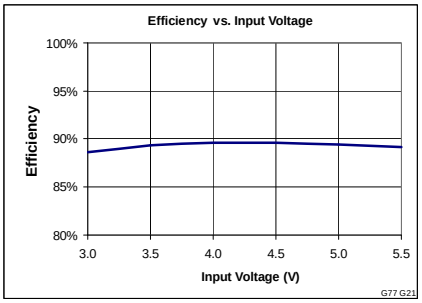
Load = No Load



5.6.1 Step-Down Regulator

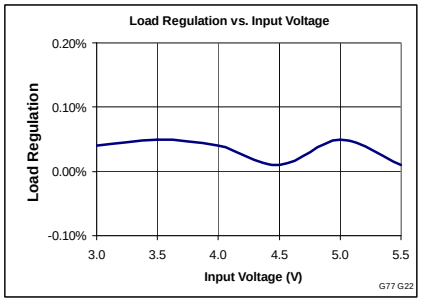


$I_{OUT(BUCK)}$ = 1.25A



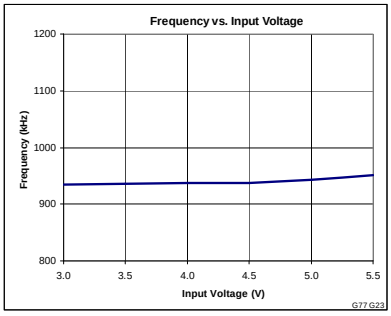
$V_{OUT(BUCK)}$ = 1.5V

$I_{OUT(BUCK)}$ = 2.5A



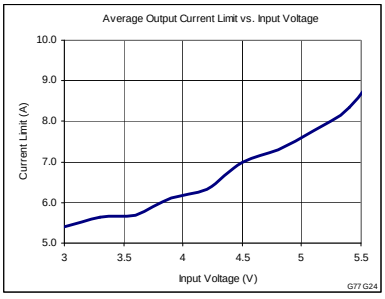
$V_{OUT(BUCK)}$ = 1.5V

$I_{OUT(BUCK)}$ = 1.25A - 5.0A

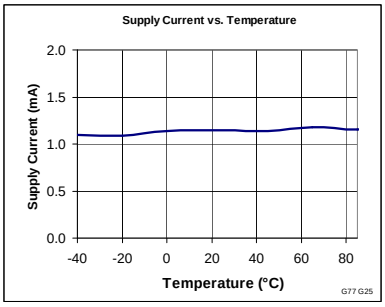


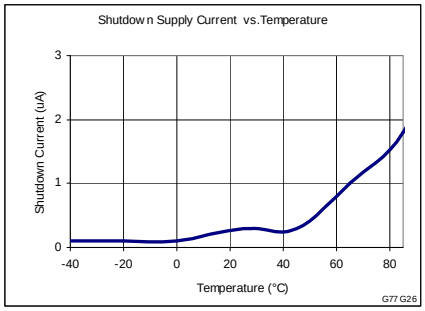
$V_{OUT(BUCK)}$ = 1.5V

$I_{OUT(BUCK)}$ = 2.5A



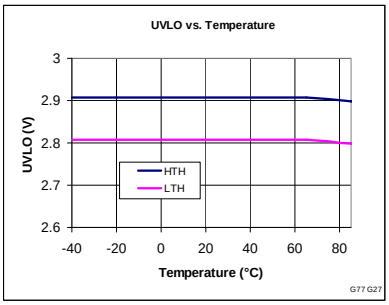
5.7 Temperature Graphs

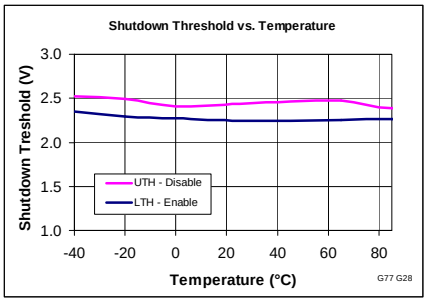




$I_{OUT(BUCK)}$ = No Load

$I_{OUT(LDO)}$ = No Load

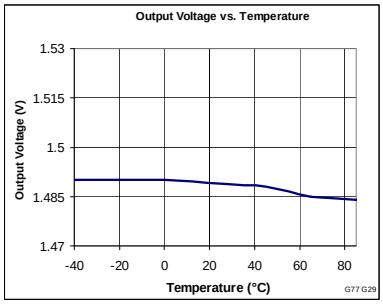




$I_{OUT(BUCK)}$ = 10 mA

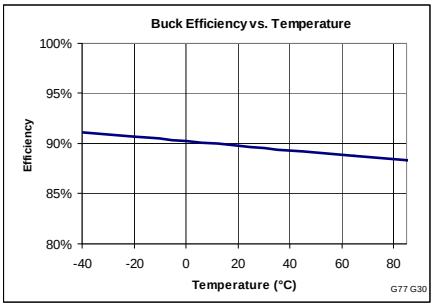
V_{IN}= 5V

5.7.1 Step-Down Regulator



V_{IN} = 5.0V

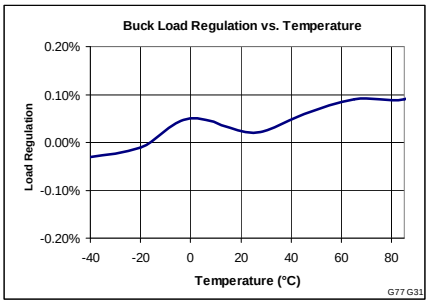
$I_{OUT(LDO)}$ = 1.2A



V_{IN} = 5.0V

$V_{OUT(BUCK)}$ = 1.5V

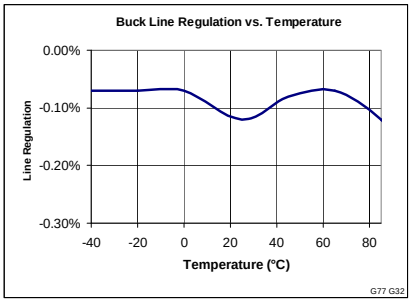
$I_{OUT(BUCK)}$ = 2.5A



V_{IN} = 5.0V

$V_{OUT(BUCK)}$ = 1.5V

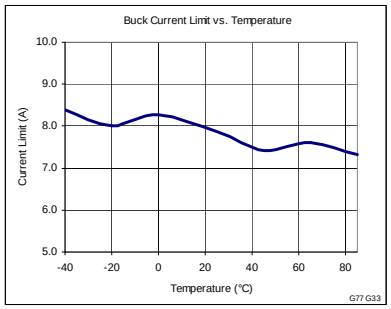
$I_{OUT(BUCK)}$ = 1.25A

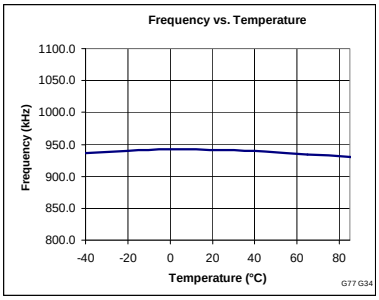


V_{IN} = 3.0V - 5.0V

$V_{OUT(BUCK)}$ = 1.5V

$I_{OUT(BUCK)}$ = 2.5A





V_{IN} = 5.0V

$I_{OUT(BUCK)}$ = 2.5A

Section 6. Applications Information

6.1 PC Board Layout Considerations and Guidelines for 88PG877

1. This is a 2-layer board with 1 ground plane and 1 routing layer.
2. Copy the routing layer in Figure 43 as much as possible and place on the top layer. The ground plane in Figure 44 can be placed on any other layer. Use the recommend BOM in Table 9. Contact the factory if substitutions are made.
3. Review the recommended solder pad layout and notes on page 51.
4. **Do not replace the Ceramic input capacitor with any other type of capacitor.** Any type of capacitor can be placed in parallel with the input capacitor as long as the Ceramic input capacitor is placed next to the IC. If Tantalum input capacitor is used, it must be rated for switching regulator applications and the operating voltage be derated by 50%.
5. Any type of capacitor can be placed in parallel with the output capacitor.
6. Low-ESR capacitors like the POSCAP from Sanyo can replace the Ceramic output capacitors as long as the capacitor value is the same or greater. Note that the Ceramic capacitors provide the lowest noise and smallest foot print solution.
7. Use planes for the ground, input and outputs power to maintain good voltage filtering and to keep power losses low.
8. If there is not enough space for a power plane for the input supply, then the input supply trace must be at least 3/8 inch wide.
9. If there is not enough space for a power plane for the output supplies, then place the output as close to the load as possible with a trace of at least 3/8 inch wide.
10. Do not lay out the inductor first. **The input capacitor placement is the most critical for proper operation.** The AC current circulating through the input capacitor and loop 1 (LP1) are square wave with rise and fall times of 8 ns and slew rates as high as 300 A/µs (Figure 41). At these fast slew rates, stray PCB inductance can generate a voltage spike as high as 3V per inch of PCB trace, VIND = L * di/dt. Therefore, the Ceramic input capacitor must be placed as close as possible to the PVIN and PGND pins with as short and wide a trace as possible. Also, the PVIN and PGND traces must be placed on the top layer. This will isolate the fast AC currents from interfering with the analog ground plane.
11. The 88PG877 has two internal grounds, analog (SGND) and power (PGND). The analog ground ties to all the noise sensitive signals (PSET, VSET, and SVIN) while the power ground ties to the higher current power paths. Noise on an analog ground can cause problems with the IC's internal control and bias signals. For this reason, separate analog and power ground traces are recommended. The signal ground is connected to the power ground at one point, which is the (-) terminal of the output capacitor.
12. Keep loop 2 (LP2) as small as possible and connect the (-) terminal of the output capacitor as close to the (-) terminal of the input capacitor. A back-to-back placing of bypass capacitors, as shown in Figure 43, is recommended for best results.
13. Keep the switching node (SW) away from the SFB pin and all sensitive signal nodes, minimizing capacitive coupling effects. If the SFB trace must cross the SW node, cross it at a right angle.
14.
15. Try not to route analog or digital lines in close proximity to the power supply especially the VSW node. If this can't be avoided, shield these lines with a power plane placed between the VSW node and the signal lines.
16. The type of solder paste recommended for QFN packages is "No clean", due to the difficulty of cleaning flux residues from beneath the QFN package.

Figure 41: PCB Layout

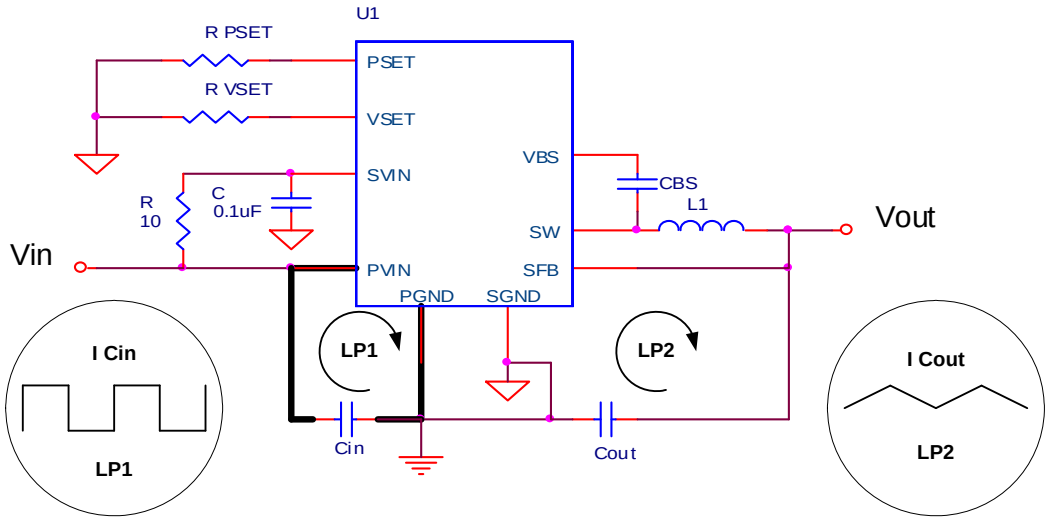
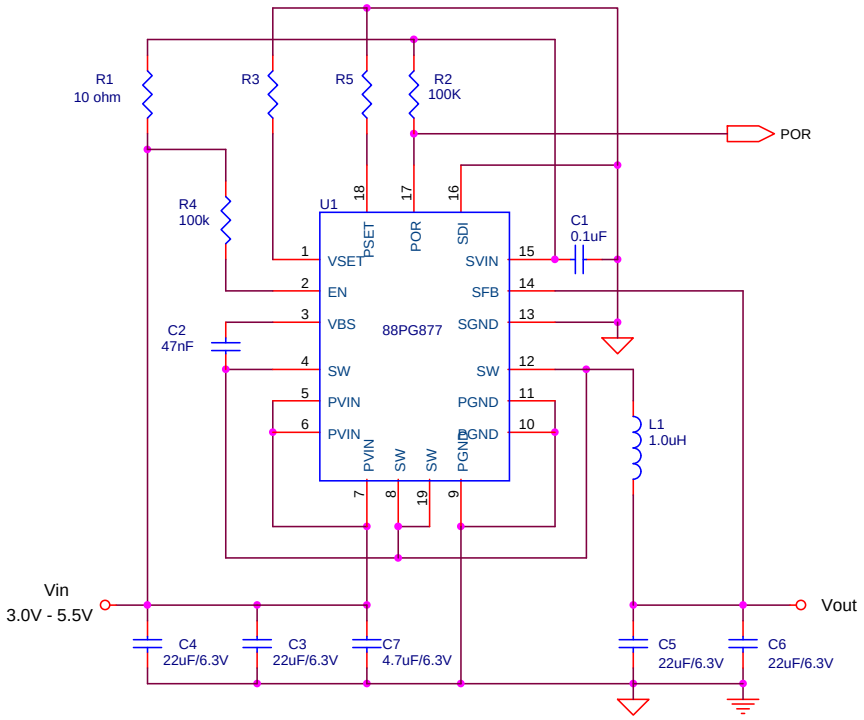


Figure 42: 88PG877 PCB Board Schematic



6.1.1 PC Board Layout Examples for 88PG877

- Total copper layers = 2 (Top and Bottom)
- All the components are on the top layer

Figure 43: Top Silk-Screen, Top Traces, Vias and Copper (Not to scale)

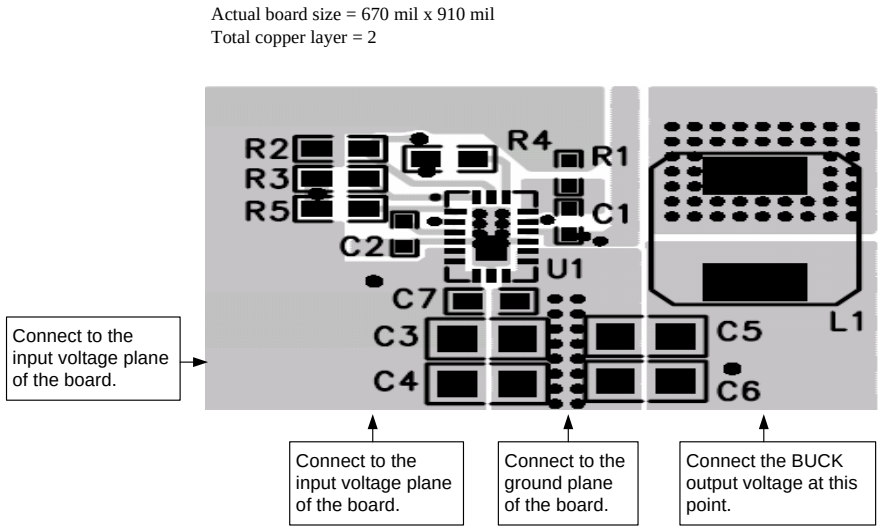
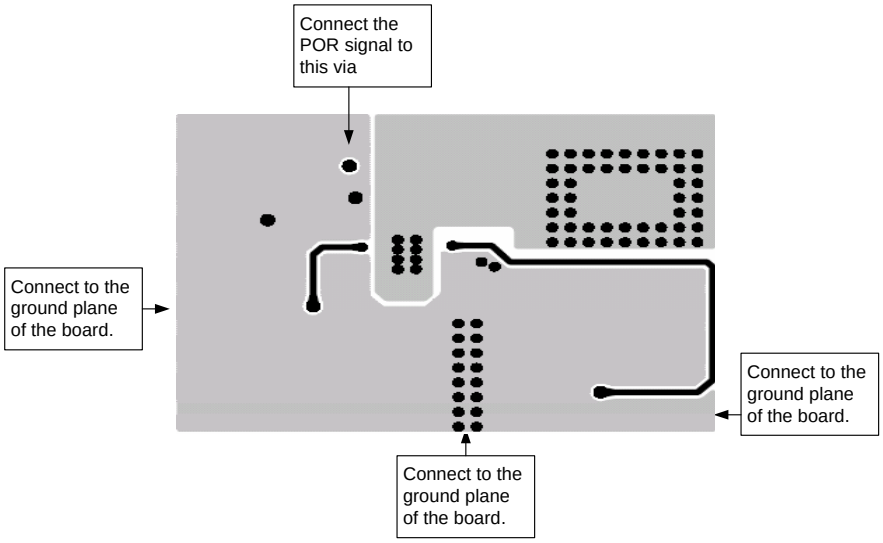


Figure 44: Bottom Silk Screen, Bottom Traces, Vias, and Copper (Not to scale)



6.1.2 Bill of materials for 88PG877

Table 9 lists the components used with the 88PG877.

Table 9: 88PG877 BOM

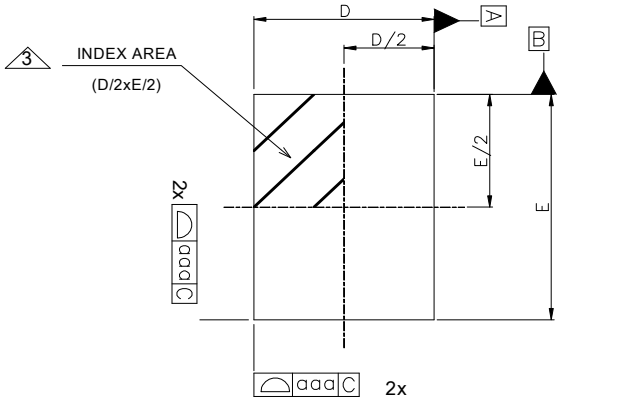
Item	Qty	Ref	Manufacturer Part No.	Manufacturer	Description
1	1	U1	88PG877	Marvell Semi-conductor Inc.	1MHz, 7.5A Peak-Current Limit Step-down Regulator
2	1	C1	C1005X5R1A104K	Taiyo-Yuden	0.1 µF, ±10%, X5R, 10V, 0402 Case Size, Ceramic Capacitor.
3	1	C2	0402YD473KAT2A	AVX Corporation	0.047 µF, ±20%, X5R, 16V, 0402 Case Size, Ceramic Capacitor.
4	4	C3,C4, C5,C6	C2012X5R0J226M	TDK	22 µF, ±20%, X5R, 6.3V, 0805 Case Size, Ceramic Capacitor.
5	1	C7	C1608X5R0J475M	TDK	4.7 µF, ±20%, X5R, 6.3V, 0603 Case Size, Ceramic Capacitor.
6	1	L1	FDV0630-1R0M=P3	Toko	1.0 µH, 9.1A, 10 mohm, H=3mm, L=7.7mm, W=7mm, SMD Inductor
7	1	R1	ERJ-2RKF10R0X	Panasonic-ECG	10.0 ohm, 1/16W, 1%, 0402 Case size, SMD Resistor
8	2	R2,R4	ERJ-3GEYJ104V	Panasonic-ECG	100 kohm, 1/10W, 5%, 0603 Case size, SMD Resistor
9	1	R3,R5			See AnyVoltage™ Programming, 1/16W, 1% 0402 Case Size

Table 10: Ceramic Capacitor Cross Reference

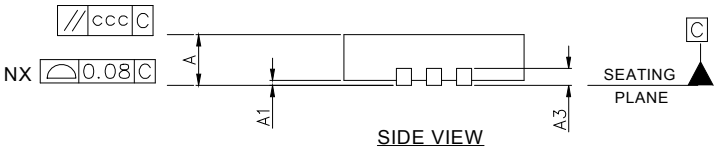
Manufacturer	Manufacturer Part #	Description
22 µF	Taiyo-Yuden	CE JMK212BJ226MG-T
	TDK	C2012X5R0J226MT
	Murata	GRM21BR60J226ME39L
10 µF	Taiyo-Yuden	CE JMK212BJ106MG-T
	TDK	C2012X5R0J106MT
	Murata	GRM219R60J106KE190
0.1 µF	Taiyo-Yuden	RM LMK105 BJ104KV-F
	TDK	C1005X5R1A104K

Section 7. Mechanical Drawing

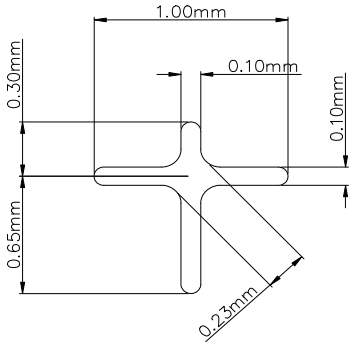
7.1 88PG877 Mechanical Drawing



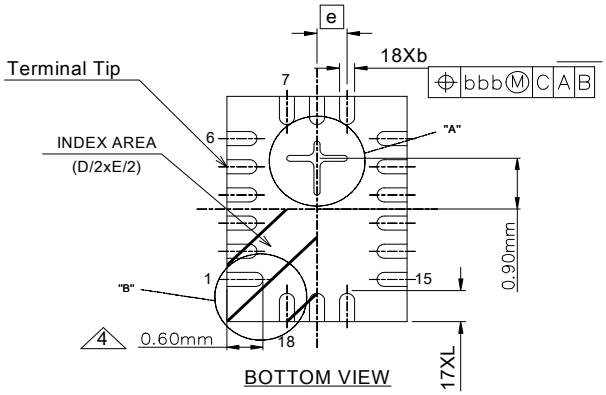
TOP VIEW



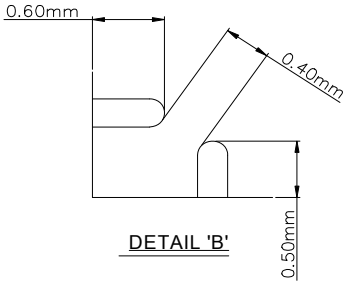
SIDE VIEW



DETAIL 'A'



BOTTOM VIEW



DETAIL 'B'

7.2 88PG877 Mechanical Dimensions

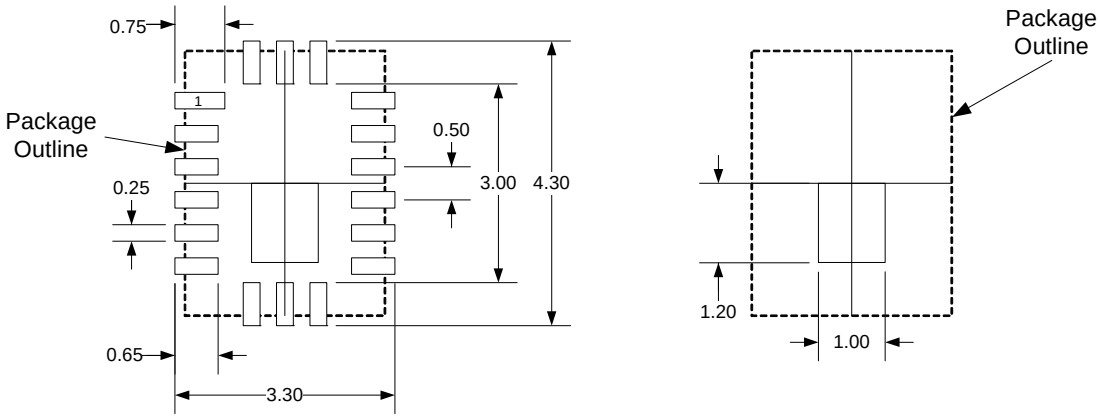
Symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	0.90	1.00
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
E	3.90	4.00	4.10
e	0.50 BSC		
L	0.40	0.50	0.60
aaa	---	---	0.15
bbb	---	---	0.10
ccc	---	---	0.10

Note:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters.
3. The terminal #1 identifier and terminal numbering convention
4. Pin 1 (0.6mm) is longer than other pins (0.5mm)

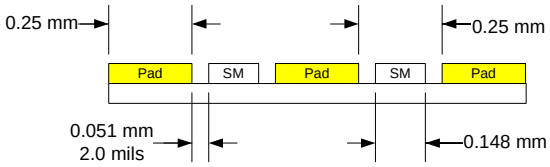
7.3 Typical Pad Layout Dimensions

7.3.1 Recommended Solder Pad Layout



88PG877

4x3 QFN-18
Land Pattern (mm)



QFN Lead with
Non-Solder Mask Defined Terminal
(Not to Scale)

Notes:

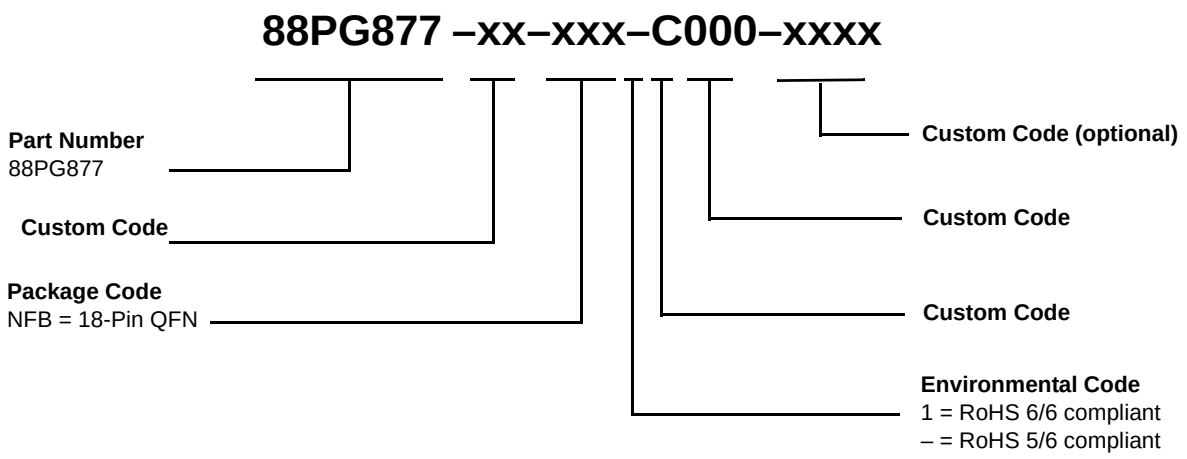
1. TOP VIEW
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE IN MILLIMETERS
4. OVERSIZE SOLDER MASK BY 4 MILS OVER PAD SIZE (2 MIL ANNULAR RING)
5. SOLDER MASK (SM) BETWEEN PADS
6. TOLERANCE ±0.05 mm
7. PIN 1 IS LONGER THAN OTHER PINS BY 0.1 mm

Section 8. Ordering Information

8.1 Ordering Part Numbers and Package Markings

Figure 45 shows the ordering part numbering scheme for the 88PG877 devices. Contact Marvell® FAEs or sales representatives for complete ordering information.

Figure 45: Sample Part Number



8.2 Sample Ordering Part Number

The standard ordering part numbers for the respective solutions are as follows:

Table 11: 88PG877 Ordering Part Numbers[1]

Marketing Part Number	Marking	Ambient Temperature Range[2]	Package[3]
88PG877-NFB1		-40 °C to 85 °C	4 X 3 QFN-18

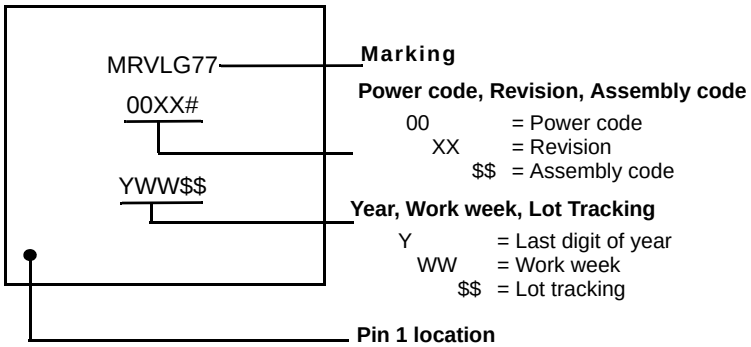
1. Contact Marvell® for details.
2. Specifications over the –40 °C to 85 °C operating temperature range are assured by design, characterization and correlation with statistical process controls.
3. Package dimensions are in mm.

8.3 Package Marking

8.3.1 88PG877 Package Marking and Pin 1 Locations

Figure 46 is an example of the package marking and pin 1 location for the 88PG877 part. Markings for the other variants are similar.

Figure 46: 88PG877 Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Locations of markings are approximate.

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