

EVALUATION KIT
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Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

General Description

The MAX17007/MAX17008 are dual Quick-PWM™ step-down controllers intended for general power generation in battery-powered systems. The two switched-mode power supplies (SMPSs) can also be combined to operate in a two-phase single-output mode. Constant on-time Quick-PWM operation provides fast response to load transients and handles wide input/output (I/O) voltage ratios with ease, while maintaining a relatively constant switching frequency. The switching frequency can be individually adjusted between 200kHz and 600kHz with external resistors. Differential output current sensing allows output sense-resistor sensing for an accurate current limit, or lossless inductor direct-current resistance (DCR) current sensing for lower power dissipation while maintaining 0.7% output accuracy. Overvoltage (MAX17007 only), undervoltage protection, and accurate user-selectable current limits (15mV, 30mV, 45mV, and 60mV) ensure robust operations.

The SMPS outputs can operate in skip mode or in ultrasonic mode for improved light-load efficiency. The ultrasonic mode eliminates audible noises by maintaining a minimum switching frequency of 25kHz in pulse-skipping mode.

The output voltage of SMPS1 can be dynamically adjusted by changing the voltage at the REFIN1 pin. The device includes a 0.5% accurate reference output that can be used to set the REFIN1 voltage. An external 5V bias supply is required to power the internal circuitry and its gate drivers.

Independent on/off controls with well-defined logic thresholds and independent open-drain power-good outputs provide flexible system configurations. To prevent current surges at startup, the internal voltage target is slowly ramped up from zero to the final target with a slew rate of 1.3mV/μs for SMPS1 at CSL1 and 0.65mV/μs for SMPS2 at FB2. To prevent the output from ringing off below ground in shutdown, the internal voltage target is ramped down from its previous value to zero with the same respective slew rates. Integrated bootstrap switches eliminate the need for external bootstrap diodes.

The MAX17007/MAX17008 are available in a space-saving, 28-pin, 4mm x 4mm, thin QFN package with an exposed backside pad.

Applications

Notebook Computers	5V and 3.3V Supplies
Low-Power I/O Supplies	2 to 4 Li+ Cells Battery-Powered Devices
GPU Core Supplies	

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Features

- ◆ Dual Quick-PWM with Fast Transient Response
- ◆ Automatic Dynamic REFIN1 Detection and PGOOD1/Fault Blanking
- ◆ Fixed and Adjustable Output Voltages
0.7% Output Accuracy Over Line and Load
OUT1: 0 to 2V Dynamic Output or Preset 1.05V
OUT2: 0.7V to 2V Range or Preset 1.5V
- ◆ Resistor-Programmable Switching Frequency
- ◆ Integrated BST Switches
- ◆ Differential Current-Sense Inputs
Low-Cost DCR Sensing or Accurate Current-Sense Resistors
Internally Coupled Current-Sense Compensation
- ◆ Combinable Mode Supports High-Current Dynamic Output Voltages
- ◆ Selectable Forced-PWM, Pulse Skip, or Ultrasonic Mode Operation
- ◆ 26V Maximum Input Voltage Rating
- ◆ Independent Enable Inputs
- ◆ Independent Power-Good Outputs
- ◆ Overvoltage Protection (MAX17007 Only)
- ◆ Undervoltage/Thermal Protection
- ◆ Automatic Dynamic REFIN1 Detection and PGOOD1/Fault Blanking
- ◆ Voltage Soft-Start and Soft-Shutdown

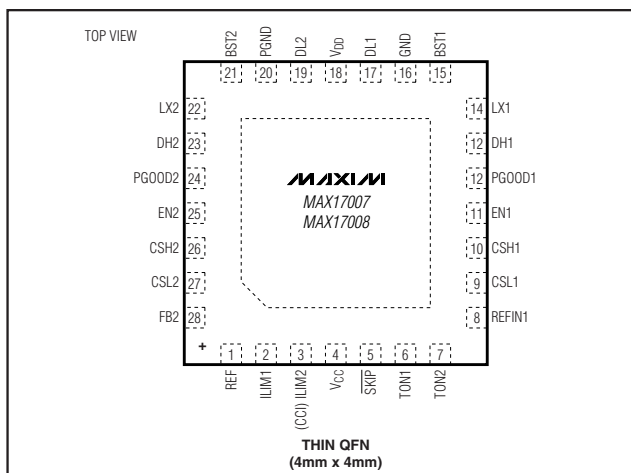
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17007GTI+	-40°C to +105°C	28 Thin QFN
MAX17008GTI+*	-40°C to +105°C	28 Thin QFN

+ Denotes a lead-free package.

*Future product—contact factory for availability.

Pin Configuration



MAX17007/MAX17008

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ABSOLUTE MAXIMUM RATINGS

BST1, BST2 to GND	-0.3V to +34V
BST1, BST2 to V _{DD}	-0.3V to +28V
TON1, TON2 to GND	-0.3V to +28V
V _{DD} to GND	-0.3V to +6V
V _{DD} to V _{CC}	-0.3V to +0.3V
LX1 to BST1	-6V to +0.3V
LX2 to BST2	-6V to +0.3V
DH1 to LX1	-0.3V to (V _{BST1} + 0.3V)
DH2 to LX2	-0.3V to (V _{BST2} + 0.3V)
ILIM1, ILIM2, REF to GND	-0.3V to (V _{CC} + 0.3V)
CSH1, CSH2, CSL1, CSL2, FB2, REFIN1 to GND	-0.3V to +6V
EN1, EN2, SKIP, PGOOD1, PGOOD2 to GND	-0.3V to +6V

DL1 to GND	-0.3V to (V _{DD} + 0.3V)
DL2 to PGND	-0.3V to (V _{DD} + 0.3V)
PGND to GND	-0.3V to + 0.3V
REF Short Circuit to GND	Continuous
Continuous Power Dissipation (T _A = +70°C)	
28-Pin TQFN T2844-1	
(derate 20.8mW/°C above +70°C)	1667mW
Extended Operating Temperature Range	-40°C to +105°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{DD} = V_{CC} = EN1 = EN2 = 5V, V_{REFIN1} = 2V, $\overline{\text{SKIP}}$ = GND, T_A = 0 to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range	V _{IN}			4.5		26	V
Quiescent Supply Current (V _{DD} , V _{CC})	I _{DD} + I _{CC}	Output forced above regulation voltage, EN1 = EN2 = 5V			1.7	2.5	mA
Shutdown Supply Current (V _{DD} , V _{CC})	I _{SHDN}	EN1 = EN2 = GND, T _A = +25°C			0.1	5	μA
On-Time (Note 1)	t _{ON1} , t _{ON2}	V _{IN} = 12V, V _{CSL1} = V _{CSL2} = V _{CCI} = 1.2V, separate or combined mode	R _{TON1} = R _{TON2} = 97.5kΩ (600kHz)	142 (-15%)	174	194 (+15%)	ns
			R _{TON1} = R _{TON2} = 200kΩ (300kHz)	305 (-10%)	336	368 (+10%)	
			R _{TON1} = R _{TON2} = 302.5kΩ (200kHz)	425 (-15%)	500	575 (+15%)	
Minimum Off-Time	t _{OFF(MIN)}	(Note 1)			250	330	ns
TON1, TON2, Shutdown Supply Current	I _{TON1} , I _{TON2}	EN1 = EN2 = GND, V _{TON1} = V _{TON2} = 26V, V _{DD} = 0V or 5V, T _A = +25°C			0.01	1	μA
REFIN1 Voltage Range	V _{REFIN1}	(Note 2)		0		V _{REF}	V
FB2 Regulation Voltage	V _{FB2}	Adjustable mode			0.7		V
FB2 Input Voltage Range		Preset mode		1.7		2.3	V
FB2 Combined-Mode Threshold		Combined mode		3.8	V _{CC} - 1V	V _{CC} - 0.4	V
REFIN1 Dual Mode™ Switchover Threshold				3.8	V _{CC} - 1V	V _{CC} - 0.4	V
REFIN1, FB2 Bias Current	I _{REFIN1} , I _{FB2}	REFIN1 = 0.5V to 2V; V _{FB2} = 0.7V, T _A = +25°C		-0.1		+0.1	μA
SMPS1 Voltage Accuracy	V _{CSL1}	Measured at CSL1, REFIN1 = V _{CC} , V _{IN} = 2V to 26V, $\overline{\text{SKIP}}$ = V _{CC} (Note 2)		1.043	1.05	1.057	V
SMPS2 Voltage Accuracy	V _{CSL2}	Measured at CSL2, FB2 = REF, V _{IN} = 2V to 26V, $\overline{\text{SKIP}}$ = V _{CC} (Note 2)		1.489	1.5	1.511	V

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ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = 12V$, $V_{DD} = V_{CC} = EN1 = EN2 = 5V$, $V_{REFIN1} = 2V$, $\overline{SKIP} = GND$, $T_A = 0$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Load Regulation Error		$I_{LOAD} = 0$ to $3A$, $\overline{SKIP} = V_{CC}$ (Note 3)		0.1		%
Line Regulation Error		$V_{DD} = 4.5V$ to $5.5V$, $V_{IN} = 4.5V$ to $26V$ (Note 3)		0.25		%
CSL1 Soft-Start/-Stop Slew Rate	SR _{SS1}	Rising/falling edge on EN1		1.25		mV/ μs
FB2 Soft-Start/-Stop Slew Rate	SR _{SS2}	Rising/falling edge on EN2		0.63		mV/ μs
Dynamic REFIN1 Slew Rate	SR _{DYN}	Rising edge on REFIN1		11.4		mV/ μs
INTERNAL REFERENCE						
Reference Voltage	V _{REF}	$V_{DD} = 4.5V$ to $5.5V$	1.990	2.000	2.010	V
Reference Lockout Voltage	V _{REF(UVLO)}	Rising edge, hysteresis = $230mV$		1.8		V
Reference Load Regulation		$I_{REF} = -10\mu A$ to $+100\mu A$	1.980		2.015	mV
FAULT DETECTION						
SMPS1 Overvoltage Trip Threshold and PGOOD1 Upper Threshold	V _{OVP1} , V _{PG1_H}	With respect to the internal target voltage (error comparator threshold); rising edge; hysteresis = $50mV$	260	300	340	mV
		Dynamic transition		V _{REF} + 0.30		V
		Minimum OVP threshold		0.7		V
SMPS2 Adjustable Mode Overvoltage Trip Threshold and PGOOD2 Upper Threshold	V _{OVP2} , V _{PG2_H}	With respect to the internal target voltage $0.7V$ (error comparator threshold); hysteresis = $50mV$	120	150	180	mV
Output Overvoltage Fault Propagation Delay	t _{OVP}	CSL1/FB2 forced $25mV$ above trip threshold		5		μs
SMPS1 Undervoltage Protection Trip Threshold and Lower PGOOD1 Threshold	V _{UVP1} , V _{PG1_L}	With respect to the internal target voltage (error comparator threshold); falling edge; hysteresis = $50mV$	-240	-200	-160	mV
SMPS2 Undervoltage Protection Trip Threshold and Lower PGOOD2 Threshold	V _{UVP2} , V _{PG2_L}	With respect to the internal target voltage $0.7V$ (error comparator threshold); falling edge; hysteresis = $50mV$	-130	-100	-70	mV
Output Undervoltage Fault Propagation Delay	t _{UVP}	CSL1/FB2 forced $25mV$ below trip threshold	110	205	310	μs
PGOOD_ Propagation Delay	t _{PGOOD}	UVP falling edge, $25mV$ overdrive		5		μs
		OVP rising edge, $25mV$ overdrive		5		
		Startup delay from regulation	100	200	300	
PGOOD_ Output Low Voltage		$I_{SINK} = 3mA$			0.4	V
PGOOD_ Leakage Current	I _{PGOOD}	CSL1 = REFIN1, FB2 = $0.7V$ (PGOOD_ high impedance), PGOOD_ forced to $5V$, $T_A = +25^\circ C$			1	μA
Dynamic REFIN1 Transition Fault-Blanking Threshold		Fault blanking initiated; REFIN1 deviation from the internal target voltage (error comparator threshold); hysteresis = $10mV$		± 50		mV
Thermal-Shutdown Threshold	T _{SHDN}	Hysteresis = $15^\circ C$ (Note 3)		160		$^\circ C$
V _{CC} Undervoltage Lockout Threshold	V _{UVLO(VCC)}	Rising edge, PWM disabled below this level, hysteresis = $100mV$	3.95	4.20	4.45	V

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ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = 12V$, $V_{DD} = V_{CC} = EN1 = EN2 = 5V$, $V_{REFIN1} = 2V$, $\overline{SKIP} = GND$, $T_A = 0$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT LIMIT						
Current-Sense Input Range		CSH1, CSH2	0		2.3	V
		CSL1, CSL2	0		2.3	
Current-Sense Input (CSH_) Leakage Current		CSH_ = GND or V_{CC} , $T_A = +25^\circ C$	-0.2		+0.2	μA
Current-Sense Input (CSL_) Leakage Current		CSL_ = V_{CC} , $T_A = +25^\circ C$			1	μA
Current-Limit Threshold (Fixed)	$V_{CSLIMIT_}$	$V_{CSH_} - V_{CSL_}$, $ILIM1 = ILIM2 = REF$, $T_A = +25^\circ C$	28	30	32	mV
		$V_{CSH_} - V_{CSL_}$, $ILIM1 = ILIM2 = REF$, $T_A = 0^\circ C$ to $+85^\circ C$	27	30	33	
		$V_{CSH_} - V_{CSL_}$, $ILIM1 = ILIM2 = V_{CC}$	56	60	64	
		$V_{CSH_} - V_{CSL_}$, $ILIM1 = ILIM2 = OPEN$	42	45	48	
		$V_{CSH_} - V_{CSL_}$, $ILIM1 = ILIM2 = GND$	13	15	17	
Current-Limit Threshold (Negative)	V_{NEG}	$V_{CSH_} - V_{CSL_}$, $\overline{SKIP} = V_{CC}$		-1.2 x $V_{CSLIMIT_}$		mV
Current-Limit Threshold (Zero Crossing)	V_{ZX}	$V_{CSH_} - V_{CSL_}$, $\overline{SKIP} = GND$ or $OPEN$; $ILIM1 = ILIM2 = REF$		1		mV
Ultrasonic Frequency		$\overline{SKIP} = OPEN$ (3.3V); $V_{CSL1} = V_{REFIN1} + 50mV$; $V_{CSL2} = V_{FB2} + 50mV$	20			kHz
Ultrasonic Current-Limit Threshold		$\overline{SKIP} = OPEN$ (3.3V), $V_{CSL1} = V_{REF1} + 50mV$	22	33	46	mV
		$\overline{SKIP} = OPEN$ (3.3V), $V_{CSL2} = V_{FB2} + 50mV$	18	30	46	
Current-Balance Amplifier (GMI) Offset		$[V(CSH1, CSL1) - V(CSH2, CSL2)]$ at $I_{CCI} = 0$	-3		+3	mV
Current-Balance Amplifier (GMI) Transconductance		$\Delta I_{CCI} / \Delta [V(CSH1, CSL1) - V(CSH2, CSL2)]$; $V_{CC1} = V_{CSL1} = V_{CSL2} = 0.5V$ to $2V$, and $V(CSH_, CSL_) = -60.0mV$ to $+60.0mV$, $ILIM1 = GND$		180		μS
GATE DRIVERS						
DH1, DH2 Gate Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V	Low state (pulldown)	1.7	4.0	Ω
			High state (pullup)	1.7	4.0	
DL1, DL2 Gate Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)		1.3	3.0	Ω
		Low state (pulldown)		0.6	2.5	
DH1, DH2 Gate Driver Source/Sink Current	I_{DH}	DH_ forced to 2.5V, BST_ - LX_ forced to 5V		1.2		A
DL1, DL2 Gate Driver Source Current	$I_{DL(SOURCE)}$	DL_ forced to 2.5V		1		A
DL1, DL2 Gate Driver Sink Current	$I_{DL(SINK)}$	DL_ forced to 2.5V		2.4		A
Driver Propagation Delay		DH_ low to DL high	10	25	40	ns
		DL_ low to DH high	15	30	45	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = 12V$, $V_{DD} = V_{CC} = EN1 = EN2 = 5V$, $V_{REFIN1} = 2V$, $\overline{SKIP} = GND$, $T_A = 0$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DL_ Transition Time		DL_ falling, $C_{DL} = 3nF$	10	20		ns
		DL_ rising, $C_{DL} = 3nF$	10	20		
DH_ Transition Time		DH_ falling, $C_{DH} = 3nF$	10	20		ns
		DH_ rising, $C_{DH} = 3nF$	10	20		
Internal BST_ Switch On-Resistance	$R_{BST_}$	$I_{BST_} = 10mA$, $V_{DD} = 5V$		6.5	11.0	Ω
LX_, BST_ Leakage Current		$V_{BST_} = V_{LX_} = 26V$, $T_A = +25^\circ C$			5	μA
INPUTS AND OUTPUTS						
EN1, EN2 Logic-Input Threshold		EN1, EN2 rising edge, hysteresis = 300mV/600mV (min/max)	1.20	1.70	2.20	V
Logic-Input Current		EN1, EN2, $T_A = +25^\circ C$	-0.5		+0.5	μA
Quad-Level Input-Logic Levels		$\overline{SKIP}$, ILIM1, ILIM2	High (5V)		$V_{CC} - 0.4$	V
			Open (3.3V)		3.0	
			Ref (2.0V)		1.7	
			Low (GND)		0.4	
Quad-Level Logic-Input Current		$\overline{SKIP}$, ILIM1, ILIM2 forced to GND or V_{CC} , $T_A = +25^\circ C$	-2		+2	μA

ELECTRICAL CHARACTERISTICS

($V_{IN} = 12V$, $V_{DD} = V_{CC} = EN1 = EN2 = 5V$, $V_{REFIN1} = 2V$, $\overline{SKIP} = GND$, $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
PWM CONTROLLER						
Input Voltage Range	V _{IN}			4.5	26	V
Quiescent Supply Current (V _{DD} , V _{CC})	I _{DD} + I _{CC}	Output forced above regulation voltage, EN1 = EN2 = 5V			2.5	mA
On-Time (Note 1)	t _{ON1} , t _{ON2}	V _{IN} = 12V, V _{CSL1} = V _{CSL2} = V _{CCI} = 1.2V, separate or combined mode	R _{TON1} = R _{TON2} = 97.5kΩ (600kHz)	142	194	ns
			R _{TON1} = R _{TON2} = 200kΩ (300kHz)	305	368	
			R _{TON1} = R _{TON2} = 302.5kΩ (200kHz)	425	575	
Minimum Off-Time	t _{OFF(MIN)}	(Note 1)			330	ns
REFIN1 Voltage Range	V _{REFIN1}			0	V _{REF}	V
FB2 Input Voltage Range		Preset mode		1.7	2.3	V
FB2 Combined-Mode Threshold		Combined mode		3.75	V _{CC} - 0.4	V
REFIN, FB2 Bias Current	I _{REFIN1} , I _{FB2}			-0.1	+0.1	μA

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ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = 12V$, $V_{DD} = V_{CC} = EN1 = EN2 = 5V$, $V_{REFIN1} = 2V$, $\overline{SKIP} = GND$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
REFIN1 Dual-Mode Switchover Threshold			3.75	$V_{CC} - 0.4$	V
SMPS1 Voltage Accuracy	V_{CSL1}	Measured at CSL1, REFIN1 = V_{CC} ; $V_{IN} = 2V$ to $26V$, $\overline{SKIP} = V_{CC}$ (Note 2)	1.039	1.061	V
SMPS2 Voltage Accuracy	V_{CSL2}	Measured at CSL2, FB2 = REF; $V_{IN} = 2V$ to $26V$, $\overline{SKIP} = V_{CC}$ (Note 2)	1.485	1.515	V
INTERNAL REFERENCE					
Reference Voltage	V_{REF}	$V_{DD} = 4.5V$ to $5.5V$	1.985	2.015	V
FAULT DETECTION					
SMPS1 Overvoltage Trip Threshold and PGOOD1 Upper Threshold	V_{OVP1} , V_{PG1_H}	With respect to the internal target voltage (error comparator threshold); rising edge; hysteresis = 50mV	260	340	mV
SMPS2 Overvoltage Trip Threshold and PGOOD2 Upper Threshold	V_{OVP2} , V_{PG2_H}	With respect to the internal target voltage 0.7V (error comparator threshold); hysteresis = 50mV	120	180	mV
SMPS1 Undervoltage Protection Trip Threshold and Lower PGOOD1 Threshold	V_{UVP1} , V_{PG1_L}	With respect to the internal target voltage (error comparator threshold) falling edge; hysteresis = 50mV	-240	-160	mV
SMPS2 Undervoltage Protection Trip Threshold and Lower PGOOD2 Threshold	V_{UVP2} , V_{PG2_L}	With respect to the internal target voltage 0.7V (error comparator threshold) falling edge; hysteresis = 50mV	-130	-70	mV
Output Undervoltage Fault Propagation Delay	t_{UVP}	REFIN1/FB2 forced 25mV below trip threshold	80	320	μs
PGOOD_ Propagation Delay	t_{PGOOD}	Startup delay from regulation	80	320	μs
PGOOD_ Output Low Voltage		$I_{SINK} = 3mA$		0.4	V
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO}(V_{CC})$	Rising edge, PWM disabled below this level; hysteresis = 100mV	3.8	4.45	V
CURRENT LIMIT					
Current-Sense Input Range		CSH1, CSH2	0	2.3	V
		CSL1, CSL2	0	2.3	
Current-Limit Threshold (Fixed)	$V_{CSLIMIT}$	$V_{CSH_} - V_{CSL_}$, $ILIM1 = ILIM2 = REF$	27	33	mV
Ultrasonic Frequency		$\overline{SKIP} = OPEN$ (3.3V); $V_{CSL1} = V_{REFIN1} + 50mV$; $V_{CSL2} = V_{FB2} + 50mV$	18		kHz
Ultrasonic Current-Limit Threshold		$\overline{SKIP} = OPEN$ (3.3V)	$V_{CSL1} = V_{REF1} + 50mV$	22	mV
			$V_{CSL2} = V_{FB2} + 50mV$	18	
Current-Balance Amplifier (GMI) Offset		$[V(CSH1, CSL1) - V(CSH2, CSL2)]$ at $I_{CCI} = 0$	-3	+3	mV

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ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = 12V$, $V_{DD} = V_{CC} = EN1 = EN2 = 5V$, $V_{REFIN1} = 2V$, $\overline{SKIP} = GND$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
GATE DRIVERS						
DH1, DH2 Gate Driver On-Resistance	R _{ON(DH)}	BST_ - LX_ forced to 5V	Low state (pulldown)	4.5		Ω
			High state (pullup)	4.0		
DL1, DL2 Gate Driver On-Resistance	R _{ON(DL)}	High state (pullup)		3		Ω
		Low state (pulldown)		2		
Driver Propagation Delay		DH_ low to DL high		8	42	ns
		DL_ low to DH high		12	48	
Internal BST_ Switch On-Resistance	R _{BST_}	I _{BST_} = 10mA, V _{DD} = 5V		11		Ω
INPUTS AND OUTPUTS						
EN1, EN2 Logic-Input Threshold		EN1, EN2 rising edge; hysteresis = 300mV/600mV (min/max)		1.20	2.20	V
Quad-Level Input Logic Levels		$\overline{\text{SKIP}}$, ILIM1, ILIM2	High (5V)	V _{CC} - 0.4		V
			Open (3.3V)	3.0	3.6	
			Ref (2.0V)	1.7	2.3	
			Low (GND)	0.4		

Note 1: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX = GND, $V_{BST} = 5V$, and a 250pF capacitor connected from DH to LX. Actual in-circuit times might differ due to MOSFET switching speeds.

Note 2: The 0 to 0.5V range is guaranteed by design, not production tested.

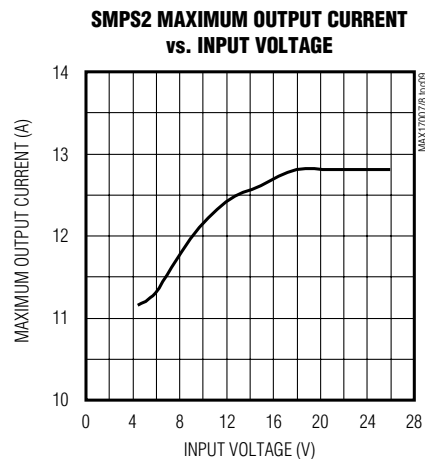
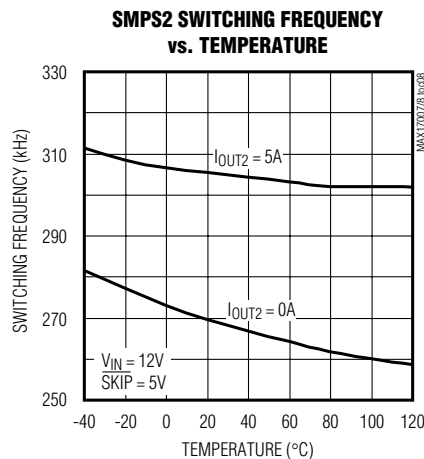
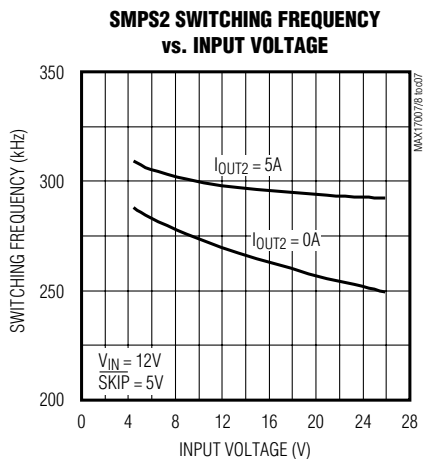
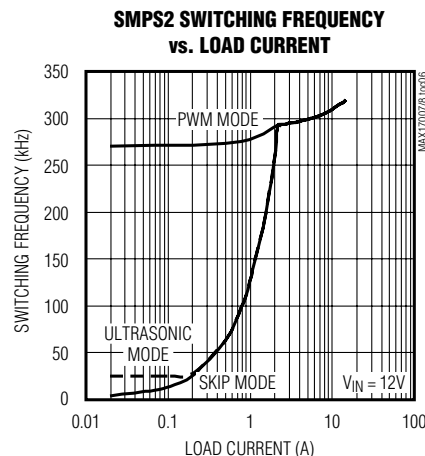
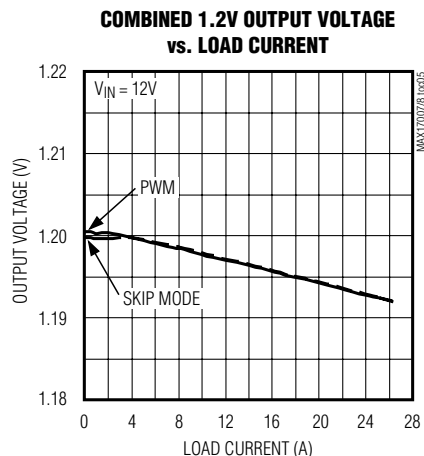
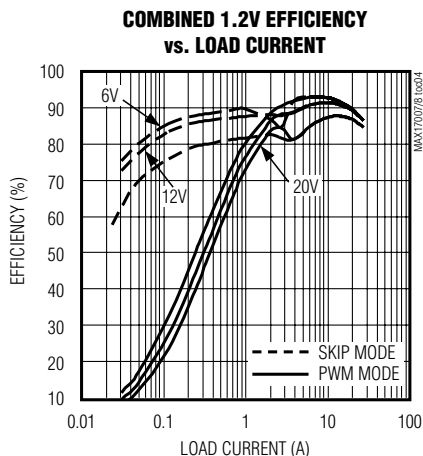
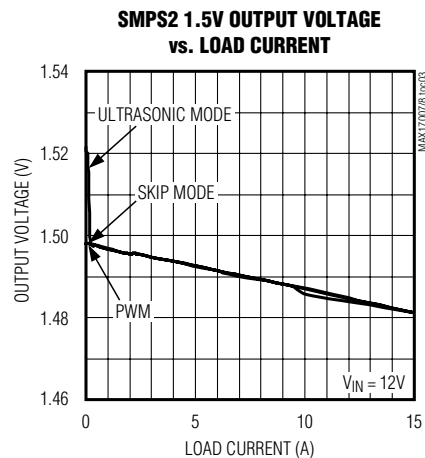
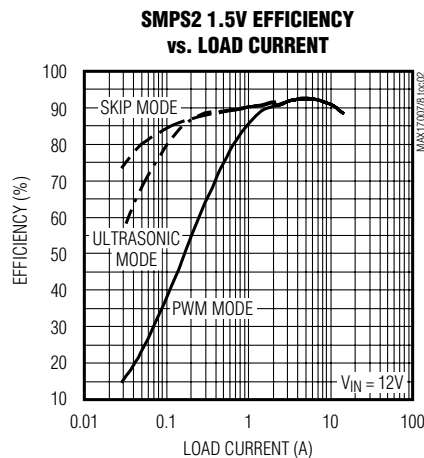
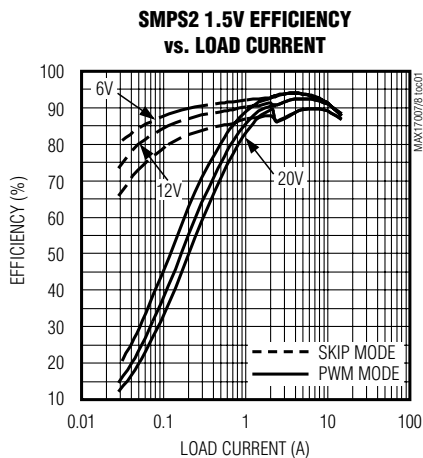
Note 3: Not production tested.

Note 4: Specifications to $T_A = -40^{\circ}C$ to $+105^{\circ}C$ are guaranteed by design, not production tested.

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

Typical Operating Characteristics

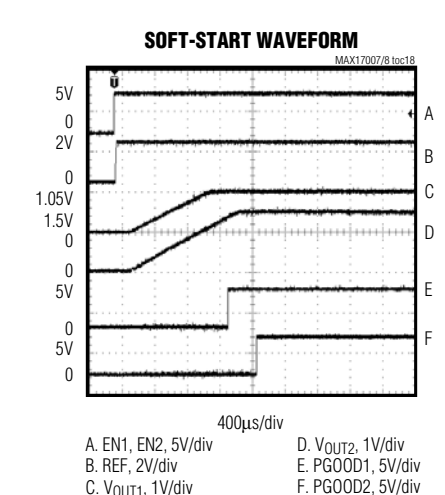
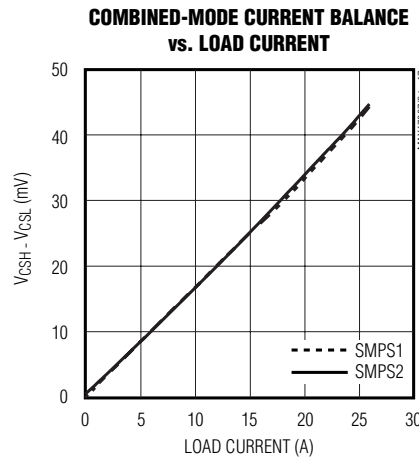
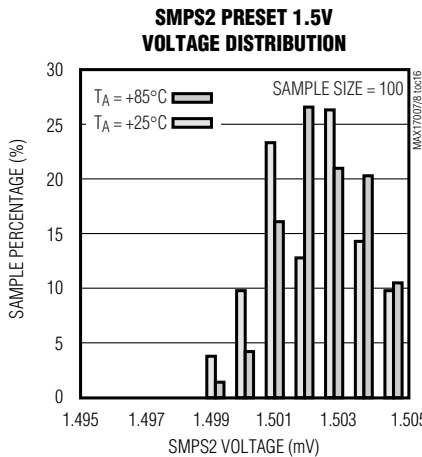
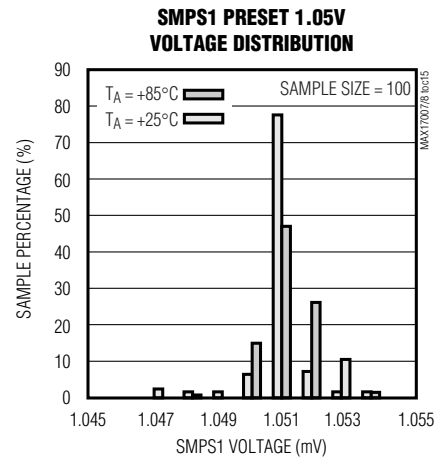
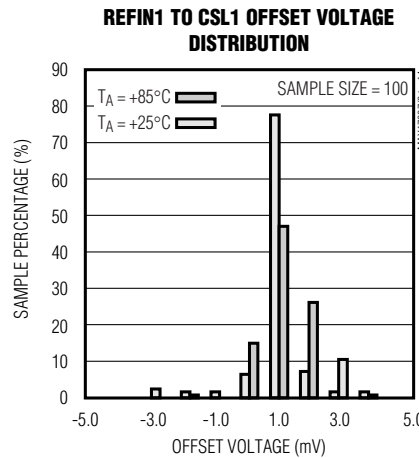
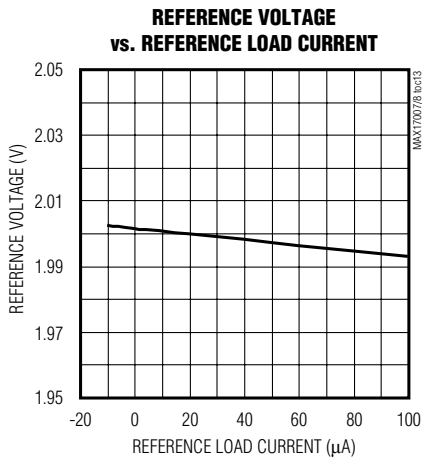
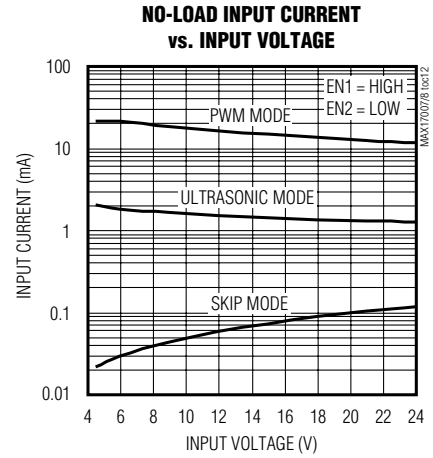
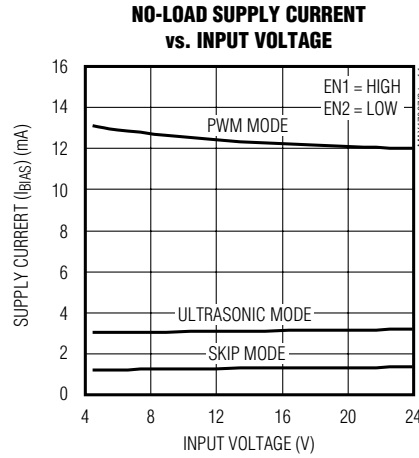
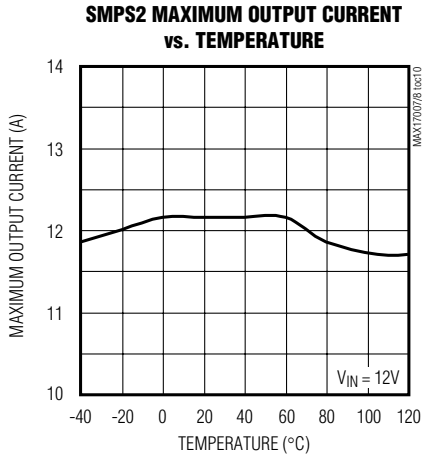
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Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

Typical Operating Characteristics (continued)

(Circuit of Figure 1, $V_{IN} = 12V$, $V_{DD} = 5V$, $\overline{SKIP} = GND$, $T_A = +25^\circ C$, unless otherwise noted.)



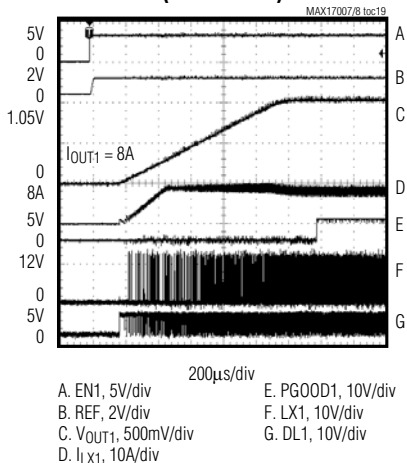
MAX17007/MAX17008

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

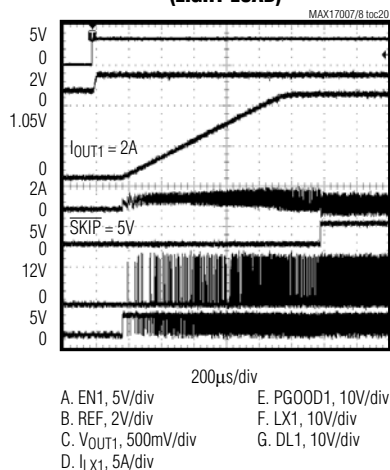
Typical Operating Characteristics (continued)

(Circuit of Figure 1, $V_{IN} = 12V$, $V_{DD} = 5V$, $\overline{SKIP} = GND$, $T_A = +25^\circ C$, unless otherwise noted.)

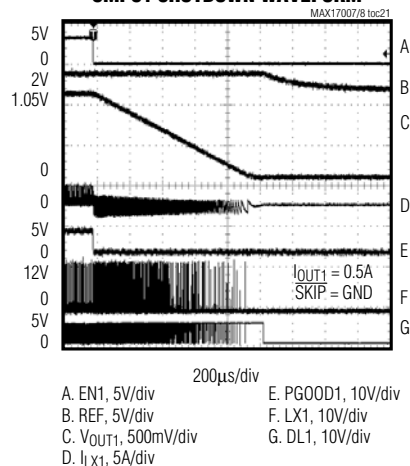
**SMPS1 STARTUP WAVEFORM
(HEAVY LOAD)**



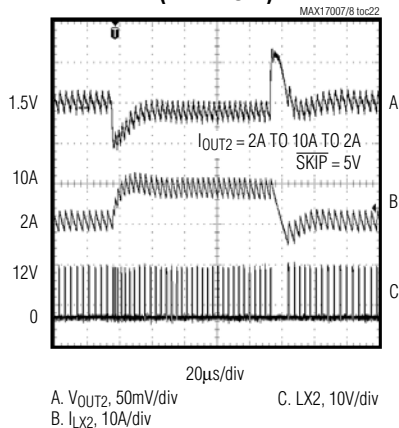
**SMPS1 STARTUP WAVEFORM
(LIGHT LOAD)**



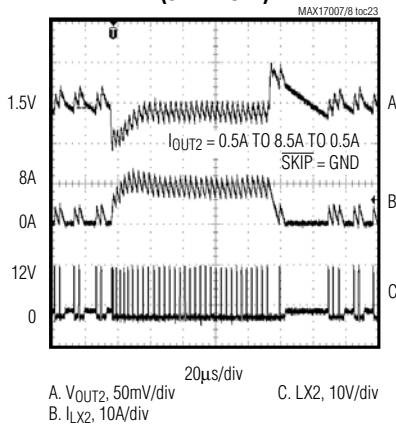
SMPS1 SHUTDOWN WAVEFORM



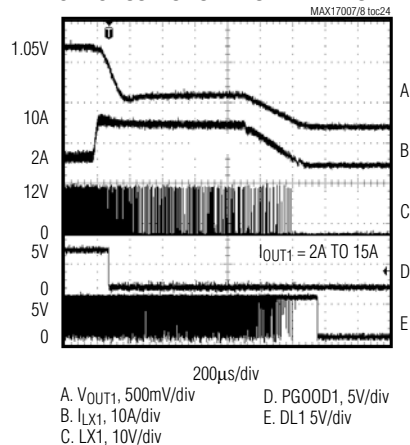
**SMPS2 LOAD-TRANSIENT RESPONSE
(PWM MODE)**



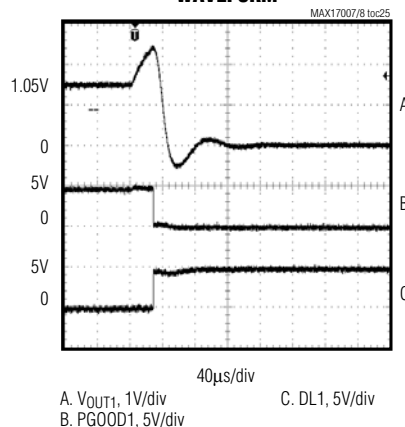
**SMPS2 LOAD-TRANSIENT RESPONSE
(SKIP MODE)**



SMPS1 OUTPUT OVERLOAD WAVEFORM



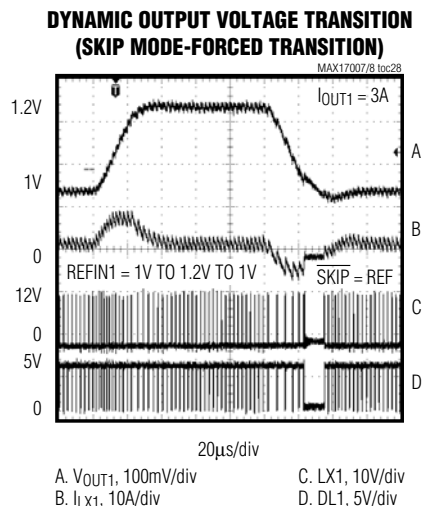
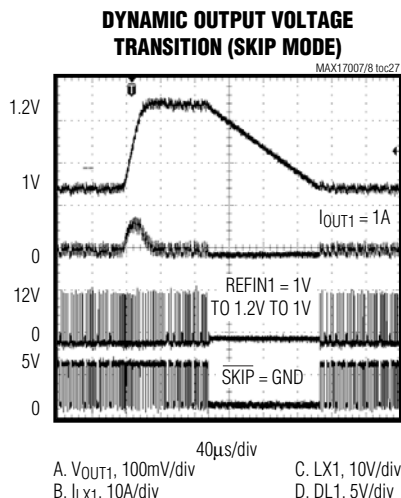
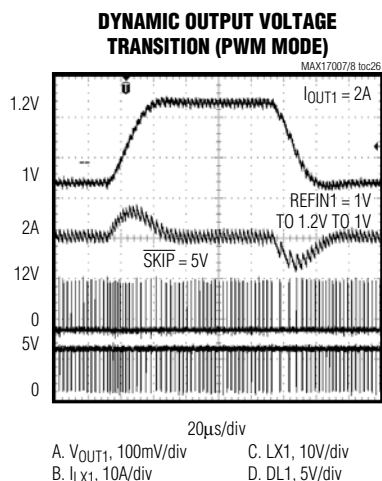
**SMPS1 OUTPUT OVERVOLTAGE
WAVEFORM**



Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

Typical Operating Characteristics (continued)

(Circuit of Figure 1, $V_{IN} = 12V$, $V_{DD} = 5V$, $\overline{SKIP} = GND$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION	
1	REF	2V Reference Voltage Output. Bypass REF to GND with a 2.2nF ceramic capacitor. The reference can source up to 100μA. Loading REF degrades output-voltage accuracy according to the REF load regulation error (see the <i>Typical Operating Characteristics</i>). The reference shuts down when both EN1 and EN2 are low.	
2	ILIM1	This four-level input determines the CSH1 to CSL1 current limit for SMPS1: V _{DD} (5V) = 60mV current limit Open (3.3V) = 45mV current limit REF (2V) = 30mV current limit GND = 15mV current limit In combined mode, ILIM1 sets the current-limit threshold for both sides.	
3	ILIM2 (CCI)	This four-level input determines the CSH2 to CSL2 current limit for SMPS2: V _{CC} (5V) = 60mV current limit Open (3.3V) = 45mV current limit REF (2V) = 30mV current limit GND = 15mV current limit In combined mode, ILIM2 is the current balance integrator (CCI) output pin. Connect a capacitor (C _{CCI}) between CCI and the output. The CCI capacitor value depends on the ILIM1 setting based on the following table:	
		ILIM1	C _{CCI} at ILIM2 (pF)
		V _{CC} (5V)	120
		Open (3.3V)	180
		REF (2V)	220
		GND	470
4	V _{CC}	5V Analog Supply Input. Bypass V _{CC} from V _{DD} using a 10_ resistor, and to analog ground using a 1μF ceramic capacitor.	

MAX17007/MAX17008

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

Pin Description (continued)

PIN	NAME	FUNCTION
5	$\overline{\text{SKIP}}$	Pulse-Skipping Control Input. This four-level input determines the mode of operation under normal steady-state conditions and dynamic output-voltage transitions: V_{DD} (5V) = Forced-PWM operation - Open (3.3V) = Ultrasonic mode (without forced-PWM during transitions) - REF (2V) = Pulse-skipping mode (with forced-PWM during transitions) - GND = Pulse-skipping mode (without forced-PWM during transitions) There are no dynamic transitions for SMPS2, so $\overline{\text{SKIP}} = 2V$ and $\overline{\text{SKIP}} = GND$ have the same pulse-skipping behavior for SMPS2 without any forced-PWM transitions. In combined mode, the ultrasonic mode is disabled, and the $\overline{\text{SKIP}} = \text{OPEN}$ (3.3V) setting is identical to the $\overline{\text{SKIP}} = GND$ setting.
6	TON1	Frequency-Setting Input for SMPS1. An external resistor between the input power source and TON1 sets the switching period (T_{SW1}) of SMPS1: $T_{SW1} = C_{TON} (R_{TON1} + 6.5k\Omega)$ where $C_{TON} = 16.26pF$. TON1 is high impedance in shutdown. In combined mode, TON1 sets the switching period for both SMPS1 and SMPS2.
7	TON2	Frequency-Setting Input for SMPS2. An external resistor between the input power source and TON2 sets the switching period (T_{SW2}) of SMPS2: $T_{SW2} = C_{TON} (R_{TON2} + 6.5k\Omega)$ where $C_{TON} = 16.26pF$. Set TON2 to a switching frequency different from TON1. A 10% to 30% difference in switching frequency between SMPS1 and SMPS2 is recommended. TON2 is high impedance in shutdown. In combined mode, TON2 cannot be left open.
8	REFIN1	External Reference Input for SMPS1. REFIN1 sets the feedback regulation voltage of CSL1. SMPS1 includes an internal window comparator to detect REFIN1 voltage changes that are greater than $\pm 50mV$ (typ), allowing the controller to blank PGOOD1 and the fault protection, and force the output transition, if enabled. When REFIN1 is tied to V_{CC}, SMPS1 regulates the output to 1.05V. In combined mode, REFIN1 sets the feedback regulation voltage of the combined output.
9	CSL1	Output-Sense and Negative Current-Sense Input for SMPS1. When using the internal preset 1.05V feedback divider ($REFIN1 = V_{CC}$), the controller uses CSL1 to sense the output voltage. Connect to the negative terminal of the current-sense element. Figure 14 describes two different current-sensing options—using accurate sense resistors or lossless inductor DCR sensing.
10	CSH1	Positive Current-Sense Input for SMPS1. Connect to the positive terminal of the current-sense element. Figure 14 describes two different current-sensing options—using accurate sense resistors or lossless inductor DCR sensing.
11	EN1	Enable Control Input for SMPS1. Connect to V_{CC} for normal operation. Pull EN1 low to disable SMPS1. The controller slowly ramps down the output voltage to ground and after the target voltage reaches 0.1V, the controller forces DL1 low. When both EN1 and EN2 are low, the device enters the low-power shutdown state. In combined mode, EN1 controls the combined SMPS output. EN2 is unused and must be grounded.
12	PGOOD1	Open-Drain Power-Good Output for SMPS1. PGOOD1 is low when the SMPS1 voltage is more than 200mV below or 300mV above the target voltage, during soft-start, and in shutdown. After the SMPS1 soft-start circuit has terminated, PGOOD1 becomes high impedance 200μs after the output is in regulation. PGOOD1 is blanked (forced high-impedance state) when a dynamic REFIN1 transition is detected.
13	DH1	High-Side Gate-Driver Output for SMPS1. DH1 swings from LX1 to BST1. DH1 is low in shutdown.

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

Pin Description (continued)

PIN	NAME	FUNCTION
14	LX1	Inductor Connection for SMPS1. Connect LX1 to the switched side of the inductor. LX1 serves as the lower supply rail for the DH1 high-side gate driver.
15	BST1	Bootstrap Capacitor Connection for SMPS1. The MAX17007/MAX17008 include an internal boost switch/diode connected between V _{DD} and BST1. Connect to an external capacitor as shown in Figure 1.
16	GND	Ground. Analog and power ground connection for the low-side gate driver of SMPS1.
17	DL1	Low-Side Gate Driver Output for SMPS1. DL1 swings from GND to V _{DD} . DL1 is forced low after the shutdown sequence has completed. DL1 is also forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that may be present. DL1 is forced low in V _{CC} UVLO.
18	V _{DD}	5V Driver Supply Input. Connect V _{DD} to V _{CC} through a 10Ω resistor. Bypass to ground through a 1μF or greater ceramic capacitor. V _{DD} is internally connected to the BST diodes and the low-side gate drivers.
19	DL2	Low-Side Gate-Driver Output for SMPS2. DL2 swings from PGND to V _{DD} . DL2 is forced low after the shutdown sequence has completed. DL2 is also forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that may be present. DL2 is forced low in V _{CC} UVLO.
20	PGND	Power Ground for the Low-Side Gate Driver of SMPS2
21	BST2	Bootstrap Capacitor Connection for SMPS2. The MAX17007/MAX17008 include an internal boost switch/diode connected between V _{DD} and BST2. Connect to an external capacitor as shown in Figure 1.
22	LX2	Inductor Connection for SMPS2. Connect LX2 to the switched side of the inductor. LX2 serves as the lower supply rail for the DH2 high-side gate driver.
23	DH2	High-Side Gate-Driver Output for SMPS2. DH2 swings from LX2 to BST2. DH2 is low in shutdown.
24	PGOOD2	Open-Drain Power-Good Output for SMPS2. PGOOD2 is low when the FB2 voltage is more than 100mV below or 150mV above the target voltage, during soft-start, and in shutdown. After the SMPS2 soft-start circuit has terminated, PGOOD2 becomes high impedance 200μs after the output is in regulation. In combined mode, PGOOD2 is not used and can be left open.
25	EN2	SMPS2 Enable Input. Connect to V _{CC} for normal operation. Pull EN2 low to disable SMPS2. The controller slowly ramps down the output voltage to ground, and after the target voltage reaches 0.1V, the controller forces DL2 low. When both EN1 and EN2 are low, the device enters the low-power shutdown state. In combined mode, EN2 is not used and should be connected to GND.
26	CSH2	Positive Current-Sense Input for SMPS2. Connect to the positive terminal of the current-sense element. Figure 14 describes two different current-sensing options—using accurate sense resistors or lossless inductor DCR sensing.
27	CSL2	Output-Sense and Negative Current-Sense Input for SMPS2. When using the internal preset 1.5V feedback divider (FB2 = REF), the controller uses CSL2 to sense the output voltage. Connect to the negative terminal of the current-sense element. Figure 14 describes two different current-sensing options—using accurate sense resistors or lossless inductor DCR sensing.
28	FB2	SMPS2 Feedback Input. Adjust the SMPS2 voltage with a resistive voltage-divider between SMPS2 output and GND. Connect FB2 to REF for preset 1.5V output. Tie FB2 to V _{CC} to configure the MAX17007/MAX17008 for combined-mode operation.
EP	PAD	Exposed Backside Pad. Connect to analog ground.

MAX17007/MAX17008

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

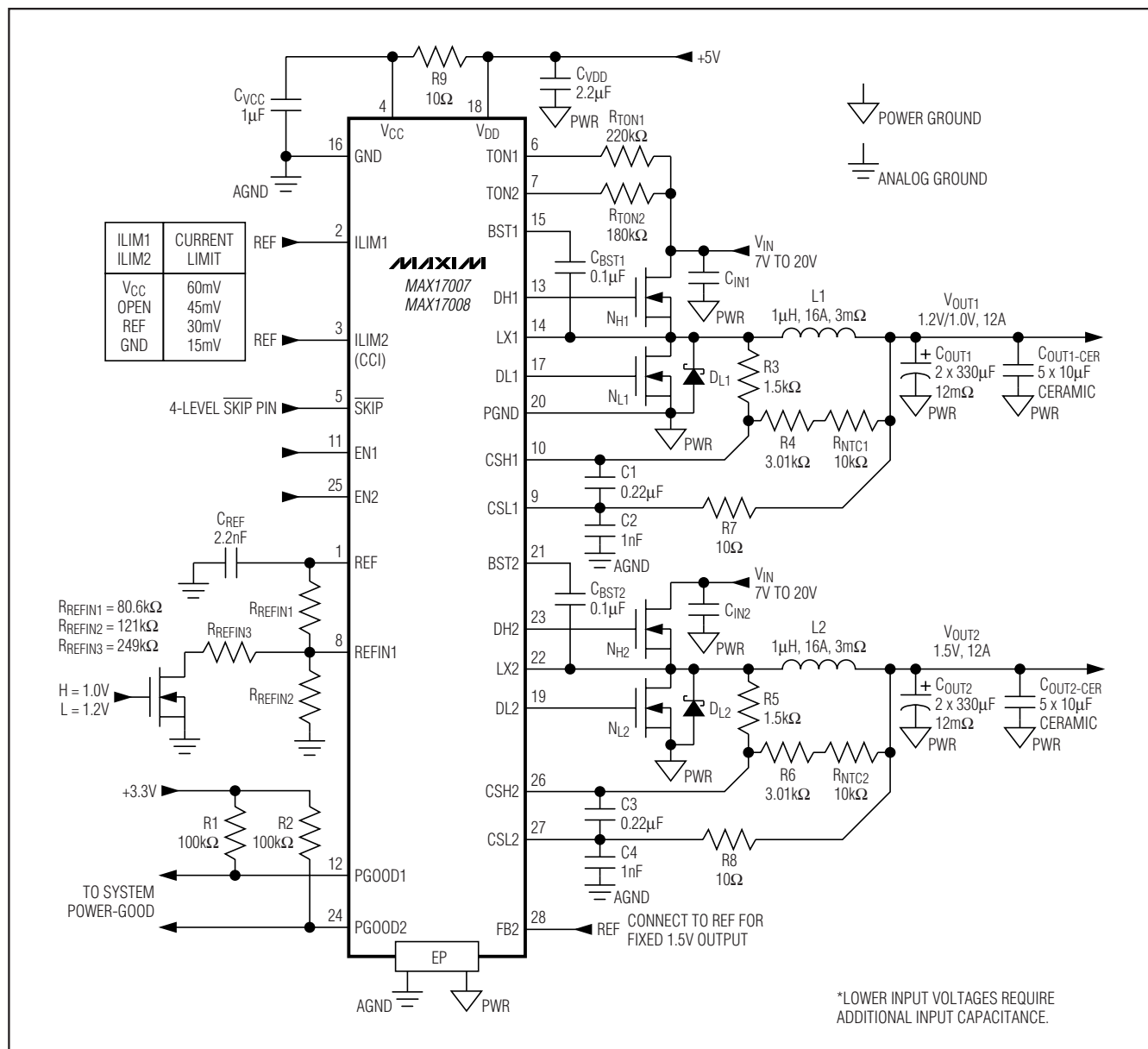


Figure 1. MAX17007/MAX17008 Separate-Mode Standard Application Circuit

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

MAX17007/MAX17008

Table 1. Component Selection for Standard Applications

COMPONENT	V _{OUT} = 1.0V/1.2V AT 12A (FIGURE 1)	V _{OUT} = 1.5V AT 12A (FIGURE 1)
	V _{IN} = 7V to 20V TON1 = 220k Ω (270kHz)	V _{IN} = 7V to 20V TON2 = 180k Ω (330kHz)
Input Capacitor (per Phase)	(2x) 10 μ F, 25V Taiyo Yuden TMK432BJ106KM	(2x) 10 μ F, 25V Taiyo Yuden TMK432BJ106KM
Output Capacitor	(2x) 330 μ F, 2.5V, 12m Ω , C case SANYO 2R5TPE330MCC2	(2x) 330 μ F, 2.5V, 12m Ω , C case SANYO 2R5TPE330MCC2
Inductor	1 μ H, 3.25m Ω , 16A Würth Electronics 7443552100	1 μ H, 3.25m Ω , 16A Würth Electronics 7443552100
Schottky Diode	2A, 30V Schottky diode (SMA) Nihon EC21QS03L Central Semiconductor CMSH2-40M	2A, 30V Schottky diode (SMA) Nihon EC21QS03L Central Semiconductor CMSH2-40M
High-Side MOSFET	Fairchild Semiconductor (1x) FDS8690 8.6m Ω /11.4m Ω (typ/max)	Fairchild Semiconductor (1x) FDS8690 8.6m Ω /11.4m Ω (typ/max)
Low-Side MOSFET	Fairchild Semiconductor (1x) FDS8670 4.2m Ω /5m Ω (typ/max)	Fairchild Semiconductor (1x) FDS8670 4.2m Ω /5m Ω (typ/max)

Table 2. Component Suppliers

MANUFACTURER	WEBSITE
AVX Corp.	www.avxcorp.com
BI Technologies	www.bitechnologies.com
Central Semiconductor Corp.	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET Corp.	www.kemet.com
NEC Tokin Corp.	www.nec-tokin.com
Panasonic Corp.	www.panasonic.com

MANUFACTURER	WEBSITE
Pulse Engineering	www.pulseeng.com
Renesas Technology Corp.	www.renesas.com
SANYO Electric Co., Ltd.	www.sanyodevice.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com
Vishay/Siliconix	www.vishay.com

Detailed Description

The MAX17007/MAX17008 standard application circuit (Figure 1) generates the 1V to 1.2V/12A and 1.5V/12A chipset voltages in a notebook computer. The input supply range is 7V to 20V for the specific application. Table 1 lists component selections, while Table 2 lists the component manufacturers. Figure 2 shows the combined-mode standard application circuit and Figure 3 is the MAX17007/MAX17008 functional diagram.

The MAX17007/MAX17008 contain two constant on-time step-down controllers designed for low-voltage power supplies. The two SMPSs can also be combined to operate as a two-phase high-current single-output regulator. Constant on-time Quick-PWM operation provides fast response to load transients and handles wide

I/O voltage ratios with ease, while maintaining a relatively constant switching frequency. The switching frequency can be adjusted between 200kHz and 600kHz with external resistors. Differential output current sensing allows output sense-resistor sensing for an accurate current-limit, lossless inductor DCR current sensing for lower power dissipation while maintaining 0.7% output accuracy. Overvoltage (MAX17007) and undervoltage protection and accurate user-selectable current limits (four different levels) ensure robust operations.

The MAX17007/MAX17008 feature a special combined-mode configuration that allows higher current outputs to be supported. A current-balance integrator maintains equal currents in the two phases, improving efficiency and power distribution.

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

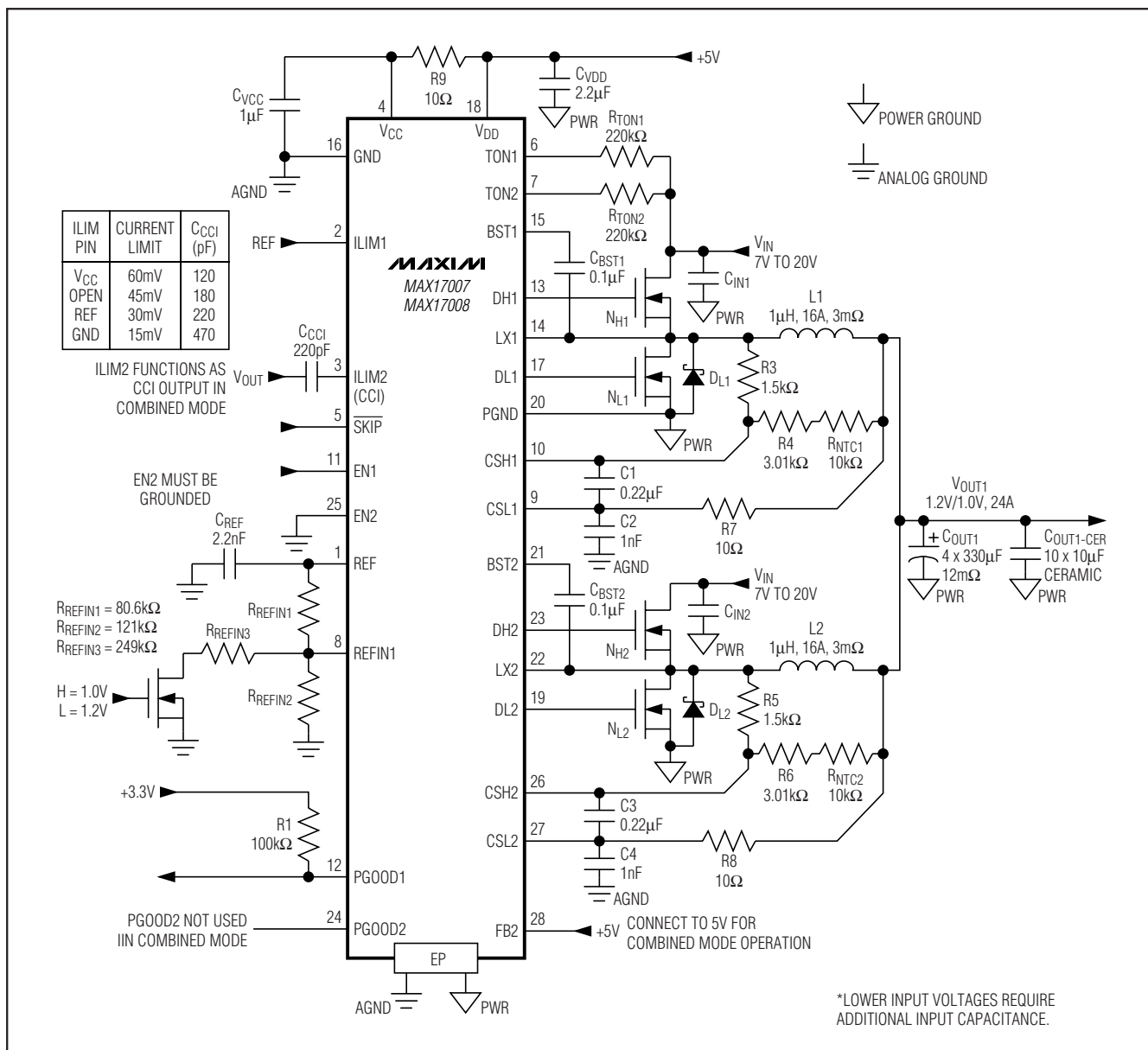


Figure 2. MAX17007/MAX17008 Combined-Mode Standard Application Circuit

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

MAX17007/MAX17008

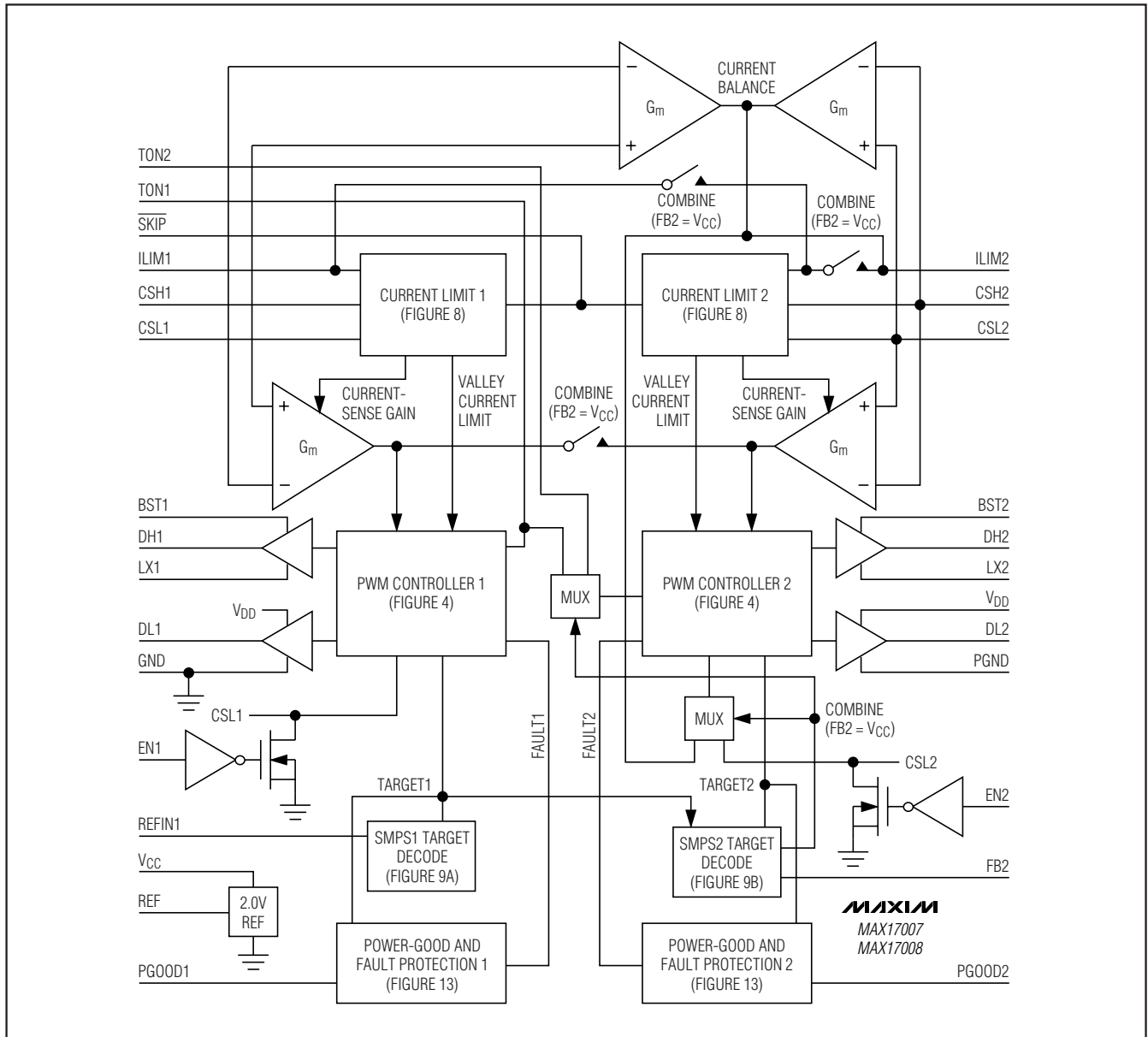


Figure 3. MAX17007/MAX17008 Functional Diagram

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

+5V Bias Supply (V_{CC} , V_{DD})

The MAX17007/MAX17008 require an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's 95%-efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the 5V supply can be generated with an external linear regulator such as the MAX1615.

The 5V bias supply powers both the PWM controllers and internal gate-drive power, so the maximum current drawn depends on the external MOSFET's gate capacitance, and the selected switching frequency:

$$I_{BIAS} = I_Q + f_{SW1}Q_G(SMPS1) + f_{SW2}Q_G(SMPS2) \\ = 4mA \text{ to } 40mA \text{ (typ)}$$

Bypass V_{CC} with a 1 μ F or greater ceramic capacitor to the analog ground. Bypass V_{DD} with a 2.2 μ F or greater ceramic capacitor to the power ground. V_{CC} and V_{DD} should be separated with a 10 Ω resistor (Figure 1).

2V Reference

The 2V reference is accurate to $\pm 1\%$ over temperature and load, making REF useful as a precision system reference. Bypass REF to GND with a 2.2nF. The reference sources up to 100 μ A and sinks 10 μ A to support external loads.

Combined-Mode Operation ($FB2 = V_{CC}$)

Combined-mode operation allows the MAX17007/MAX17008 to support even higher output currents by sharing the load current between two phases, distributing the power dissipation over several power components to improve the efficiency. The MAX17007/MAX17008 are configured in combined mode by connecting FB2 to V_{CC} . See Figure 2 for the combined-mode standard application circuit.

Table 3 lists the pin function differences between combined mode and separate mode. See the *Pin Description* table for additional details.

Table 3. Pin Function in Combined and Separate Modes

PIN	COMBINED MODE	SEPARATE MODE
FB2	Connect to V_{CC} to configure MAX17007/MAX17008 for combined-mode operation	Connect to REF for preset 1.5V, or use a resistor-divider to set the SMPS2 output voltage
REFIN1	Sets the combined output voltage—dynamic, fixed, and preset voltages supported	Sets the SMPS1 output voltage—dynamic, fixed, and preset voltages supported
EN1	Enables/disables combined output	Enables/disables SMPS1
EN2	Not used; connect to GND	Enables/disables SMPS2
PGOOD1	Power-good indicator for combined output voltage	Power-good indicator for SMPS1
PGOOD2	Not used; can be left open	Power-good indicator for SMPS2
TON1	Sets the per-phase switching frequency for both SMPSs	Sets the switching frequency for SMPS1
TON2	Use the same resistor as TON1	Sets the switching frequency for SMPS2
ILIM1	Sets the per-phase current limit for both SMPSs	Sets SMPS1 current limit
ILIM2 (CCI)	Current-balance integrator output; connect a capacitor from CCI to the output	Sets SMPS2 current limit
$\overline{SKIP}$	Only three distinct modes of operation; ultrasonic mode not supported	Supports all four modes of operation

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

SMPS Detailed Description

Free-Running Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator with voltage feed-forward. This architecture relies on the output filter capacitor's ESR to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (150ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out. Figure 4 is the PWM controller block diagram.

On-Time One-Shot

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. In independent mode, the high-side switch on-time is inversely proportional to the battery voltage as sensed by the TON1 and TON2 inputs, and proportional to the voltages on CSL1 and CSL2 pins:

$$\text{SMPS1 On-Time } t_{\text{ON1}} = T_{\text{SW1}} (V_{\text{CSL1}}/V_{\text{IN}})$$

$$\text{SMPS2 On-Time } t_{\text{ON2}} = T_{\text{SW2}} (V_{\text{CSL2}}/V_{\text{IN}})$$

where T_{SW1} (switching period of SMPS1) is set by the resistance between TON1 and V_{IN} , T_{SW2} is set by the resistance between TON2 and V_{IN} . This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator.

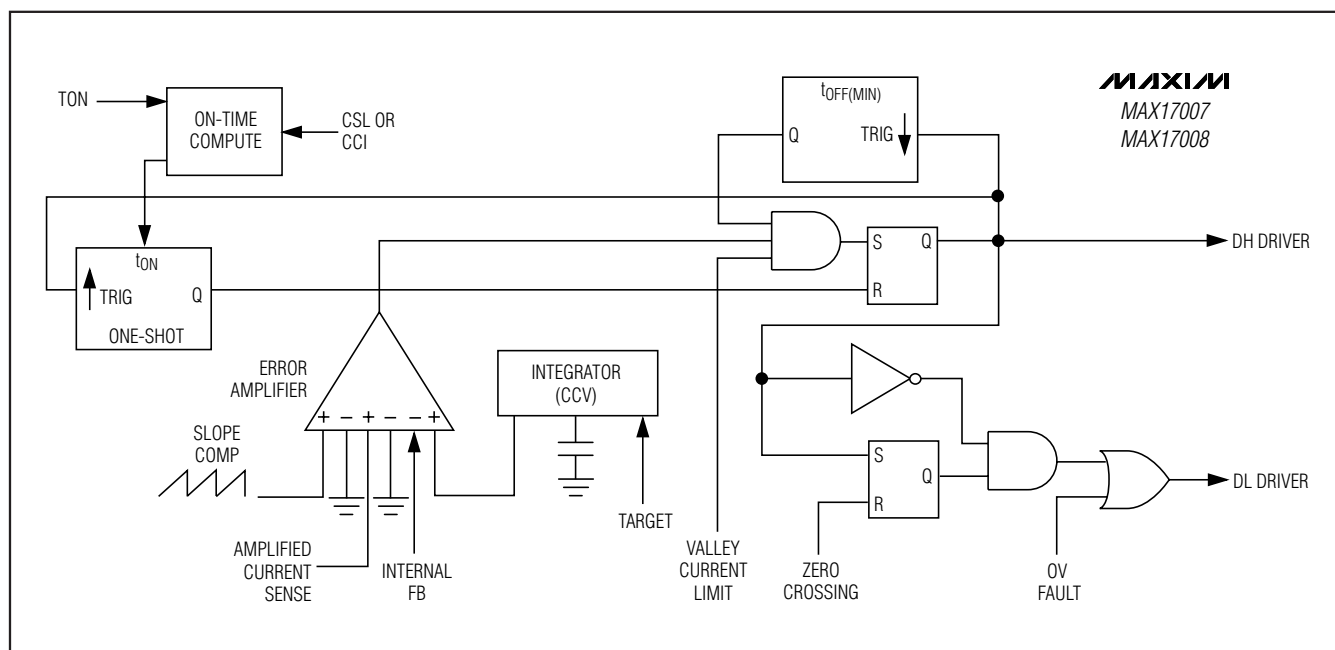


Figure 4. PWM Controller Block Diagram

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

Switching Frequency

The MAX17007/MAX17008 feature independent resistor-programmable switching frequencies for each SMPS, providing flexibility for applications where one SMPS operates at a lower switching frequency when connected to a high-voltage input rail while the other SMPS operates at a higher switching frequency when connected to a lower voltage rail as a second-stage regulator. Connect a resistor (R_{TON}) between TON and V_{IN} to set the switching period $T_{SW} = 1/f_{SW}$:

$$T_{SW1} = C_{TON} (R_{TON1} + 6.5k\Omega)$$

$$T_{SW2} = C_{TON} (R_{TON2} + 6.5k\Omega)$$

where $C_{TON} = 16.26pF$. A $97.5k\Omega$ to $302.5k\Omega$ corresponds to switching periods of $1.67\mu s$ (600kHz) to $5\mu s$ (200kHz) for SMPS1 and SMPS2. High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

For continuous conduction operation, the actual switching frequency can be estimated by:

$$f_{SW} = \frac{V_{OUT} + V_{DIS}}{t_{ON}(V_{IN} + V_{CHG})}$$

where V_{DIS} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and printed-circuit board (PCB) resistances; V_{CHG} is the sum of the resistances in the charging path, including the high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time calculated by the on-time block.

When operating in separate mode, it is recommended that both SMPS switching frequencies be set apart by 10% to 30% to prevent the two sides from beating against each other.

Combined-Mode On-Time One-Shot

In combined mode ($FB2 = V_{CC}$), $TON1$ sets the on-time, and hence the switching frequency, for both SMPS. The on-time is programmed using the $TON1$ equation, which sets the switching frequency per phase. The effective switching frequency as seen on the input and output capacitors is twice the per-phase frequency.

Combined-Mode Current Balance

In combined mode, the one-shot for SMPS2 varies the on-time in response to the input voltage and the difference between the SMPS1 and SMPS2 inductor currents. The SMPS1 one-shot in combined mode behaves the same way as it does in separate mode. As such, SMPS2 regulates the current balance, while SMPS1 regulates the voltage.

Two identical transconductance amplifiers integrate the difference between SMPS1 and SMPS2 current-sense signals. The summed output is internally connected to CCI, allowing adjustment of the integration time constant with a compensation network (usually a capacitor) connected between CCI and the output.

The resulting compensation current and voltage are determined by the following equations:

$$I_{CCI} = G_m[(V_{CSH1} - V_{CSL1}) - (V_{CSH2} - V_{CSL2})]$$

$$V_{CCI} = V_{OUT} + I_{CCI}Z_{CCI}$$

where Z_{CCI} is the impedance at the CCI output. The SMPS2 on-time one-shot uses this integrated signal (V_{CCI}) to set the SMPS2 high-side MOSFETs on-time. When SMPS1 and SMPS2 current-sense signals ($V_{CSH1} - V_{CSL1}$ and $V_{CSH2} - V_{CSL2}$) become unbalanced, the transconductance amplifiers adjust the SMPS2 on-time, which increases or decreases the SMPS2 inductor current until the current-sense signals are properly balanced. In combined mode, the SMPS2 on-time is given by:

$$\text{SMPS2 On-Time } t_{ON2} = T_{SW2} (V_{CCI}/V_{IN})$$

SMPS Enable Controls (EN1, EN2)

EN1 and EN2 provide independent control of output soft-start and soft-shutdown. This allows flexible control of startup and shutdown sequencing. The outputs can be started simultaneously, sequentially, or independently. To provide sequential startup, connect EN of one regulator to PGOOD of the other. For example, with EN1 connected to PGOOD2, OUT1 soft-starts after OUT2 is in regulation.

When configured in separate mode, the two outputs are independent. A fault at one output does not trigger shutdown of the other.

When configured in combined mode ($FB2 = V_{CC}$), EN1 is the master control input that enables/disables the combined output, while EN2 has no function and must be connected to GND. The startup slew rate follows that of SMPS1.

Toggle EN low to clear the overvoltage, undervoltage, and thermal-fault latches.

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Soft-Start

Soft-start begins when EN is driven high and REF is in regulation. During soft-start, the output is ramped up from 0V to the final set voltage at 1.3mV/μs slew rate for SMPS1, and 0.65mV/μs for SMPS2, reducing the inrush current and providing a predictable ramp-up time for power sequencing:

$$t_{\text{START1}} = t_{\text{SHDN1}} = \frac{V_{\text{REFIN1}}}{\text{SR}_{\text{SS1}}} = \frac{V_{\text{REFIN1}}}{1.3\text{mV}/\mu\text{s}}$$

$$t_{\text{START2}} = t_{\text{SHDN2}} = \frac{V_{\text{FB2}}}{\text{SR}_{\text{SS2}}} = \frac{V_{\text{FB2}}}{0.65\text{mV}/\mu\text{s}}$$

The soft-start circuitry does not use a variable current limit, so full output current is available immediately. The respective PGOOD becomes high impedance approximately 200μs after the target voltage has been reached. The MAX17007/MAX17008 automatically use pulse-skipping mode during soft-start and use forced-PWM mode during soft-shutdown, regardless of the SKIP configuration.

For automatic startup, the battery voltage should be present before VCC. If the controller attempts to bring the output into regulation without the battery voltage present, the fault latch trips. The controller remains shut down until the fault latch is cleared by toggling EN or cycling the VCC power supply below 0.5V.

Soft-Shutdown

Soft-shutdown begins when the system pulls EN low, an output undervoltage fault, or a thermal fault. During soft-shutdown, the respective PGOOD is pulled low immediately and the output voltage ramps down with the same startup slew rate for the respective outputs. After the controller reaches the 0V target, the drivers are disabled (DL_ and DH_ pulled low) and the internal 10Ω discharge on CSL_ activated. The MAX17007/MAX17008 shut down completely when both EN are low—the reference turns off after both SMPSs have reached the 0V target, and the supply current drops to about 1μA (max).

Slowly discharging the output capacitors by slewing the output over a long period of time (typically 0.5ms to 2ms) keeps the average negative inductor current low (damped response), thereby preventing the negative output-voltage excursion that occurs when the controller discharges the output quickly by permanently turning on the low-side MOSFET (underdamped

response). This eliminates the need for the Schottky diode normally connected between the output and ground to clamp the negative output-voltage excursion.

Modes of Operation

Forced-PWM Mode ($\overline{\text{SKIP}} = 5\text{V}$)

The low-noise forced-PWM mode ($\overline{\text{SKIP}} = 5\text{V}$) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH maintains a duty factor of $V_{\text{OUT}}/V_{\text{IN}}$. The benefit of forced-PWM mode is to keep the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V bias current remains between 2mA to 5mA, depending on the switching frequency.

The MAX17007/MAX17008 automatically use forced-PWM operation during shutdown, regardless of the SKIP configuration.

Automatic Pulse-Skipping Mode ($\overline{\text{SKIP}} = \text{GND or } 2\text{V}$)

In skip mode ($\overline{\text{SKIP}} = \text{GND or } 2\text{V}$), an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator threshold is set by the differential across CSL_ and CSH_.

DC output-accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the MAX17007/MAX17008 regulate the valley of the output ripple, so the actual DC output voltage is higher than the trip level by 50% of the output ripple voltage. In discontinuous conduction ($\overline{\text{SKIP}} = \text{GND or } 2\text{V}$ and $I_{\text{OUT}} < I_{\text{LOAD}}(\text{SKIP})$), the output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation. However, the internal integrator corrects for most of it, resulting in very little load regulation.

When $\overline{\text{SKIP}} = 2\text{V}$, the MAX17007/MAX17008 use forced-PWM operation during all dynamic output-voltage transitions until 100μs after the transition has been completed—REFIN1 and the internal target are within ±50mV (typ) and an error-amplifier transition is detected. Since SMPS2 does not support dynamic transitions, $\overline{\text{SKIP}} = 2\text{V}$ and $\overline{\text{SKIP}} = \text{GND}$ have the same pulse-skipping behavior without any forced-PWM transitions.

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When $\overline{\text{SKIP}}$ is pulled to GND, the MAX17007/MAX17008 remain in pulse-skipping mode. Since the output is not able to sink current, the timing for negative dynamic output-voltage transitions depends on the load current and output capacitance. Letting the output voltage drift down is typically recommended in order to reduce the potential for audible noise since this eliminates the input current surge during negative output-voltage transitions. Figure 5 shows the pulse-skipping/discontinuous crossover point.

Ultrasonic Mode ($\overline{\text{SKIP}} = \text{Open} = 3.3\text{V}$)

Leaving $\overline{\text{SKIP}}$ unconnected or connecting $\overline{\text{SKIP}}$ to 3.3V activates a unique pulse-skipping mode with a minimum switching frequency of 25kHz. This ultrasonic pulse-skipping mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the controller automatically transitions to fixed-frequency PWM operation when the load reaches the same critical conduction point ($I_{\text{LOAD}}(\text{SKIP})$) that occurs when normally pulse skipping.

An ultrasonic pulse occurs when the controller detects that no switching has occurred within the last 30 μs . Once triggered, the ultrasonic controller pulls DL high, turning on the low-side MOSFET to induce a negative inductor current (Figure 6). After the inductor current reaches the negative ultrasonic current threshold, the controller turns off the low-side MOSFET (DL pulled low) and triggers a constant on-time (DH driven high). When the on-time has expired, the controller reenables the low-side MOSFET until the controller detects that the inductor current dropped below the zero-crossing threshold. Starting with a DL pulse greatly reduces the peak output voltage when compared to starting with a DH pulse.

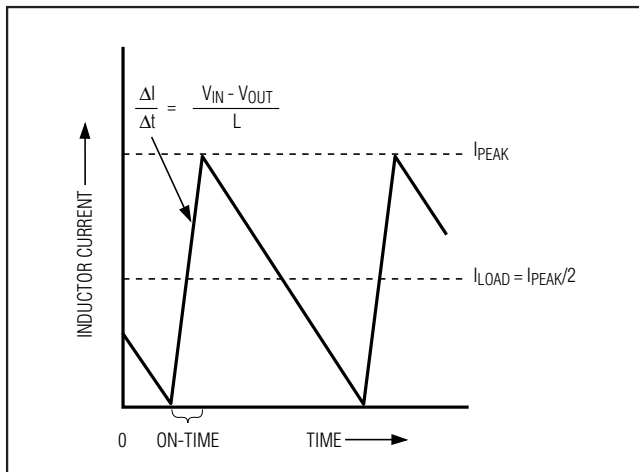


Figure 5. Pulse-Skipping/Discontinuous Crossover Point

The output voltage at the beginning of the ultrasonic pulse determines the negative ultrasonic current threshold, resulting in the following equations for SMPS1:

$$V_{\text{ISONIC1}} = I_{L1}R_{\text{CS1}} = (V_{\text{REFIN1}} - V_{\text{CSL1}}) \times 0.65$$

(SMPS1 adjustable mode)

$$V_{\text{ISONIC1}} = I_{L1}R_{\text{CS1}} = (1.05\text{V} - V_{\text{CSL1}}) \times 0.65$$

(SMPS1 preset mode)

where $V_{\text{CSL1}} > V_{\text{REFIN1}}$ in adjustable mode, $V_{\text{CSL1}} > 1.05\text{V}$ in preset mode, and R_{CS1} is the current-sense resistance seen across CSH1 to CSL1.

Similarly for SMPS2:

$$V_{\text{ISONIC2}} = I_{L2}R_{\text{CS2}} = (0.7\text{V} - V_{\text{FB2}}) \times 0.65$$

(SMPS2 adjustable mode)

$$V_{\text{ISONIC2}} = I_{L2}R_{\text{CS2}} = (1.5\text{V} - V_{\text{CSL2}}) \times 0.65$$

(SMPS2 preset mode)

where $V_{\text{CSL2}} > 0.7\text{V}$ in adjustable mode, $V_{\text{CSL2}} > 1.5\text{V}$ in preset mode, and R_{CS2} is the current-sense resistance seen across CSH2 to CSL2.

In combined mode, ultrasonic mode setting is disabled, and the $\overline{\text{SKIP}} = \text{OPEN}$ (3.3V) setting is identical to the $\overline{\text{SKIP}} = \text{GND}$ setting.

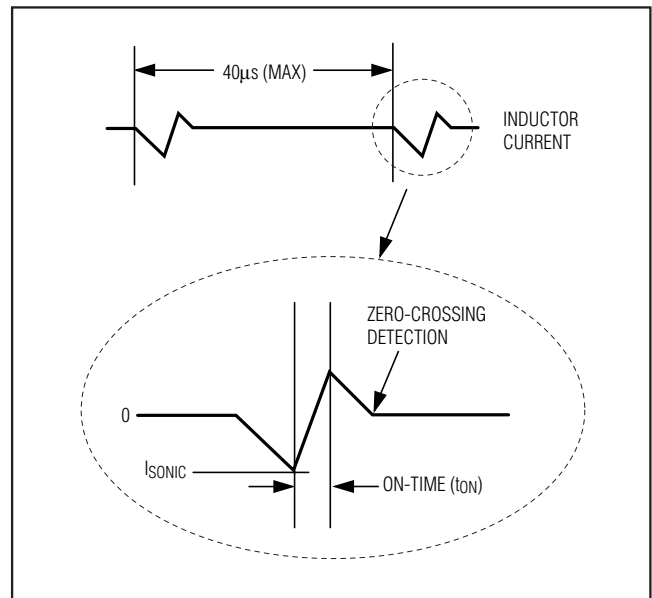


Figure 6. Ultrasonic Waveform

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Valley Current-Limit Protection

The current-limit circuit employs a unique “valley” current-sensing algorithm that senses the inductor current across the output current-sense element—inductor DCR or current-sense resistor, which generates a voltage between CSH₋ and CSL₋. If the current exceeds the valley current-limit threshold during the low-side MOSFET conduction time, the PWM controller is not allowed to initiate a new cycle. The valley current-limit threshold is set by the four-level ILIM₋ pin, with selectable limits of 15mV, 30mV, 45mV, and 60mV.

The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current (Figure 7). Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance. See Figure 8.

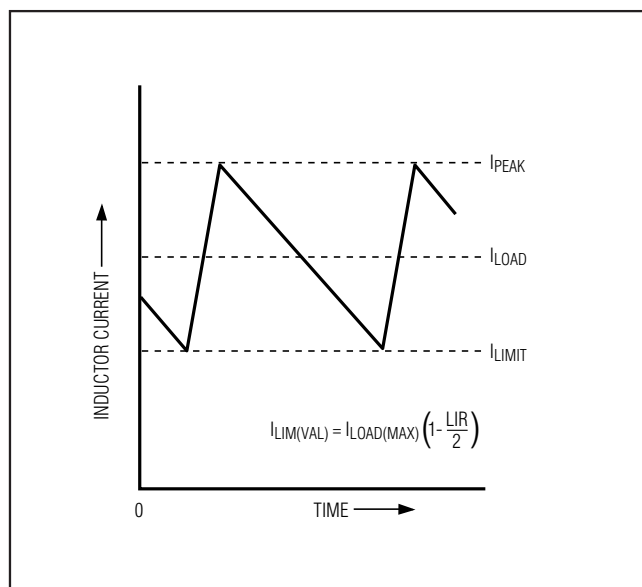


Figure 7. “Valley” Current-Limit Threshold Point

In forced-PWM mode, the MAX17007/MAX17008 also implement a negative current limit to prevent excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit.

In combined mode, ILIM1 sets the per-phase current limit for both phases.

MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. The high-side gate driver (DH) sources and sinks 1.2A, and the low-side gate driver (DL) sources 1.0A and sinks 2.4A. This ensures robust gate drive for high-current applications. The DH floating high-side MOSFET driver is powered by internal boost switch charge pumps at BST, while the DL synchronous-rectifier driver is powered directly by the 5V bias supply (V_{DD}).

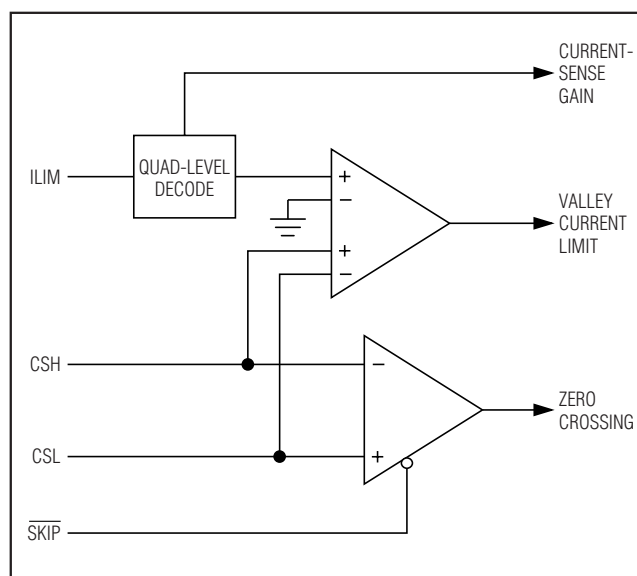


Figure 8. Current-Limit Block Diagram

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Output Voltage

The MAX17007/MAX17008 feature preset and adjustable output voltages for both SMPSs, and dynamic output voltages for SMPS1. In combined mode, the output voltage is set by REFIN1, and all features for SMPS1 output-voltage configuration and dynamic voltage changes apply to the combined output. Figure 9 is the SMPS target decode block diagram.

Preset/Adjustable Output Voltages (Dual-Mode Feedback)

Connect REFIN1 to V_{CC} to set the SMPS1 voltage to preset 1.05V. Connect FB2 to REF to set the SMPS2

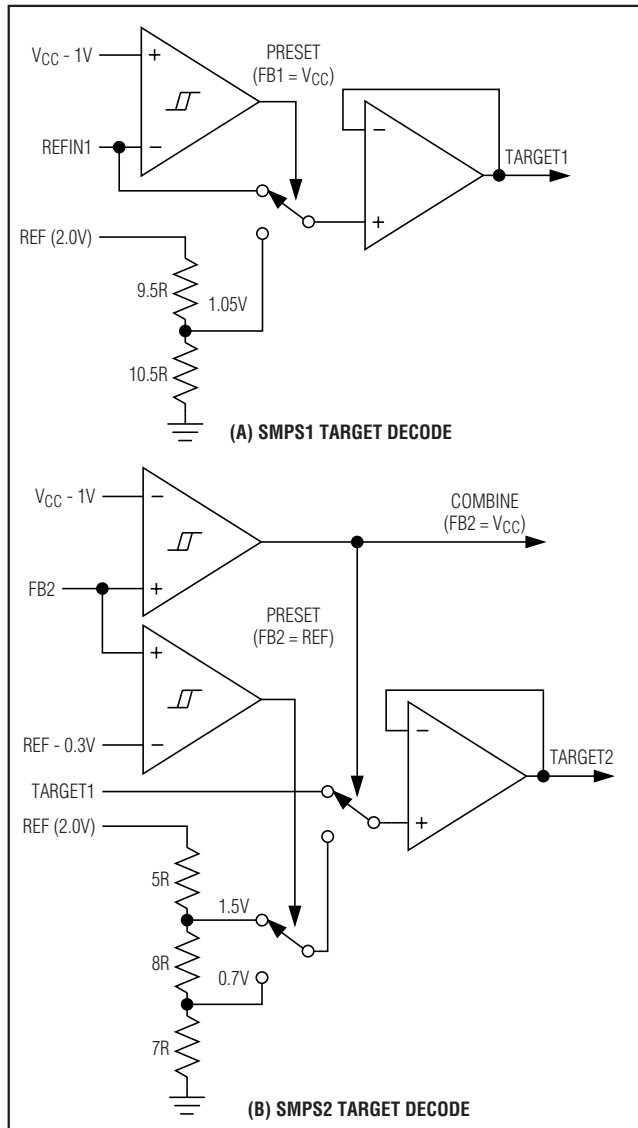


Figure 9. SMPS Target Decode Block Diagram

voltage to preset 1.5V. The SMPS1 output voltage can be adjusted up to 2V by changing REFIN1 voltage without using an external resistive voltage-divider. The output voltage of SMPS2 can be adjusted with an external resistive voltage-divider between CSL2 and GND with the center tap connected to FB2 (Figure 10). Choose R_{FB2LO} (resistance from FB2 to GND) to be approximately 10k Ω and solve for R_{FB2HI} (resistance from CSL2 to FB2) using the equation:

$$R_{FB2HI} = R_{FB2LO} \left(\frac{V_{CSL2}}{0.7V} - 1 \right)$$

The MAX17007/MAX17008 regulate the valley of the output ripple, so the actual DC output voltage is higher than the slope compensated target by 50% of the output ripple voltage. Under steady-state conditions, the MAX17007/MAX17008s' internal integrator corrects for this 50% output ripple voltage error, resulting in an output-voltage accuracy that is dependent only on the offset voltage of the integrator amplifier provided in the *Electrical Characteristics* table.

Dynamic Output Voltages (REFIN1)

The MAX17007/MAX17008 regulate the output to the voltage set at REFIN1. By changing the voltage at REFIN1 (Figure 1), the MAX17007/MAX17008 can be used in applications that require dynamic output voltage changes between two set points. For a step-voltage change at REFIN, the rate of change of the output voltage is limited either by the internal 9.5mV/ μ s slew-rate circuit or by the component selection—inductor current ramp, the total output capacitance, the current limit, and the load during the transition—whichever is slower. The total output capacitance determines how much current is needed to change the output voltage, while the inductor limits the current ramp rate.

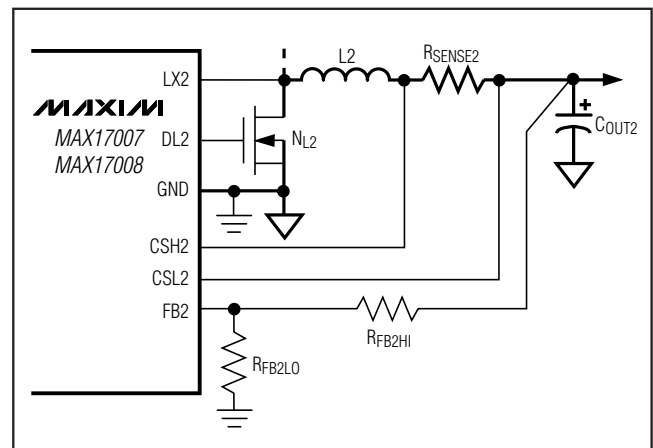


Figure 10. Setting V_{OUT2} with a Resistive Voltage-Divider

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Additional load current can slow down the output voltage change during a positive REFIN1 voltage change, and can speed up the output voltage change during a negative REFIN1 voltage change.

Automatic Fault Blanking (SMPS1)

When the MAX17007/MAX17008 detect that the internal target and REFIN1 are more than $\pm 50\text{mV}$ (typ) apart, the controller automatically blanks PGOOD1, blanks the

UVP protection, and sets the OVP threshold to max REF + 300mV. The blanking remains until 1) the internal target and REFIN1 are within $\pm 30\text{mV}$ of each other, and 2) an edge is detected on the error amplifier signifying that the output is in regulation. This prevents the system or internal fault protection from shutting down the controller during transitions. Figure 11 shows the dynamic REFIN transition ($\overline{\text{SKIP}} = \text{GND}$) and Figure 12 shows the dynamic REFIN1 transition ($\overline{\text{SKIP}} = \text{REF}$).

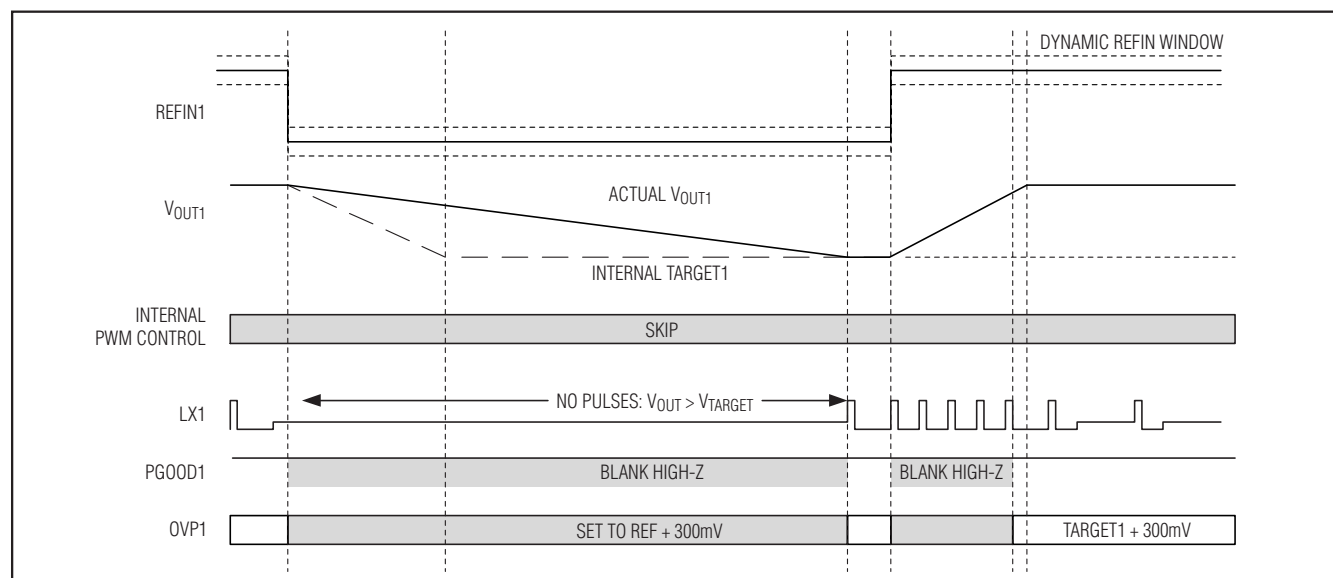


Figure 11. Dynamic REFIN1 Transition ($\overline{\text{SKIP}} = \text{GND}$)

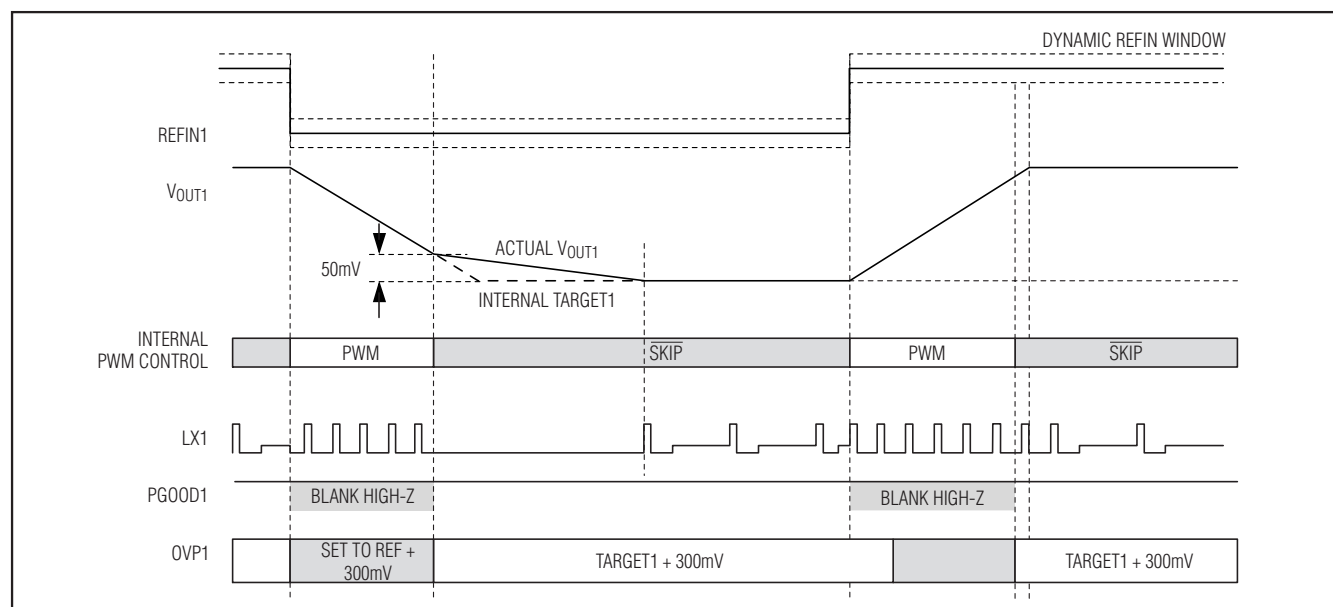


Figure 12. Dynamic REFIN1 Transition ($\overline{\text{SKIP}} = \text{REF}$)

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Internal Integration

An integrator amplifier forces the DC average of the FB voltage to equal the target voltage. This internal amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 4), allowing accurate DC output-voltage regulation regardless of the compensated feedback ripple voltage and internal slope-compensation variation. The integrator amplifier has the ability to shift the output voltage by $\pm 140\text{mV}$ (typ).

The MAX17007/MAX17008 disable the integrator by connecting the amplifier inputs together at the beginning of all dynamic REFIN1 transitions done in pulse-skipping mode. The integrator remains disabled until 20 μs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

Power-Good Outputs (PGOOD) and Fault Protection

PGOOD_ is the open-drain output that continuously monitors the respective output voltage for undervoltage and overvoltage conditions. The respective PGOOD_ is actively held low in shutdown ($\text{EN}_- = \text{GND}$) during soft-start and soft-shutdown. Approximately 200 μs after the soft-start terminates, PGOOD_ becomes high impedance as long as the respective output voltage is in regulation.

PGOOD1 goes low if the output voltage drops 200mV below the target voltage (REFIN1 or fixed 1.05V), or rises 300mV above the target voltage (REFIN1 or fixed 1.05V), or the SMPS1 controller is shut down.

In adjustable mode, PGOOD2 goes low if the feedback voltage drops 100mV below the target voltage (0.7V), or rises 150mV above the target voltage (0.7V), or the SMPS2 controller is shut down. In preset mode (fixed 1.5V), the PGOOD2 thresholds are -200mV and +300mV.

For a logic-level PGOOD output voltage, connect an external pullup resistor between PGOOD and V_{DD} . A 100k Ω pullup resistor works well in most applications. See Figure 13.

Overvoltage Protection (OVP, MAX17007 Only)

When the internal feedback voltage rises above the overvoltage threshold, the OVP comparator immediately pulls DH low and forces DL high, pulls PGOOD low, sets the fault latch, and disables the faulted SMPS controller. Toggle EN or cycle V_{CC} power below the V_{CC} POR to clear the fault latch and restart the controller.

The overvoltage thresholds are +300mV for SMPS1 (fixed 1.05V and adjustable REFIN1), +300mV for SMPS2 in preset mode (fixed 1.5V output), and +150mV for SMPS2 in adjustable mode (0.7V feedback).

An OV fault on one side does not affect the other side.

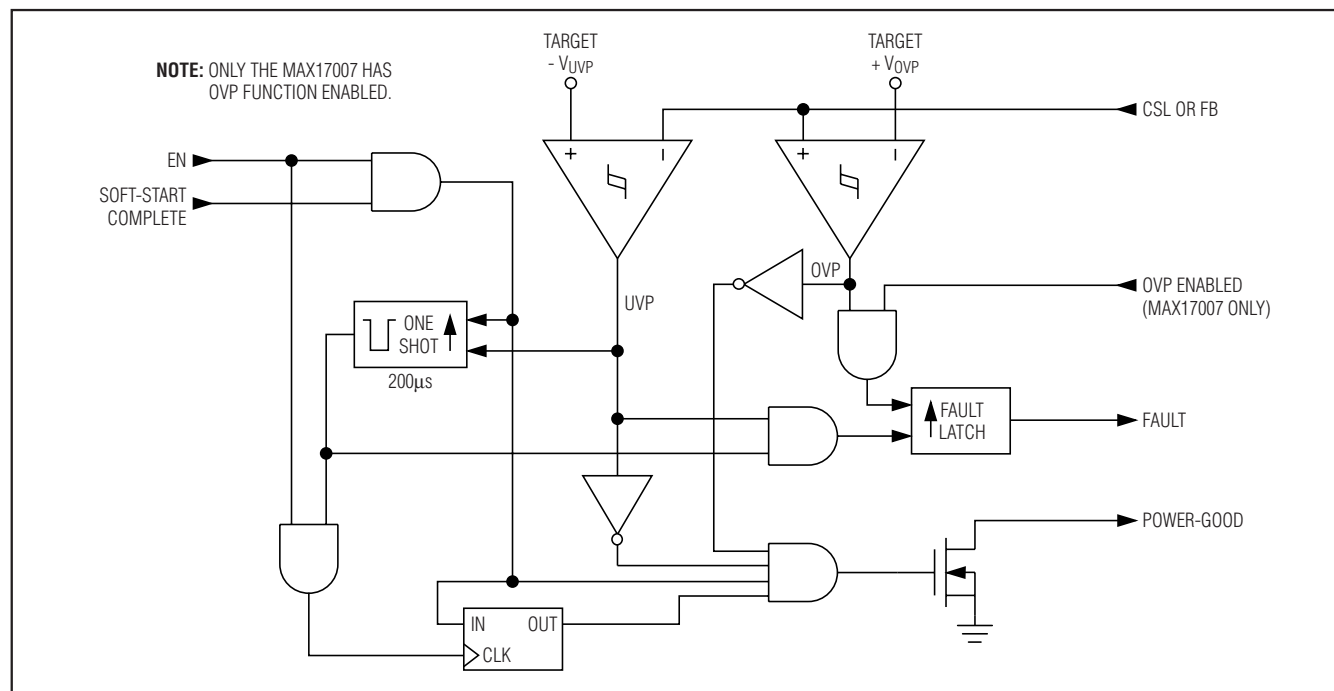


Figure 13. Power-Good and Fault Protection

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Undervoltage Protection (UVP)

When the feedback voltage drops below the undervoltage threshold, the controller immediately pulls PGOOD low and triggers a 200 μ s one-shot timer. If the feedback voltage remains below the undervoltage fault threshold for the entire 200 μ s, then the undervoltage fault latch of the faulted SMPS is set and that SMPS begins its shutdown sequence. When the internal target voltage drops below 0.1V, the MAX17007/MAX17008 force DL low for the faulted SMPS. Toggle EN or cycle VCC power below VCC POR to clear the fault latch and restart the controller.

The undervoltage thresholds are -200mV for SMPS1 (fixed 1.05V and adjustable REFIN1), -200mV for SMPS2 in preset mode (fixed 1.5V output), and -100mV for SMPS2 in adjustable mode (0.7V feedback).

A UV fault on one side does not affect the other side.

Thermal-Fault Protection (TSHDN)

The MAX17007/MAX17008 feature a thermal-fault protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD low, and shuts down the controller. Both DL and DH are pulled low. Toggle EN or cycle VCC power below VCC POR to reactivate the controller after the junction temperature cools by 15°C.

VCC POR and UVLO

Each SMPS of the MAX17007/MAX17008 is enabled when its respective EN is driven high. On the first rising EN, the reference powers up first. Once the reference exceeds its undervoltage lockout (UVLO) threshold (~ 60 μ s), the internal analog blocks are turned on and masked by a 140 μ s one-shot delay in order to allow the bias circuitry and analog blocks enough time to settle to their proper states. With the control circuitry reliably powered up, the PWM controller begins switching. The second rising EN, if controlled separately, also has the 140 μ s one-shot delay before its first DH pulse.

Power-on reset (POR) occurs when VCC rises above approximately 3V, resetting the fault latch and preparing the controller for operation. The VCC UVLO circuitry inhibits switching until VCC rises above 4.25V. The controller powers up the reference once the system enables the controller, VCC exceeds 4.25V, and either EN is driven high. With the reference in regulation, the controller ramps the output voltage to the target voltage with a 1.3mV/ μ s slew rate for SMPS1 and 0.65mV/ μ s for SMPS2.

If the VCC voltage drops below 4.25V, the controller assumes that there is not enough supply voltage to make valid decisions. To protect the output from overvoltage faults, the controller shuts down immediately and forces a high-impedance output (DL and DH pulled low).

Table 4. Fault Protection and Shutdown Operation

MODE	CONTROLLER STATE	DRIVER STATE
Shutdown (EN_ = High to Low) Output UVP (Latched) Thermal Fault (Latched)	Voltage soft-shutdown initiated. Error amplifier target slowly ramped down to GND.	DL_ low and DH_ low after soft-shutdown completed, internal 10 discharge on CSL_ activated.
Output OVP (Latched)	Controller shuts down and internal target slews down. Controller remains off until EN_ toggled or VCC power cycled.	DL_ immediately forced high, DH_ pulled low (high-side MOSFET disabled).
VCC UVLO Falling Edge	Controller shuts down and the internal target slews down. Controller remains off until VCC rises back above UVLO threshold.	DL_ low, DH_ low, internal 10 discharge on CSL_ activated.
VCC UVLO Rising Edge	SMPS controller enabled (assuming EN_ pulled high).	DL_, DH_ switching.
VCC POR	SMPS inactive.	DL_ low.

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Quick-PWM Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input voltage range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case input supply voltage allowed by the notebook's AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum load current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Most notebook loads generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.
- **Switching frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage due to MOSFET switching losses that are proportional to frequency and V_{IN}^2 . The optimum frequency is also a moving target due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor operating point:** This choice provides trade-offs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

Inductor Selection

The per-phase switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = \left(\frac{V_{IN} - V_{OUT}}{f_{SW} I_{LOAD(MAX)} LIR} \right) \left(\frac{V_{OUT}}{V_{IN}} \right)$$

For example: $I_{LOAD(MAX)} = 15A$, $V_{IN} = 12V$, $V_{OUT} = 1.5V$, $f_{SW} = 300kHz$, 30% ripple current or $LIR = 0.3$:

$$L = \left(\frac{12V - 1.5V}{300kHz \times 15A \times 0.3} \right) \left(\frac{1.5V}{12V} \right) = 0.97\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} \left(1 + \frac{LIR}{2} \right)$$

In combined mode, $I_{LOAD(MAX)}$ is the per-phase maximum current, which is half the actual maximum load current for the combined output.

Transient Response

The inductor ripple current impacts transient-response performance, especially at low $V_{IN} - V_{OUT}$ differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time. The worst-case output sag voltage can be determined by:

$$V_{SAG} = \frac{L (\Delta I_{LOAD(MAX)})^2 \left[\left(\frac{V_{OUT} T_{SW}}{V_{IN}} \right) + t_{OFF(MIN)} \right]}{2C_{OUT} V_{OUT} \left[\left(\frac{V_{IN} - V_{OUT}}{V_{IN}} \right) T_{SW} - t_{OFF(MIN)} \right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics* table).

The amount of overshoot due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{N_{PH} 2C_{OUT} V_{OUT}}$$

where N_{PH} is the number of active phases per output. N_{PH} is 1 for separate mode, and N_{PH} is 2 for combined-mode operation.

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Setting the Valley Current Limit

The minimum current-limit threshold must be high enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current; therefore:

$$I_{LIMIT(LOW)} > \frac{I_{LOAD(MAX)}}{N_{PH}} \left(1 - \frac{LIR}{2} \right)$$

where $I_{LIMIT(LOW)}$ equals the minimum current-limit threshold voltage divided by the output sense element (inductor DCR or sense resistor).

The four-level ILIM setting sets a valley current limit of 15mV, 30mV, 45mV, or 60mV across the CSH_ to CSL_ differential input.

Special attention must be made to the tolerance and thermal variation of the on-resistance in the case of DCR sensing. Use the worst-case maximum value for R_{DCR} from the inductor data sheet, and add some margin for the rise in R_{DCR} with temperature. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise, which must be included in the design margin unless the design includes an NTC thermistor in the DCR network to thermally compensate the current-limit threshold.

The current-sense method (Figure 14) and magnitude determine the achievable current-limit accuracy and power loss. The sense resistor can be determined by:

$$R_{SENSE_} = V_{LIM_}/I_{LIMIT_}$$

For the best current-sense accuracy and overcurrent protection, use a 1% tolerance current-sense resistor between the inductor and output as shown in Figure 14a. This configuration constantly monitors the inductor current, allowing accurate current-limit protection. However, the parasitic inductance of the current-sense resistor can cause current-limit inaccuracies, especially when using low-value inductors and current-sense resistors. This parasitic inductance (L_{ESL}) can be cancelled by adding an RC circuit across the sense resistor with an equivalent time constant:

$$C_{EQ}R_{EQ} = \frac{L_{ESL}}{R_{SENSE}}$$

Alternatively, low-cost applications that do not require highly accurate current-limit protection can reduce the overall power dissipation by connecting a series RC circuit across the inductor (Figure 14b) with an equivalent time constant:

$$R_{CS} = \frac{R_2}{R_1 + R_2} R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}} \times \left[\frac{1}{R_1} + \frac{1}{R_2} \right]$$

where R_{CS} is the required current-sense resistance and R_{DCR} is the inductor's series DC resistance. Use the worst-case inductance and R_{DCR} values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load.

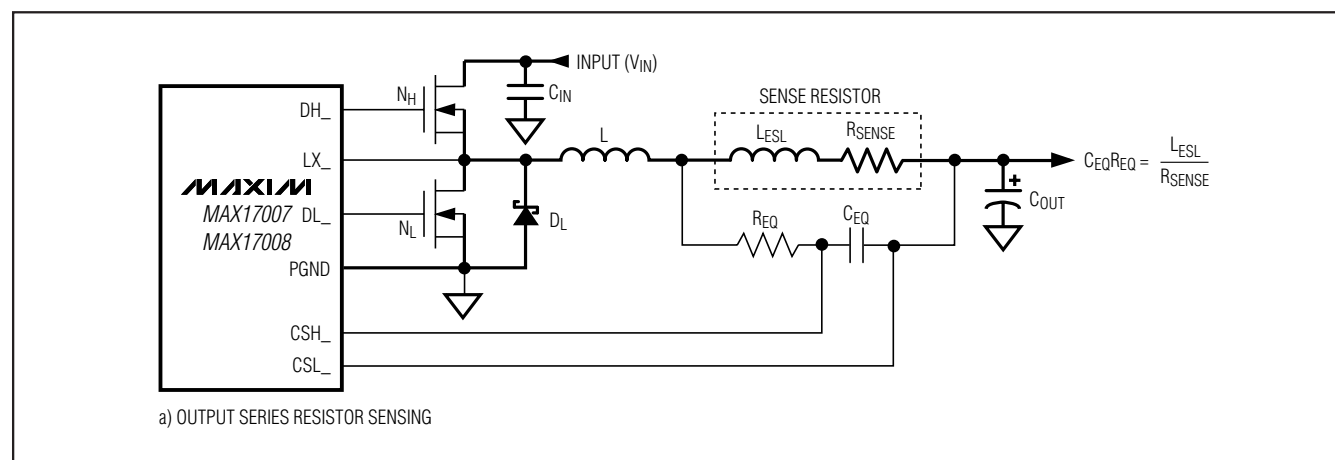


Figure 14. Current-Sense Configurations (Sheet 1 of 2)

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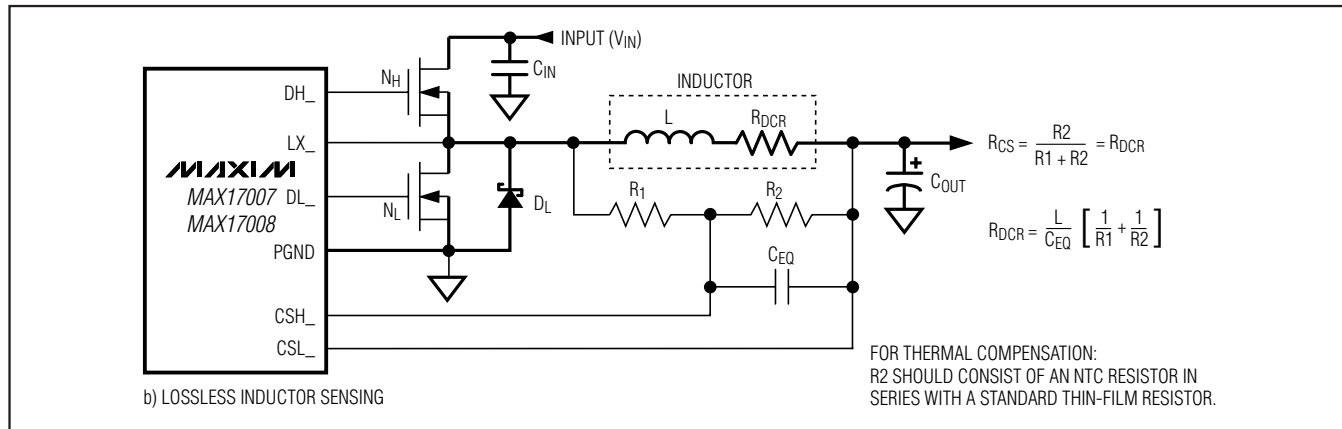


Figure 14. Current-Sense Configurations (Sheet 2 of 2)

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

In core and chipset converters and other applications where the output is subject to large-load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$(R_{ESR} + R_{PCB}) \leq \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In low-power applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. The maximum ESR to meet ripple requirements is:

$$R_{ESR} \leq \left[\frac{V_{IN} f_{SW} L}{(V_{IN} - V_{OUT}) V_{OUT}} \right] V_{RIPPLE}$$

where f_{SW} is the switching frequency.

With most chemistries (polymer, tantalum, aluminum, electrolytic), the actual capacitance value required relates to the physical size needed to achieve low ESR and the chemistry limits of the selected capacitor technology. Ceramic capacitors provide low ESR, but the capacitance and voltage rating (after derating) are determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the

rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). Thus, the output capacitor selection requires carefully balancing capacitor chemistry limitations (capacitance vs. ESR vs. voltage rating) and cost.

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the in-phase feedback ripple relative to the switching frequency, which is typically dominated by the output ESR. The boundary of instability is given by the following equation:

$$\frac{f_{SW}}{\pi} \geq \frac{1}{2\pi R_{EFF} C_{OUT}}$$

$$R_{EFF} \geq \frac{1}{2f_{SW} C_{OUT}}$$

$$R_{EFF} = R_{ESR} + A_{CS} R_{CS}$$

where C_{OUT} is the total output capacitance, R_{ESR} is the total ESR of the output capacitors, R_{CS} is the current-sense resistance, and A_{CS} is the current-sense gain as determined by the $ILIM$ setting. A_{CS} equals 2, 2.67, 4, and 8 for $ILIM$ settings of 5V, 3.3V, 2V, and GND, respectively.

For a 300kHz application, the effective zero frequency must be well below 95kHz, preferably below 50kHz. For the standard application circuit with ceramic output capacitors, the output ripple cannot be relied upon to be in phase with the inductor current due to the low ESR of the ceramic capacitors. Stability is mainly dependent on the current-sense gain. With $ILIM = 2V$, $A_{CS} = 4$, and an effective current-sense resistance of approximately 3.5mΩ, then the ESR zero works out to:

$$1/[2\pi \times (2 \times 330\mu F + 5 \times 10\mu F) \times 4 \times 3.5m\Omega] = 16kHz$$

This is well within the stability requirements.

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When only using ceramic output capacitors, output overshoot (V_{SOAR}) typically determines the minimum output capacitance requirement. Their relatively low capacitance value can allow significant output overshoot when stepping from full-load to no-load conditions, unless designed with a small inductance value and high switching frequency to minimize the energy transferred from the inductor to the capacitor during load-step recovery.

Unstable operation manifests itself in two related but distinctly different ways: double pulsing and feedback loop instability. Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The I_{RMS} requirements can be determined by the following equation for a single-phase application:

$$I_{RMS} = \frac{\sqrt{I_{LOAD1}^2 V_{OUT1} (V_{IN} - V_{OUT1}) + I_{LOAD2}^2 V_{OUT2} (V_{IN} - V_{OUT2})}}{V_{IN}}$$

In combined mode, the input RMS current simplifies to:

$$I_{RMS} = \left(\frac{I_{LOAD}}{2V_{IN}} \right) \sqrt{2V_{OUT} (V_{IN} - V_{OUT})}$$

where I_{LOAD} is the combined output current of both phases.

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the

input. If the Quick-PWM controller is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both of these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of N_H (reducing $R_{DS(ON)}$ but with higher C_{GATE}). Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of N_H (increasing $R_{DS(ON)}$ to lower C_{GATE}). If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin SOs, DPAK, or D²PAK), and is reasonably priced. Make sure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems might occur (see the *MOSFET Gate Drivers (DH, DL)* section).

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD(N_H \text{ Resistive}) = \left(\frac{V_{OUT}}{V_{IN(MIN)}} \right) (I_{LOAD})^2 R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power dissipation often limits how small the MOSFET can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

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Calculating the power dissipation in high-side MOSFET (N_H) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H :

$$PD(N_H \text{ Switching}) = V_{IN(MAX)} I_{LOAD} f_{SW} \left(\frac{Q_{G(SW)}}{I_{GATE}} \right) + \frac{C_{OSS} V_{IN(MAX)}^2 f_{SW}}{2}$$

where C_{OSS} is the N_H MOSFET's output capacitance, $Q_{G(SW)}$ is the charge needed to turn on the N_H MOSFET, and I_{GATE} is the peak gate-drive source/sink current (2.4A typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied due to the squared term in the $C \times V_{IN}^2 \times f_{SW}$ switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum input voltage:

$$PD(N_L \text{ Resistive}) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}} \right) \right] (I_{LOAD})^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$, but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, you can "over design" the circuit to tolerate:

$$I_{LOAD} = \left(I_{VALLEY(MAX)} + \frac{\Delta I_{INDUCTOR}}{2} \right) \\ = I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)} L_{IR}}{2} \right)$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good size heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time. Select a diode that can handle the load current during the dead times. This diode is optional and can be removed if efficiency is not critical.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate-charging requirements of the high-side MOSFETs. Typically, 0.1 μ F ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1 μ F. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and Q_{GATE} is the gate charge specified in the MOSFET's data sheet. For example, assume (2) IRF7811W n-channel MOSFETs are used on the high side. According to the manufacturer's data sheet, a single IRF7811W has a maximum gate charge of 24nC ($V_{GS} = 5V$). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{2 \times 24nC}{200mV} = 0.24\mu F$$

Selecting the closest standard value, this example requires a 0.22 μ F ceramic capacitor.

Applications Information

Minimum Input Voltage Requirements and Dropout Performance

The output-voltage adjustable range for continuous-conduction operation is restricted by the nonadjustable minimum off-time one-shot. For best dropout performance, use the slower (200kHz) on-time settings. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the on-times. This error is greater at higher frequencies. Also, keep in mind that transient response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the *Transient Response* section (the V_{SAG} equation) in the *Quick-PWM Design Procedure* section).

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In a single-phase configuration, the absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{\text{UP}} / \Delta I_{\text{DOWN}}$ is an indicator of the ability to slew the inductor current higher in response to increased load and must always be greater than 1. As h approaches 1—the absolute minimum dropout point—the inductor current cannot increase as much during each switching cycle, and V_{SAG} greatly increases unless additional output capacitance is used. A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between V_{SAG} , output capacitance, and minimum operating voltage. For a given value of h , the minimum operating voltage can be calculated as:

$$V_{\text{IN(MIN)}} = \left(\frac{V_{\text{OUT}} - V_{\text{CHG}}}{1 - (h \times t_{\text{OFF(MIN)}} f_{\text{SW}})} \right)$$

where V_{CHG} is the parasitic voltage drop in the charge path (see the *On-Time One-Shot* section), and $t_{\text{OFF(MIN)}}$ is from the *Electrical Characteristics* table. The absolute minimum input voltage is calculated with $h = 1$.

If the calculated $V_{\text{IN(MIN)}}$ is greater than the required minimum input voltage, then reduce the operating frequency or add output capacitance to obtain an acceptable V_{SAG} . If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout Design Example:

$V_{\text{OUT}} = 1.5\text{V}$

$f_{\text{SW}} = 300\text{kHz}$

$t_{\text{OFF(MIN)}} = 250\text{ns}$

$V_{\text{CHG}} = 150\text{mV}$ (10A load)

$h = 1.5$

$$V_{\text{IN(MIN)}} = \left[\frac{1.5\text{V} + 150\text{mV}}{1 - (0.25\mu\text{s} \times 1.5 \times 300\text{kHz})} \right] = 1.86\text{V}$$

Calculating again with $h = 1$ gives the absolute limit of dropout:

$$V_{\text{IN(MIN)}} = \left[\frac{1.5\text{V} + 150\text{mV}}{1 - (0.25\mu\text{s} \times 1.0 \times 300\text{kHz})} \right] = 1.78\text{V}$$

Therefore, V_{IN} must be greater than 1.78V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 2.0V.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
- Connect all analog grounds to a separate solid copper plane, which connects to the GND pin of the Quick-PWM controller. This includes the V_{CC} bypass capacitor, REF bypass capacitors, REFIN1 components, and feedback compensation/dividers.
- Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single $\text{m}\Omega$ of excess trace resistance causes a measurable efficiency penalty.
- Keep the high current, gate-driver traces (DL, DH, LX, and BST) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes away from sensitive analog areas (REF, REFIN1, FB2, CSH, and CSL).

Layout Procedure

- 1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN} , C_{OUT} , and anode of the low-side Schottky). If possible, make all these connections on the top layer with wide, copper-filled areas.
- 2) Mount the controller IC adjacent to the low-side MOSFET. The DL gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC).

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- 3) Group the gate-drive components (BST capacitors, V_{DD} bypass capacitor) together near the controller IC.
- 4) Make the DC-DC controller ground connections as shown in Figures 1 and 2. This diagram can be viewed as having four separate ground planes: I/O ground, where all the high-power components go; the power ground plane, where the PGND pin and V_{DD} bypass capacitor go; the master's analog ground plane where sensitive analog components, the master's GND pin, and V_{CC} bypass capacitor go; and the slave's analog ground plane where the slave's GND pin and V_{CC} bypass capacitor go. The master's GND plane must meet the PGND plane only at a single point directly beneath the IC. Similarly, the slave's GND plane must meet the PGND plane only at a single point directly beneath

the IC. The respective master and slave ground planes should connect to the high-power output ground with a short metal trace from PGND to the source of the low-side MOSFET (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.

- 5) Connect the output power planes (V_{OUT} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical. See Figure 15.

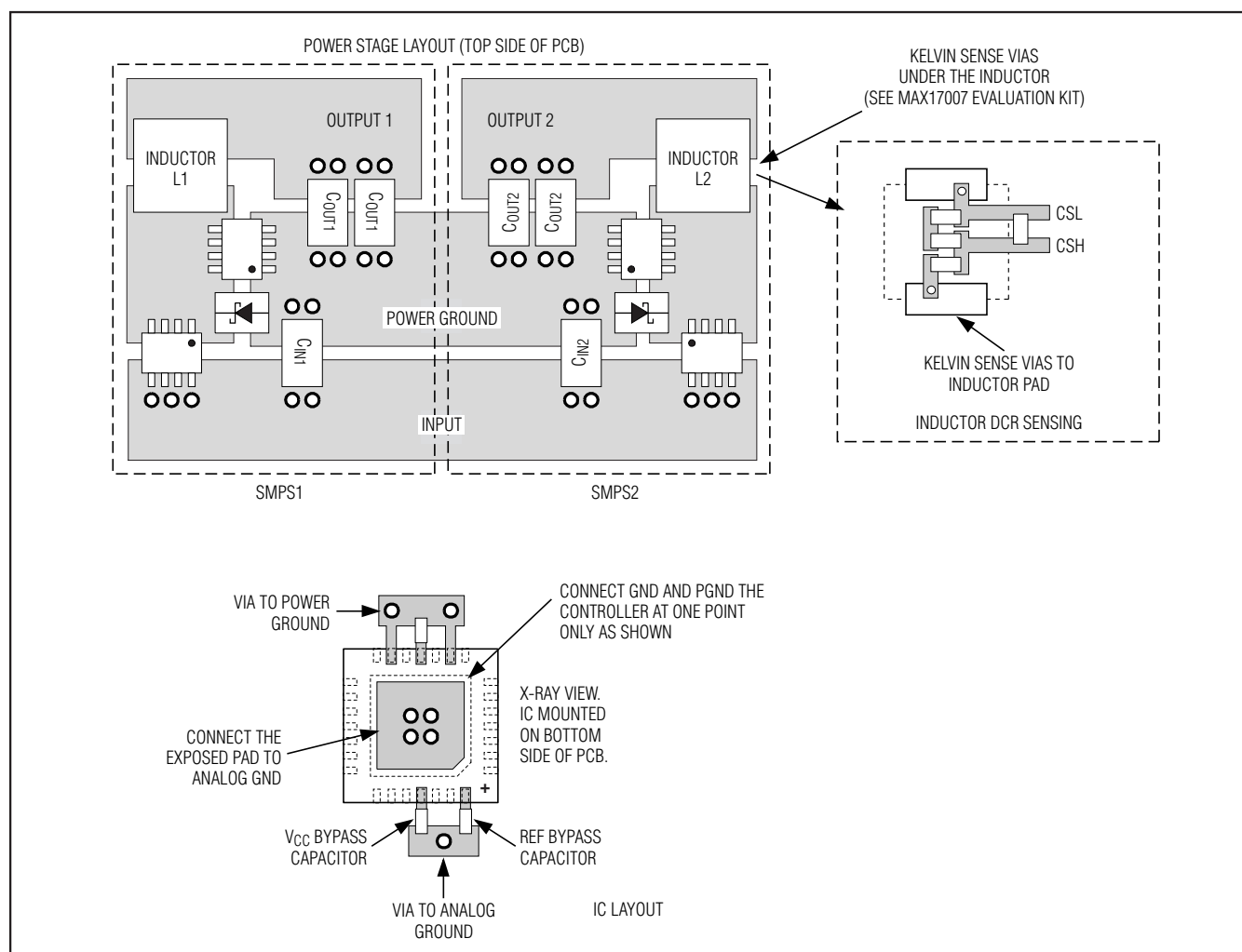


Figure 15. PCB Layout Example

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Chip Information

TRANSISTOR COUNT: 13,103

PROCESS: BiCMOS

Package Information

For the latest package outline information, go to
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PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TQFN	T2844-1	21-0139

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