Click here for production status of specific part numbers.

MAX38888

2.5V–5.0V, 0.5A/2.5A Reversible Buck/Boost Regulator for Backup Power Applications

General Description

The MAX38888 is a storage capacitor or capacitor bank backup regulator designed to efficiently transfer power between a storage element and a system supply rail in reversible buck and boost operations using the same inductor.

When the main supply is present and above the minimum system supply voltage, the regulator operates in buck mode and charges the storage element at up to 500mA peak inductor current. Once the storage element is charged, the circuit draws only 2.5µA of current while it maintains the super capacitor or other storage element in its ready state. When the main supply is removed, the regulator operates in boost mode and prevents the system from dropping below the minimum operating voltage, discharging the storage element at up to 2.5A peak inductor current.

The MAX38888 is externally programmable for minimum and maximum voltage of the storage element, such as super capacitor, minimum system voltage, and maximum charge and discharge currents. The internal DC/DC converter requires only a 1µH inductor.

Applications

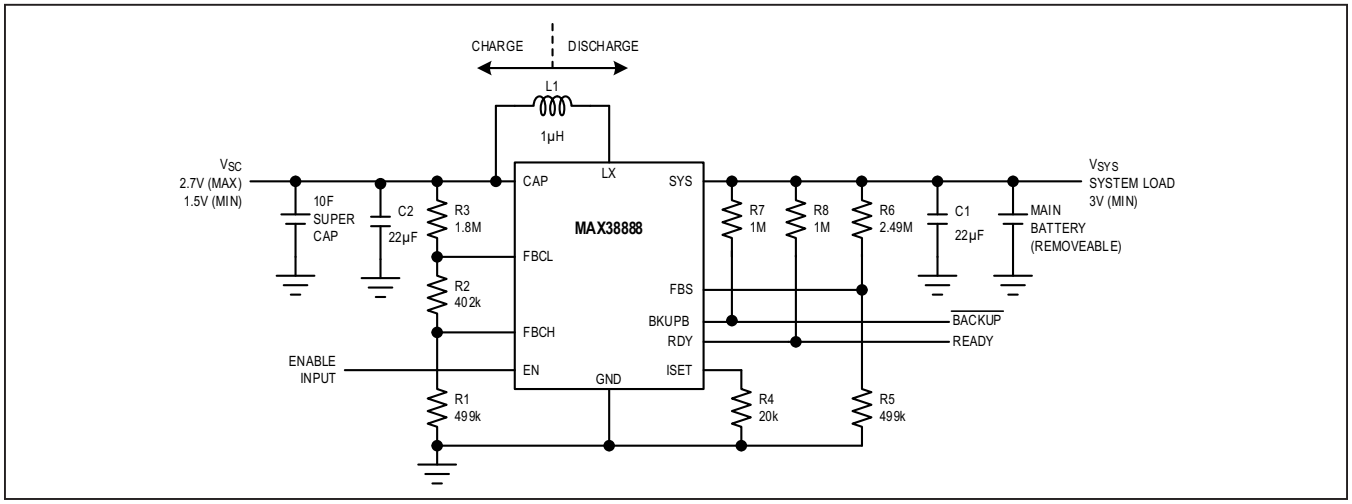
- Handheld Industrial Equipment
- Portable Computers
- Portable Devices with a Removable Battery

Benefits and Features

- 2.5V to 5V System Output Voltage
- 0.8V to 4.5V Cap Voltage Range
- Up to 2.5A Peak Inductor Discharge Current
- Programmable Voltage and Current Thresholds
- ±2% Threshold Accuracy
- Up to 95% Efficiency, Charge or Discharge
- 2.5µA Ready Quiescent Current
- Small Solution Size
- 3mm x 3mm x 0.75mm TDFN Package

Ordering Information *appears at end of data sheet.*

Typical Application Circuit



maxim integrated™

Absolute Maximum Ratings

CAP, EN, SYS, LX, BKUPB, RDY to GND.....-0.3V to +6V
FBCH, FBCL to GND .....-0.3V to CAP + 0.3V
FBS, ISET to GND .....-0.3V to SYS + 0.3V
PGND to GND.....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C, TDFN, derate 24.4mW/°C above +70°C).....1951.2mW
Operating Temperature Range..... -40°C to +125°C
Storage Temperature Range..... -65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 10 seconds).....+300°C
LX RMS Current.....±2.0A_{RMS}
Output Short-Circuit Duration.....Continuous

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TDFN

Package Code	T1433+2C
Outline Number	**21-0137**
Land Pattern Number	**90-0063**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SYS} = 3.7V, V_{CAP} = 2.7V, T_J = -40°C to +125°C (typical values at T_J = 25°C), circuit of Figure 1, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYS Voltage Range	V_{VSYS}		2.5		5	V
CAP Voltage Range	V_{VSC}		0.8		4.5	V
SYS Shutdown Current	I_{SYS_SD}	EN = 0V, T_A = 25°C		0.01	1	µA
		EN = 0V		0.1		
SYS Charging Supply Current	I_{SYS_CHG}	V_{FBS} = 0.6V, V_{FBCH} = V_{FBCL} = 0.485V		1.5		mA
SYS Backup Supply Current	I_{SYS_BUP}	V_{FBS} = V_{FBCH} = V_{FBCL} = 0.515V, T_A = 25°C		35	65	µA
		V_{FBS} = V_{FBCH} = V_{FBCL} = 0.515V		35		
SYS Ready Supply Current	I_{SYS_RDY}	V_{FBS} = 0.6V, V_{FBCH} = V_{FBCL} = 0.515V, T_A = 25°C		2.5	5	µA
		V_{FBS} = 0.6V, V_{FBCH} = V_{FBCL} = 0.515V		2.5		
CAP Shutdown Current	I_{CAP_SD}	EN = 0V, T_A = 25°C		0.01	1	µA
		EN = 0V		0.1		
UVLO Threshold	V_{UVLOF}	V_{VSYS} falling, 100mV typical hysteresis	1.7	1.8	1.9	V
FBS Backup Voltage	V_{FBS}	FBS rising, when discharging stops	-2%	0.5	+2%	V
FBS Charging Threshold	$V_{TH\_FBS\_CHG}$	Above FBS Backup Voltage, when charging begins, 30mV typical hysteresis	25	60	95	mV
FBCH Threshold	V_{TH_FBCH}	FBCH rising, when charging stops, 25mV typical hysteresis	-2%	0.5	+2%	V
FBCL Threshold	V_{TH_FBCL}	FBCL falling, when preserve mode starts, 25mV typical hysteresis	-3.5%	0.475	+3.5%	V
EN Threshold	V_{IL}	When LX stops switching, EN falling	225	600		mV
	V_{IH}	EN rising		660	925	
ISET Resistor Range	R_{ISET}	Guaranteed by LX Peak Current Limits	20		100	kΩ
LX Peak Backup Current Limit (Note 1)	I_{DCHG}	Circuit of Figure 1, V_{CAP} = 2V, V_{SYS} = 2.9V, R_{ISET} = 20kΩ	2.0	2.5	3.0	A
		Circuit of Figure 1, V_{CAP} = 2V, V_{SYS} = 2.9V, R_{ISET} = 100kΩ		0.50		
LX Peak Charge Current Limit (Note 1)	ICHG	Circuit of Figure 1, V_{SYS} = 3.7V, V_{CAP} = 2V, R_{ISET} = 20kΩ	400	500	600	mA
		Circuit of Figure 1, V_{SYS} = 3.7V, V_{CAP} = 2V, R_{ISET} = 100kΩ		100		
FBS/FBCH/FBCL Input Bias Current	$I_{FBS/FBCH/FBCL}$	$V_{FBS/FBCH/FBCL}$ = 0.5V, T_A = 25°C	-0.1	0.001	0.1	µA
		$V_{FBS/FBCH/FBCL}$ = 0.5V		0.01		

Electrical Characteristics (continued)

(V_{SYS} = 3.7V, V_{CAP} = 2.7V, T_J = -40°C to +125°C (typical values at T_J = 25°C), circuit of Figure 1, unless otherwise specified.)

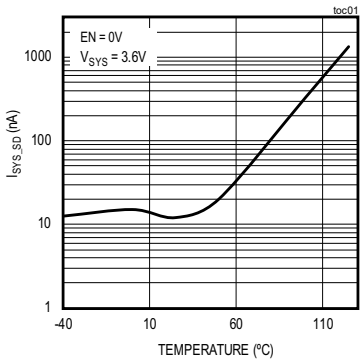
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN Input Leakage Current	I_{EN}	0V < V_{EN} < 5.5V, T_A = 25°C	-0.1	0.001	0.1	µA
		0V < V_{EN} < 5.5V		0.01		
LX Switching Frequency	f_{SW}	Delivering maximum current from CAP		2		MHz
LX Low-Side FET Resistance	R_{LOW}	V_{SYS} = 3V, LX switched to GND		50	100	mΩ
LX High-Side FET Resistance	R_{HIGH}	V_{SYS} = 3V, LX switched to SYS		80	160	mΩ
LX Leakage Current	I_{LX_LKG}	V_{EN} = 0V, V_{SYS} = 5V, V_{LX} = 0V/5V, T_A = 25°C	-1		1	µA
		V_{EN} = 0V, V_{SYS} = 5V, V_{LX} = 0V/5V		0.1		
Maximum On-Time	t_{ON}	Backup Mode, V_{FBS} = 0.485V	320	400	480	ns
Minimum Off-Time	t_{OFF}	Backup Mode, V_{FBS} = 0.485V	80	100	120	ns
Overtemperature Lockout Threshold	T_{OTLO}	T_J rising, 15°C typical hysteresis		165		°C
High-Side FET Zero-Crossing (Note 1)	I_{ZXP}	Circuit of Figure 1, V_{CAP} = 2V, V_{SYS} = 2.9V	25	50	75	mA
Low-Side FET Zero-Crossing (Note 1)	I_{ZXN}	Circuit of Figure 1, V_{SYS} = 3.7V, V_{CAP} = 2V	25	50	75	mA
BKUPB Leakage Current	I_{BKUPB}	V_{EN} = 0V, V_{BKUPB} = 5V, T_A = 25°C	-1		1	µA
		V_{EN} = 0V, V_{BKUPB} = 5V		0.1		
BKUPB Output Voltage Low	V_{BKUPB_L}	V_{FBS} = 0.48V, V_{FBCH} = V_{FBCL} = 0.515V, I_{SINK} = 2mA			0.4	V
RDY Leakage Current	I_{RDY}	V_{FBCH} = 0.54V, V_{RDY} = 5V, T_A = 25°C	-1		1	µA
		V_{FBCH} = 0.54V, V_{RDY} = 5V		0.1		
RDY Output Voltage Low	V_{RDY_L}	V_{EN} = 0V, I_{SINK} = 2mA			0.4	V

Note 1: DC measurement, actual zero-crossing and peak current accuracy in circuit will be affected by the propagation delay time.

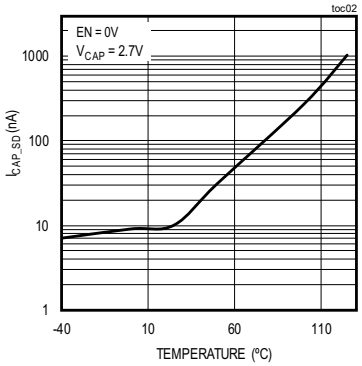
Typical Operating Characteristics

(MAX38888, V_{SYS} = 3.6V, V_{CAP} = 2.0V, C1 = 22µF, C2 = 22µF, T_A = +25°C, unless otherwise noted.)

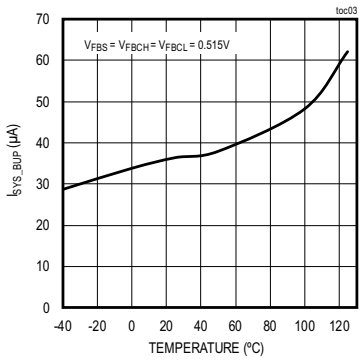
SYS PIN SHUTDOWN CURRENT



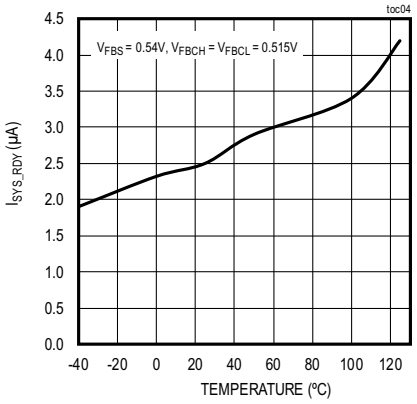
CAP PIN SHUTDOWN CURRENT



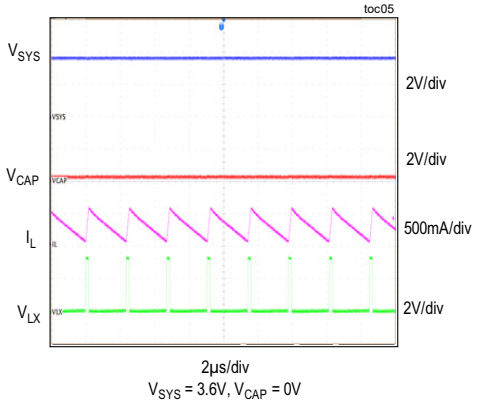
SYS BACKUP SUPPLY CURRENT



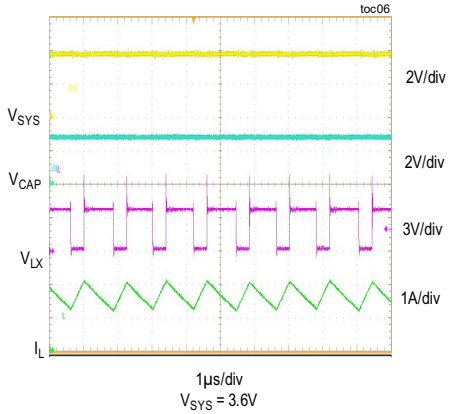
SYS READY SUPPLY CURRENT



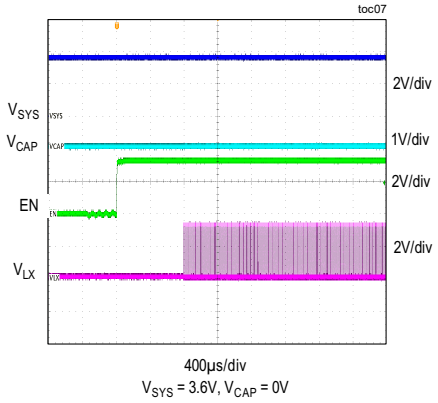
SWITCHING WAVEFORM WHILE CHARGING



SWITCHING WAVEFORM HEAVY LOAD



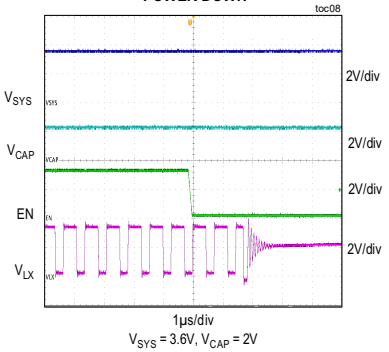
POWER-UP



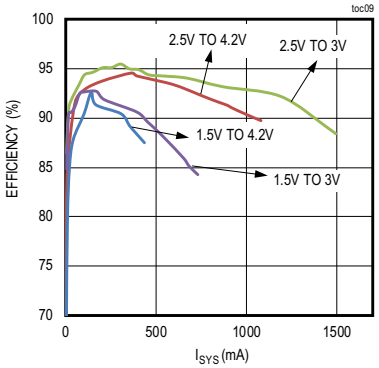
Typical Operating Characteristics (continued)

(MAX38888, V_{SYS} = 3.6V, V_{CAP} = 2.0V, C1 = 22µF, C2 = 22µF, T_A = +25°C, unless otherwise noted.)

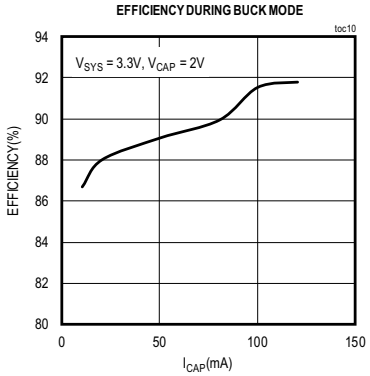
POWER-DOWN



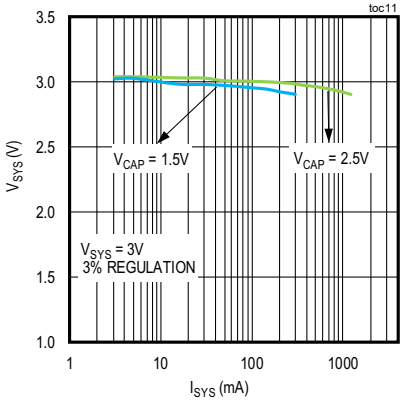
EFFICIENCY DURING BOOST MODE



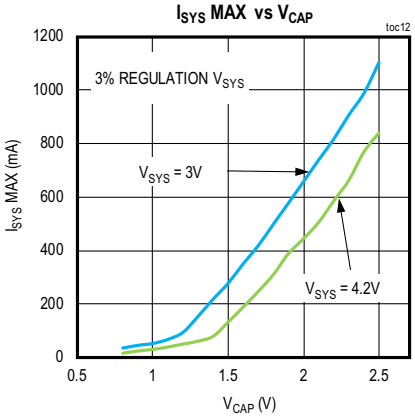
EFFICIENCY DURING BUCK MODE



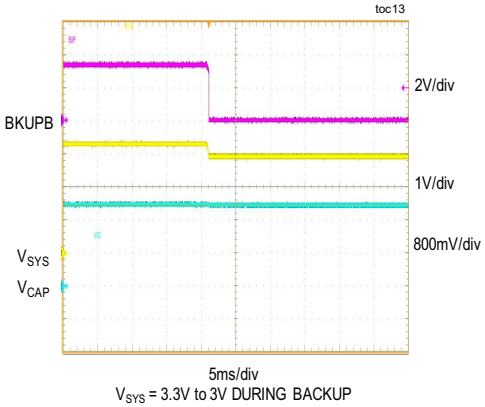
LOAD REGULATION DURING BOOST



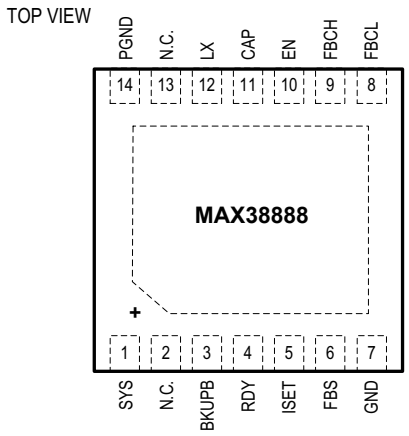
ISYS MAX vs VCAP



VSYS TRANSITION DURING BACKUP



Pin Configuration

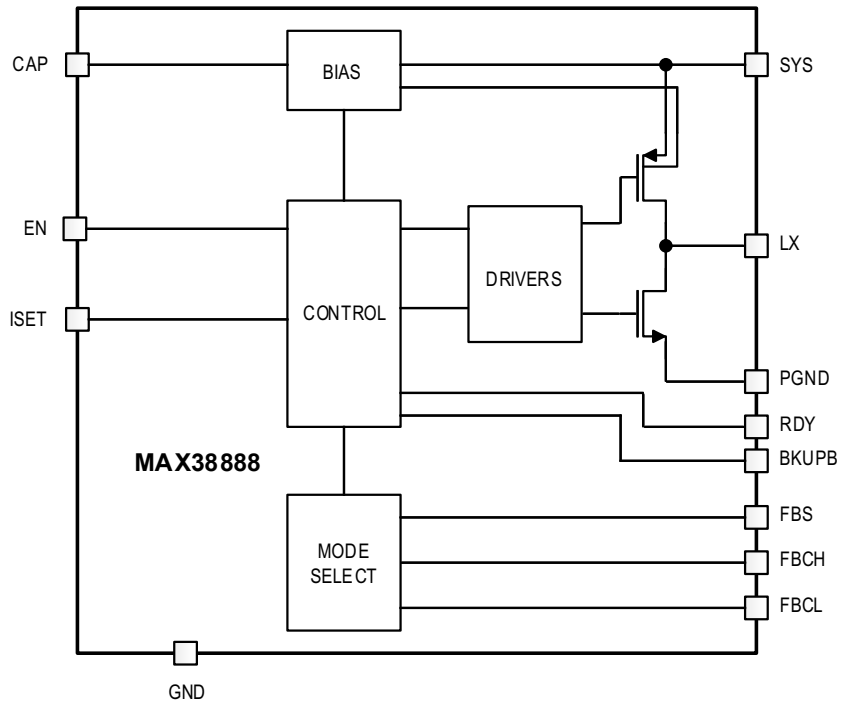


TDFN
(3mm x 3mm)

Pin Description

PIN	NAME	FUNCTION
1	SYS	System Supply Rail. Connect to a system supply rail or removable battery between 2.5V and 5V and bypass with a 22µF capacitor to GND.
2	NC	No Connect.
3	BKUPB	Open-Drain Backup Indicator. BKUPB is held low when the part is in backup mode i.e. when FBS < 0.5V and FBCL > 0.5V. BKUPB is released High when FBCL < 0.475V or FBS > 0.56V. Connect to external pullup resistor.
4	RDY	Open-Drain Supercap Ready Indicator. RDY goes high when the supercap is fully charged (i.e., FBCH > 0.5V). RDY is pulled low when FBCL < 0.475V. Connect to an external pullup resistor.
5	ISET	Charge/Discharge Current Input. The peak discharge current is set by $50kV/R_{ISET}$ while the peak charging current is 1/5 the discharging current.
6	FBS	SYS Feedback. Connect to the center point of a resistor divider from SYS to GND. SYS will boost to 0.5V x $(1 + R_{STop}/R_{SBot})$ when V_{FBS} < 0.5V.
7	GND	Analog Ground.
8	FBCL	CAP Feedback. Connect to the upper point of a resistor divider from CAP to GND. Part enters preserve mode when V_{FBCL} < 0.475V.
9	FBCH	CAP Feedback. Connect to the lower point of a resistor divider from CAP to GND. CAP will charge to 0.5V x $(1 + R_{CTop}/R_{CBot})$ when V_{FBS} > 0.56V.
10	EN	Enable Input. Force this pin high to enable the regulator or force pin low to disable the part and enter shutdown. If not driven, tie it to the SYS rail.
11	CAP	Super Cap. Connect to a super cap rated between 0.8V to 5V with a maximum voltage less than V_{SYS}.
12	LX	Inductor Switching Node. Connect a 1.0µH to 4.7uH inductor from LX to CAP.
13	NC	No Connect.
14, EP	PGND	Power Ground.

Functional Diagrams



Detailed Description

The MAX38888 is a flexible storage capacitor or capacitor bank backup regulator efficiently transferring power between a storage element and a system supply rail.

When the main supply is present and its voltage above the minimum system supply voltage, the regulator operates in the charging mode of operation and charges the storage element at up to 500mA peak inductor current. Once the storage element is charged, the RDY flag will assert and the circuit will draw only 2.5µA of current while maintaining the storage element in its ready state.

When the main supply is removed, the regulator prevents the system from dropping below the minimum operating voltage, boosting V_{SYS} by discharging the storage element at up to 2.5A peak inductor current. During this backup mode of operation, the MAX38888 utilizes a fixed on-time, current-limited, pulse-frequency-modulation (PFM) control scheme. Once MAX38888 is in the backup mode, the BKUPB flag is asserted.

The external pins allow a wide range of system and storage element, such as super capacitor voltage settings, as well as charging and discharging peak inductor current settings.

The MAX38888 implements a true shutdown feature disconnecting V_{SYS} from V_{CAP} as well as protecting against a SYS short or if $V_{CAP} > V_{SYS}$.

Application Circuit

The typical application of the MAX38888 is shown in Figure 1.

Super Capacitor Voltage Configuration

The maximum super capacitor voltage is set using a resistor divider from CAP to FBCH to GND. Recommended value for R1 is 499kΩ. Because resistor tolerance will have direct effect on voltage accuracy, these resistors should have 1% accuracy or better.

$$R2 + R3 = R1 \times ((V_{CAP\ MAX}/0.5) - 1)$$

V_{CAP} halts charging when V_{FBCH} reaches 0.5V. The maximum super capacitor voltage is where the super capacitor will remain after it is completely charged and ready for backup.

The minimum super capacitor discharge voltage is set using a resistor divider from CAP to FBCL to GND.

$$R3 = (R1 + R2) \times ((V_{CAP\ MIN}/0.5) - 1)$$

FBCL prevents the super capacitor from further discharge when V_{FBCL} reaches 0.475V during a backup event in order to preserve the remaining capacity for keeping alive a real-time clock, memory, or other low-level function. In this preserve mode, the IC disconnects all circuitry from the super capacitor and draws 2.5µA current from it.

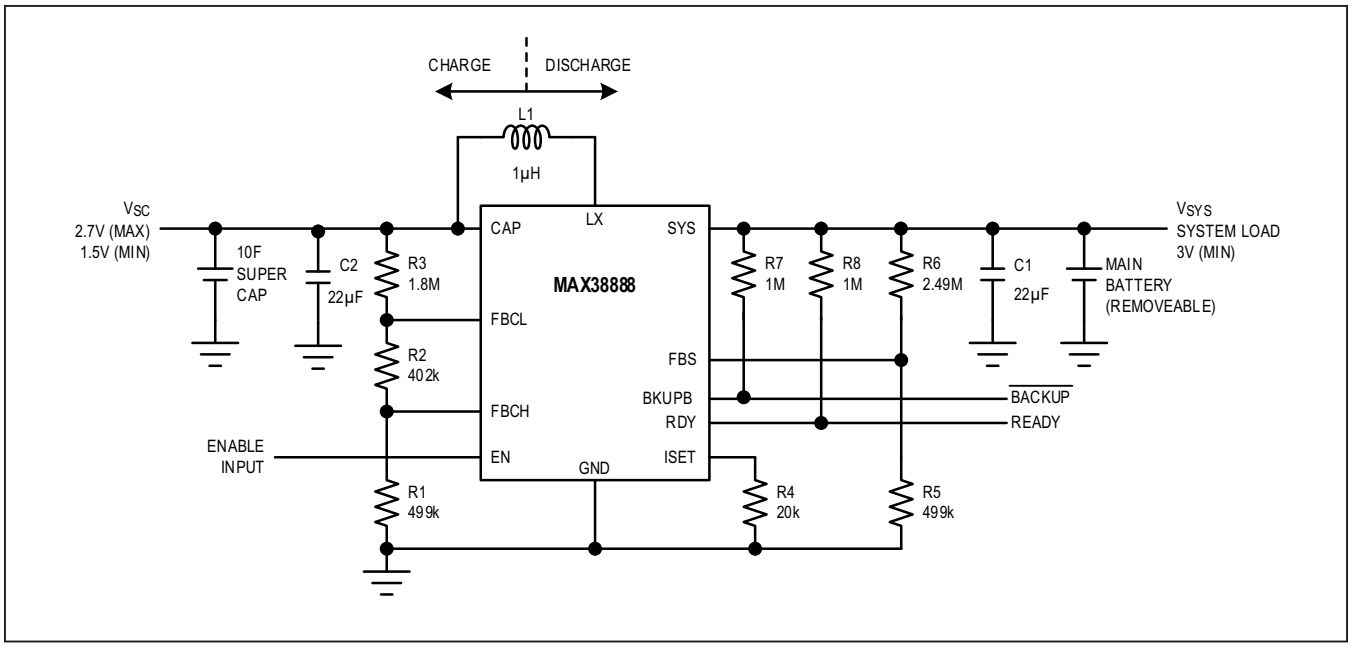


Figure 1. Typical Application

In applications where SYS voltage needs to be boosted to higher levels, selecting V_{CAP} min has to take into account duty cycle limitation of the boosting phase which is 80%.

MAX38888 detects when V_{SYS} falls below V_{CAP}. The device will not enable if V_{SYS} is below V_{CAP}. Raising V_{SYS} above the backup threshold re-initiates charging and backup.

System Voltage Configuration

The minimum system voltage is set using a resistor divider from SYS to FBS to GND. Recommended value for R5 is 499kΩ. Because resistor tolerance will have direct effect on voltage accuracy, these resistors should have 1% accuracy or better.

$$R6 = R5 \times ((V_{SYS\ MIN}/0.5) - 1)$$

When V_{FBS} is above 0.56V, the DC/DC regulator will draw power from the SYS pin to charge the super capacitor to the maximum voltage set by FBCH and be ready for backup. When the main battery is removed, V_{FBS} drops to 0.5V and the SYS pin is regulated to the programmed minimum voltage with up to 2A of CAP current.

Charge/Discharge Current Configuration

The peak inductor discharge current is set by placing a resistor from ISET to GND. The values of R_{ISET} resistor is calculated by following formula:

$$I_{DISCHARGE} = 2.5A \times (20k\Omega/R_{ISET})$$

The super capacitor charging current is internally set to 1/5 of the discharge current.

$$I_{CHARGE} = 0.5A \times (20k\Omega/R_{ISET})$$

Value of R_{ISET} between 20kΩ and 100kΩ is recommended to ensure accurate current compliance.

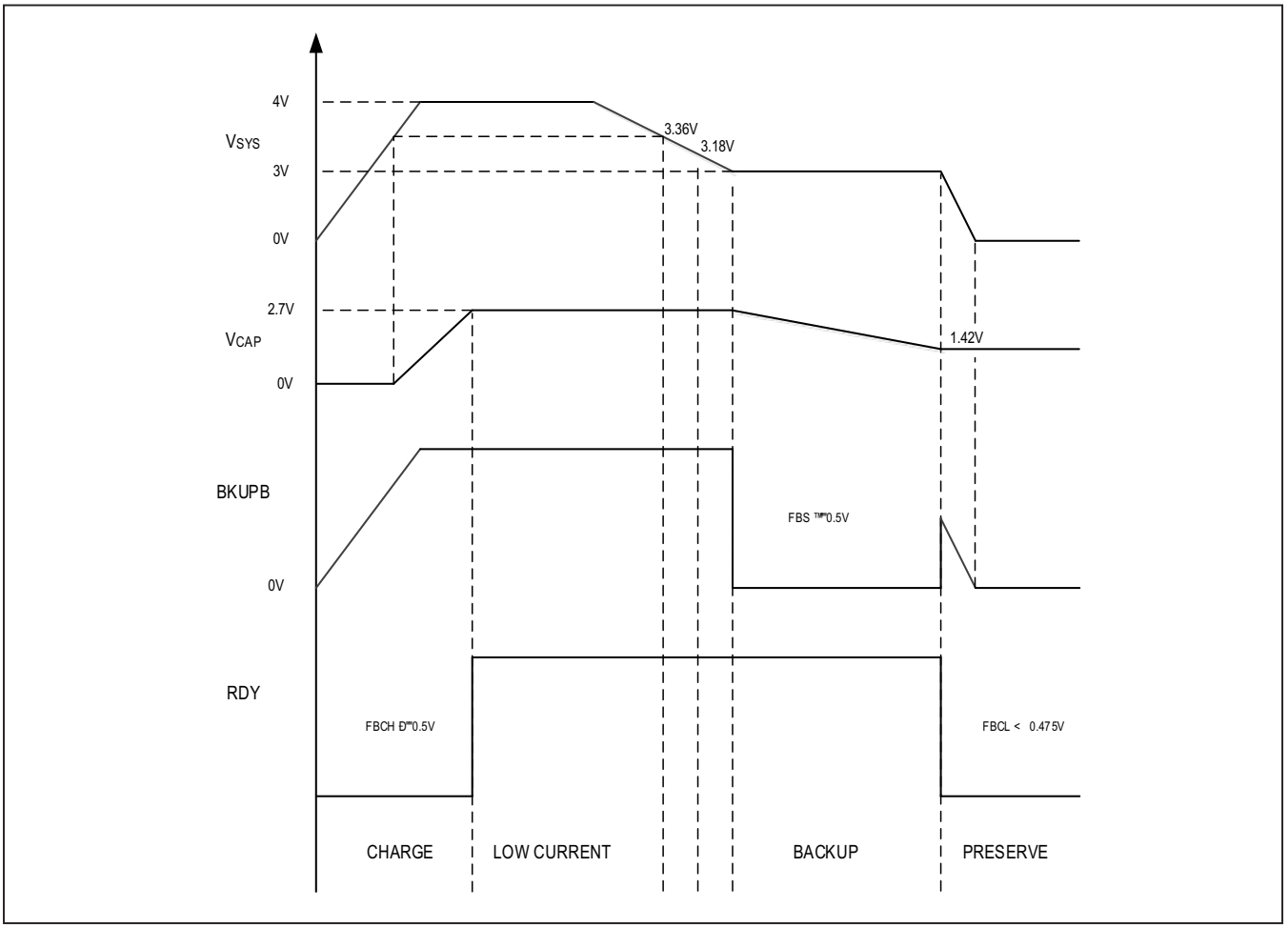


Figure 2. System Waveforms

System Waveforms

The waveforms in Figure 2 represent system behavior of MAX38888 in the *Typical Application Circuits*.

Applications Information

Capacitor Selection

Capacitors at SYS and CAP pins reduce current peaks and increase efficiency. Ceramic capacitors are recommended because they have the lowest equivalent series resistance (ESR), smallest size, and lowest cost. Choose an acceptable dielectric such as X5R or X7R. Due to ceramic capacitors' capacitance derating with DC bias standard 22µF ceramic capacitors are recommended at both pins for most applications.

Super Capacitor Selection

When the power source supplying the V_{SYS} voltage is removed, power to the output is provided by MAX38888 operating in the back-up or boost mode of operation using the super capacitor as its source. In order to ensure the supply voltage stays in regulation, the amount of power the super capacitor can deliver at its minimal voltage should be greater than that required by the system. MAX38888 will present a constant power load to the super capacitor where smaller current will be pulled out of the super capacitor near its maximum V_{CAP} voltage. However, current drawn from the super capacitor will increase as it discharges to maintain constant power at the load. The amount of energy required in the backup mode will be the product of the constant back up power and time defined as backup time, t_{BACKUP}.

The amount of energy available in the super capacitor is calculated using the following formula:

$$E = 1/2 \times C_{SCAP} \times (V_{CAPMAX}^2 - V_{CAPMIN}^2) \quad (J)$$

The amount of energy required to complete the backup equals to:

$$E = V_{SYS} \times I_{SYS} \times t_{BACKUP}) \quad (J)$$

where, I_{SYS} will be the system load during backup.

Since energy required at the system side during the backup event comes from available energy in the super capacitor, and assuming conversion efficiency η, and given t_{BACKUP}, the required C_{SCAP} will be determined by the following equation:

$$C_{SCAP} = (2 \times V_{SYS} \times I_{SYS} \times t_{BACKUP})/[(V_{CAPMAX}^2 - V_{CAPMIN}^2) \times \eta] \quad (F)$$

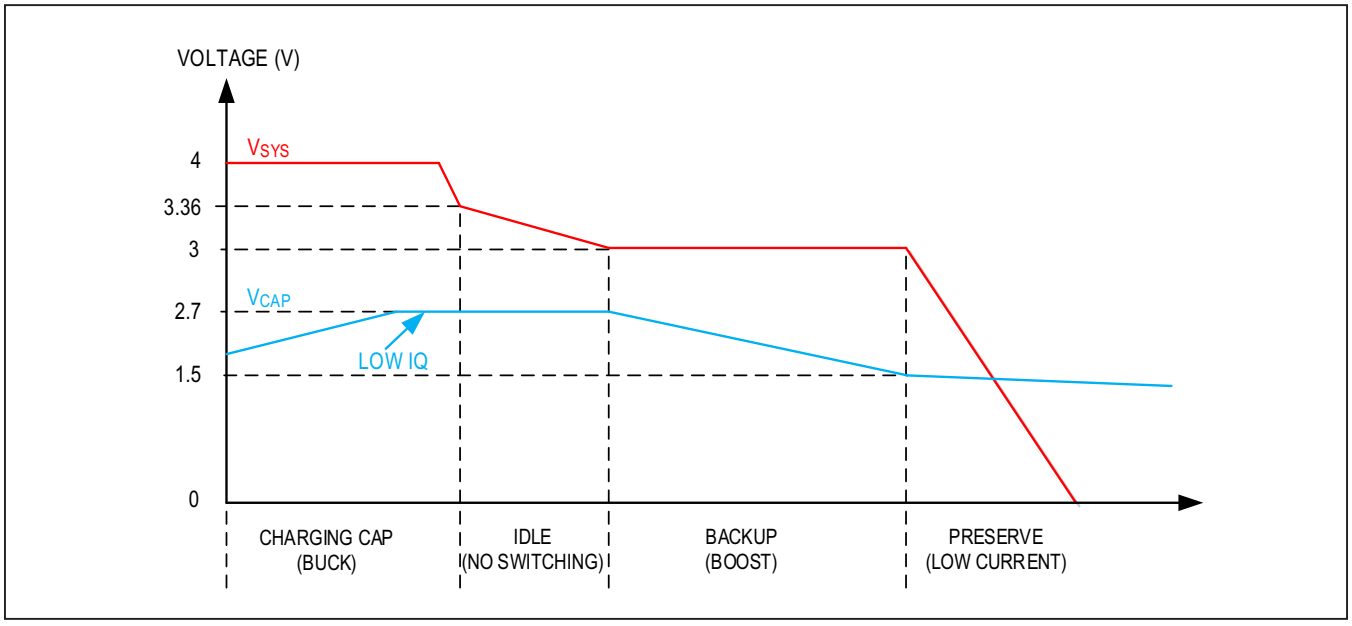


Figure 3. Charging/Discharging Waveforms

For example, in Figure 1 (Application Circuit), minimum value of the super capacitor required for 1s backup time, assuming 200mA system load and average efficiency of 93%, will be:

$C_{SCAP} \geq (2 \times 3.0V \times 0.2A \times 1s)/[((2.7V)^2 - (1.5V)^2) \times 0.93] = 256mF$

Inductor Selection

MAX38888 works with 1µH inductor in most applications. In applications where lower peak currents are desired, larger inductance may be used in order to reduce the ripple. Recommended inductance range is from 1µH to 4.7µH. Select 4.7µH for higher RISET value [100k]. 1µH is not supported for 100k RISET value.

Status Flags

MAX38888 has two dedicated pins to report the device status to the host processor. Ready output (RDY) will be high when the super capacitor is fully charged (i.e., FBCH > 0.5V). RDY is pulled low when FBCL < 0.475V. The other status flag is the Backup Output (BKUPB), which will be held low when the part is in the backup mode (i.e., when FBS < 0.5V and FBCL > 0.5V). BKUPB is released high when FBCL < 0.475V or FBS > 0.56V. Both output pins are open-drain type and require external pullup resistors. Recommended values for the pullup resistors are 1MΩ. The pins should be pulled up to the SYS rail.

Enabling Device

The MAX38888 has a dedicated enable pin. The pin can either be driven by a digital signal, pulled up, or strapped to the SYS rail.

PCB Layout Guidelines

Minimize trace lengths to reduce parasitic capacitance, inductance and resistance, and radiated noise. Keep the main power path from SYS, LX, CAP, and PGND as tight and short as possible. Minimize the surface area used for LX since this is the noisiest node. The trace between the feedback resistor dividers should be as short as possible and should be isolated from the noisy power path. Refer to the EV kit layout for best practices.

The PCB layout is important for robust thermal design. The junction to ambient thermal resistance of the package greatly depends on the PCB type, layout, and pad connections. Using thick PCB copper and having the SYS, LX, CAP, and PGND copper pours will enhance the thermal performance. The TDFN package has a large thermal pad under the package which creates excellent thermal path to PCB. This pad is electrically connected to PGND. Its PCB pad should have multiple thermal vias connecting the pad to internal PGND plane. Thermal vias should either be capped or have small diameter to minimize solder wicking and voids.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	FEATURES
MAX38888ATD+	-40°C to +125°C	14 TDFN	Enable Input, Selectable Voltages and Currents

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—
1	7/18	Updated *General Description* and *Benefits and Features*	1
2	10/18	Update *General Description, Benefits and Features* section, *Electrical Characteristics* table, *Typical Operating Characteristics*, *Detailed Description*	1, 3–6, 9–12
3	7/19	Updated *Super Capacitor Voltage Configuration* section	9
4	12/19	Updated *Enabling Device* section	12

