MAX40075/MAX40088 10MHz/42MHz Low Noise, Low Bias Op-Amps

General Description

The MAX40075/MAX40088 are wideband, low-noise, low-input bias current operational amplifiers offering rail-to-rail outputs and single-supply operation down to 2.7V. They draw 2.2mA of quiescent supply current per amplifier when enabled. Ultra-low distortion (0.0002% THD+N), as well as low input voltage-noise density (4.2nV/√Hz) and low input current-noise density (0.5fA/√Hz). The low input bias current and low noise together with the wide bandwidth will suit transimpedance amplifiers and imaging applications.

For power conservation, the MAX40075/MAX40088 offer a low-power shutdown mode that reduces supply current to 0.1µA and places the amplifiers outputs into a high impedance state. These amplifiers have outputs which swing rail-to-rail and their input common-mode voltage range includes ground. The MAX40075 is unity-gain stable with a gain-bandwidth product of 10MHz. The MAX40088 is gain-of-5 stable with a gain-bandwidth product of 42MHz.

Applications

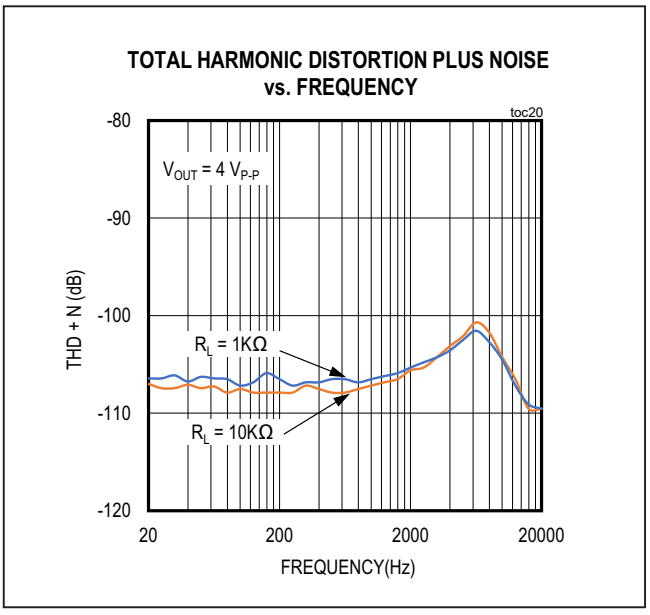
- ADC Buffers
- DAC Output Amplifiers
- Low-Noise Microphone/Preamplifiers
- Digital Scales
- Strain Gauges/Sensor Amplifiers
- Trans Impedance Amplifiers
- Medical Instrumentation
- Automotive Power Train

***Ordering Information** appears at end of data sheet.*

Benefits and Features

- Low Input Voltage-Noise Density: 4.2nV/√Hz at 30kHz
- Low Input Current-Noise Density: 0.5fA/√Hz
- Low Input Bias Current: <1pA (Typical)
- Low Distortion: 0.00035% or -109dB THD+N (1kΩ Load)
- Single-Supply Operation from +2.7V to +5.5V
- Input Common-Mode Voltage Range Includes Ground
- Rail-to-Rail Output Swings with a 1kΩ Load
- 10MHz GBW Product, Unity-Gain Stable (MAX40075 Only)
- 42MHz GBW Product, Gain ≥ 5V/V (MAX40088 Only)
- Excellent DC Characteristics: Input V_{OS} ≤ 70µV
- Low-Power Shutdown Mode: Reduces Supply Current to ≤1µA
- Available in Space-Saving 6-SOT23 and 6-WLP Packages
- AEC-Q100 Qualified, Refer to Ordering Information

THD+N Performance



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Absolute Maximum Ratings

Input Differential Voltage
MAX40075/MAX40088 (continuous) ..... -3V to +3V
MAX40075/MAX40088 (transient, 10s) ..... -6V to +6V
Power-Supply Voltage (V_{DD} to V_{SS}) ..... -0.3V to +6V
Analog Input Voltage (IN+, IN-) ..... V_{SS} -0.3V to V_{DD} +0.3V
$\overline{SHDN}$ Input Voltage ($\overline{SHDN}$) ..... V_{SS} -0.3V to +6V
Continuous Input Current (IN+, IN-) ..... ±20mA
Output Short-Circuit Duration to Either Supply ..... Continuous
Operating Temperature Range ..... -40°C to 125°C

Continuous Power Dissipation
SOT23-6 (derate 8.7mW/°C at +70°C) 696mW
6-Bump WLP (derate 10.19mW/°C at +70°C) 815mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature ((soldering, 10s)) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

6-SOT23

PACKAGE CODE	U6+1, U6+1A
Outline Number	21-0058
Land Pattern Number	90-0175
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	N/A
Junction-to-Case (θ_{JC})	80°C/W
Thermal Resistance, Multi-Layer Board:	
Junction-to-Ambient (θ_{JA})	115°C/W
Junction-to-Case (θ_{JC})	80°C/W

6-WLP

PACKAGE CODE	N60F1+1
Outline Number	21-100174
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	98.06°C/W
Junction-to-Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{DD} = +5V, V_{SS}=0V, V_{CM} = 2.5V, $\overline{SHDN}$ = V_{DD}, V_{OUT} = V_{DD}/2, R_L = Tied to V_{DD}/2, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range		Guaranteed by PSRR test	2.7		5.5	V
Quiescent Supply Current, per amplifier		V_{DD} = 3.3V		2.2	3.0	mA
		V_{DD} = 5V		2.5	3.3	
Power-Up time		V_{DD} = 0 to 5V step, V_{OUT} -> 2.5V ±1%		13		µs
Shutdown Supply Current		Overtemperature, to 125°C		0.4	1.7	µA
Input Offset Voltage		At 25°C		30	150	µV
		Over the full temperature range			450	
Input Offset Drift		Over temperature, to 125°C		0.3	3	µV/°C
Input Bias Current (Note 2)				1	2300	pA
Input offset Current (Note 2)				0.2	500	pA
Differential Input Resistance				1000		GΩ
Input Capacitance		Either input, over entire CMIR		10		pF
Input Common Mode Range		Guaranteed by CMRR test, at 25°C	-0.2		V_{DD} - 1.5	V
		Guaranteed by CMRR test, full temperature range	-0.1		V_{DD} - 1.5	
Common Mode Rejection Ratio		DC, -0.2V < CMIR < V_{DD} - 1.5V, at 25°C	90	109		dB
		DC, -0.1V < CMIR < V_{DD} - 1.5V, full temperature range	89			
Common Mode Rejection Ratio, AC		100 mV_{P-P} 1MHz, with DC in 0V to V_{DD} - 2V range		60		dB
Power Supply Rejection Ratio, DC		DC, 2.7V < V_{DD} < 5.5V	90	107		dB
Power Supply Rejection Ratio, AC		AC, 100mV_{PP} 1MHz, superimposed on VDD		40		dB
Open-Loop Gain		R_L = 10kΩ to V_{DD}/2, V_{OUT} = 200mV to V_{DD}-250mV	93	114		dB
		R_L = 1kΩ to V_{DD}/2, V_{OUT} = 200mV to V_{DD}-250mV	87	109		
		R_L = 500Ω to V_{DD}/2, V_{OUT} = 200mV to V_{DD}-250mV	85	107		
Output Voltage Swing High		R_L = 10kΩ to V_{DD}/2, V_{DD} - V_{OH}		3	10	mV
		R_L = 1kΩ to V_{DD}/2, V_{DD} - V_{OH}		30	60	
		R_L = 500Ω to V_{DD}/2, V_{DD} - V_{OH}		60	120	
Output Voltage Swing Low		R_L = 10kΩ to V_{DD}/2, V_{DD} - V_{SS}		3	10	mV
		R_L = 1kΩ to V_{DD}/2, V_{OL} - V_{SS}		30	60	
		R_L = 500Ω to V_{DD}/2, V_{OL} - V_{SS}		60	120	
Short-Circuit Current		Shorted to either power supply		48		mA
Output Leakage Current When Shut Down		V_{SS} < V_{OUT} < V_{DD}		0.01	1	µA
Shut-Down Input Low level					0.3 x V_{DD}	V

Electrical Characteristics (continued)

(V_{DD} = +5V, V_{SS}=0V, V_{CM} = 2.5V, $\overline{SHDN}$ = V_{DD}, V_{OUT} = V_{DD}/2, R_L = Tied to V_{DD}/2, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shut-Down Input High level			0.7 x V_{DD}			V
Shut-Down Input Bias				0.01	1	µA
-3dB Bandwidth		Unity-gain version, Av = +1		10		MHz
		Gain of 5 stable, Av = +5		42		
Phase Margin		Unity-gain version, Av = +1		70		°
		Gain of 5 stable, Av = +5		80		
Gain Margin				12		dB
Slew Rate		Unity-gain version, Av = +1		3		V/µs
		Gain of 5 stable, Av = +5		10		
Settling Time		Unity-gain version, Av = +1, to 0.01%, V_{OUT} = 2V step		2		µs
		Gain of 5 Stable, Av = +5, to 0.01%, V_{OUT} = 2V step		2		
Stable Capacitive Load		Guaranteed stability over all conditions		50		pF
Integrated 1/f Input Voltage Noise		0.1Hz to 10Hz		1.7		μV_{PP}
Input Voltage Noise Density		f = 10Hz		260		nV/√Hz
		f = 1kHz		5.5		
		f = 30kHz		4.2		
Input Current Noise Density		f = 1kHz		0.5		fA/√Hz
Total Harmonic Distortion + Noise		Unity-gain version, Av = +1, V_{OUT} = $4V_{PP}$, 10kΩ to GND, 1kHz		-114.0		dBc
		Unity-gain version, Av = +1, V_{OUT} = $4V_{PP}$, 10kΩ to GND, 20kHz		-103.1		
		Unity-gain version, Av = +1, V_{OUT} = $4V_{PP}$, 1kΩ to GND, 1kHz		-114.0		
		Unity-gain version, Av = +1, V_{OUT} = $4V_{PP}$, 1kΩ to GND, 20kHz		-100.0		
		Gain of 5 version, Av = +5, V_{OUT} = $4V_{PP}$, 10kΩ to GND, 1kHz		-108.0		
		Gain of 5 version, Av = +5, V_{OUT} = $4V_{PP}$, 10kΩ to GND, 20kHz		-110		
		Gain of 5 version, Av = +5, V_{OUT} = $4V_{PP}$, 1kΩ to GND, 1kHz		-106.0		
		Gain of 5 version, Av = +5, V_{OUT} = $4V_{PP}$, 1kΩ to GND, 20kHz		-110		
Electromagnetic Interference Rejection Ratio		V_{RF_PP} = 100mV, F = 900MHz to 2400MHz		55		dB

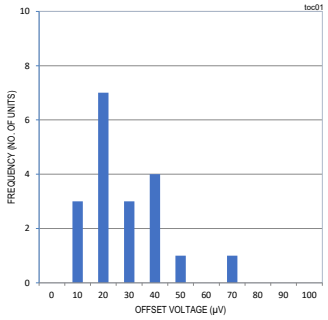
Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

2: Guaranteed by design and bench characterization.

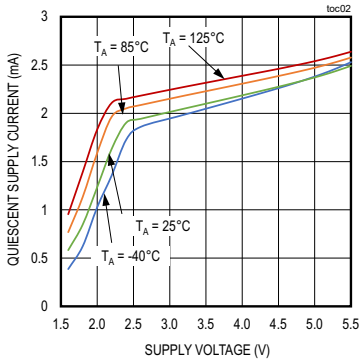
Typical Operating Characteristics

V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, C_L=10pF to GND, T_A = +25°C, unless otherwise noted.

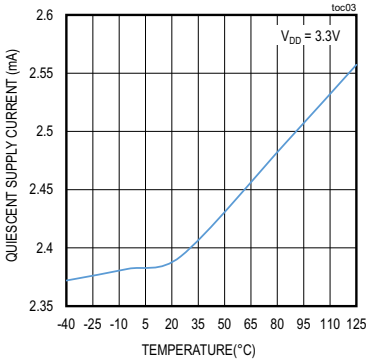
OFFSET VOLTAGE HISTOGRAM



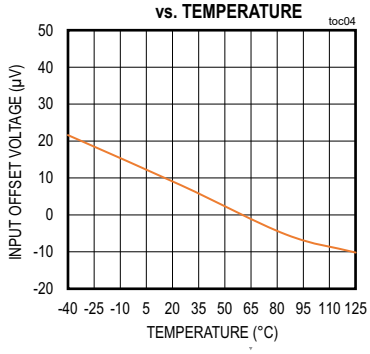
SUPPLY CURRENT vs. SUPPLY VOLTAGE



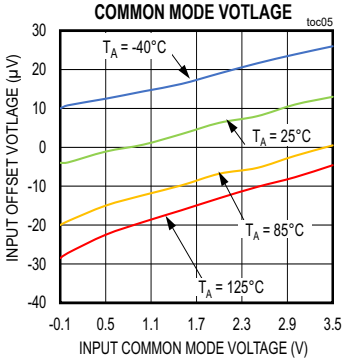
SUPPLY CURRENT vs. TEMPERATURE



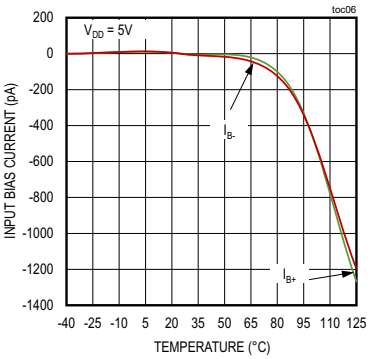
INPUT OFFSET VOLTAGE vs. TEMPERATURE



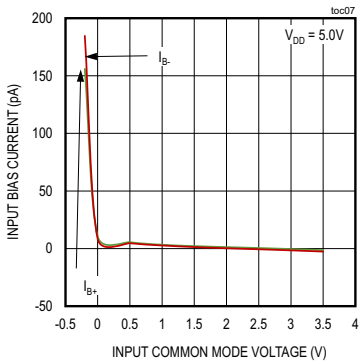
INPUT OFFSET VOLTAGE vs. INPUT COMMON MODE VOTLAGE



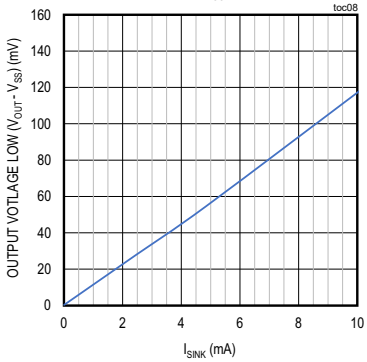
INPUT BIAS CURRENT vs. TEMPERATURE



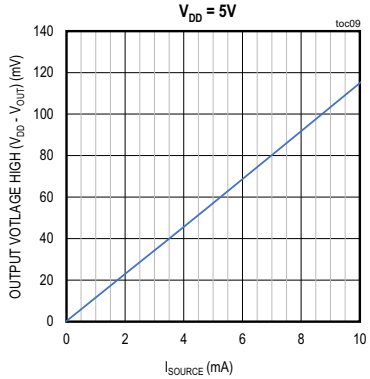
INPUT BIAS CURRENT vs. INPUT COMMON MODE VOLTAGE



OUTPUT VOLTAGE LOW vs. OUTPUT SINK CURRENT V_{DD} = 5V, V_{SS} = 0V



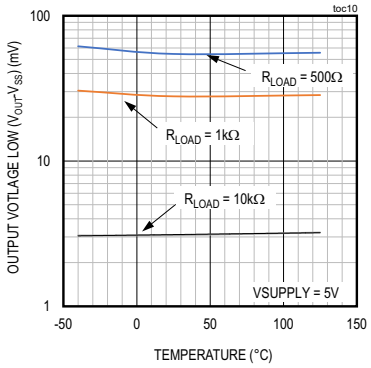
OUTPUT VOLTAGE HIGH vs. OUTPUT SOURCE CURRENT V_{DD} = 5V



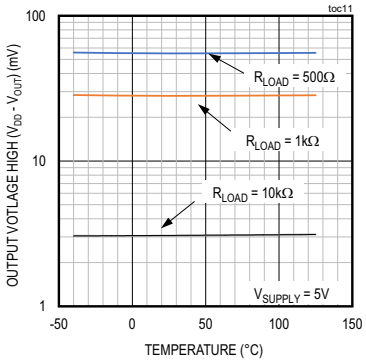
Typical Operating Characteristics (continued)

V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, C_L=10pF to GND, T_A = +25°C, unless otherwise noted.

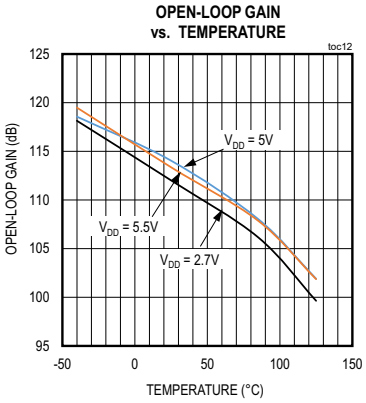
OUTPUT VOLTAGE LOW vs. TEMPERATURE



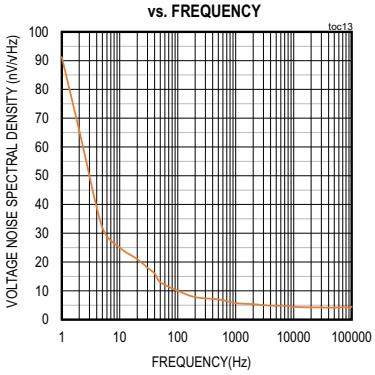
OUTPUT VOLTAGE HIGH vs. TEMPERATURE



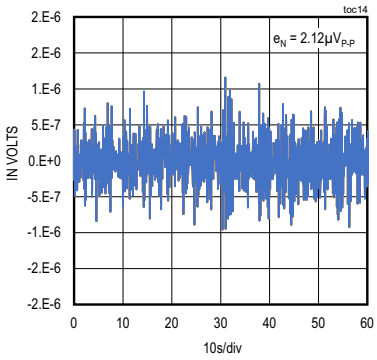
OPEN-LOOP GAIN vs. TEMPERATURE



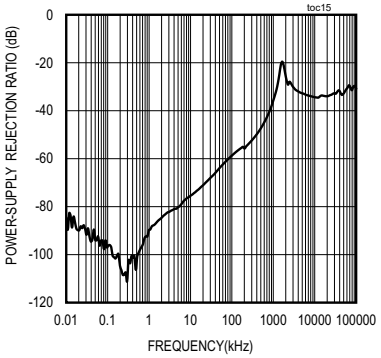
VOLTAGE NOISE DENSITY vs. FREQUENCY



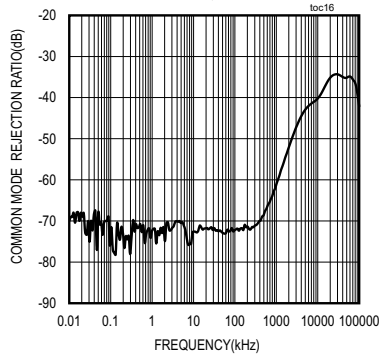
INPUT VOLTAGE NOISE 0.1Hz TO 10Hz NOISE



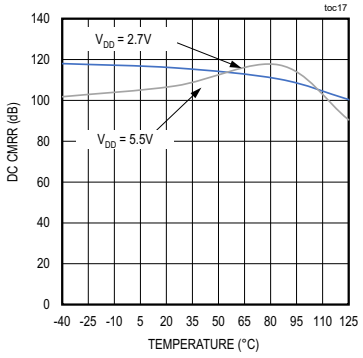
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



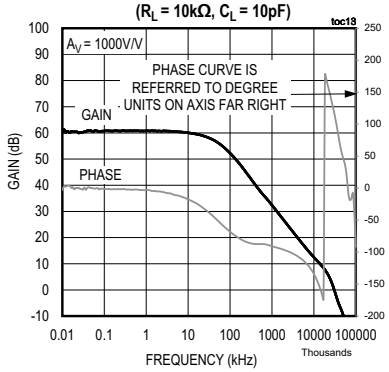
COMMON MODE REJECTION RATIO vs. FREQUENCY



COMMON MODE REJECTION RATIO vs. TEMPERATURE



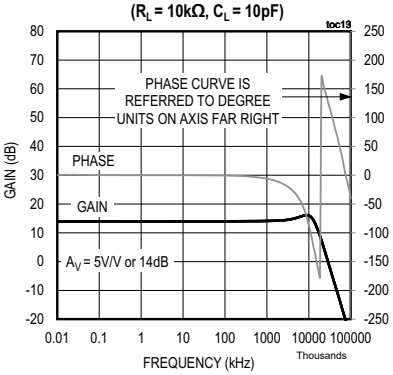
GAIN AND PHASE vs. FREQUENCY (R_L = 10kΩ, C_L = 10pF)



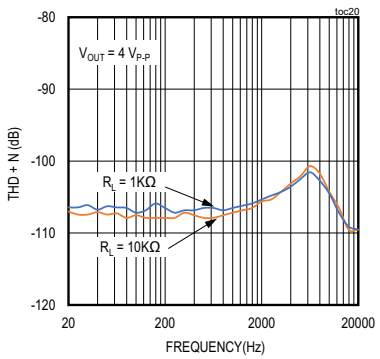
Typical Operating Characteristics (continued)

V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, C_L=10pF to GND, T_A = +25°C, unless otherwise noted.

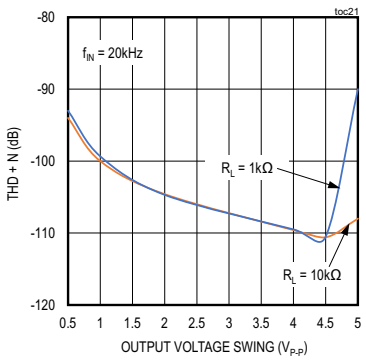
GAIN AND PHASE vs. FREQUENCY (R_L = 10kΩ, C_L = 10pF)



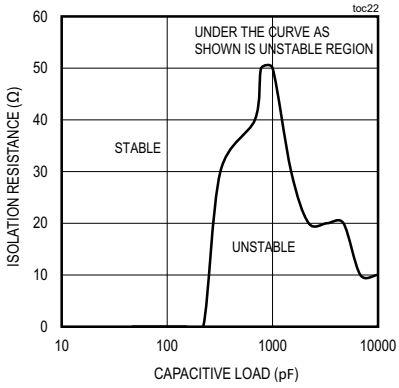
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



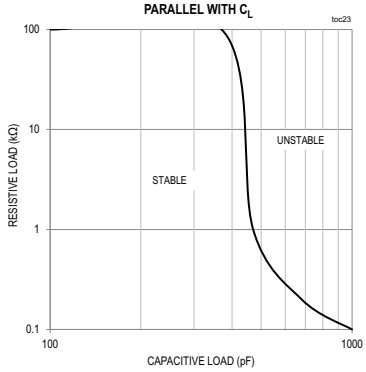
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT VOLTAGE SWING



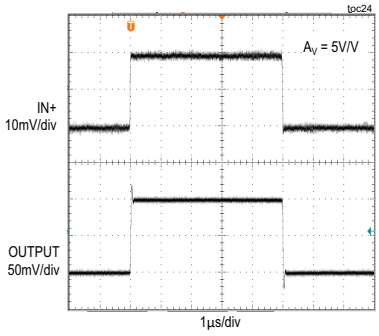
ISOLATION RESISTANCE vs. CAPACITIVE STABILITY



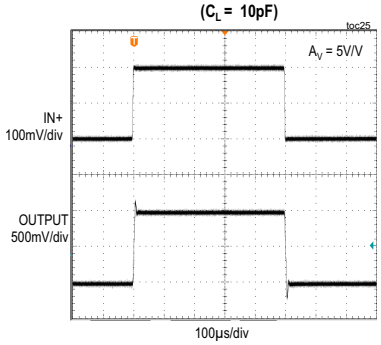
STABILITY vs. CAPACITIVE AND RESISTIVE LOAD IN PARALLEL WITH C_L



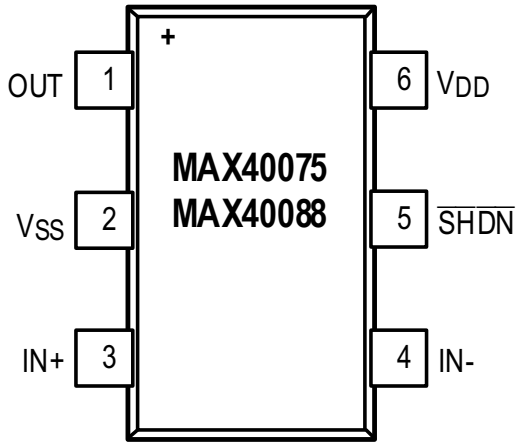
SMALL-SIGNAL PULSE RESPONSE (C_{LOAD}= 10pF)



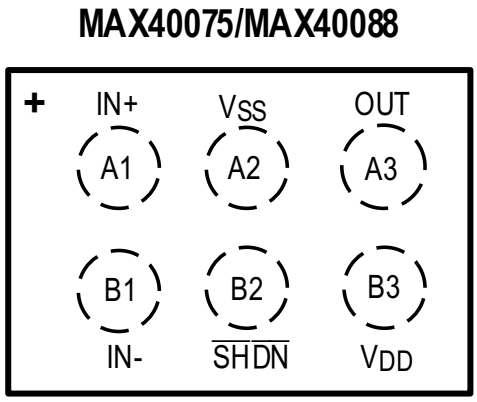
LARGE-SIGNAL PULSE RESPONSE (C_L = 10pF)



Pin Configurations



6-SOT23
(TOP VIEW)



6-WLP
(TOP VIEW)

Pin Description

PIN		NAME	FUNCTION
6-SOT23	6-WLP		
1	A3	OUT	Amplifier Output
2	A2	V_{SS}	Negative Supply. Connect to ground for single-supply operation.
3	A1	IN+	Non-Inverting Amplifier Input
4	B1	IN-	Inverting Amplifier Input
5	B2	$\overline{SHDN}$	Shutdown, Active Low. Connect to V_{DD} for normal operation (amplifier enabled)
6	B3	V_{DD}	Positive Supply. Connect 0.1µF and 4.7µF from V_{DD} to V_{SS}.

Functional Diagrams

Internal ESD protection

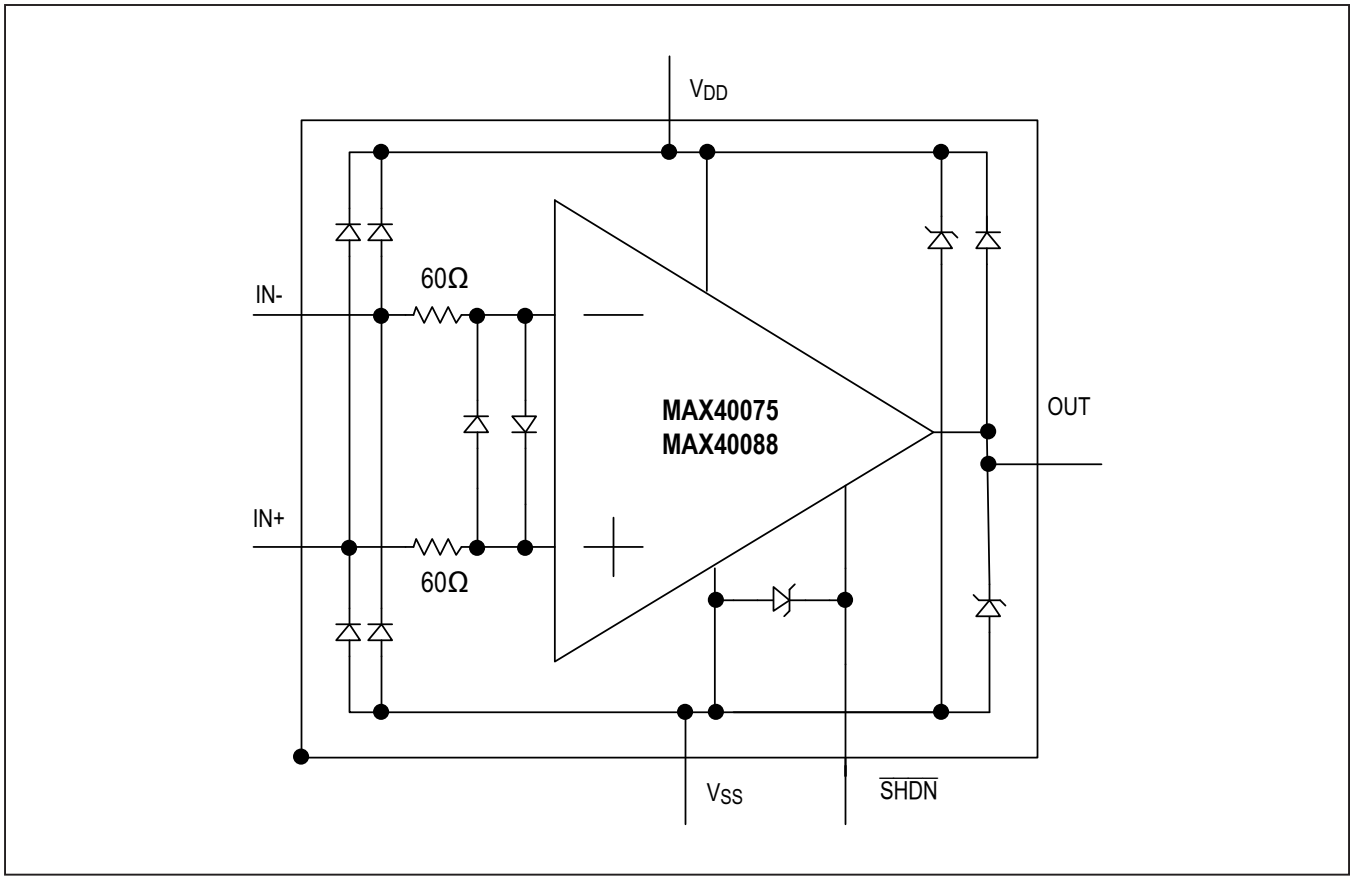


Figure 1. Internal ESD protection

Detailed Description

The MAX40075/MAX40088 single-supply operational amplifiers feature ultra-low noise and distortion. Their low distortion and low noise make them ideal for use as pre-amplifiers in wide dynamic range applications, such as 16-bit analog-to-digital converters. Their high input impedance and low noise are also useful for signal conditioning of high-impedance sources, such as piezo-electric transducers.

These devices have true rail-to-rail output operation, drive output resistive loads as low as 1kΩ while maintaining DC accuracy and can drive capacitive loads up to 200pF without any oscillation. The input common-mode voltage range extends from 0.2V below V_{SS} to (V_{DD} - 1.5V). The push-pull output stage maintains excellent DC characteristics, while delivering up to ±20 mA of source/sink output current.

The MAX40075 is unity-gain stable, while the MAX40088 is a decompensated version that has higher slew rate and is stable for Gain ≥ 5V/V. Both devices feature a low-power shutdown mode, which reduces the supply current to 0.1µA and places amplifiers outputs into a high-impedance state.

Low Noise

The amplifiers input-referred voltage noise density is dominated by flicker noise (also known as 1/f noise) at lower frequencies and by thermal noise at higher frequencies. Overall thermal noise contribution is affected by the parallel combination of resistive feedback network ($R_F||R_G$) depicted in Figure 2. These resistors should be reduced in cases where system bandwidth is large and thermal noise is dominant. Noise contribution factor can be reduced with increased gain settings.

For example, the input noise voltage density(e_N) of the circuit with R_F = 100kΩ, R_G = 10kΩ (in Figure 2) with Gain = 10V/V non-inverting configuration is e_N = 12nV/√Hz.

e_N can be reduced to 6nV/√Hz by choosing R_F = 10kΩ, R_G = 1kΩ (in Figure 2) with Gain = 10V/V, as before, but at the expense of higher current consumption and higher distortion. Having a gain of 100V/V with R_F = 100kΩ, R_G = 1kΩ (in Figure 2), input referred voltage noise density is still a low 6nV/√Hz.

Low Distortion

Many factors can affect the noise and distortion performance of the amplifier based on the design choices made. The following guidelines offer valuable information on the impact of design choices on Total Harmonic Distortion (THD). Choosing correct feedback and gain resistor values for a particular application can be a very important factor in reducing THD. In general, the smaller the closed-loop gain, the smaller the THD generated, especially when driving heavy resistive loads (e.g., smaller resistive load with higher output current). Operating the device near or above the full-power bandwidth significantly degrades distortion.

Referencing the load to either supply also improves the amplifier distortion performance, because only one of the MOSFETs of the push-pull output stage drives the output. Referencing the load to mid-supply increases the amplifier distortion for a given load and feedback setting (see the *Total Harmonic Distortion vs. Frequency* graph in *Typical Operating Characteristics*).

For gains ≥ 5V/V, the decompensated MAX40088 deliver the best distortion performance as they have a higher slew rate and provide a higher amount of loop gain for a given closed-loop gain setting. Capacitive loads below 100pF do not significantly affect distortion results. Distortion performance is relatively constant over supply voltages.

Using a Feed-Forward Compensation Capacitor, Cz

The amplifier's input capacitance is 10pF and if the resistance seen by the inverting input is large (in Figure 2) as a result of feedback network, this resistance and capacitance combination can introduce a pole within the amplifier's bandwidth resulting in reduced phase margin. Compensate the reduced phase margin by introducing a feed-forward capacitor (C_Z) between the inverting input and the output (shown in Figure 2). This effectively cancels the pole from the inverting input of the amplifier. Choose the value of C_Z as follows:

$$C_Z = 10 \times (R_F/R_G)\ [pF]$$

In the unity-gain stable MAX40075, the use of right C_Z is most important for closed loop non-inverting gain A_V = +2V/V, and inverting gain A_V = -1V/V.

In the decompensated MAX40088, C_Z is most important for closed loop gain A_V = +10V/V.

Using a slightly smaller C_Z than suggested by the formula above achieves a higher bandwidth at the expense of reduced phase and gain margin. As a general guideline, consider using C_Z for cases where $R_G||R_F$ is greater than 20kΩ (for MAX40075) and greater than 5kΩ (for MAX40088).

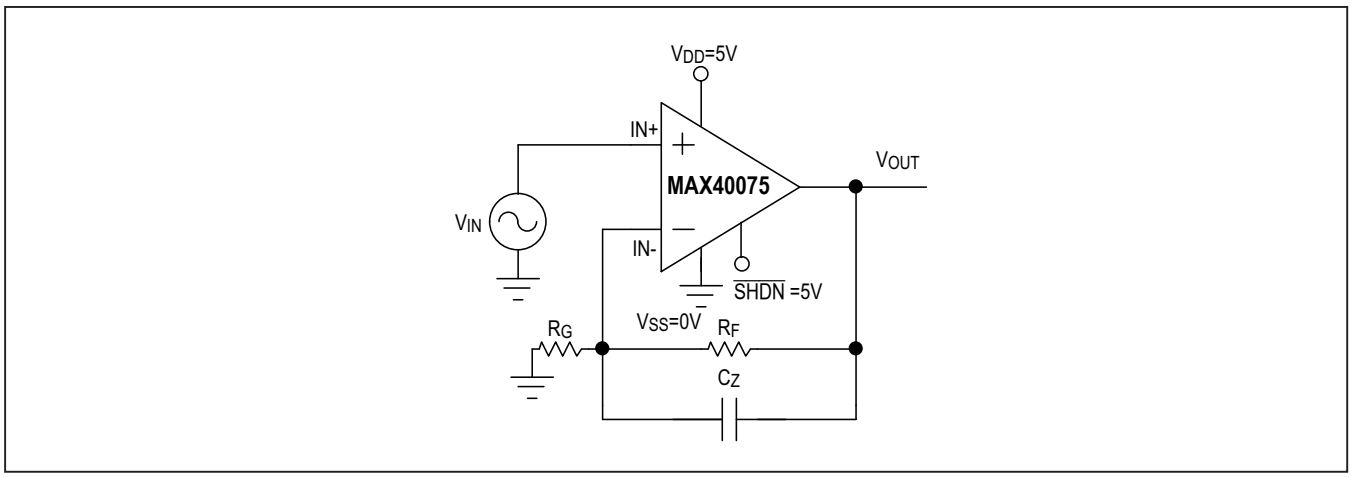


Figure 2. Adding Feed-Forward Compensation

Applications Information

Applications Information

The MAX40075/MAX40088 combine good driving capability with ground-sensing input and rail-to-rail output operation. With their low distortion and low noise, these devices are ideal for use in ADC buffers, DAC output buffers, medical instrumentation systems and other noise-sensitive applications.

Ground-Sensing and Rail-to-Rail Outputs

The common-mode input range of these devices extends below ground over temperature that offers excellent common mode rejection and can be used in low side current sensing applications. These devices are guaranteed not to undergo phase-reversal when the input is overdriven over input common mode voltage range as shown in Figure 3.

Figure 4 showcases the true rail-to-rail output operation of the amplifier, configured with A_V = 5V/V. The output swings to within 8mV of the supplies with a 10kΩ load, making the devices ideal in low-supply voltage applications.

Power Supplies and Layout

The MAX40075/MAX40088 operate from a single +2.7V to +5.5V power supply or from dual supplies of ±1.35V to ±2.75V. For single-supply operation, bypass the V_{DD} power supply pin with a 0.1µF ceramic capacitor placed close to the V_{DD} pin. If operating from dual supplies, bypass both V_{DD} and V_{SS} supply pins with 0.1µF ceramic capacitor to ground. If additional decoupling is needed add another 4.7µF or 10µF where supply voltage is applied on PCB.

Good layout improves performance by decreasing the amount of stray capacitance and noise at the op amp inputs and output. To decrease stray capacitance, minimize PC board trace lengths and resistor leads, and place external components close to the op amp's pins.

Typical Application Circuit

The *Typical Application Circuit* shows the single MAX40075 configured as an output buffer for the MAX5541 16-bit DAC. Because the MAX5541 has an unbuffered voltage output, the input bias current of the op amp used must be less than 6nA to maintain 16-bit accuracy. This family of amplifiers have an input bias current of only 2.3nA (max) over temperature, virtually eliminating this as a source of error. In addition, the MAX40075 has excellent open-loop gain and common-mode rejection, making this an excellent output buffer amplifier.

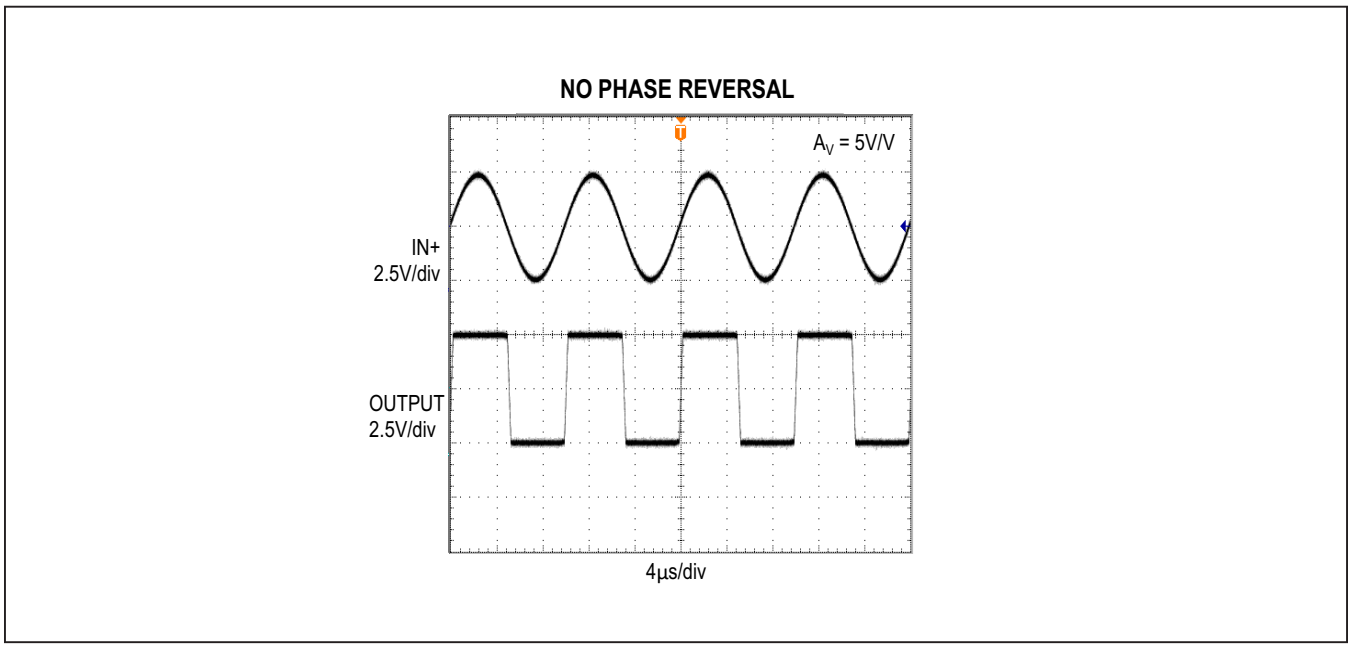


Figure 3. Scope Plot Showing Overdriven Input with No Phase Reversal

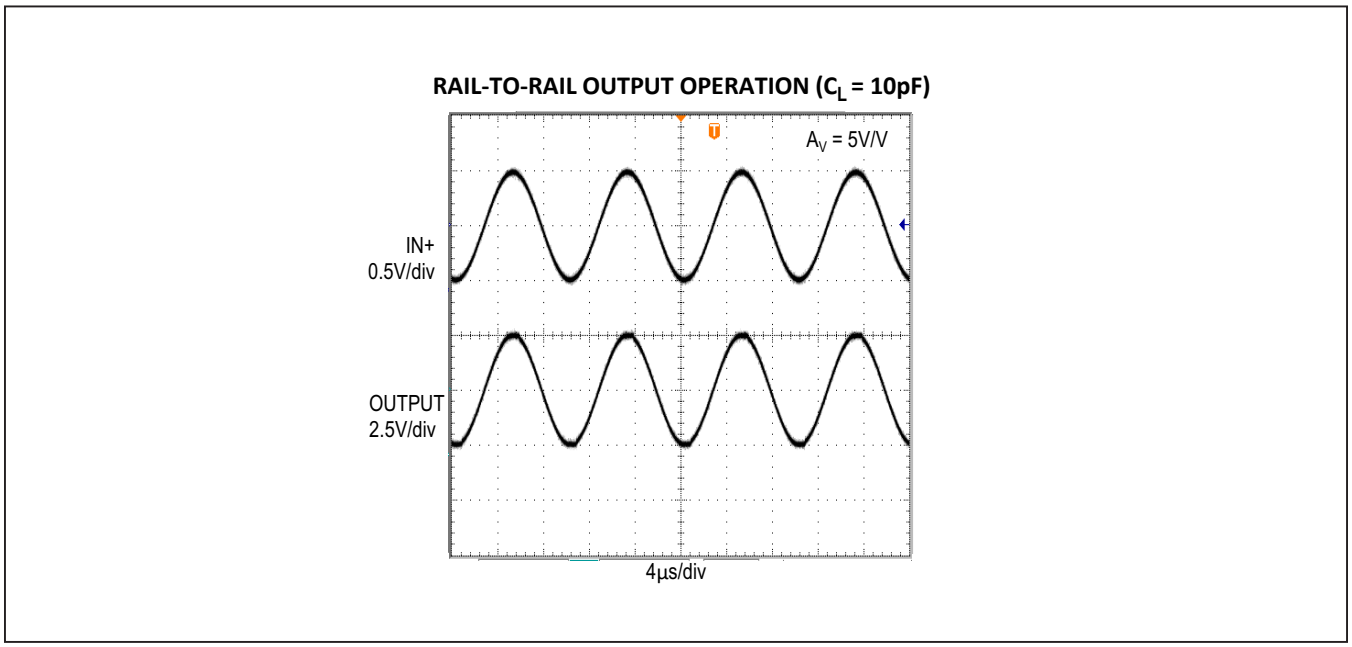
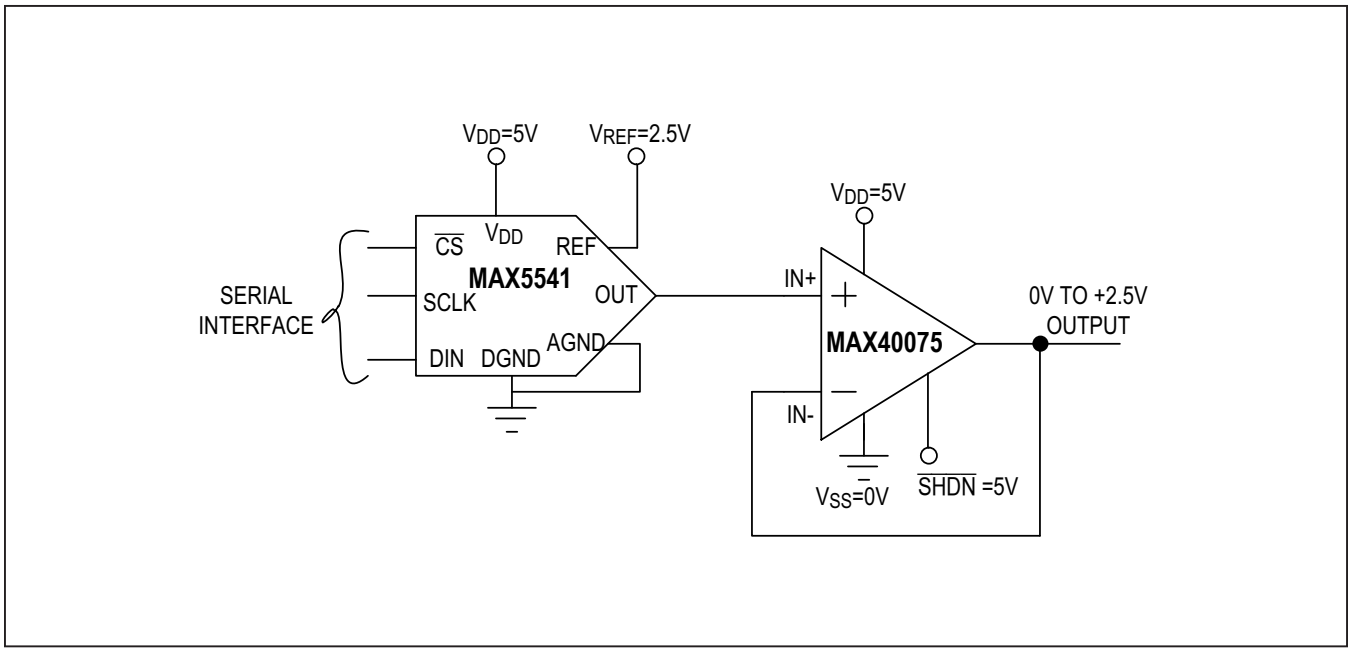


Figure 4. Rail-to-Rail Output Operation with 10KΩ and AV = 5V/VI

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	STABLE GAIN (V/V)	BW	TOP MARK
MAX40075AUT/V+T	-40°C to +125°C	6-SOT23	1	10MHz	ACVK
MAX40075ANT+T	-40°C to +125°C	6-WLP	1	10MHz	—
MAX40075AUT+T	-40°C to +125°C	6-SOT23	1	10MHz	ACVD
MAX40088ANT+T	-40°C to +125°C	6-WLP	5	42MHz	—
MAX40088AUT+T	-40°C to +125°C	6-SOT23	5	42MHz	ACVE

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

/V denotes an automotive qualified part.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—
1	7/17	Updated *Typical Operating Characteristics* section	5, 6
2	12/17	Updated *Ordering Information* table	13
3	9/18	Updated *Package Information* and *Ordering Information*	2, 13
4	6/19	Updated *Ordering Information*	13
5	7/19	Updated *Pin Configuration*	8
6	10/19	Updated *Applications* and *Benefits and Features*	1