



# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

MAX6895-MAX6899

## General Description

The MAX6895-MAX6899 is a family of small, low-power, voltage-monitoring circuits with sequencing capability. These miniature devices offer tremendous flexibility with an adjustable threshold capable of monitoring down to 0.5V and an external capacitor-adjustable time delay. These devices are ideal for use in power-supply sequencing, reset sequencing, and power-switching applications. Multiple devices can be cascaded for complex sequencing applications.

A high-impedance input with a 0.5V threshold allows an external resistive divider to set the monitored threshold. The output asserts ( $\text{OUT} = \text{high}$  or  $\overline{\text{OUT}} = \text{low}$ ) when the input voltage rises above the 0.5V threshold and the enable input is asserted ( $\text{ENABLE} = \text{high}$  or  $\overline{\text{ENABLE}} = \text{low}$ ). When the voltage at the input falls below 0.5V or when the enable input is deasserted ( $\text{ENABLE} = \text{low}$  or  $\overline{\text{ENABLE}} = \text{high}$ ), the output deasserts ( $\text{OUT} = \text{low}$  or  $\overline{\text{OUT}} = \text{high}$ ). All devices provide a capacitor-programmable delay time from when the input rises above 0.5V to when the output is asserted. The MAX689\_A versions provide the same capacitor-adjustable delay from when enable is asserted to when the output asserts. The MAX689\_P devices have a 1 $\mu\text{s}$  propagation delay from when enable is asserted to when the output asserts.

The MAX6895A/P offers an active-high enable input and an active-high push-pull output. The MAX6896A/P offers an active-low enable input and an active-low push-pull output. The MAX6897A/P offers an active-high enable input and an active-high open-drain output. Finally, the MAX6898A/P offers an active-low enable input and an active-low open-drain output. The MAX6899A/P offers an active-low enable with an active-high push-pull output.

All devices operate from a 1.5V to 5.5V supply voltage and are fully specified over the  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  operating temperature range. These devices are available in ultra-small 6-pin  $\mu\text{DFN}$  (1.0mm x 1.5mm) and thin SOT23 (1.60mm x 2.90mm) packages.

## Applications

|                         |                                   |
|-------------------------|-----------------------------------|
| Automotive              | Computers/Servers                 |
| Medical Equipment       | Critical $\mu\text{P}$ Monitoring |
| Intelligent Instruments | Set-Top Boxes                     |
| Portable Equipment      | Telecom                           |

**Typical Operating Circuit and Selector Guide appear at end of data sheet.**

## Features

- ◆ 1.8% Accurate Adjustable Threshold Over Temperature
- ◆ Operate from  $V_{\text{CC}}$  of 1.5V to 5.5V
- ◆ Capacitor-Adjustable Delay
- ◆ Active-High/-Low Enable Input Options
- ◆ Active-High/-Low Output Options
- ◆ Open-Drain (28V Tolerant)/Push-Pull Output Options
- ◆ Low Supply Current (10 $\mu\text{A}$ , typ)
- ◆ Fully Specified from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- ◆ Ultra-Small 6-Pin  $\mu\text{DFN}$  Package or Thin SOT23 Package

## Ordering Information

| PART          | PIN-PACKAGE          | TOP MARK | PKG CODE |
|---------------|----------------------|----------|----------|
| MAX6895AALT+  | 6 $\mu\text{DFN}$ -6 | +AW      | L611-1   |
| MAX6895AAZT+  | 6 Thin SOT23-6       | +AADK    | Z6-1     |
| MAX6895PALT+T | 6 $\mu\text{DFN}$ -6 | +AX      | L611-1   |
| MAX6895PAZT+  | 6 Thin SOT23-6       | +AADL    | Z6-1     |
| MAX6896AALT+  | 6 $\mu\text{DFN}$ -6 | +AY      | L611-1   |
| MAX6896AAZT+  | 6 Thin SOT23-6       | +AADO    | Z6-1     |
| MAX6896PALT+T | 6 $\mu\text{DFN}$ -6 | +AZ      | L611-1   |
| MAX6896PAZT+  | 6 Thin SOT23-6       | +AADP    | Z6-1     |

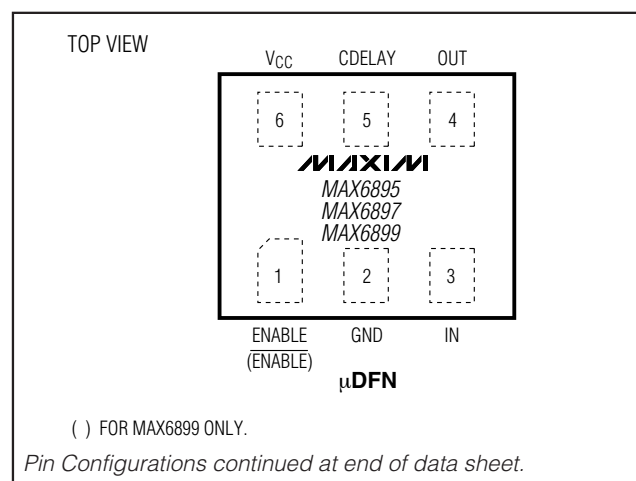
**Ordering Information continued at end of data sheet.**

**Note:** All devices are specified over the  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  operating temperature range.

+Denotes a lead-free package.

T = Tape and reel.

## Pin Configurations



# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

## ABSOLUTE MAXIMUM RATINGS

V<sub>CC</sub>, ENABLE,  $\overline{\text{ENABLE}}$ , IN.....-0.3V to +6V  
 OUT,  $\overline{\text{OUT}}$  (push-pull) .....-0.3V to (V<sub>CC</sub> + 0.3V)  
 OUT,  $\overline{\text{OUT}}$  (open-drain).....-0.3V to +30V  
 CDELAY.....-0.3V to (V<sub>CC</sub> + 0.3V)  
 Output Current (all pins).....±20mA  
 Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
   6-Pin  $\mu$ DFN (derate 2.1mW/°C above +70°C).....167.7mW  
   6-Pin Thin SOT23 (derate 2.7mW/°C above +70°C) ...219.1mW

Operating Temperature Range .....-40°C to +125°C  
 Storage Temperature Range .....-65°C to +150°C  
 Junction Temperature .....+150°C  
 Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 1.5V to 5.5V, T<sub>A</sub> = -40°C to +125°C, unless otherwise specified. Typical values are at V<sub>CC</sub> = 3.3V and T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER                                           | SYMBOL              | CONDITIONS                                                  | MIN   | TYP  | MAX   | UNITS |
|-----------------------------------------------------|---------------------|-------------------------------------------------------------|-------|------|-------|-------|
| <b>SUPPLY</b>                                       |                     |                                                             |       |      |       |       |
| Operating Voltage Range                             | V <sub>CC</sub>     |                                                             | 1.5   |      | 5.5   | V     |
| Undervoltage Lockout (Note 2)                       | UVLO                | V <sub>CC</sub> falling                                     | 1.20  |      | 1.35  | V     |
| V <sub>CC</sub> Supply Current                      | I <sub>CC</sub>     | V <sub>CC</sub> = 3.3V, no load                             |       | 10   | 20    | μA    |
| <b>IN</b>                                           |                     |                                                             |       |      |       |       |
| Threshold Voltage                                   | V <sub>TH</sub>     | V <sub>IN</sub> rising, 1.5V < V <sub>CC</sub> < 5.5V       | 0.491 | 0.5  | 0.509 | V     |
| Hysteresis                                          | V <sub>HYST</sub>   | V <sub>IN</sub> falling                                     |       | 5    |       | mV    |
| Input Current (Note 3)                              | I <sub>IN</sub>     | V <sub>IN</sub> = 0V or V <sub>CC</sub>                     | -15   |      | +15   | nA    |
| <b>CDELAY</b>                                       |                     |                                                             |       |      |       |       |
| Delay Charge Current                                | I <sub>CD</sub>     |                                                             | 200   | 250  | 300   | nA    |
| Delay Threshold                                     | V <sub>TCD</sub>    | CDELAY rising                                               | 0.95  | 1.00 | 1.05  | V     |
| CDELAY Pulldown Resistance                          | R <sub>CDELAY</sub> |                                                             |       | 130  | 500   | Ω     |
| <b>ENABLE/<math>\overline{\text{ENABLE}}</math></b> |                     |                                                             |       |      |       |       |
| Input Low Voltage                                   | V <sub>IL</sub>     |                                                             |       |      | 0.4   | V     |
| Input High Voltage                                  | V <sub>IH</sub>     |                                                             | 1.4   |      |       | V     |
| Input Leakage Current                               | I <sub>LEAK</sub>   | ENABLE, $\overline{\text{ENABLE}}$ = V <sub>CC</sub> or GND | -100  |      | +100  | nA    |

# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

MAX6895-MAX6899

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = 1.5V$  to  $5.5V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise specified. Typical values are at  $V_{CC} = 3.3V$  and  $T_A = +25^{\circ}C$ , unless otherwise noted.) (Note 1)

| PARAMETER                                                  | SYMBOL      | CONDITIONS                                                               | MIN                       | TYP | MAX | UNITS   |
|------------------------------------------------------------|-------------|--------------------------------------------------------------------------|---------------------------|-----|-----|---------|
| <b>OUT/<math>\overline{OUT}</math></b>                     |             |                                                                          |                           |     |     |         |
| Output Low Voltage (Open-Drain or Push-Pull)               | $V_{OL}$    | $V_{CC} \geq 1.2V$ , $I_{SINK} = 90\mu A$ , MAX6895/MAX6897/MAX6899 only |                           |     | 0.3 | V       |
|                                                            |             | $V_{CC} \geq 2.25V$ , $I_{SINK} = 0.5mA$                                 |                           |     | 0.3 |         |
|                                                            |             | $V_{CC} \geq 4.5V$ , $I_{SINK} = 1mA$                                    |                           |     | 0.4 |         |
| Output High Voltage (Push-Pull)                            | $V_{OH}$    | $V_{CC} \geq 2.25V$ , $I_{SOURCE} = 500\mu A$                            | $0.8 \times V_{CC}$       |     |     | V       |
|                                                            |             | $V_{CC} \geq 4.5V$ , $I_{SOURCE} = 800\mu A$                             | $0.8 \times V_{CC}$       |     |     |         |
| Output Open-Drain Leakage Current                          | $I_{LKG}$   | Output high impedance, $V_{OUT} = 28V$                                   |                           |     | 1   | $\mu A$ |
| <b>TIMING</b>                                              |             |                                                                          |                           |     |     |         |
| IN to OUT/ $\overline{OUT}$ Propagation Delay              | $t_{DELAY}$ | $V_{IN}$ rising                                                          | $CC_{DELAY} = 0$          | 40  |     | $\mu s$ |
|                                                            |             |                                                                          | $CC_{DELAY} = 0.047\mu F$ | 190 |     | ms      |
|                                                            | $t_{DL}$    | $V_{IN}$ falling                                                         |                           | 16  |     | $\mu s$ |
| Startup Delay (Note 4)                                     |             |                                                                          |                           | 2   |     | ms      |
| ENABLE/ $\overline{ENABLE}$ Minimum Input Pulse Width      | $t_{PW}$    |                                                                          | 1                         |     |     | $\mu s$ |
| ENABLE/ $\overline{ENABLE}$ Glitch Rejection               |             |                                                                          |                           | 100 |     | ns      |
| ENABLE/ $\overline{ENABLE}$ to OUT/ $\overline{OUT}$ Delay | $t_{OFF}$   | From device enabled to device disabled                                   |                           | 150 |     | ns      |
| ENABLE/ $\overline{ENABLE}$ to OUT/ $\overline{OUT}$ Delay | $t_{PROPP}$ | From device disabled to device enabled (P version)                       |                           | 150 |     | ns      |
|                                                            | $t_{PROPA}$ | From device disabled to device enabled (A version)                       | $CC_{DELAY} = 0$          | 20  |     | $\mu s$ |
|                                                            |             |                                                                          | $CC_{DELAY} = 0.047\mu F$ | 190 |     | ms      |

**Note 1:** All devices are production tested at  $T_A = +25^{\circ}C$ . Limits over temperature are guaranteed by design.

**Note 2:** When  $V_{CC}$  falls below the UVLO threshold, the outputs will deassert (OUT goes low,  $\overline{OUT}$  goes high). When  $V_{CC}$  falls below 1.2V, the output state cannot be determined.

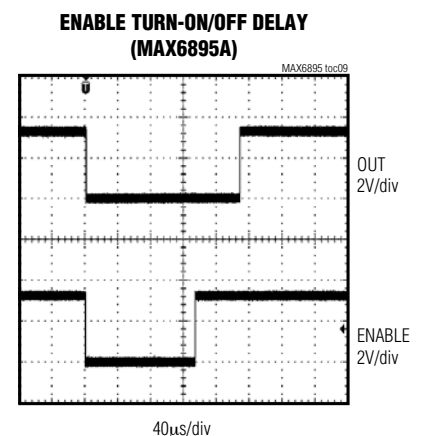
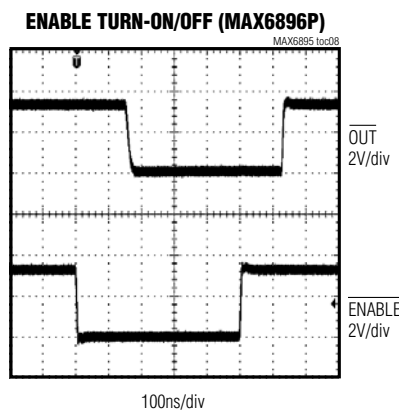
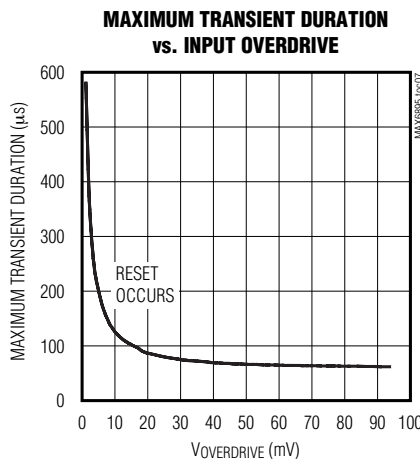
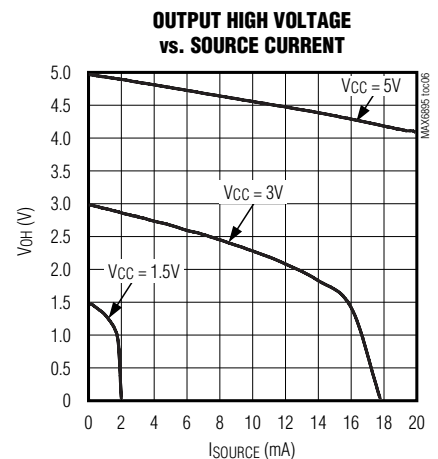
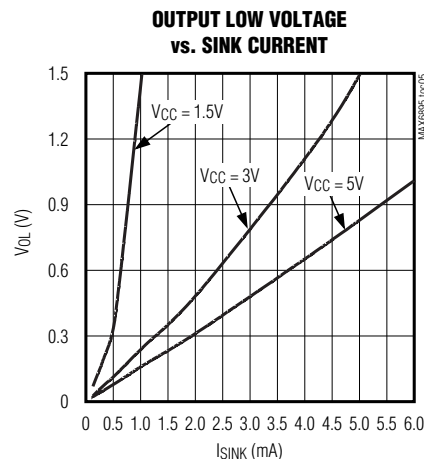
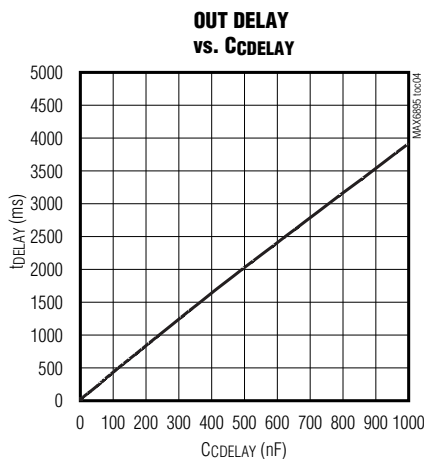
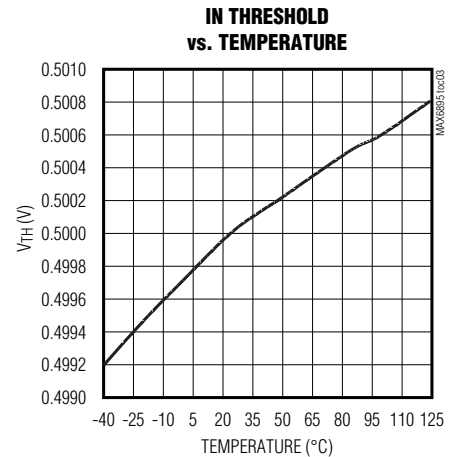
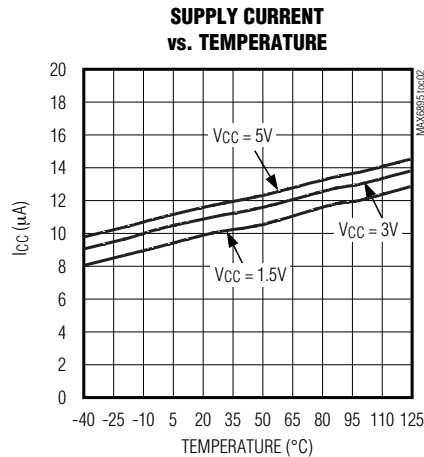
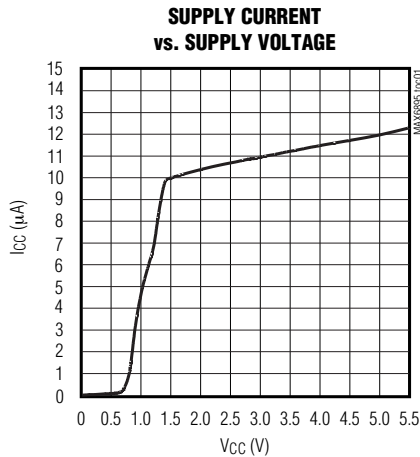
**Note 3:** Guaranteed by design.

**Note 4:** During the initial power-up,  $V_{CC}$  must exceed 1.5V for at least 2ms before the output is guaranteed to be in the correct state.

# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

## Typical Operating Characteristics

( $V_{CC} = 3.3V$  and  $T_A = +25^\circ C$ , unless otherwise noted.)



# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

## Pin Description

MAX6895-MAX6899

| PIN                 |               |                     |               |         |               | NAME                       | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------------------|---------------|---------------------|---------------|---------|---------------|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MAX6895/<br>MAX6897 |               | MAX6896/<br>MAX6898 |               | MAX6899 |               |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| μDFN                | THIN<br>SOT23 | μDFN                | THIN<br>SOT23 | μDFN    | THIN<br>SOT23 |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 1                   | 1             | —                   | —             | —       | —             | ENABLE                     | Active-High Logic-Enable Input. Drive ENABLE low to immediately deassert the output to its false state (OUT = low or $\overline{\text{OUT}}$ = high) independent of $V_{\text{IN}}$ . With $V_{\text{IN}}$ above $V_{\text{TH}}$ , drive ENABLE high to assert the output to its true state (OUT = high or $\overline{\text{OUT}}$ = low) after the adjustable delay period (MAX689_A) or a 150ns propagation delay (MAX689_P).                                                                                                                                                                                                                 |
| —                   | —             | 1                   | 1             | 1       | 1             | $\overline{\text{ENABLE}}$ | Active-Low Logic-Enable Input. Drive $\overline{\text{ENABLE}}$ high to immediately deassert the output to its false state (OUT = low or $\overline{\text{OUT}}$ = high) independent of $V_{\text{IN}}$ . With $V_{\text{IN}}$ above $V_{\text{TH}}$ , drive $\overline{\text{ENABLE}}$ low to assert the output to its true state (OUT = high or $\overline{\text{OUT}}$ = low) after the adjustable delay period (MAX689_A) or a 150ns propagation delay (MAX689_P).                                                                                                                                                                          |
| 2                   | 2             | 2                   | 2             | 2       | 2             | GND                        | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 3                   | 3             | 3                   | 3             | 3       | 3             | IN                         | High-Impedance Monitor Input. Connect IN to an external resistive divider to set the desired monitored threshold. The output changes state when $V_{\text{IN}}$ rises above 0.5V and when $V_{\text{IN}}$ falls below 0.495V.                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 4                   | 4             | —                   | —             | 4       | 4             | OUT                        | Active-High Sequencer/Monitor Output, Push-Pull (MAX6895/MAX6899) or Open-Drain (MAX6897). OUT is asserted to its true state (OUT = high) when $V_{\text{IN}}$ is above $V_{\text{TH}}$ and the enable input is in its true state (ENABLE = high or $\overline{\text{ENABLE}}$ = low) for the capacitor-adjusted delay period. OUT is deasserted to its false state (OUT = low) immediately after $V_{\text{IN}}$ drops below $V_{\text{TH}}$ - 5mV or the enable input is in its false state (ENABLE = low or $\overline{\text{ENABLE}}$ = high). The open-drain version requires an external pullup resistor.                                 |
| —                   | —             | 4                   | 4             | —       | —             | $\overline{\text{OUT}}$    | Active-Low Sequencer/Monitor Output, Push-Pull (MAX6896) or Open-Drain (MAX6898). OUT is asserted to its true state ( $\overline{\text{OUT}}$ = low) when $V_{\text{IN}}$ is above $V_{\text{TH}}$ and the enable input is in its true state (ENABLE = high or $\overline{\text{ENABLE}}$ = low) for the CDELAY adjusted timeout period. OUT is deasserted to its false state ( $\overline{\text{OUT}}$ = high) immediately after $V_{\text{IN}}$ drops below $V_{\text{TH}}$ - 5mV or the enable input is in its false state (ENABLE = low or $\overline{\text{ENABLE}}$ = high). The open-drain version requires an external pullup resistor. |
| 5                   | 6             | 5                   | 6             | 5       | 6             | CDELAY                     | Capacitor-Adjustable Delay. Connect an external capacitor (CDELAY) from CDELAY to GND to set the IN to OUT (and ENABLE to OUT or $\overline{\text{ENABLE}}$ to OUT for A version devices) delay period. $t_{\text{DELAY}} = (\text{CDELAY} \times 4.0 \times 10^6) + 40\mu\text{s}$ . There is a fixed short delay (40μs, typ) for the output deasserting when $V_{\text{IN}}$ falls below $V_{\text{TH}}$ .                                                                                                                                                                                                                                    |
| 6                   | 5             | 6                   | 5             | 6       | 5             | VCC                        | Supply Voltage Input. Connect a 1.5V to 5.5V supply to VCC to power the device. For noisy systems, bypass with a 0.1μF ceramic capacitor to GND.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

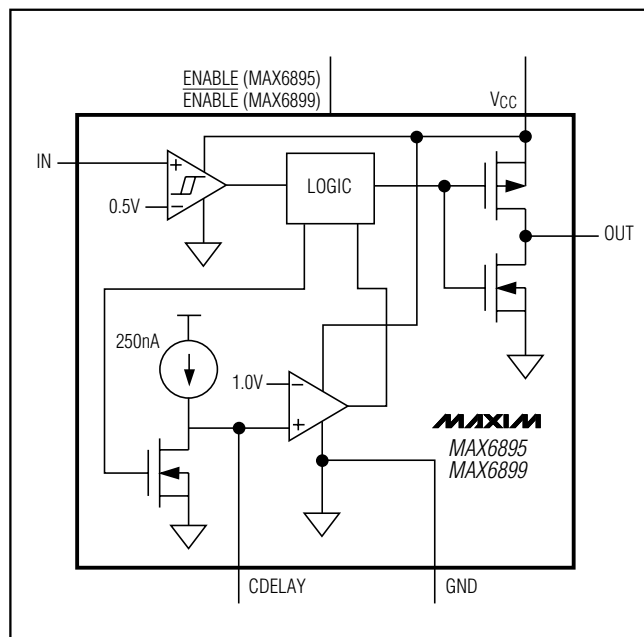


Figure 1. MAX6895/MAX6899 Functional Diagram

## Detailed Description

The MAX6895–MAX6899 is a family of ultra-small, low-power, sequencing/supervisory circuits. These devices provide adjustable voltage monitoring for inputs down to 0.5V. They are ideal for use in power-supply sequencing, reset sequencing, and power-switching applications. Multiple devices can be cascaded for complex sequencing applications.

Voltage monitoring is performed through a high-impedance input (IN) with an internally fixed 0.5V threshold. When the voltage at IN falls below 0.5V or when the enable input is deasserted (ENABLE = low or  $\overline{\text{ENABLE}}$  = high), the output deasserts (OUT goes low or  $\overline{\text{OUT}}$  goes high). When  $V_{\text{IN}}$  rises above 0.5V and the enable input is asserted (ENABLE = high or  $\overline{\text{ENABLE}}$  = low), the output asserts (OUT goes high or  $\overline{\text{OUT}}$  goes low) after a capacitor-programmable time delay.

With  $V_{\text{IN}}$  above 0.5V, the enable input can be used to turn the output on or off. After the enable input is asserted, the output turns on with a capacitor-programmable delay period (A version) or with a 150ns propagation delay (P version). Tables 1, 2, and 3 detail the output state depending on the various input and enable conditions.

Table 1. MAX6895/MAX6897 Output

| IN                              | ENABLE | OUT                             |
|---------------------------------|--------|---------------------------------|
| $V_{\text{IN}} < V_{\text{TH}}$ | Low    | Low                             |
| $V_{\text{IN}} < V_{\text{TH}}$ | High   | Low                             |
| $V_{\text{IN}} > V_{\text{TH}}$ | Low    | Low                             |
| $V_{\text{IN}} > V_{\text{TH}}$ | High   | OUT = $V_{\text{CC}}$ (MAX6895) |
|                                 |        | OUT = high impedance (MAX6897)  |

Table 2. MAX6896/MAX6898 Output

| IN                              | ENABLE | $\overline{\text{OUT}}$                                   |
|---------------------------------|--------|-----------------------------------------------------------|
| $V_{\text{IN}} < V_{\text{TH}}$ | Low    | $\overline{\text{OUT}} = V_{\text{CC}}$ (MAX6896)         |
|                                 |        | $\overline{\text{OUT}} = \text{high impedance}$ (MAX6898) |
| $V_{\text{IN}} < V_{\text{TH}}$ | High   | $\overline{\text{OUT}} = V_{\text{CC}}$ (MAX6896)         |
|                                 |        | $\overline{\text{OUT}} = \text{high impedance}$ (MAX6898) |
| $V_{\text{IN}} > V_{\text{TH}}$ | Low    | Low                                                       |
| $V_{\text{IN}} > V_{\text{TH}}$ | High   | $\overline{\text{OUT}} = V_{\text{CC}}$ (MAX6896)         |
|                                 |        | $\overline{\text{OUT}} = \text{high impedance}$ (MAX6898) |

Table 3. MAX6899 Output

| IN                              | ENABLE | OUT  |
|---------------------------------|--------|------|
| $V_{\text{IN}} < V_{\text{TH}}$ | Low    | Low  |
| $V_{\text{IN}} < V_{\text{TH}}$ | High   | Low  |
| $V_{\text{IN}} > V_{\text{TH}}$ | Low    | High |
| $V_{\text{IN}} > V_{\text{TH}}$ | High   | Low  |

## Supply Input ( $V_{\text{CC}}$ )

The device operates with a  $V_{\text{CC}}$  supply voltage from 1.5V to 5.5V. To maintain a 1.8% accurate threshold,  $V_{\text{CC}}$  must be above 1.5V. When  $V_{\text{CC}}$  falls below the UVLO threshold, the output deasserts. When  $V_{\text{CC}}$  falls below 1.2V the output state cannot be determined. For noisy systems, connect a 0.1 $\mu\text{F}$  ceramic capacitor from  $V_{\text{CC}}$  to GND as close to the device as possible. For the push-pull active-high output option, a 100k $\Omega$  external pulldown resistor to ground ensures the correct logic state for  $V_{\text{CC}}$  down to 0.

## Ultra-Small, Adjustable Sequencing/Supervisory Circuits

### Monitor Input (IN)

Connect the center point of a resistive divider to IN to monitor external voltages (see R1 and R2 of the *Typical Operating Circuit*). IN has a rising threshold of  $V_{TH} = 0.5V$  and a falling threshold of  $0.495V$  (5mV hysteresis). When  $V_{IN}$  rises above  $V_{TH}$  and ENABLE is high (or  $\overline{ENABLE}$  is low) OUT goes high ( $\overline{OUT}$  goes low) after the programmed  $t_{DELAY}$  period. When  $V_{IN}$  falls below  $0.495V$ , OUT goes low ( $\overline{OUT}$  goes high) after a  $16\mu s$  delay. IN has a maximum input current of  $15nA$  so large-value resistors are permitted without adding significant error to the resistive divider.

### Adjustable Delay (CDELAY)

When  $V_{IN}$  rises above  $V_{TH}$  with ENABLE high ( $\overline{ENABLE}$  low), the internal  $250nA$  current source begins charging an external capacitor connected from CDELAY to GND. When the voltage at CDELAY reaches  $1V$ , the output

asserts (OUT goes high or  $\overline{OUT}$  goes low). When the output asserts,  $C_{DELAY}$  is immediately discharged. Adjust the delay ( $t_{DELAY}$ ) from when  $V_{IN}$  rises above  $V_{TH}$  (with ENABLE high or  $\overline{ENABLE}$  low) to OUT going high ( $\overline{OUT}$  going low) according to the equation:

$$t_{DELAY} = C_{DELAY} \times 4.0 \times 10^6 + 40\mu s$$

where  $C_{DELAY}$  is the external capacitor from CDELAY to GND.

For adjustable delay devices (A version), when  $V_{IN} > 0.5V$  and ENABLE goes from low to high ( $\overline{ENABLE}$  goes from high to low) the output asserts after a  $t_{DELAY}$  period. For nonadjustable delay devices (P version) there is a  $1\mu s$  propagation delay from when the enable input is asserted to when the output asserts. Figures 2 through 5 show the timing diagrams for the adjustable and fixed delay versions, respectively.

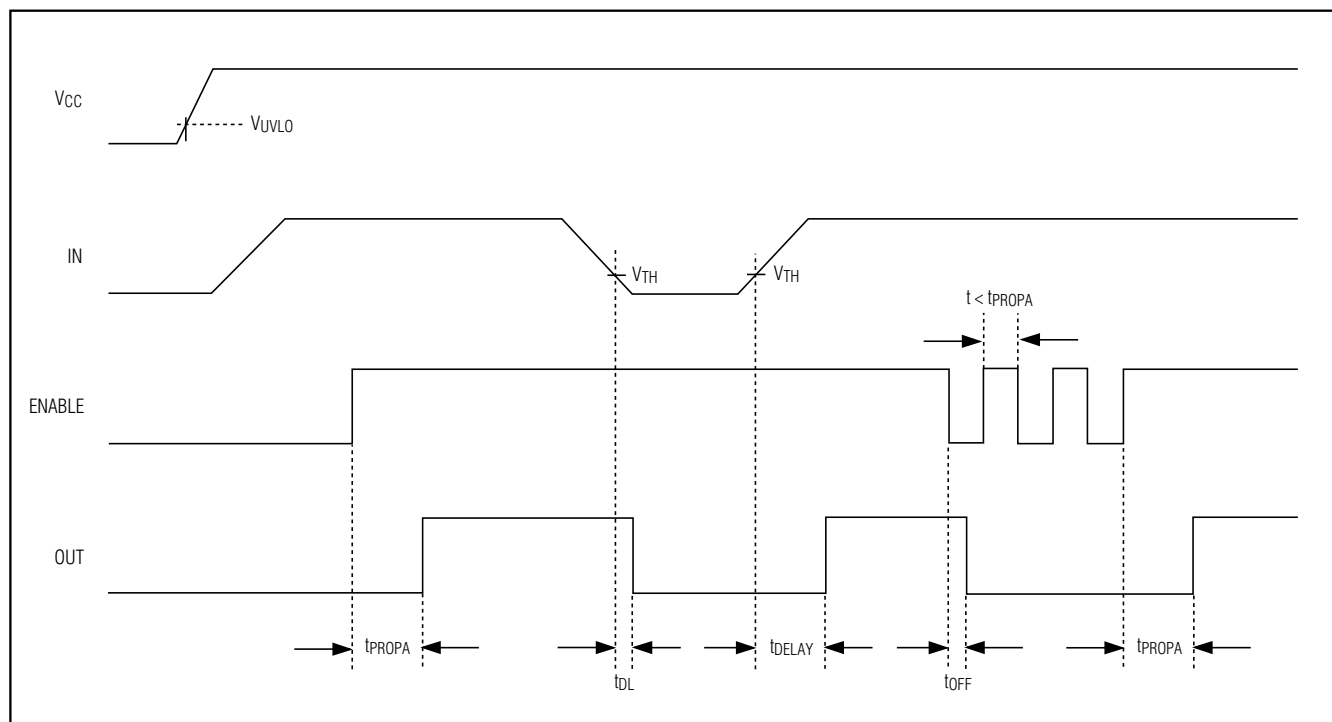
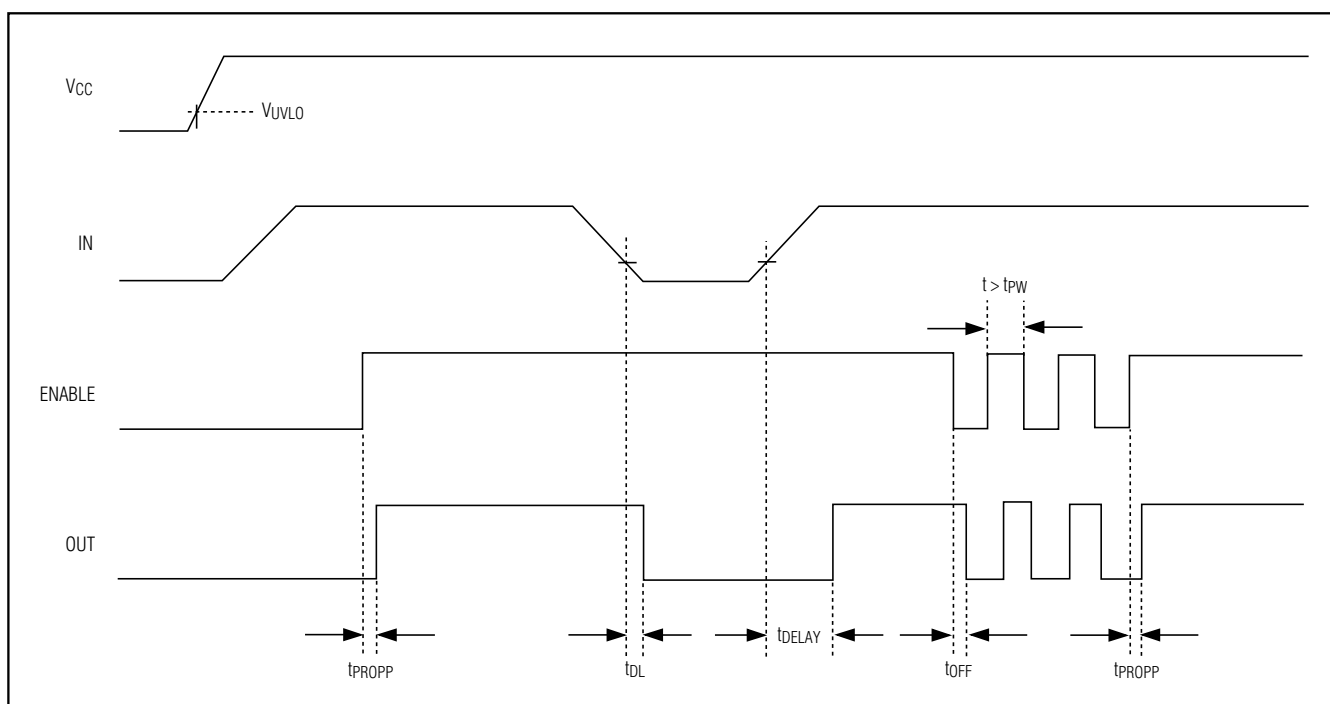
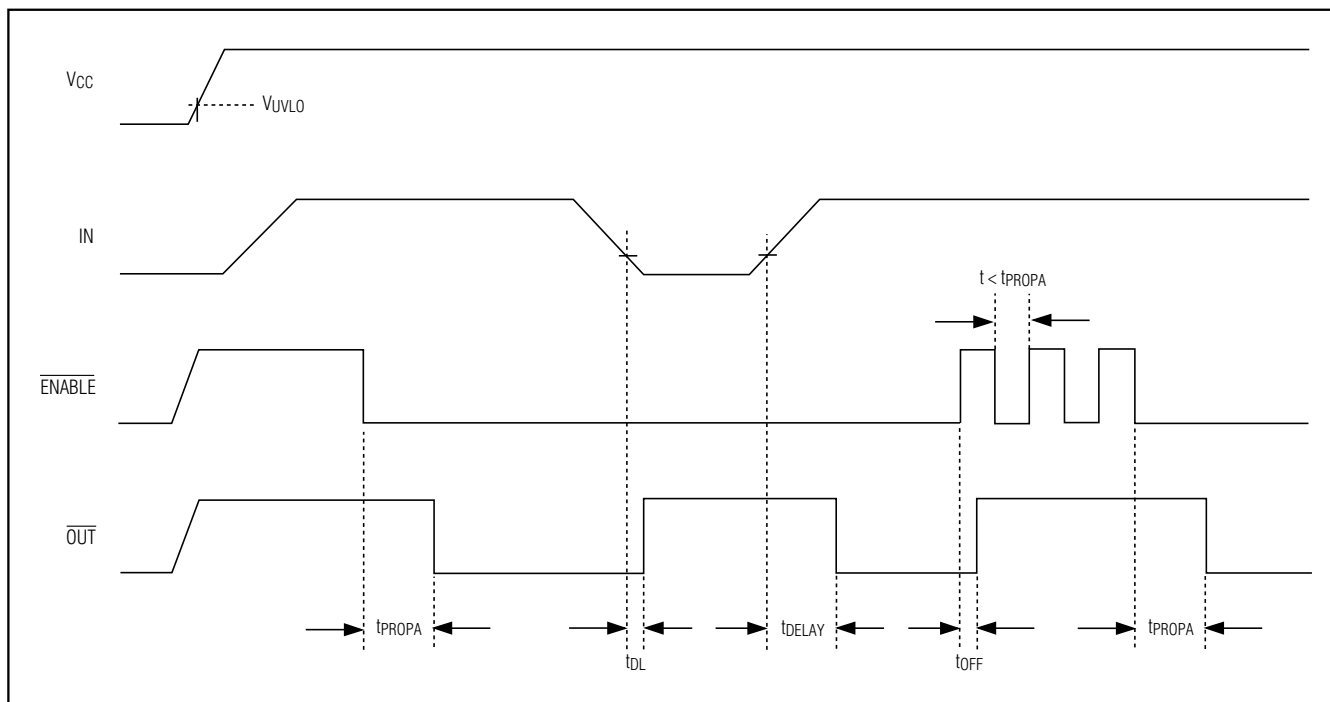


Figure 2. MAX6895A/MAX6897A Timing Diagram

# Ultra-Small, Adjustable Sequencing/Supervisory Circuits





# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

MAX6895-MAX6899

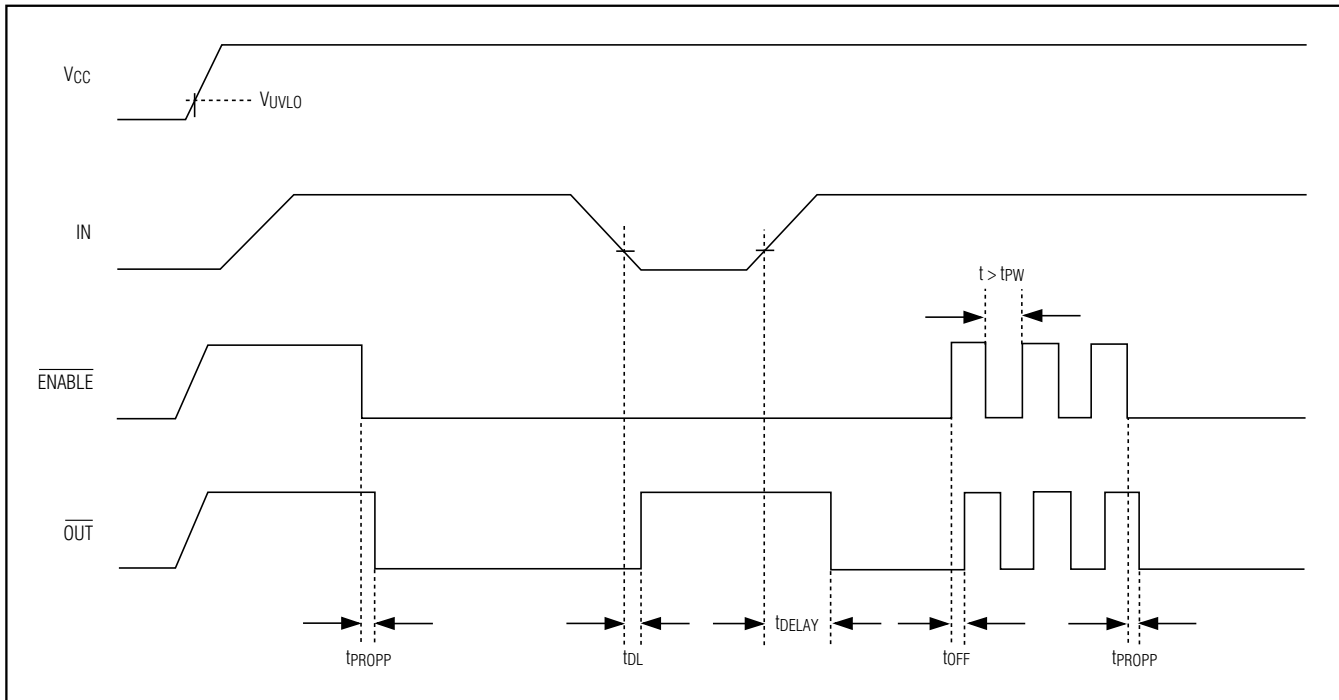


Figure 5. MAX6896P/MAX6898P Timing Diagram

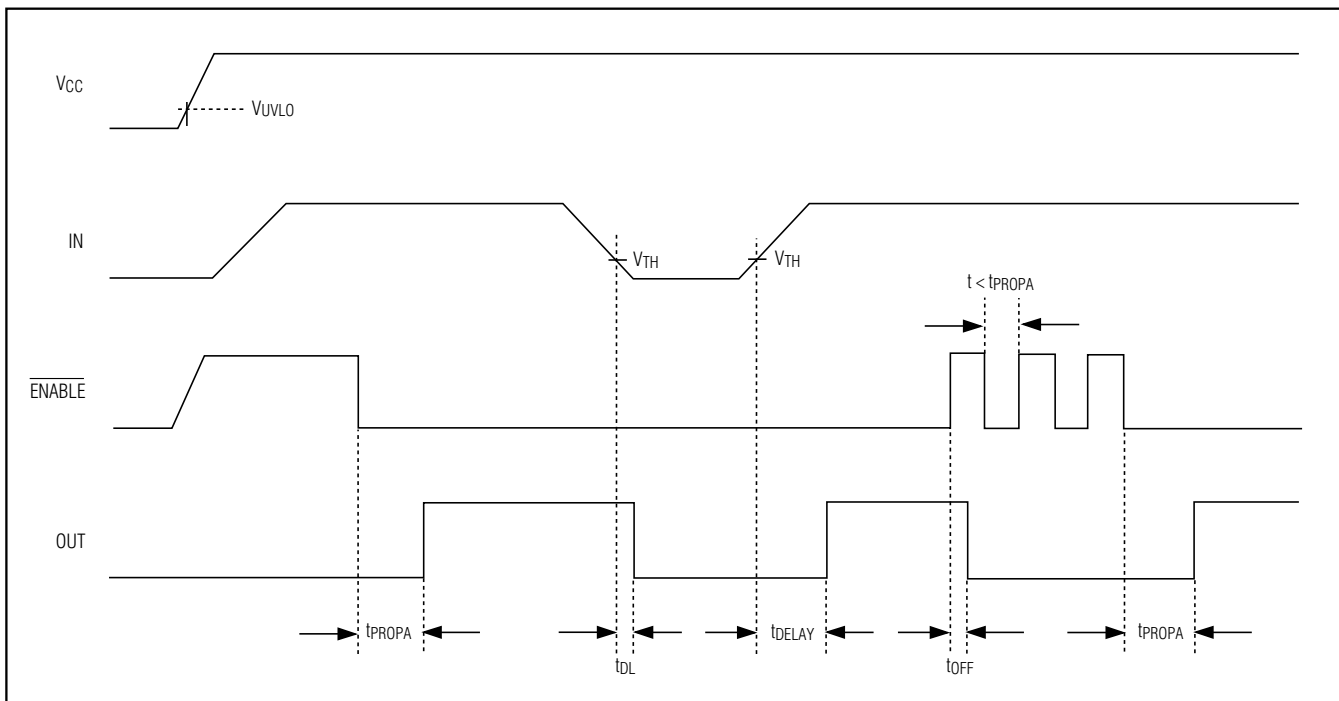


Figure 6. MAX6899A Timing Diagram

# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

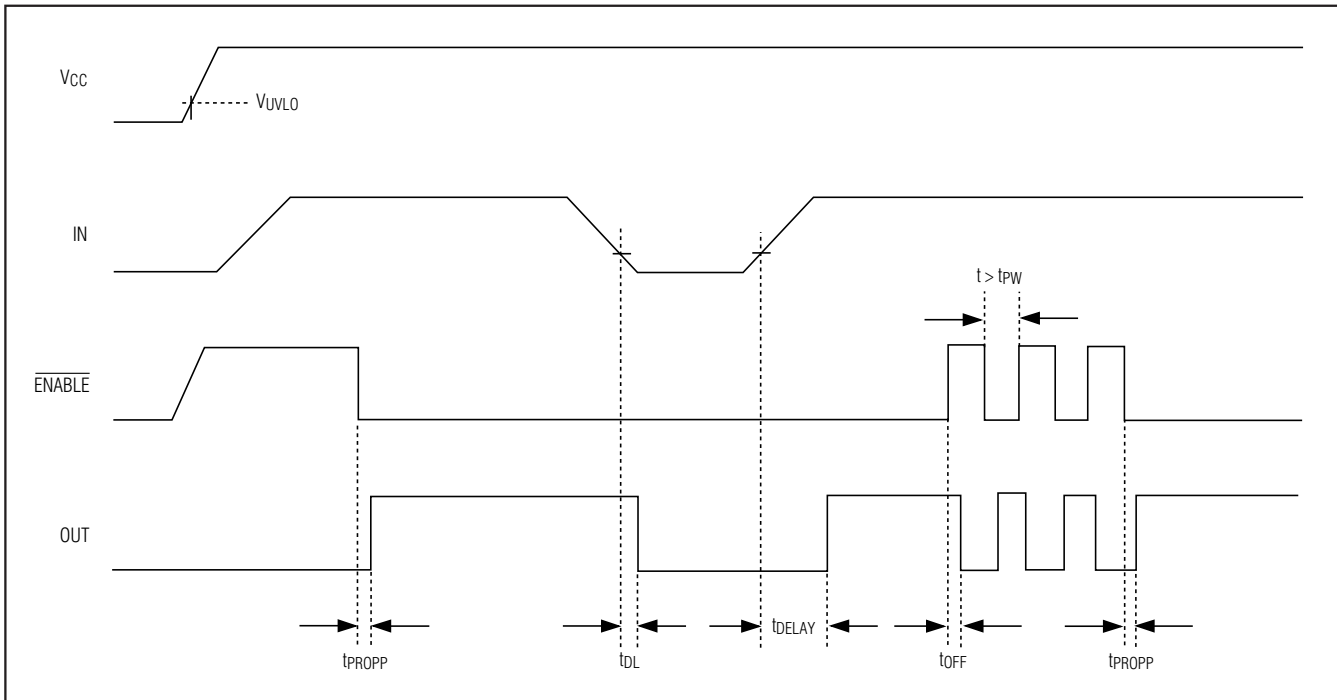


Figure 7. MAX6899P Timing Diagram

## Enable Input (ENABLE or $\overline{\text{ENABLE}}$ )

The MAX6895/MAX6897 offer an active-high enable input (ENABLE), while the MAX6896/MAX6898/MAX6899 offer an active-low enable input ( $\overline{\text{ENABLE}}$ ). With  $V_{IN}$  above  $V_{TH}$ , drive ENABLE high ( $\overline{\text{ENABLE}}$  low) to force OUT high ( $\overline{\text{OUT}}$  low) after the adjustable delay time (A versions). For P version devices, when  $V_{IN} > 0.5V$  and enable is asserted, the output asserts after typically 150ns.

The enable input has logic-high and logic-low voltage thresholds of 1.4V and 0.4V, respectively. For both versions, when  $V_{IN} > 0.5V$ , drive ENABLE low ( $\overline{\text{ENABLE}}$  high) to force OUT low ( $\overline{\text{OUT}}$  high) within 150ns typ.

## Output (OUT or $\overline{\text{OUT}}$ )

The MAX6895/MAX6899 offer an active-high, push-pull output (OUT), and the MAX6896 offers an active-low push-pull output ( $\overline{\text{OUT}}$ ). The MAX6897 offers an active-high open-drain output (OUT), and the MAX6898 offers an active-low open-drain output ( $\overline{\text{OUT}}$ ).

Push-pull output devices are referenced to  $V_{CC}$ . Open-drain outputs can be pulled up to 28V.

## Applications Information

### Input Threshold

The MAX6895–MAX6899 monitor the voltage on IN with an external resistive divider (see R1 and R2 in the *Typical Operating Circuit*). Connect R1 and R2 as close to IN as possible. R1 and R2 can have very high values to minimize current consumption due to low IN leakage currents ( $\pm 15nA$  max). Set R2 to some conveniently high value (1M $\Omega$ , for example) and calculate R1 based on the desired monitored voltage using the following formula:

$$R1 = R2 \times \left[ \frac{V_{\text{MONITOR}}}{V_{IN}} - 1 \right]$$

where  $V_{\text{MONITOR}}$  is the desired monitored voltage and  $V_{IN}$  is the detector input threshold (0.5V).

## Ultra-Small, Adjustable Sequencing/Supervisory Circuits

### Pullup Resistor Values (MAX6897/MAX6898)

The exact value of the pullup resistors for the open-drain outputs is not critical, but some consideration should be made to ensure the proper logic levels when the device is sinking current. For example, if  $V_{CC} = 2.25V$  and the pullup voltage is 28V, you would try to keep the sink current less than 0.5mA as shown in the *Electrical Characteristics* table. As a result, the pullup resistor should be greater than 56k $\Omega$ . For a 12V pullup, the resistor should be larger than 24k $\Omega$ . It should be noted that the ability to sink current is dependent on the  $V_{CC}$  supply voltage.

### Typical Application Circuits

Figures 8, 9, 10 show typical applications for the MAX6895-MAX6899. Figure 8 shows the MAX6895

used with a p-channel MOSFET in an overvoltage protection circuit. Figure 9 shows the MAX6895 in a low-voltage sequencing application using an n-channel MOSFET. Figure 10 shows the MAX6895 used in a multiple-output sequencing application.

### Using an n-Channel Device for Sequencing

In higher power applications, using an n-channel device reduces the loss across the MOSFETs as it offers a lower drain-to-source on-resistance. However, an n-channel MOSFET requires a sufficient  $V_{GS}$  voltage to fully enhance it for a low  $R_{DS(on)}$ . The application in Figure 9 shows the MAX6895 in a switch sequencing application using an n-channel MOSFET.

Similarly, if a higher voltage is present in the system, the open-drain version can be used in the same manner.

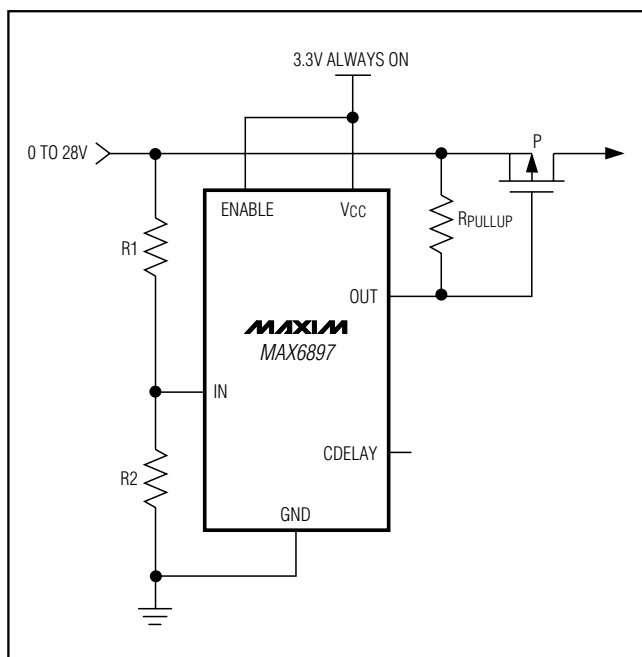


Figure 8. Overvoltage Protection

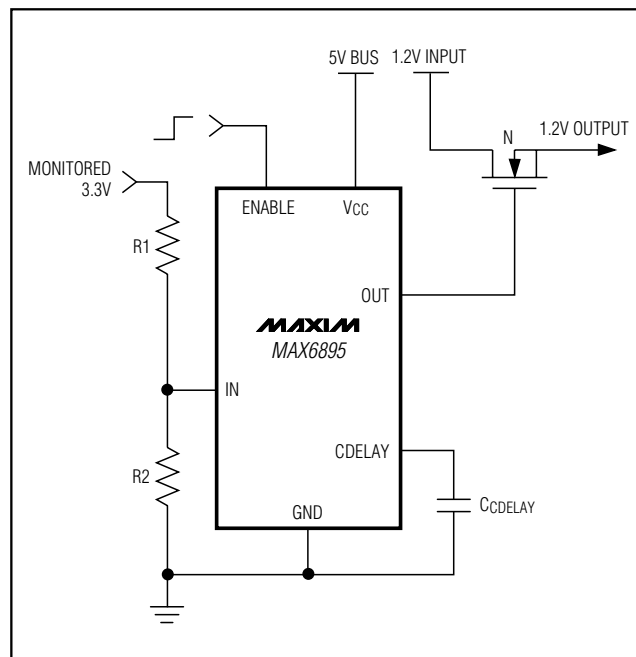


Figure 9. Low-Voltage Sequencing Using an n-Channel MOSFET

## Ultra-Small, Adjustable Sequencing/Supervisory Circuits

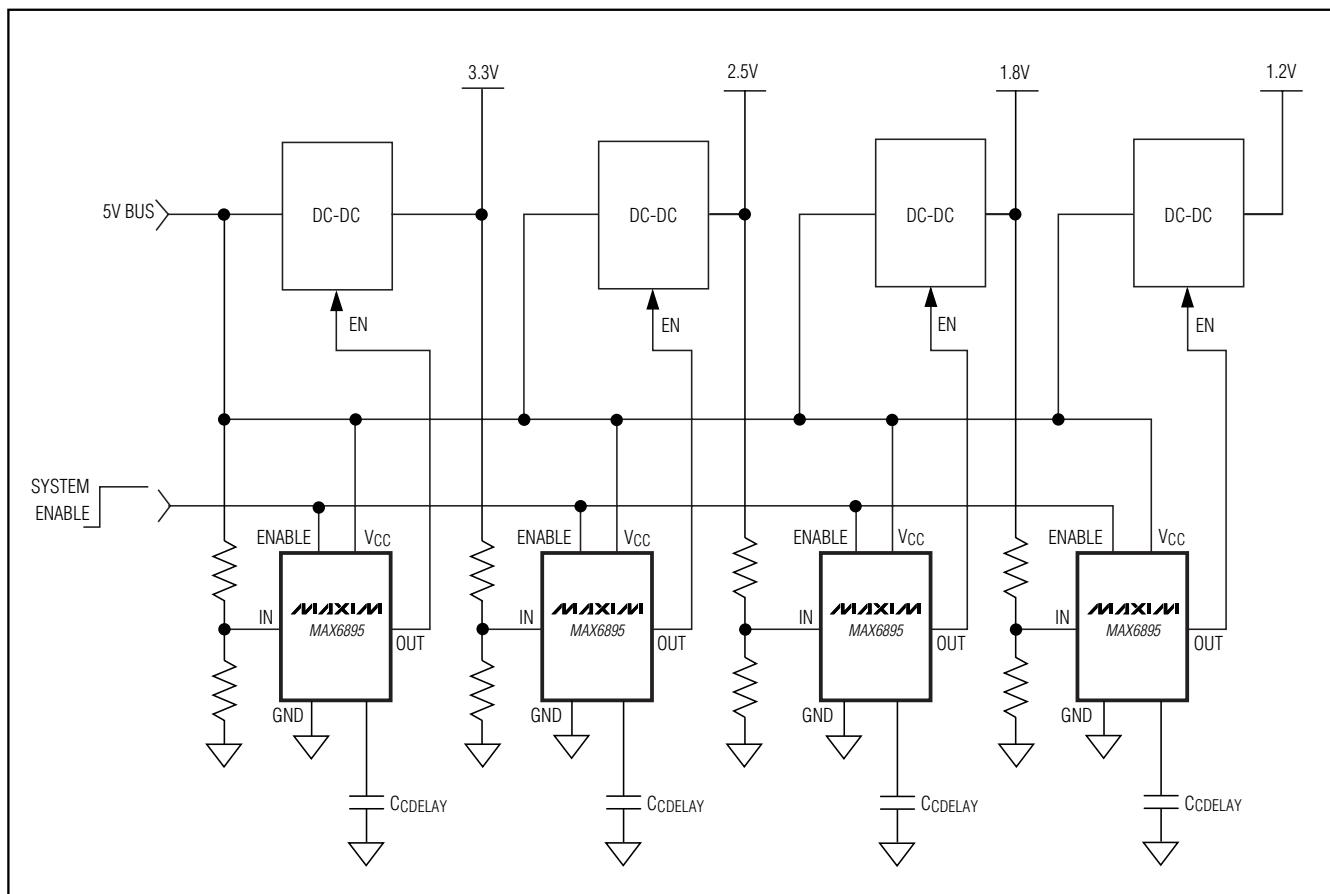


Figure 10. Multiple-Output Sequencing

# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

## Selector Guide

MAX6895-MAX6899

| PART          | ENABLE INPUT | OUTPUT                  | INPUT (IN) DELAY     | ENABLE DELAY         |
|---------------|--------------|-------------------------|----------------------|----------------------|
| MAX6895AALT+T | Active-High  | Active-High, Push-Pull  | Capacitor Adjustable | Capacitor Adjustable |
| MAX6895AAZT+T | Active-High  | Active-High, Push-Pull  | Capacitor Adjustable | Capacitor Adjustable |
| MAX6895PALT+T | Active-High  | Active-High, Push-Pull  | Capacitor Adjustable | 150ns Delay          |
| MAX6895PAZT+T | Active-High  | Active-High, Push-Pull  | Capacitor Adjustable | 150ns Delay          |
| MAX6896AALT+T | Active-Low   | Active-Low, Push-Pull   | Capacitor Adjustable | Capacitor Adjustable |
| MAX6896AAZT+T | Active-Low   | Active-Low, Push-Pull   | Capacitor Adjustable | Capacitor Adjustable |
| MAX6896PALT+T | Active-Low   | Active-Low, Push-Pull   | Capacitor Adjustable | 150ns Delay          |
| MAX6896PAZT+T | Active-Low   | Active-Low, Push-Pull   | Capacitor Adjustable | 150ns Delay          |
| MAX6897AALT+T | Active-High  | Active-High, Open-Drain | Capacitor Adjustable | Capacitor Adjustable |
| MAX6897AAZT+T | Active-High  | Active-High, Open-Drain | Capacitor Adjustable | Capacitor Adjustable |
| MAX6897PALT+T | Active-High  | Active-High, Open-Drain | Capacitor Adjustable | 150ns Delay          |
| MAX6897PAZT+T | Active-High  | Active-High, Open-Drain | Capacitor Adjustable | 150ns Delay          |
| MAX6898AALT+T | Active-Low   | Active-Low, Open-Drain  | Capacitor Adjustable | Capacitor Adjustable |
| MAX6898AAZT+T | Active-Low   | Active-Low, Open-Drain  | Capacitor Adjustable | Capacitor Adjustable |
| MAX6898PALT+T | Active-Low   | Active-Low, Open-Drain  | Capacitor Adjustable | 150ns Delay          |
| MAX6898PAZT+T | Active-Low   | Active-Low, Open-Drain  | Capacitor Adjustable | 150ns Delay          |
| MAX6899AALT+T | Active-Low   | Active-High, Push-Pull  | Capacitor Adjustable | Capacitor Adjustable |
| MAX6899AAZT+T | Active-Low   | Active-High, Push-Pull  | Capacitor Adjustable | Capacitor Adjustable |
| MAX6899PALT+T | Active-Low   | Active-High, Push-Pull  | Capacitor Adjustable | 150ns Delay          |
| MAX6899PAZT+T | Active-Low   | Active-High, Push-Pull  | Capacitor Adjustable | 150ns Delay          |

## Ordering Information (continued)

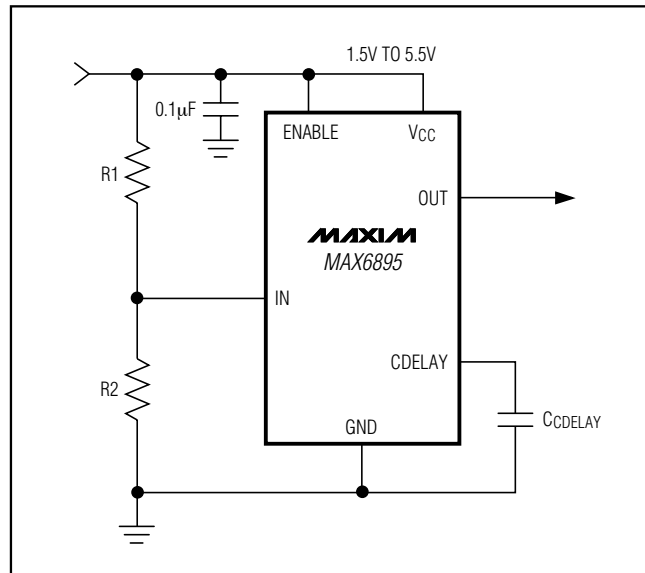
| PART          | PIN-PACKAGE    | TOP MARK | PKG CODE |
|---------------|----------------|----------|----------|
| MAX6897AALT+  | 6 $\mu$ DFN-6  | +BA      | L611-1   |
| MAX6897AAZT+  | 6 Thin SOT23-6 | +AADQ    | Z6-1     |
| MAX6897PALT+T | 6 $\mu$ DFN-6  | +BB      | L611-1   |
| MAX6897PAZT+  | 6 Thin SOT23-6 | +AADR    | Z6-1     |
| MAX6898AALT+  | 6 $\mu$ DFN-6  | +BD      | L611-1   |
| MAX6898AAZT+  | 6 Thin SOT23-6 | +AADS    | Z6-1     |
| MAX6898PALT+T | 6 $\mu$ DFN-6  | +BC      | L611-1   |
| MAX6898PAZT+  | 6 Thin SOT23-6 | +AADT    | Z6-1     |
| MAX6899AALT+  | 6 $\mu$ DFN-6  | +LO      | L611-1   |
| MAX6899AAZT+  | 6 Thin SOT23-6 | +AADM    | Z6-1     |
| MAX6899PALT+T | 6 $\mu$ DFN-6  | +LP      | L611-1   |
| MAX6899PAZT+  | 6 Thin SOT23-6 | +AADN    | Z6-1     |

**Note:** All devices are specified over the -40°C to +125°C operating temperature range.

+Denotes a lead-free package.

T = Tape and reel.

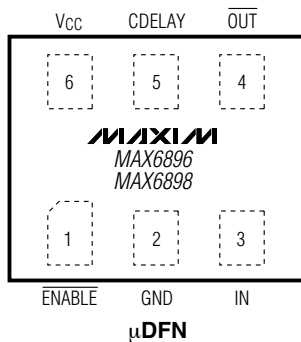
## Typical Operating Circuit



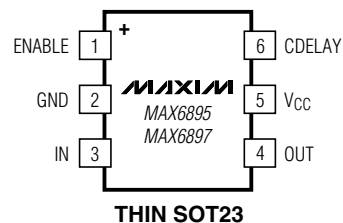
# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

## Pin Configurations (continued)

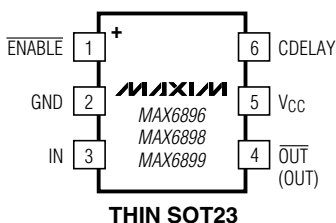
TOP VIEW



TOP VIEW



TOP VIEW



( ) FOR MAX6899 ONLY.

## Chip Information

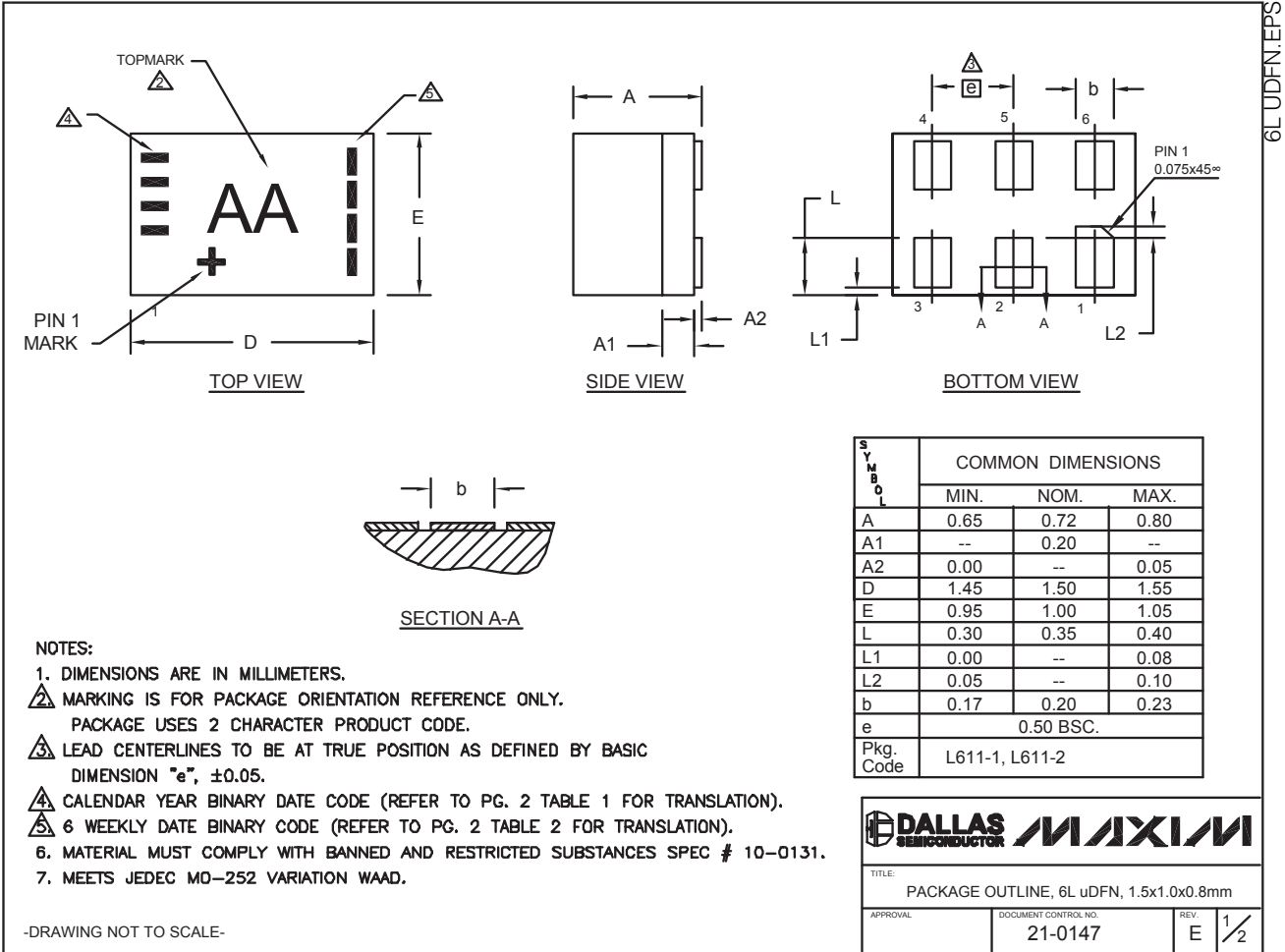
PROCESS: BiCMOS

# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX6895-MAX6899



# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

**TABLE 1** Translation Table for Calendar Year Code

| Calendar Year | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 |
|---------------|------|------|------|------|------|------|------|------|------|------|
|               |      |      |      |      |      |      |      |      |      |      |
|               |      |      |      |      |      |      |      |      |      |      |
|               |      |      |      |      |      |      |      |      |      |      |
|               |      |      |      |      |      |      |      |      |      |      |

Legend: Marked with bar Blank space - no bar required

**TABLE 2** Translation Table for Payweek Binary Coding

| Payweek | 06-11 | 12-17 | 18-23 | 24-29 | 30-35 | 36-41 | 42-47 | 48-51 | 52-05 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
|         |       |       |       |       |       |       |       |       |       |
|         |       |       |       |       |       |       |       |       |       |
|         |       |       |       |       |       |       |       |       |       |
|         |       |       |       |       |       |       |       |       |       |

Legend: Marked with bar Blank space - no bar required

|                                                               |                                                |                                        |
|---------------------------------------------------------------|------------------------------------------------|----------------------------------------|
|                                                               |                                                |                                        |
| <small>TITLE:</small> PACKAGE OUTLINE, 6L uDFN, 1.5x1.0x0.8mm |                                                |                                        |
| <small>APPROVAL</small>                                       | <small>DOCUMENT CONTROL NO.</small><br>21-0147 | <small>REV.</small><br>E $\frac{2}{2}$ |

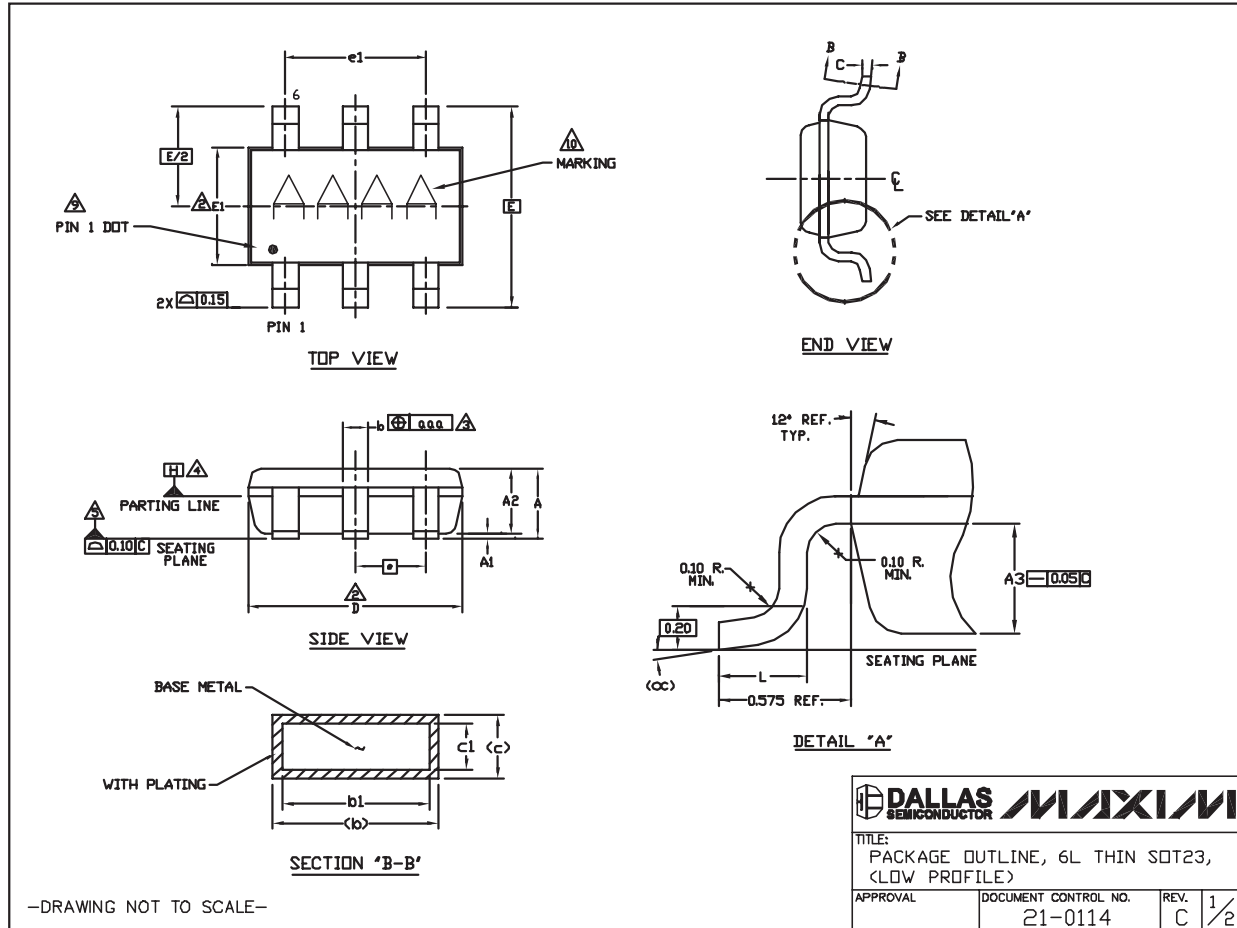
-DRAWING NOT TO SCALE-



# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



# Ultra-Small, Adjustable Sequencing/Supervisory Circuits

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

### NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. 'D' AND 'E1' ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm ON 'D' AND 0.25mm ON 'E' PER SIDE.

3. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.

4. DATUM PLANE 'H' LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.

5. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-J] AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-J] IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.10mm AT SEATING PLANE.

6. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE 'e' DIMENSION WHICH IS 0.95mm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.

7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.

8. WARPAGE SHALL NOT EXCEED 0.10mm.

9. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

11. ALL DIMENSIONS APPLY TO BOTH LEADED (<->) AND LEAD FREE (<+>) PACKAGE CODES.

### SYMBOLS

|                        | MIN      | NOM   | MAX  |
|------------------------|----------|-------|------|
| A                      | -        | -     | 1.10 |
| A1                     | 0.00     | 0.075 | 0.10 |
| A2                     | 0.85     | 0.88  | 0.90 |
| A3                     | 0.50 BSC |       |      |
| b                      | 0.30     | -     | 0.45 |
| b1                     | 0.25     | 0.35  | 0.40 |
| c                      | 0.15     | -     | 0.20 |
| c1                     | 0.12     | 0.127 | 0.15 |
| D                      | 2.80     | 2.90  | 3.00 |
| E                      | 2.75 BSC |       |      |
| E1                     | 1.55     | 1.60  | 1.65 |
| L                      | 0.30     | 0.40  | 0.50 |
| e1                     | 1.90 BSC |       |      |
| e                      | 0.95 BSC |       |      |
| OC                     | 0°       | 4°    | 8°   |
| aaa                    | 0.20     |       |      |
| Pkg. codes: Z6-1J Z6-2 |          |       |      |

-DRAWING NOT TO SCALE-

|                                                                                       |                                 |
|---------------------------------------------------------------------------------------|---------------------------------|
|  |                                 |
| TITLE:<br>PACKAGE OUTLINE, 6L THIN SOT23,<br>(LOW PROFILE)                            |                                 |
| APPROVAL                                                                              | DOCUMENT CONTROL NO.<br>21-0114 |
| REV. C                                                                                | 2/2                             |

## Revision History

Pages changed at Rev 3: 1, 3, 5, 6, 9, 10, 11, 13, new part number added (all pages)

Pages changed at Rev 4: 1, 2, 5, 7, 12-18

Pages changed at Rev 5: 1, 13, 18

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

18 **Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600**

© 2007 Maxim Integrated Products

**MAXIM** is a registered trademark of Maxim Integrated Products, Inc.