MCDP2900

DisplayPort1.4 to HDMI2.0a protocol converter with HDCP2.2 repeater

Datasheet

Rev. A

MegaChips

MegaChips' Proprietary Information

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  - Programmable input offset
  - Programmable output offset
  - Programmable output clipping levels
- Chroma Down Sampling
  - 5-tap H & V FIR filters with programmable coefficients
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  - 12 bits per color output width
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  - 4Kp60Hz, RGB/YCbCr444, 8 bpc
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  - 4Kp60Hz, YCbCr420, up to 16 bpc
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  - Read-protected embedded HDCP keys
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- Device configuration options
  - 8Mbit SPI flash for firmware binary image storage
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  - Configurable through DPCD registers
- EMI reduction support
  - Spread spectrum for DP input
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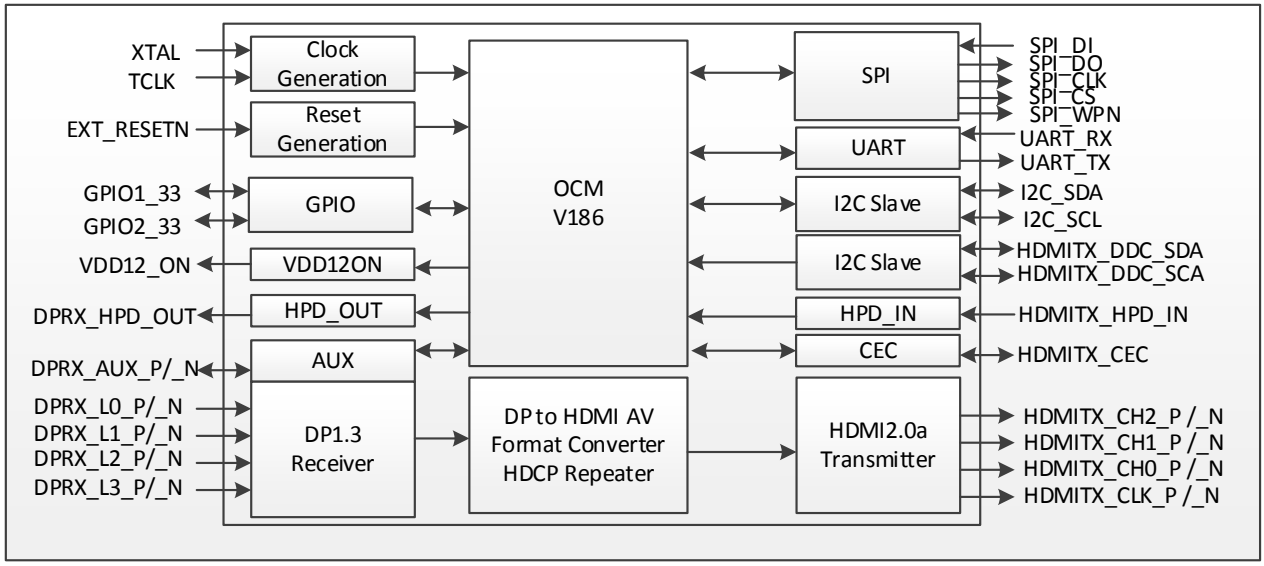
- Low power operation
  - 570 mW in protocol converter operation
  - 11 mW sleep mode operation
  - 4 mW in Connected Standby operation
- ESD specification
  - ESD: +/-2 KV HBM, 500 V CDM
  - ESD: +/-6.5 KV HBM connector facing pins
- Package
  - 64 LFBGA (7 x 7 mm)
- Power supply voltages
  - 3.3 V I/O; 1.2 V core

Applications

- Notebook, Tablet Accessories (USB Type-C dongles, docking stations)
- TV, Signage, Game consoles, STB

Figure 1. MCDP2900 block diagram



1. Description

The MCDP2900 is a power-optimized DisplayPort1.4-to-HDMI2.0a converter, targeted for enabling USB Type-C DP Alt mode on TVs, Game consoles and other consumer equipment as well as for mobile PC and tablet accessory applications. This device functions as an active protocol converter with HDCP1.x/ HDCP2.2 repeater supporting HDR video quality for deep color media content playback.

MCDP2900 behaves as a DP branch device with a DP-to-HDMI transport protocol converter function and allows a DP or USB Type-C source to drive an HDMI2.0a sink device. The maximum TMDS character clock frequency supported is 600 Mchar/s (per HDMI2.0a specification).

The MCDP2900 operates with two power supply voltages: 1.2 V and 3.3 V. It consumes:

- 570 mW in protocol converter operation
- 11 mW sleep mode operation
- 4 mW in connected standby mode operation

The MCDP2900 has a DP1.4 receiver and an HDMI2.0a transmitter. The DP receiver supports up to 5.4Gbps/lane over 4 lanes. It supports DP SST transport format on its main link and Manchester-coded AUX signaling as the side band channel. The downstream HDMI TX port is HDMI2.0a specification compliant.

The MCDP2900 is capable of supporting Ultra High-Definition video formats with resolutions as high as 4096 x 2160 progressive @ 60 Hz (4K2Kp60Hz). It supports RGB/YCbCr video color formats with a color depth of 16 bpc (bits per component or 48 bits per pixel) as long as it fits within the DP and HDMI link bandwidth. This device also supports pixel encoding conversion from RGB or YCbCr444 to YCbCr420 and a YcbCr420 pass-through function. In addition, High Dynamic Range (HDR) with deep color up to 12bpc at 4Kp60Hz is supported through the conversion of RGB/YCbCr444 over DP link to YCbCr420 on the HDMI output with a horizontal expansion to CEA timings.

This device offers secure reception and transmission of high bandwidth digital audio and video content with HDCP1.3 and HDCP2.2 content protection for the upstream DP interface. It also has a repeater function for HDCP1.4 and HDCP2.2 for the downstream HDMI interface.

The MCDP2900 uses an external crystal of 27 MHz as a reference clock for its operation. An internal Power On Reset (POR) circuit senses the voltage on the reset input and provides the chip reset during system power-up. The device has an internal microcontroller with SPI, UART (debug only), and I2C system interface signals. It uses an external 8Mbit SPI flash memory for storing a secure signed firmware image with fail-safe recovery. Firmware updates of the SPI flash are done securely through the DP AUX_CH or I2C, depending on the application.

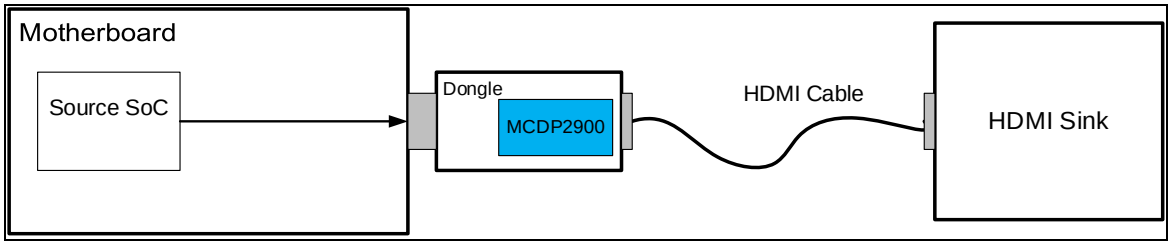
2. Application overview

The target applications of MCDP2900 are the notebook, tablet accessories i.e., adaptors (dongles), docking stations and other AV accessories. MCDP2900 is also intended for enabling USB Type-C DP alternative mode for inside-the-box applications such as TVs, game consoles and other consumer equipment.

2.1. Adaptor application

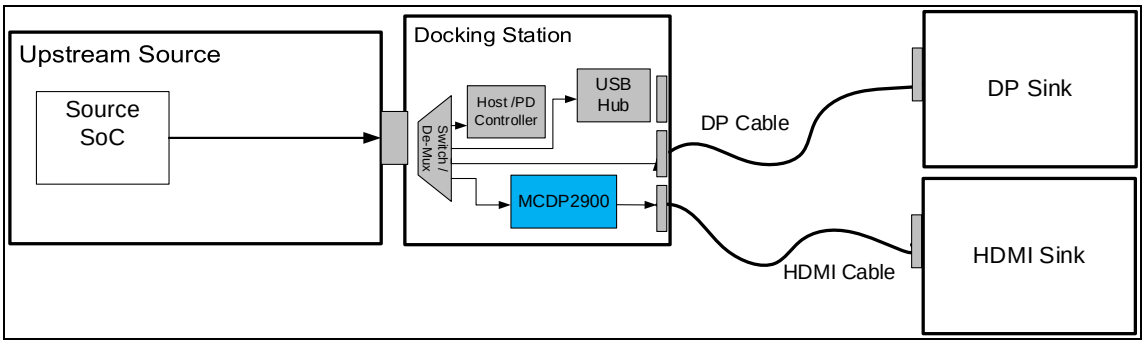
In a dongle topology the MCDP2900 is part of the source side adaptor that plugs into a DP source device via a DisplayPort connector (e.g. full-size DP or mini-DP receptacle or USB-Type-C Alt-Mode receptacle on the upstream facing port). In the conventional DP-to-HDMI dongle application, MCDP2900 functions as a system master and operates as a protocol converter, an HDCP1.x repeater or an HDCP2.2 repeater. In a Type-C dongle design, a PD controller functions as the system master. The upstream source typically powers the dongle.

Figure 2. MCDP2900 adaptor (dongle) use case



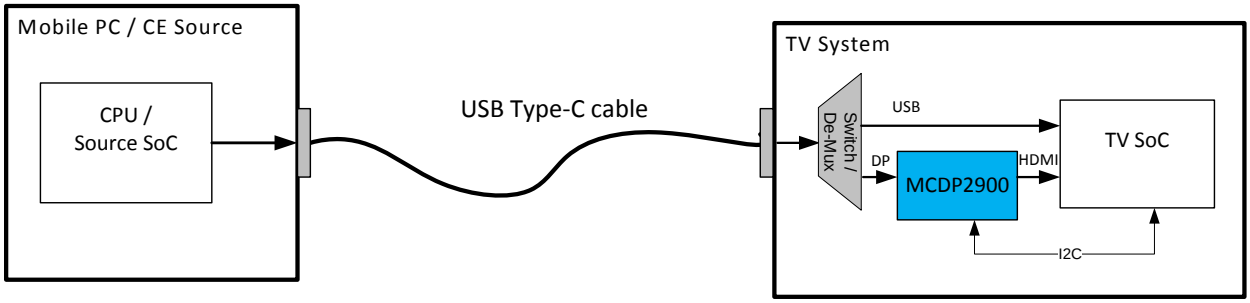
2.2. Docking station application

In a docking station topology, the MCDP2900 is part of a larger system into which a DP source device plugs in via a custom connector or USB-Type-C Alt-Mode receptacle on the upstream facing port. In a docking station design the MCDP2900 typically co-exists with other system components such as the system host or PD controller, AV switch, and USB hub. In this application, the MCDP2900 functions as a protocol converter, an HDCP1.x repeater, or an HDCP2.2 repeater.



2.3. TV Application

A TV system featuring the USB Type-C connector supporting the DP Alt-mode requires a DP-to-HDMI protocol converter. The MCDP2900 is an ideal fit for such applications; it supports video resolution up to 4K60Hz with HDR video quality for deep color media playback, end-to-end HDCP2.2 content protection, and CEC tunneling over DP for single-point remote-control access for all connected devices.

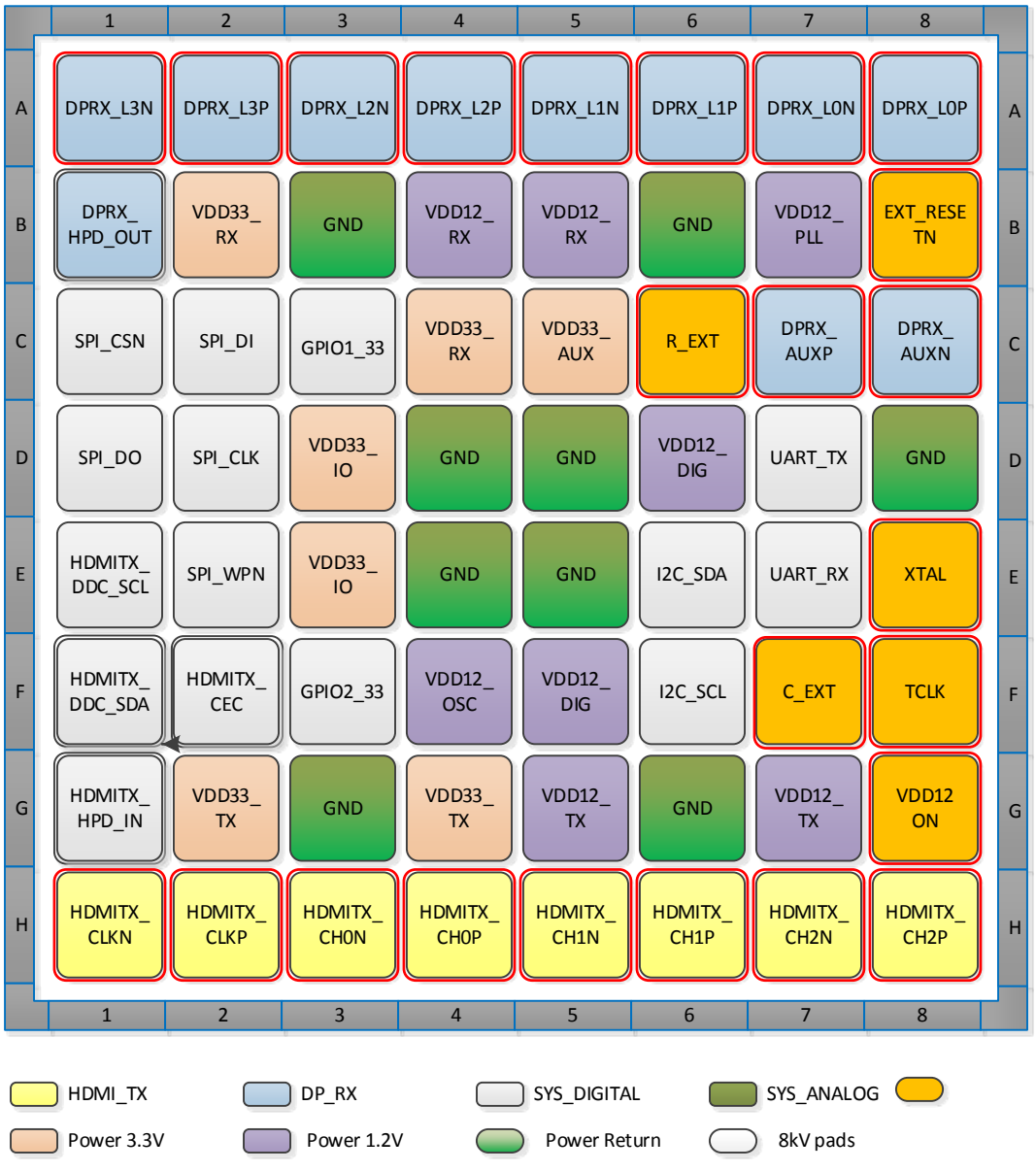


3. BGA footprints and pin list

The ball grid array (BGA) diagrams give the allocation of pins to the package, shown from the top looking down using the PCB footprint.

Some signal names in BGA diagrams have been abbreviated. Refer to the pin list for full signal names sorted by pin number.

Figure 3. MCDP2900 BGA diagram



Reference: bobcat_pinlist_ballmap.xlsx revision 1r5 dated June 3, 2013

3.1. Signal mapping sorted by ball (pin) number

Table 1. Pin list

Pin number	Net name
A1	DPRX_L3N
A2	DPRX_L3P
A3	DPRX_L2N
A4	DPRX_L2P
A5	DPRX_L1N
A6	DPRX_L1P
A7	DPRX_L0N
A8	DPRX_L0P
B1	DPRX_HPD_OUT
B2	VDD33_RX
B3	GND
B4	VDD12_RX
B5	VDD12_RX
B6	GND
B7	VDD12_PLL
B8	EXT_RESETN
C1	SPI_CSN
C2	SPI_DI
C3	GPIO1_33
C4	VDD33_RX

Pin number	Net name
C5	VDD33_AUX
C6	R_EXT
C7	DPRX_AUXP
C8	DPRX_AUXN
D1	SPI_DO
D2	SPI_CLK
D3	VDD33_IO
D4	GND
D5	GND
D6	VDD12_DIG
D7	UART_TX
D8	GND
E1	HDMITX_DDC_SCL
E2	SPI_WPN
E3	VDD33_IO
E4	GND
E5	GND
E6	I2C_SDA
E7	UART_RX
E8	XTAL
F1	HDMITX_DDC_SDA
F2	HDMITX_CEC
F3	GPIO2_33

Pin number	Net name
F4	VDD12_OSC
F5	VDD12_DIG
F6	I2C_SCL
F7	C_EXT
F8	TCLK
G1	HDMITX_HPD_IN
G2	VDD33_TX
G3	GND
G4	VDD33_TX
G5	VDD12_TX
G6	GND
G7	VDD12_TX
G8	VDD12ON
H1	HDMITX_CLKN
H2	HDMITX_CLKP
H3	HDMITX_CH0N
H4	HDMITX_CH0P
H5	HDMITX_CH1N
H6	HDMITX_CH1P
H7	HDMITX_CH2N
H8	HDMITX_CH2P

4. Connections

4.1. Pin list

I/O Legend: I = Input; O = Output; P = Power; G = Ground; I/O = Bi-direction; AI = Analog Input

Note: Some pins can have multiple functionalities, which are configured under register control. The alternate functionality for each pin is listed in the Description column.

Table 2. DisplayPort receiver pins

Pin	Assignment	I/O	VDD Domain	Description
A1	DPRX_L3N	I	1.2V	DisplayPort receiver main link Lane 3 negative analog input. Main Link receiver pins (DPRX_LxN or DPRX_LxP where N = 0 ~ 3) and AUX CH pins of MCDP2900 are internally terminated to 1.2V power rail. Therefore external AC-coupling capacitors are required for DPRX Main LInk and AUX CH pins.
A2	DPRX_L3P	I	1.2V	DisplayPort receiver main link Lane 3 positive analog input.
A3	DPRX_L2N	I	1.2V	DisplayPort receiver main link Lane 2 negative analog input.
A4	DPRX_L2P	I	1.2V	DisplayPort receiver main link Lane 2 positive analog input.
A5	DPRX_L1N	I	1.2V	DisplayPort receiver main link Lane 1 negative analog input.
A6	DPRX_L1P	I	1.2V	DisplayPort receiver main link Lane 1 positive analog input.
A7	DPRX_L0N	I	1.2V	DisplayPort receiver main link Lane 0 negative analog input.
A8	DPRX_L0P	I	1.2V	DisplayPort receiver main link Lane 0 positive analog input.
C7	DPRX_AUXP	I/O	3.3V	DisplayPort receiver auxiliary channel positive analog input/output.
C8	DPRX_AUXN	I/O	3.3V	DisplayPort receiver auxiliary channel negative analog input/output.
B1	DPRX_HPD_OUT	O	3.3V	To the upstream HPD signal pin (DP source), to be externally pulled down (100K Ω).

Pin	Assignment	I/O	VDD Domain	Description
C6	R_EXT	I/O	1.2V	Termination calibration reference resistor; 249 Ω 1% resistor must be connected from this pin to VDD12_RX.

Table 3. HDMI output pins

Pin	Assignment	I/O	VDD Domain	Description
H1	HDMITX_CLKN	O	3.3V	HDMI transmitter CLOCK_N to TX connector.
H2	HDMITX_CLKP	O	3.3V	HDMI transmitter CLOCK_P to TX connector.
H3	HDMITX_CH0N	O	3.3V	HDMI transmitter DATA0_N to TX connector.
H4	HDMITX_CH0P	O	3.3V	HDMI transmitter DATA0_P to TX connector.
H5	HDMITX_CH1N	O	3.3V	HDMI transmitter DATA1_N to TX connector.
H6	HDMITX_CH1P	O	3.3V	HDMI transmitter DATA1_P to TX connector.
H7	HDMITX_CH2N	O	3.3V	HDMI transmitter DATA2_N to TX connector.
H8	HDMITX_CH2P	O	3.3V	HDMI transmitter DATA2_P to TX connector.
E1	HDMI_DDC_SCL	O	3.3V, 5V TOL	HDMI TX DDC I2C master SCL. 3.3 V logic level, 5 V tolerant. Open drain, to be externally pulled up to DDC5V via a 1.5K ~ 2.2K Ω resistor.
F1	HDMI_DDC_SDA	I/O	3.3V, 5V TOL	HDMI TX DDC I2C master SDA. 3.3 V logic level, 5 V tolerant. Open drain, to be externally pulled up to DDC5V via a 1.5K ~ 2.2K Ω resistor.
F2	HDMITX_CEC	I/O	3.3V, 5V TOL	CEC input. 3.3 V open drain IO. Connect to HDMI CEC pin, to be externally pulled up to 3.3 V via 27K Ω resistor as per HDMI1.4b specification. Use external 27K Ω pull up when CEC is not used.

Pin	Assignment	I/O	VDD Domain	Description
G1	HDMITX_HDP_IN	I	3.3V, 5V TOL	3.3 V logic level, 5 V tolerant input from HDMI connector. To be externally pulled down via 20K Ω resistor.

Note: HDMI TX output is terminated at the receiver through a 50 ohm resistor.

Table 4. System interface pins

Pin	Assignment	I/O	VDD Domain	Reset State	Description
B8	EXT_RESETN	I	3.3 V	Input	Power-ON chip reset (active low) input signal, to be pulled up to 3.3V power rail via 2.2K Ω +/- 10% resistor as shown in Figure 8.
E8	XTAL	I/O	1.2V	NA	Connect to 27MHz crystal with 22pF to VDD12_OSC as shown in figure 5.
F8	TCLK	I/O	1.2V	NA	Connect to 27 MHz crystal with 22pF to VDD12_OSC as shown in Figure 5.
F7	C_EXT	O	3.3V	NA	Capacitor for filtering internal 2.5V LDOR. Connect to GND through 2.2uF capacitor.
G8	VDD12ON	O	3.3 V	Logic 1, output	1.2V power control signal to control external 1.2V power as shown in figure 1. Reset State definition assumes 3.3V Rail is ramped up to full voltage. Currently VDD12ON is not used.
E6	I2C_SDA	IO	3.3 V	Input, Internal PU	Host I2C interface data line up to 400kbps. Programmable Slew Rate and Drive Strength when this is being used as a GPIO.
F6	I2C_SCL	I	3.3 V	Input, internal PU	Host I2C interface clock line up to 400 kbps. Programmable Slew Rate and Drive Strength when this is being used as a GPIO.
C3	GPIO1_33	IO	3.3 V	Input, Internal PD	3.3V General purpose input/output with programmable slew rate and drive control. Internal PD 50K Ohm.
F3	GPIO2_33	I/O	3.3V	Input, internal PD	3.3V General purpose input/output with programmable slew rate and drive control. Internal PD 50K Ohm.
C1	SPI_CSN	O	3.3 V	Input, Internal PU	Serial peripheral interface chip select. Programmable Slew Rate and Drive Strength.
C2	SPI_DI	I	3.3 V	Input, Internal PD	Serial peripheral interface data input.
D1	SPI_DO	O	3.3 V	Input, Internal PD	Serial peripheral interface data output. Programmable Slew Rate and Drive Strength.

Pin	Assignment	I/O	VDD Domain	Reset State	Description
D2	SPI_CLK	O	3.3 V	Input, Internal PD	Serial peripheral interface clock. Programmable Slew Rate and Drive Strength.
E2	SPI_WPN	O	3.3 V	Input, Internal PU	Serial peripheral interface write protect. Programmable Slew Rate and Drive Strength.
D7	UART_TX	O	3.3 V	Input, Internal PU	Universal asynchronous serial Tx output. Programmable Slew Rate and Drive Strength.
E7	UART_RX	I	3.3 V	Input, Internal PU	Universal asynchronous serial Rx input. Internal PU can be changed to Internal PD by register program.

Table 5. Power and ground pins

Pin	Assignment	Voltage Level	Description
B2, C4	VDD33_RX	3.3 V	DisplayPort RX analog power
B4, B5	VDD12_RX	1.2 V	DisplayPort RX analog power
C5	VDD33_AUX	3.3 V	DisplayPort AUX power
B7	VDD12_PLL	1.2 V	PLL analog power
F4	VDD12_OSC	1.2 V	Oscillator circuit power
G2, G4	VDD33_TX	3.3 V	HDMI TX analog power
G5, G7	VDD12_TX	1.2 V	HDMI TX analog power
D6, F5	VDD12_DIG	1.2 V	Core and 1.2V IO power
D3, E3	VDD33_IO	3.3 V	3.3V IO power
B3, B6, D4, D5, E4, E5, G3, G6, D8	GND	GND	Power return for all supplies

4.2. Bootstrap configuration

DC levels on the bootstrap pins shown below are latched during the de-asserting edge of power-on reset (EXT_RESETN goes HIGH). The levels specified below must be adhered to for the normal function of the device.

Table 6. Bootstrap configuration

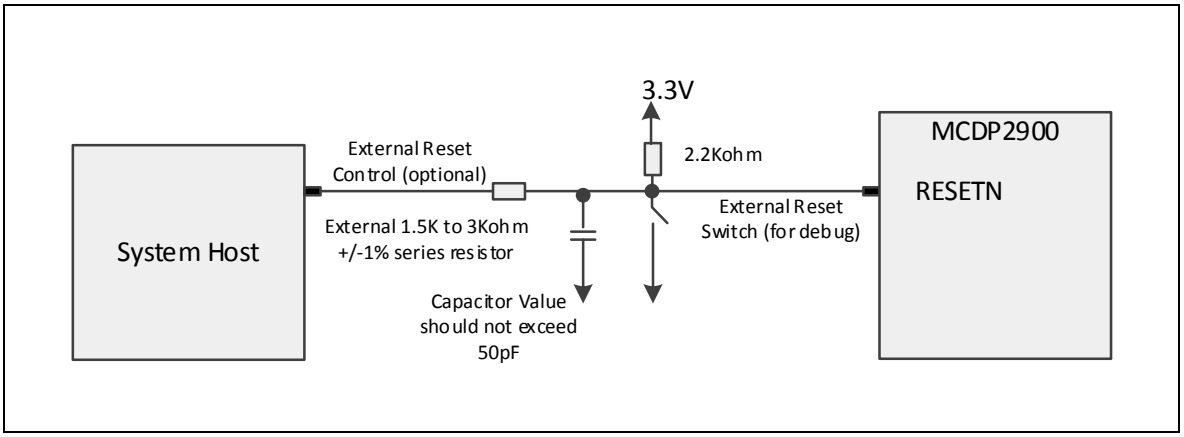
Bootstrap signal name	Internal PU/PD	Assignment	Function
Bootstrap '0'	PULLUP	UART_TX (D7)	RESERVED. Leave as NC.
Bootstrap '1'	PULLUP	SPI_WPN (E2)	RESERVED. Leave as NC.
Bootstrap '2'	PULLDN	SPI_CLK (D2)	RESERVED. Leave as NC.
Bootstrap '3'	PULLDN	SPI_DO (D1)	RESERVED. Leave as NC.
Bootstrap '4'	PULLUP	SPI_CSN (C1)	RESERVED. Leave as NC.
Bootstrap '5'	PULLDN	GPIO1_33 (C3)	Can be used for customized application configuration.
Bootstrap '6'	PULLDN	GPIO2_33 (F3)	Can be used for customized application configuration.

Note: When the pin corresponding to a specific bootstrap is left NC, the pin takes the value of the assigned by the internal PULLUP (Level 1) or PULLDN (Level 0). The internal resistor used is around 50 k Ω. To select a non-default value on a bootstrap, an external PULLUP or PULLDN resistor tied to the opposite direction that overcomes the internal PULLUP or PULLDN needs to be used.

4.3. EXT_RESETN connection

The EXT_RESETN pin must be pulled up to 3.3 V via a 2.2 Kohm +/- 10% resistor as shown below. The chip also supports an active low, external reset pulse to EXT_RESETN allowing a system host controller to reset the system. The recommended way to drive EXT_RESETN is through an open-drain output. Alternately, if an open-drain output is not available, the series resistor shown in the figure below is required.

Figure 4. EXT_RESETN Connection to MCDP2900

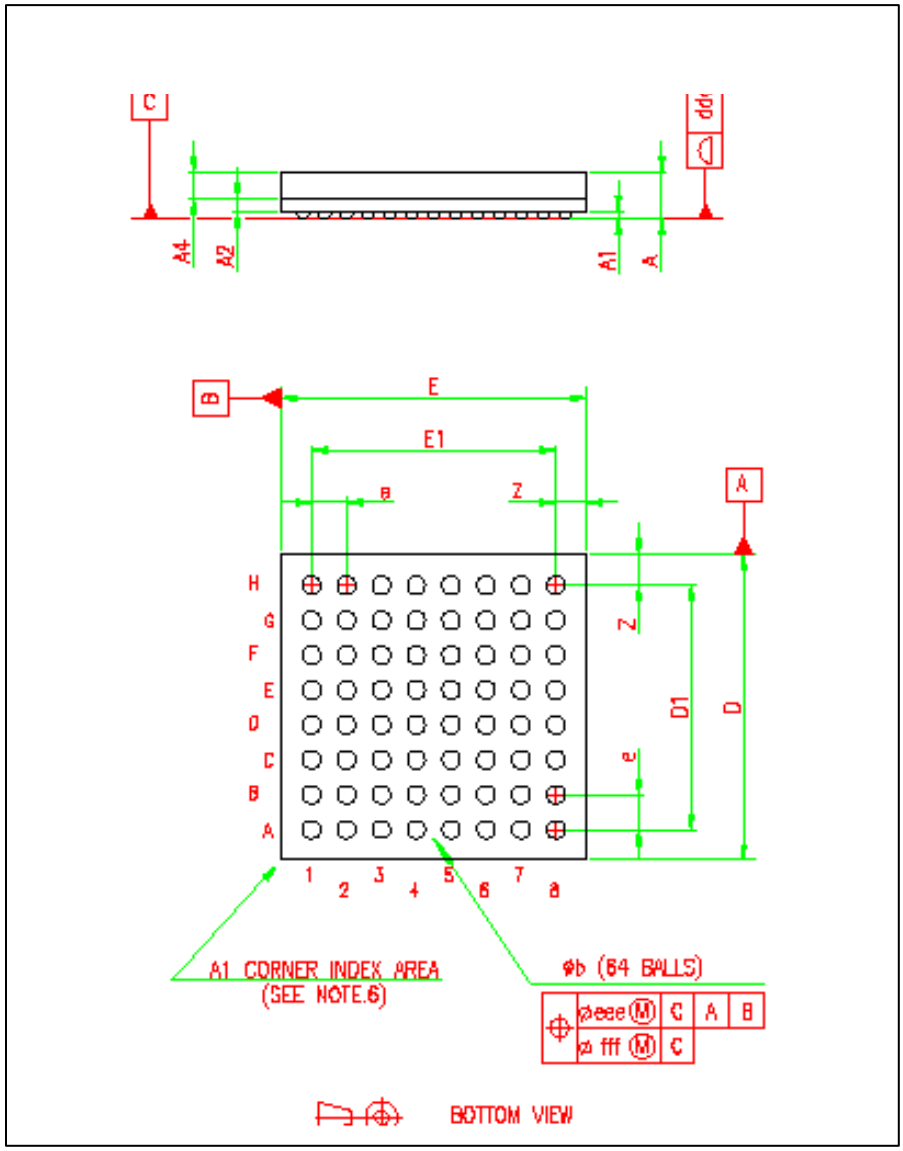


5. Package

Package type: LFBGA (7x7x1.4 mm, 64, F8x8, Pitch 0.8, Ball 0.4)

5.1. Package drawing

Figure 5. MCDP2900 package drawing



5.2. LFBGA 7 x 7 dimensions

Table 7. MCDP2900 package dimensions

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A			1.4			1.24	(1)
A1	0.25			0.25	0.30	0.35	
A2		0.29		0.24	0.28	0.32	
A4			0.60	0.57	0.585	0.60	
b	0.35	0.40	0.45	0.35	0.40	0.45	(2)
D	6.95	7.00	7.05	6.95	7.00	7.05	
D1		5.60			5.60		
E	6.95	7.00	7.05	6.95	7.00	7.05	
E1		5.60			5.60		
e		0.80			0.80		
Z		0.70			0.70		
ddd			0.08			0.08	
eee			0.09			0.09	(4)
fff			0.05			0.05	(5)

NOTES:

(1) - LFBGA stands for Low profile Fine Pitch Ball Grid Array.
- Thin profile: 1.00mm < A ≤ 1.20mm / Fine pitch: e < 1.00mm pitch.
- The total profile height (Dim A) is measured from the seating plane to the top of the component
- The maximum total package height is calculated by the following methodology:
A Max = A1 Typ + A2 Typ + A4 Typ +√ ($A1^2$ + $A2^2$ + $A4^2$ tolerance values)

(2) – The typical ball diameter before mounting is 0.40mm.

(3) – LFBGA with 0.40mm pitch is not yet registered into JEDEC Publications.

(4) - The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

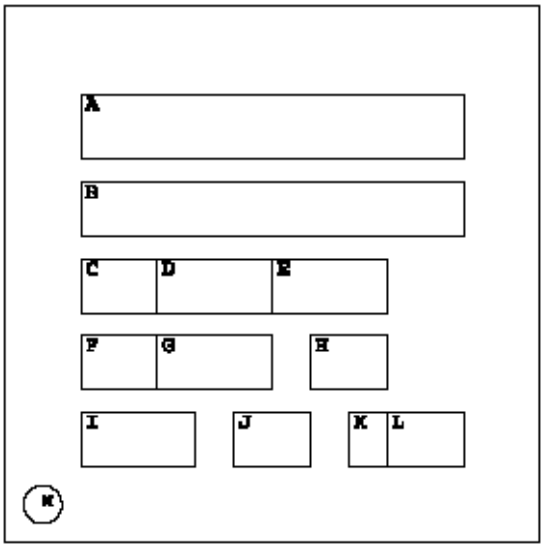
(5) - The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.

(6) - The terminal A1 corner must be identified on the top surface by using a corner chamfer, Ink or metallized markings, or other feature of package body or integral heatslug.
- A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

5.4. Marking field template and descriptors

The MCDP2900 marking template is shown below:

Figure 6. Marking template



Field descriptors are shown below.

Table 8. Field descriptors

Field	Description	Marking
A	Standard MegaChips logo	MegaChips
B	Product code	MCDP2900A2
C	2-character diffusion plant code	VQ
D	3-digit wafer start date	“YWW”
E	3-character FE sequence code	“ABC”
F	2-character assembly plant code	99
G	3-character BE sequence code	“XYZ”
H	Optional marking	FX or <blank>
I	3-character country of origin code	MYS
J	2-character test plant code	8U
K	1-digit assembly year	“Y”
L	2-digit assembly week	“WW”
M	Ball A1 identifier	a DOT

5.5. Classification reflow profile

Please refer to the DisplayPort Application Note: Classification reflow profile for SMD devices (C0353-APN-06) for reflow diagram and details.

6. Electrical specifications

6.1. Absolute maximum ratings

Applied conditions greater than those listed under “Absolute maximum ratings”, may cause permanent damage to the device. The device should never exceed absolute maximum conditions since it may affect device reliability.

Table 9. Absolute maximum ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3 V supply voltages (1,2)	$V_{VDD\_3.3}$	-0.3	3.3	3.96	V
1.2 V supply voltages (1.2)	$V_{VDD\_1.2}$	-0.3	1.2	1.44	V
Input voltage tolerance for 3.3 V, 5 V tolerant I/O pins	V_{IN5tol}	-0.3		5.5	V
Input voltage tolerance for 3.3 V I/O pins	V_{IN3V3}	-0.3		3.75	V
ESD – Human Body Model (HBM)[JESD22-A114 spec] For all pins	V_{ESD}	-	-	+/- 2.0	kV
ESD – Human Body Model (HBM) [IEC61000-4 spec] For DP and HDMI connector-facing pins	V_{ESD}	-	-	+/- 6.5	kV
ESD – Charged Device Model (CDM) [JESD22-C101 spec]	V_{ESD}	-	-	+/- 500	V
Latch-up [JESD78 spec]	I_{LA}	-	-	+/- 100	mA
Ambient operating temperature	T_A	0	-	70	°C
Storage temperature	T_{STG}	-40	-	150	°C
Operating junction temperature	T_J	0	75	125	°C
Thermal resistance (Junction to Ambient)(3)	θ_{JA}	-	-	37.6	°C/W
Thermal resistance (Junction to Case)(3)	θ_{JC}	-	-	18.8	°C/W
Peak IR reflow soldering temperature	T_{SOL}	-	-	260	°C

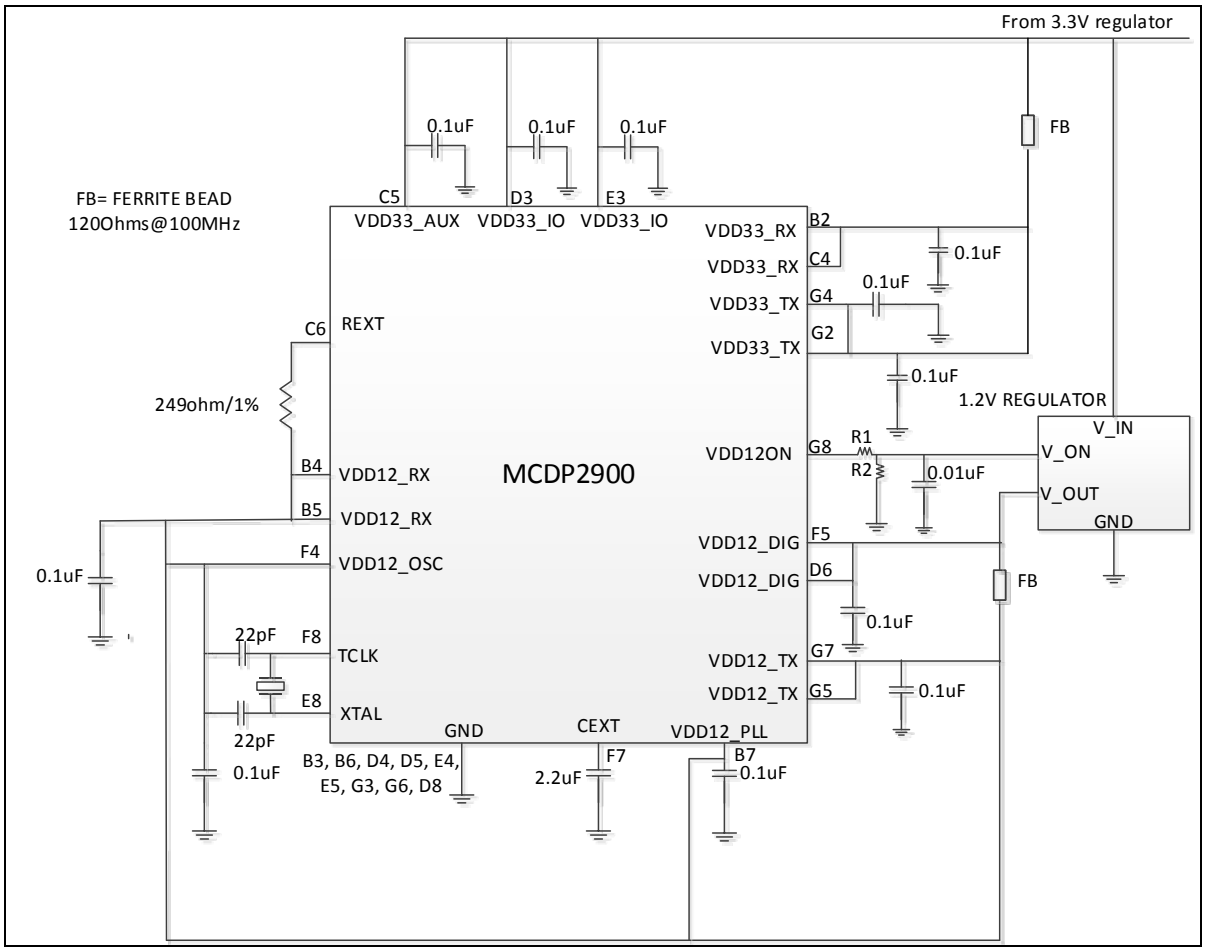
Note 1: All voltages are measured with respect to GND.

Note 2: Absolute maximum voltage ranges are for transient voltage excursions.

Note 3: These are simulated results under the following conditions – Four layer JEDEC PCB, no heat spreader, Air flow = 0 m/s.

6.2. Power connections

Figure 7. Recommended Power supply connections for MCDP2900



6.3. DC characteristics

Table 10. DC characteristics

Parameter	Symbol	Min	Typ	Max	Units
3.3 V supply voltages (analog and digital)	$V_{VDD\_1.8}$	3.14	3.3	3.47	V
1.2 V supply voltages (analog and digital)	$V_{VDD\_1.2}$	1.14	1.2	1.26	V
Power					
Protocol converter Mode Measurement condition: Nominal corner, 25°C, Nominal power supply 4k x 2k / 60 Hz 4L HBR2-to-HDMI test pattern: ON-OFF			482	570	mW
4k x 2k / 30 Hz 4L HBR2-to-HDMI test pattern: ON-OFF			413	480	mW
1920 x 1080 / 60 Hz 4L HBR2-to-HDMI test pattern: ON-OFF			380	440	mW
Sleep			11		mW
Connected Standby			4		mW
Supply Current					
Measurement conditions: Nominal corner, 25°C, Nominal power supply 4k x 2k @60 MHz 4L HBR to HDMI2.0a VDD (analog and digital) 3.3V VDD (analog and digital) 1.2V			 25 332	 27 390	 mA

Note: Ripple amplitude for power supplies should be 30 mV or lower with max ripple freq up to 30 MHz.

Table 11. IO DC characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Inputs 3.3 V IO signals, 5 V tolerant open drain type					
High voltage	V_{IH}	2.0		5.5	V
Low voltage	V_{IL}	-0.3		0.8	V
Input Hysteresis voltage	V_{HYST}	300			mV
High current (V_{IN} = 3.3 V)	I_{IH}			+/- 10	µA
Low current (V_{IN} = 0.8 V)	I_{IL}			+/- 10	µA
Input capacitance	C_{IN}		5		pF
Outputs 3.3 V IO signals, 5 V tolerant open drain type					
Low Current (VOL = 0.2 V)	IOL	4			mA
Tri-state leakage current	IOZ			10	µA
VDD12ON Output					
Output Low Voltage (IOL=0.25mA)	VOL			0.4	V
Output High Voltage(IOH=0.25mA)	VOH	2.9			V
Low Level output Current	IOL	0.25			
High Level Output Current	IOH	0.25			
Inputs 3.3 V IO signals, 3.3 V tolerant, TRISTATE					
High voltage	VIH	2.0			V
Low voltage	VIL			0.8	V
Input Hysteresis voltage	VHYST	300			mV
High current (VIN = 3.3 V)	IIH			±10	µA
Low current (VIN = 0.8 V)	IIL			±10	µA
Input capacitance	CIN		1.0		pF
Outputs 3.3 V IO signals, 3.3 V tolerant, TRISTATE					
Output Impedance, VOL=0.3V	Rout		50		Ω
Tri-state leakage current	IOZ			±10	mA

6.4. AC characteristics

Table 12. Maximum speed of operation

Clock domain	Max speed of operation
Reference Input Clock (TCLK)	27 MHz
Reference Internal Clock (RCLK)	324 MHz
On-Chip Microcontroller Clock (OCLK)	150 MHz
2-Wire Serial Slave (SLAVE_SCL)	400 kHz
DDC Master (MSTRx_SCL)	400 kHz
SPI Clock	50 MHz

6.4.1. DisplayPort receiver

Table 15. DisplayPort receiver characteristics

Parameter	Symbol	Min	Typ	Max	Units	Comments
Receiver operating range						
Differential Input Voltage Range	$V_{RX\_DIF\_PP\_RANGE}$		0.04~1		V	
RX Termination Control Range	$R_{RX\_TERM\_RANGE}$		80 ~120		ohm	
DisplayPort receiver system parameters						
HBR2 unit interval (5.4Gbps)	UI_{HBR2}		185		ps	
HBR unit interval (2.7Gbps)	UI_{HBR}		370		ps	
RBR unit interval (1.62Gbps)	UI_{RBR}		617		ps	
Link clock down spreading		0		0.5	%	Modulation frequency range 0f 30 kHz to 33 kHz
DisplayPort receiver TP3 parameters						
Receiver Eye TP3 RBR	$T_{RBR\_EYE\_TP3}$	0.25			UI	@ 40mV V_diff_pp
Receiver Eye TP3_EQ HBR	$T_{HBR\_EYE\_TP3EQ}$	0.4			UI	@ 135mV V_diff_pp
Receiver Eye TP3_EQ HBR2	$T_{HBR2\_EYE\_TP3EQ}$	0.3			UI	@ 70mV V_diff_pp
Lane intra-pair skew tolerance	$T_{SKEW\_INTRA\_RBR}$			260	ps	Skew contribution from the cable in addition to the stressed EYE at TP3.
	$T_{SKEW\_INTRA\_HBR}$			60	ps	
	$T_{SKEW\_INTRA\_HBR2}$			50	ps	

Parameter	Symbol	Min	Typ	Max	Units	Comments
Target bit error rate 10^{-9}						
Non-ISI at 1.62 Gbps	$T_{RX\_Non\text{-}ISI\_RBR}$			0.180	UI	1.62Gbps signal @ TP3
TJ at 1.62 Gbps	$T_{RX\_TJ\_RBR}$			0.750	UI	1.62Gbps signal @ TP3
Non-ISI at 2.7 Gbps	$T_{RX\_Non\text{-}ISI\_HBR}$			0.330	UI	2.7Gbps signal @ TP3_EQ
TJ at 2.7 Gbps	$T_{RX\_TJ\_HBR}$			0.491	UI	2.7 Gbps signal @ TP3_EQ
DJ at 5.4 Gbps	$T_{RX\_DJ\_HBR2}$			0.49	UI	5.4 Gbps signal @ TP3_EQ
TJ at 5.4 Gbps	$T_{RX\_TJ\_HBR2}$			0.62	UI	5.4 Gbps signal @ TP3_EQ
AUX parameters						
Differential Input Voltage Range	$V_{AUX\_RX\_DIF\_RANGE}$		0.14~1		V	
RX Termination Control Range	$R_{AUX\_TERM\_RANGE}$		40~60		ohms	
AUX TX peak-peak Range	$V_{AUX\_TX\_DIF\_PP}$		0~1		V	7.8125mV/step in 128 steps

6.4.2. HDMI transmitter I/O specifications

Table 13. HDMI transmitter DC specifications

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Differential output: single ended swing amplitude	V_{TX_PP}	0.4	0.5	0.6	V	
Differential output: Differential swing amplitude	$V_{TX\_DIF\_PP}$	0.8	1	1.2	V	
Differential high level output	$V_{TX\_DIF\_HIGH}$	3.12	3.3	3.49	V	
Differential low level output	$V_{TX\_DIF\_LOW}$	3.12		3.49	V	

Table 14. HDMI transmitter AC characteristics

Parameters	Symbol	Min	Typ	Max	Unit	Comments
TMDS Character Clock	$f_{TX\_CHR\_CLK}$	25		600	MHz	Programmable
Differential Output Voltage	$V_{TX\_DIF\_PP}$	0		1200	mV	In 128 steps
TX Edge Rate	t_{TX_ER}	75		145	pS	1V $V_{TX\_DIF\_PP}$ and Premphasis at 0dB in 8 steps
TX Pre-Emphasis Level	A_{PREMPH}	0		6	dB	1V $V_{TX\_DIF\_PP}$ in 16 steps
TX Termination Control Range	$R_{TX\_TERM\_RANGE}$	100		600	ohms	Programmable Termination
TX Jitter <1.65Gbps for Pattern $_{D10.2}$	$T_{TX\_J\_D102\_LF}$			60	pS	
TX Jitter <1.65Gbps for Pattern$_{PRBS7}$	$T_{TX\_J\_PRBS7\_LF}$			70	pS	
TX Jitter >1.65Gbps, < 3.4Gbps for Pattern$_{D10.2}$	$T_{TX\_J\_D102\_MF}$			35	pS	
TX Jitter >1.65Gbps, < 3.4Gbps for Pattern$_{PRBS7}$	$T_{TX\_J\_PRBS7\_MF}$			45	pS	
TX Jitter >3.4Gbps for Pattern$_{D10.2}$	$T_{TX\_J\_D102\_HF}$			30	pS	
TX Jitter >3.4Gbps for Pattern$_{PRBS7}$	$T_{TX\_J\_PRBS7\_HF}$			35	pS	

6.4.3. I2C interface timing

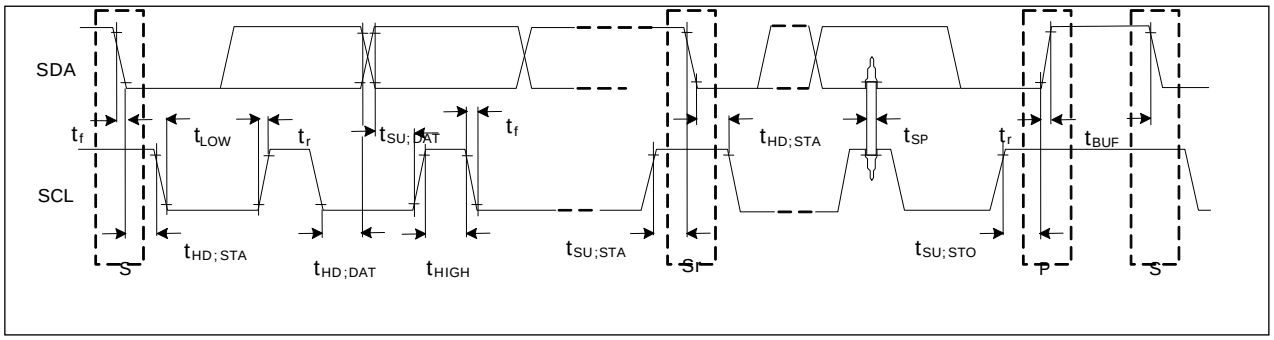
Table 15. I2C interface timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock rate	Fast mode	0	-	400	kHz
$t_{HD\text{-}STA}$	Hold time START	After this period, the 1st clock starts	1.2	-	-	µs
t_{LOW}	Low period of clock	SCL	1.3	-	-	µs
t_{HIGH}	High period of clock	SCL	1.2	-	-	µs
$T_{su;STA}$	Set up time for a repeated START		1.2	-	-	µs
$t_{HD;DAT}$	Data hold time	For master	0.7	-	0.9$^{(1)}$	µs
$t_{SU;DAT}$	Data setup time		380	-	-	ns
T_{BUF}	Bus free time between STOP		1.3	-	-	µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	and START					
C_b	Capacitance load for each bus line		-	100	400	pF
t_r	Rise time		220	-	300	ns
t_f	Fall time		60	-	300	ns
V_{nh}	Noise margin at high level		0.25VDD	-	-	V
V_{nl}	Noise margin at low level		0.2VDD	-	-	

Note 1: The maximum tHD;DAT only has to be met if the device does not stretch the low period tLOW of the SCL signal. In the diagram below, S = start, P = stop, Sr = Repeated start, and SP= Repeated stop conditions.

Figure 8. I2C timing



6.4.4. SPI interface timing

The table below specifies the typical SPI_CLK output frequency and the minimum requirements of the interface between the SPI NOR Flash device and the MCDP2900 SPI interface.

Table 16. SPI interface timing

Symbol	Parameter	Min	Typ	Max	Units
F_{CLK}	SPI_CLK output clock frequency		50		MHz
T_{SCKH}	Serial clock high time		20		ns
T_{SCKL}	Serial clock low time		20		ns
$T_{R\_SPI\_CLK}$	SPI_CLK rise time @10mA drive 10pF load			2.8	ns
$T_{F\_SPI\_CLK}$	SPI_CLK fall time @10mA drive 10pF load			3.2	ns
T_{CSN_SU}	CSN output setup time requirement	7			ns
T_{CSN_HLD}	CSN output hold time requirement	7			ns
$T_{\_DO\_PD}$	Data Output propagation delay			6	ns
T_{DI_SU}	Data Input setup time	3			ns
T_{DI_HLD}	Data Input hold time	5			ns

7. Ordering information

Table 17. Order codes

Part number	Description
MCDP2900A2	64 LFBGA (7x7x1.4 mm) in Tray
MCDP2900A2T	64 LFBGA (7x7x1.4 mm) in Tape & Reel
MCDP2900A2 FX	64 LFBGA (7x7x1.4 mm) in Tray

8. Revision history

Table 18. Document revision history

Date	Revision	Changes
16-MAY-2016	A	Initial version.

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