

32-Channel 128-Level Amplitude Gray-Shade Display Column Driver

Features

- ❑ 5V CMOS inputs
- ❑ Up to 80V modulation voltage
- ❑ Capable of 128 levels of gray shading
- ❑ 24MHz data throughput rate
- ❑ 32 outputs per device (can be cascaded)
- ❑ Pin-programmable shift direction (DIR)
- ❑ D/A conversion cycle time is 20µs
- ❑ Diodes in output structure allow usage in energy recovery systems
- ❑ Integrated HVCMOS® technology
- ❑ Available in 3-sided 64-lead gullwing package

Applications

- ❑ Electroluminescent Displays
- ❑ Polycholesteric Displays

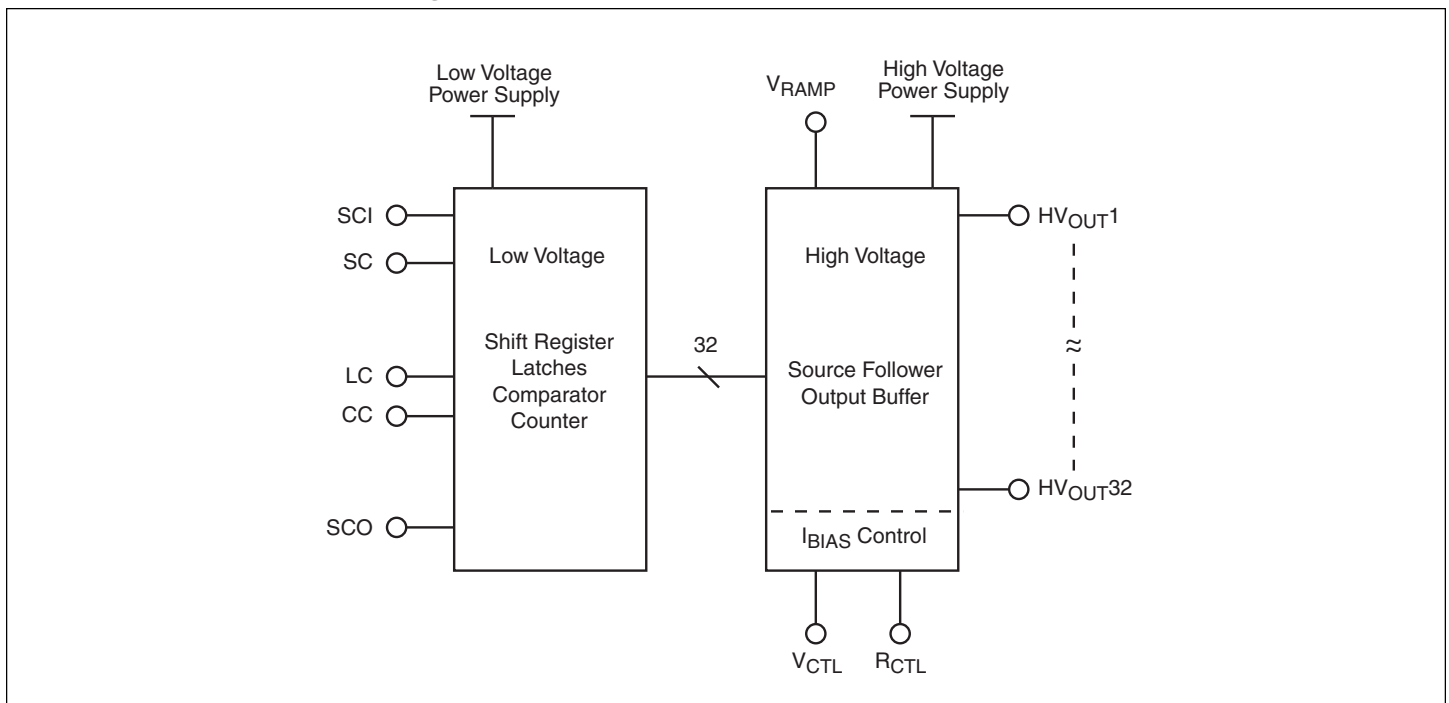
General Description

The HV633 is a 32-channel driver IC for gray shade display use. It is designed to produce varying output voltages between 3 and 80 volts. This amplitude modulation at the output is facilitated by an external ramp voltage V_R . See Theory of Operation for detailed explanation.

This device consists of a dual 16-bit shift registers, 32 data latches and comparators, and control logic to preform 128 levels of gray shading. There are 7 bits of data inputs. Data is shifted through the shift registers at both edges of the clock, resulting a data transfer rate of twice of the shift clock frequency. When the DIR pin is high, CSI/CSO is the input/output for the chip select pulse. When DIR is low, CSI/CSO is the output/input for the chip select pulse. The DIR = HIGH also allows the HV633 to shift data in the counter-clockwise direction when viewed from the top of the package. When the DIR pin is low, data is shifted in the clockwise direction.

The output circuitry allows the energy which is stored in the output capacitance to be returned to V_{PP} through the body diode of the output transistor.

Functional Block Diagram



Absolute Maximum Ratings

| | |
|--|-------------------------|
| Supply voltage, V_{DD}^1 | -0.5V to +7.5V |
| Supply voltage, V_{PP}^1 | -0.5V to +90V |
| Logic input levels ¹ | -0.5 to $V_{DD} + 0.5V$ |
| Ground current ² | 1.5A |
| Continuous total power dissipation ³ | 2.0W |
| Maximum junction temperature | 125°C |
| Storage temperature range | -65°C to +150°C |
| Lead temperature 1.6mm (1/16 inch) from case for 10 seconds | 260°C |

Notes:

- All voltages are referenced to GND.
- Duty cycle is limited by the total power dissipated in the package.
- For operation above 25°C ambient derate linearly to 125°C at 22.2mW/°C.

Ordering Information

| Package Option | | |
|----------------|----------------------------------|--------|
| Device | 64-Lead 3-sided Plastic Gullwing | Die |
| HV633 | HV633PG | HV633X |

Power-up sequence should be the following:

- Connect ground.
- Apply V_{DD} .
- Set all inputs (Data, CLK, Enable, etc.) to a known state.
- Apply V_{PP} .

Power-down sequence should be the reverse of the above.

Electrical Characteristics (at $T_A = 25^\circ\text{C}$, over operating conditions unless otherwise specified)

Low-Voltage DC Characteristics (Digital)

| Symbol | Parameter | Min | Typ ¹ | Max | Units | Conditions |
|------------|--------------------------------------|------|------------------|-----|---------------|--|
| I_{DD} | V_{DD} supply current | | 12 | 20 | mA | $f_{SC} = 12\text{MHz}$ $f_{CC} = 12\text{MHz}$ |
| I_{DDQ} | Quiescent V_{DD} supply current | | | 200 | μA | All $V_{IN} = 0V$, $V_{DD} = \text{max}$ |
| I_{IH} | High-level input current | | 1.0 | 50 | μA | $V_{IH} = V_{DD}$ |
| I_{IL} | Low-level input current | | -1.0 | -50 | μA | $V_{IL} = 0V$ |
| C_{IN}^2 | Input capacitance (data, LC, SC, CC) | | | 15 | pF | $V_{IN} = 0V$, $f = 1.0\text{MHz}$ |
| I_{OH} | High-level output current | -2.0 | | | mA | $V_{DD} = 4.5V$ |
| I_{OL} | Low-level output current | 2.0 | | | mA | $V_{DD} = 4.5V$ |

Notes

- All typical values are at $V_{DD} = 5.0V$.
- Guaranteed by design.

Low-Voltage DC Characteristics (Analog)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|-----------|-----------------------------------|-----|-----|-----|---------------|--|
| I_{DD} | V_{DD} supply current | | | 500 | μA | $f_{SC} = 12\text{MHz}$ $f_{CC} = 12\text{MHz}$ |
| I_{DDQ} | Quiescent V_{DD} supply current | | | 200 | μA | All $V_{IN} = 0V$, $V_{DD} = \text{max}$ |

High-Voltage Bias Circuit for Output Variation Control

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|--|-----|-----|-----|-------|--|
| I_{PP} | V_{PP} supply current for bias circuit | | 2.0 | | mA | Depending on external bias circuit, see Table 1. |

High-Voltage DC Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|--------------|--|------------------------|-----|-----------|-------|---|
| I_{AOH} | High-voltage analog output source current | See Performance Curves | | | mA | $V_{PP} = 80V$ See test circuit |
| I_{AOL} | High-voltage analog output sink current | See Performance Curves | | | mA | $V_{PP} = 80V$, $V_{DD} = 4.5V$ $V_{AO} = 2.0V$ |
| ΔV_O | Maximum delta voltage between high voltage outputs of the same level | | | ± 0.2 | V | At all gray levels |

Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units |
|------------|---|--------------|-----|--------------|-------|
| V_{DD} | Low-voltage digital supply voltage | 4.5 | 5.0 | 5.5 | V |
| V_{DD} | Low-voltage analog supply voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | High-level input voltage (analog and digital) | $V_{DD} - 1$ | | V_{DD} | V |
| V_{IL} | Low-level input voltage (analog and digital) | 0 | | 1.0 | V |
| V_{BIAS} | I_{PP} control circuit bias voltage | -2.0 | 0 | | V |
| V_{CTL} | I_{PP} control circuit control voltage | | 0 | 2.0 | V |
| V_{PP} | High-voltage supply | -0.3 | | 80 | V |
| V_R | Ramp voltage | 0 | | $V_{PP} - 2$ | V |
| f_{SC} | Shift clock operating frequency (at $V_{DD} = 5.5V$) | | | 12 | MHz |

Electrical Characteristics

AC Characteristics ($V_{DD} = 5.5V$, $T_A = 25^\circ C$)

Logic Timing

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|--------------|---|------|-----|-----|---------|------------|
| f_{SC} | Shift clock operating frequency | | | 12 | MHz | |
| f_{DIN} | Data-in frequency | | | 24 | MHz | |
| t_{SS} | CSI/CSO pulse to shift clock setup time | | 40 | | ns | |
| t_{HS} | CSI/CSO pulse to shift clock hold time | | 0 | | ns | |
| t_{WA} | CSI pulse width | | 49 | | ns | |
| t_{DS} | Data to shift clock setup time | | 20 | | ns | |
| t_{DH} | Data to shift clock hold time | | 0 | | ns | |
| t_{WD} | Data-in pulse width | | 24 | | ns | |
| t_{WLC} | Load count pulse width | | 98 | | ns | |
| t_{DLCR} | Load count to ramp delay | 1.0 | | | μs | |
| t_{DRCC}^1 | Ramp to count clock delay | 0.47 | | | μs | |
| t_{DSL} | Shift clock to load count delay time | | 98 | | ns | |
| t_{CSC} | Shift clock cycle time | 98 | | | ns | |
| t_{WSC} | Shift clock pulse width | 49 | | | ns | |
| t_{CCC} | Count clock cycle time | 98 | | | ns | |
| t_{WCC} | Count clock pulse width | 49 | | | ns | |

Note 1: Count clock starts counting after 0.47 μs min. This is equivalent to a time duration for a linear ramp V_R to ramp from 0 to 3V, assuming the minimum value of T_{RR} , ramp size time of 12 μs for $V_R = 80V$.

V_{RAMP} Timing

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|------------|---------------------------|------|-----|-----|---------|------------------|
| t_{CR} | Cycle time of ramp signal | 15 | | | μs | |
| t_{RR} | Ramp rise time | 10.6 | | | μs | |
| t_{HR}^2 | Ramp hold time | 2 | | 15 | μs | |
| t_{FR} | Ramp fall time | 3 | | | μs | $C_{LOAD} = 1nF$ |

Note 2: The maximum ramp hold time may be longer than 15 μs , but the output voltage HV_{OUT} will droop due to leakage.

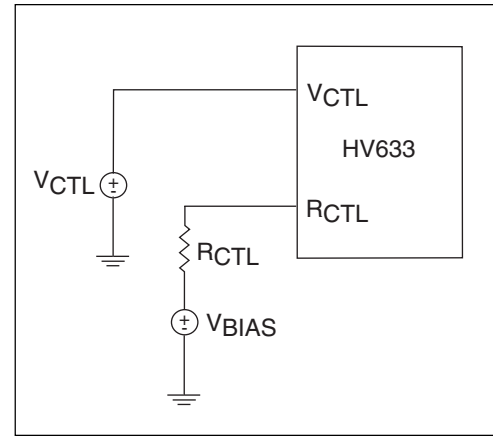
Table 1:Schemes to control I_{PP} bias current, typical I_{PP}

Option 1

| V_{BIAS} (V) | V_{CTL} (V) | R_{CTL} (Ω) | I_{PP} (mA) |
|-------------------|------------------|---------------------------|------------------|
| 0 | 0.1 | 56K | 2 |
| 0 | 1.0 | 56K | 7 |

Option 2

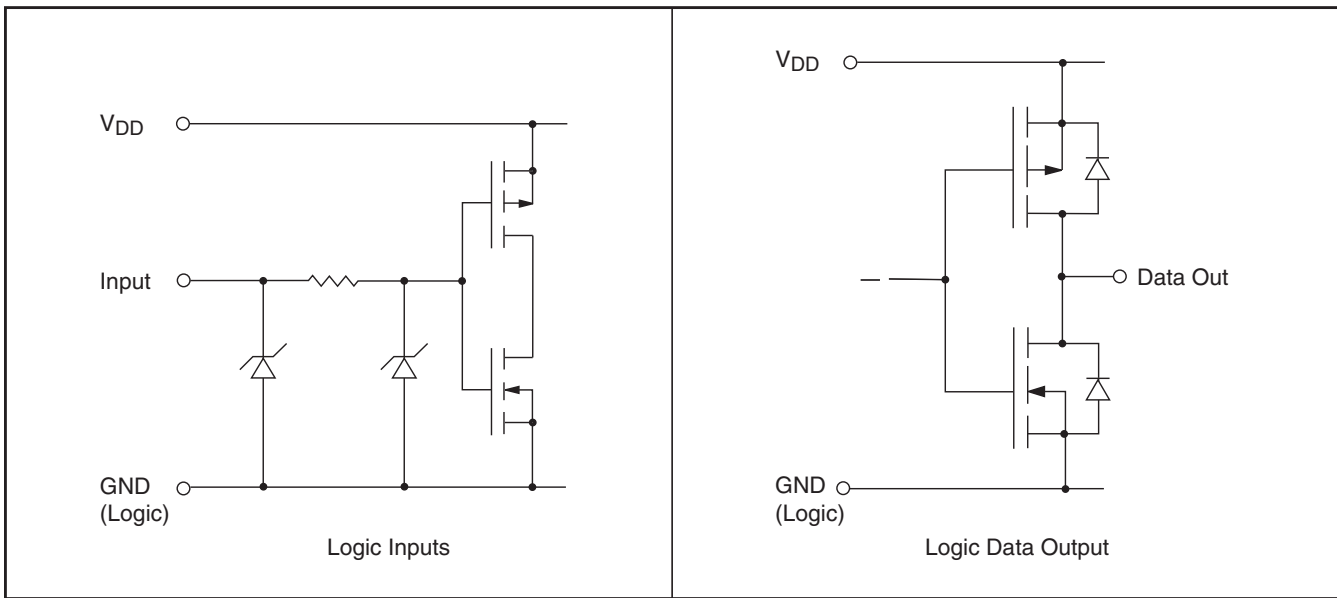
| V_{BIAS} (V) | V_{CTL} (V) | R_{CTL} (Ω) | I_{PP} (mA) |
|-------------------|------------------|---------------------------|------------------|
| -1.0 | 0 | 56K | 4 |
| -2.0 | 0 | 56K | 5.5 |



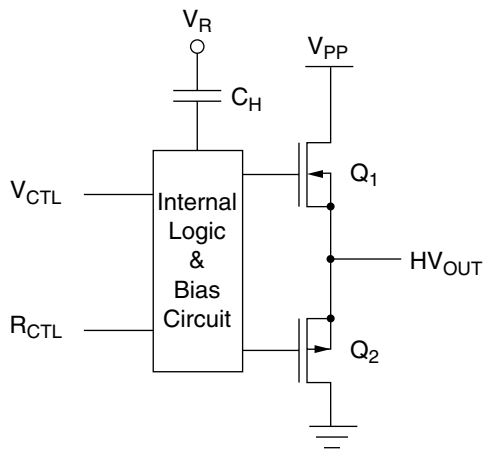
Pin Definitions

| Pin # | Name | Function |
|---------------|-------------------------------|--|
| 30-36 | D1-D7 | Inputs for binary-format parallel data. |
| 26 | SC (Shift Clock) | Triggers data on both rising and falling edges. This implies that the data rate is always twice the clock rate (data rate = 20MHz max if clock rate = 10MHz max). |
| 22 | CSI (Chip Select Input) | Input pin for the chip select pulse (when DIR is high). Output pin for the chip select pulse (when DIR is low). |
| 43 | CSO (Chip Select Output) | Input pin for the chip select pulse (when DIR is low). Output pin for the chip select pulse (when DIR is high). |
| 40 | LC (Load Count) | Input for a pulse whose rising edge causes data from the input latches to enter the comparator latches, and whose falling edge initiates the conversion of this binary data to an output level (D-to-A). Also, the HV_{OUT} will clear to zero after the load count is initiated. |
| 42 | CC (Count Clock) | Input to the count clock generator whose increments are compared to the data in the comparator latches. |
| 18, 47 | V_R | High-voltage ramp input for charging the output stage hold capacitors (C_H). This input can be linear or non-linear as desired. |
| 28 | DIR | When this pin is connected to V_{DD} , input data is shifted in ascending order, i.e., corresponding to HV_{OUT1} to HV_{OUT32} . When connected to LVGND, input data is shifted in descending order, i.e., corresponding to HV_{OUT32} to HV_{OUT1} . |
| 27, 38 | LVGND | This is ground for the logic section. HVGND and LVGND should be connected together externally. |
| 17, 48 | HVGND | This is ground for the high-voltage (output) section. HVGND and LVGND should be connected together externally. |
| 19, 45 | V_{PP} | This input biases the output source followers. |
| 1-16 49-64 | HV_{OUT1} - HV_{OUT32} | High-voltage outputs. |
| 21 | V_{DD} (Analog) | Low-voltage analog supply voltage. |
| 29 | V_{DD} (Digital) | Low-voltage digital supply voltage. |
| 24 | V_{CTL} | Voltage supply pin to prevent output voltage from being affected by its adjacent outputs ($V_{CTL} = 2V$ for a particular panel). The combination of V_{CTL} and R_{CTL} will reduce the output voltage variation to less than $\pm 0.2V$ of delta voltage between high voltage outputs of the same level at all gray levels. |
| 25 | R_{CTL} | Current sense resistor to ground to prevent output voltage from being affected by its adjacent outputs ($R_{CTL} = 56K\Omega$ for a particular panel). See V_{CTL} function above. |

Input and Output Equivalent Circuits

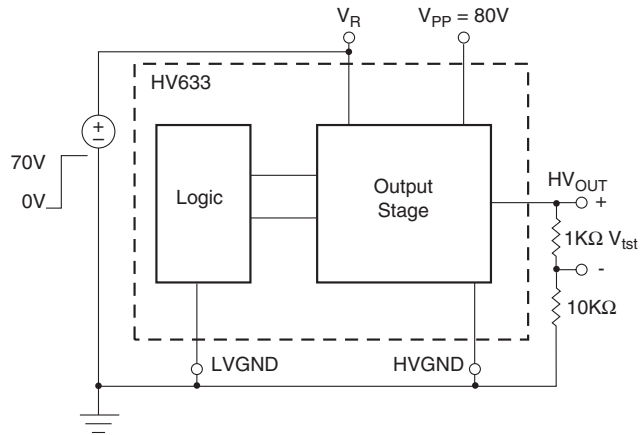


Output Stage Detail



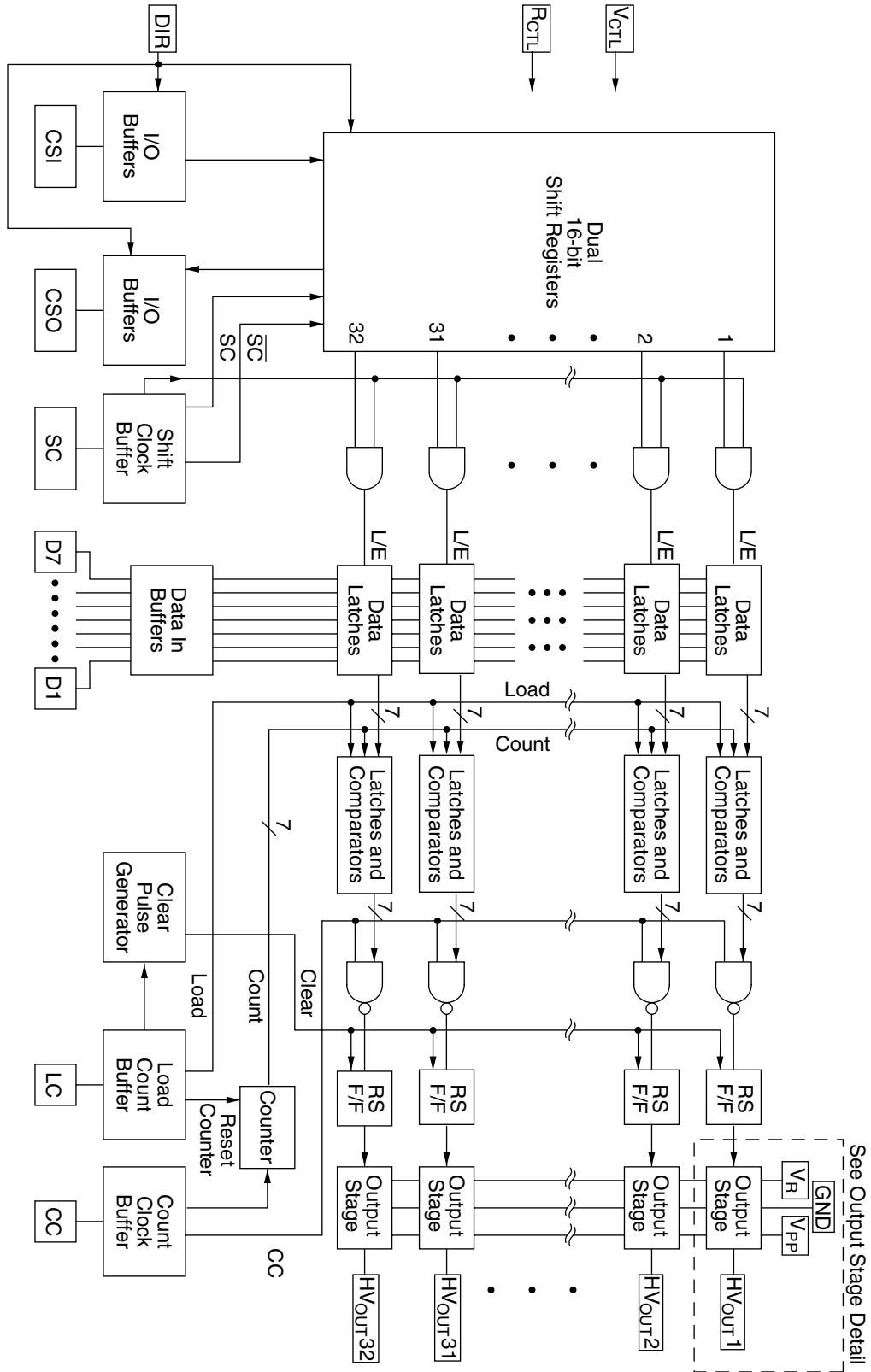
Test Circuit

High-voltage Analog Output Source Current (I_{AOH})
 For gray shade #1 (000 0000)



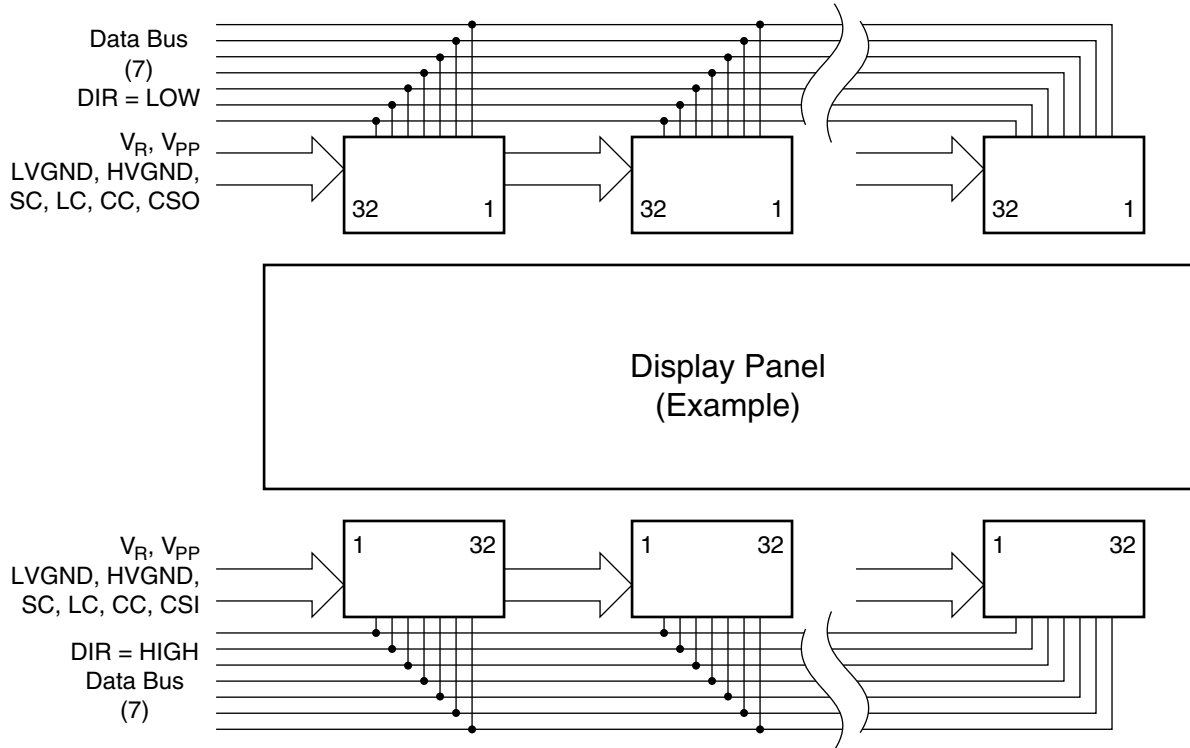
1. Set $HV_{OUT} = \text{Low}$.
2. Apply $V_{PP} = 80V$.
3. Apply a step voltage of 70V at V_R (slew rate = $4.1V/\mu s$).
4. Measure voltage across the 1K Ω resistor.
5. Output source current can be calculated by using $\frac{V_{tst}}{1K}$.

Functional Block Diagram



SC = Shift Clock
 LC = Load Count
 CC = Count Clock
 CSI = Chip Select Input
 CSO = Chip Select Output
 *Strobe = twice the SC frequency

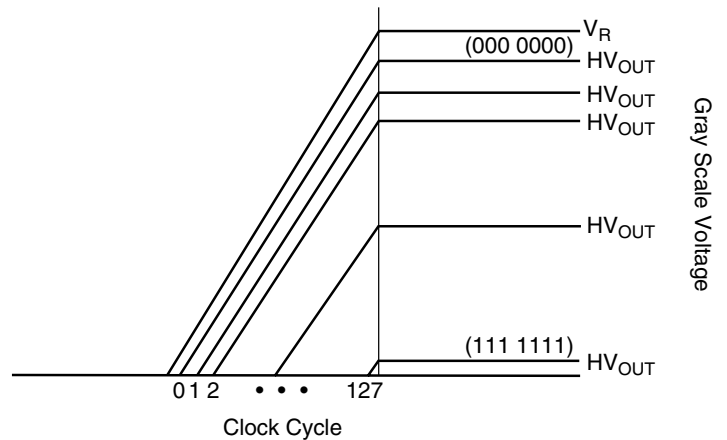
Typical Panel Connections



Gray Shade Decoding Scheme

| Shade Number | D7 | D6 | D5 | D4 | D3 | D2 | D1 |
|--------------|----|----|----|----|----|----|----|
| 128 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 127 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 126 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 125 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 124 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 123 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 122 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 121 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| ... | | | | | | | |
| 7 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 6 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 5 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 4 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 3 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Gray Scale Voltage

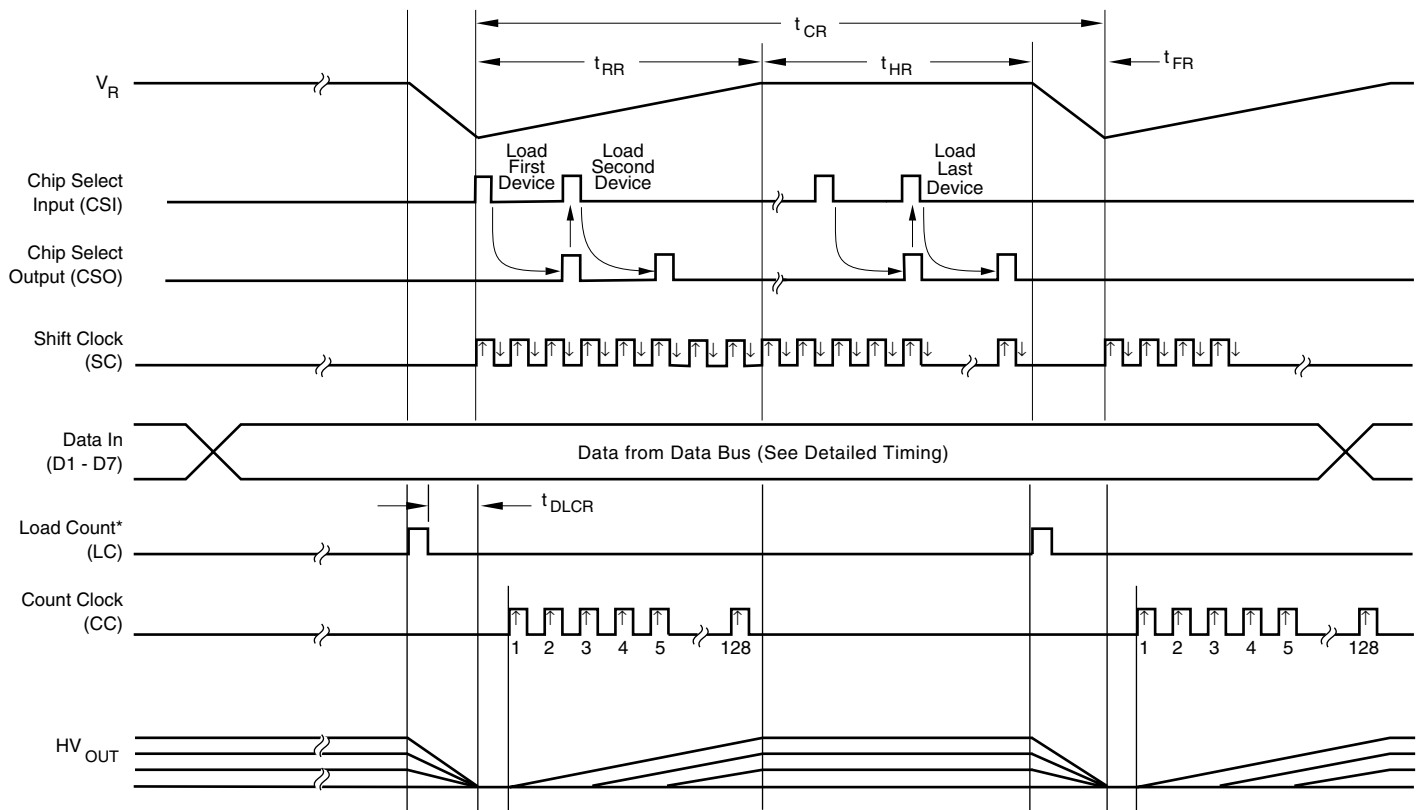


Function Table

| Sequence | Function | DIR | Data-In (D1 - D7) | CSI | CSO | Shift Clock | Load Count | Count Clock | V _R | HV _{OUT} | | | | |
|----------|---|-----|-------------------|----------------------|--------|-------------|------------|-------------|----------------|-------------------|---|---|-----------------------------|---|
| 1 | Shift Data from HV _{OUT} 1 to 32 | H | H | | Output | | L | L | L | L | | | | |
| | | | L | | | | | | | H | | | | |
| 2 | Shift Data from HV _{OUT} 32 to 1 | L | H | Output | | | L | L | L | L | | | | |
| | | | L | | | | | | | H | | | | |
| 3 | Load Shift Register | X | X | Pre-define by 1 or 2 | | | L | L | L | - | | | | |
| 4 | Load Counter | X | X | | | | | | | L | | L | L | - |
| 5 | Counting/Voltage Conversion | X | X | | | | | | | L | L | | Initiates V _{RAMP} | - |

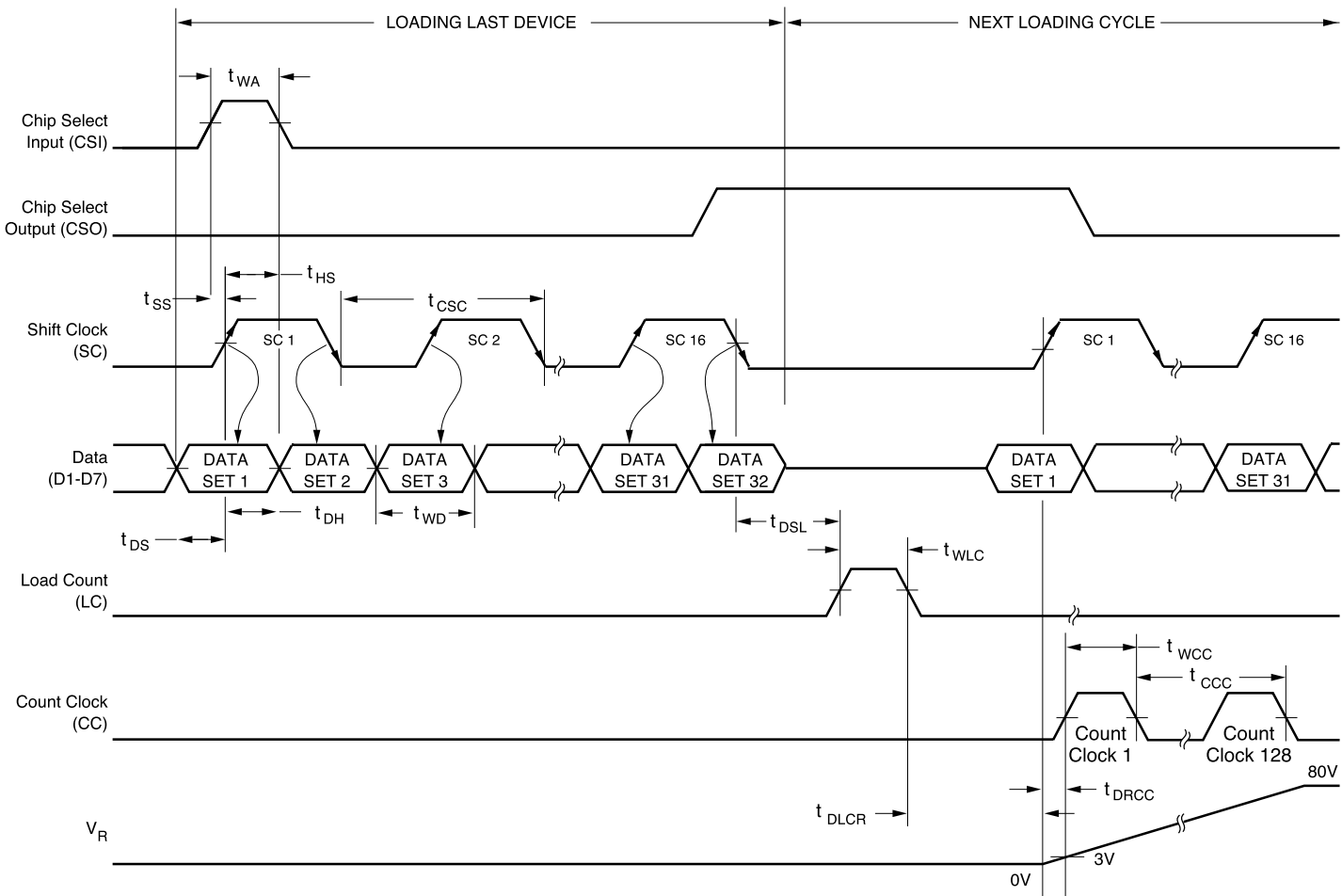
Timing Diagrams

(a) Basic System Timing



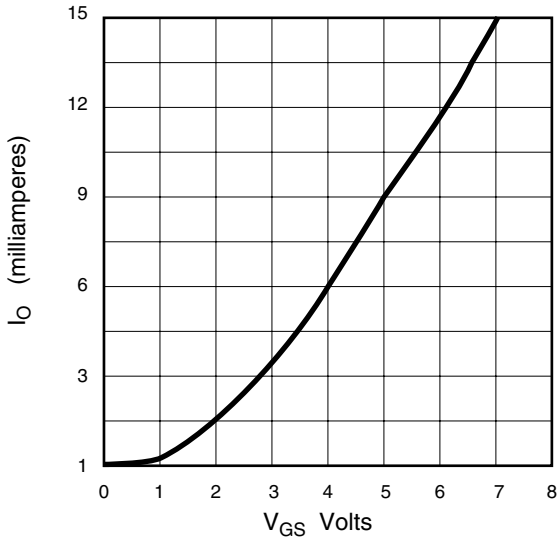
*HV_{OUT} will clear to zero with load count.

(b) Detailed Device Timing

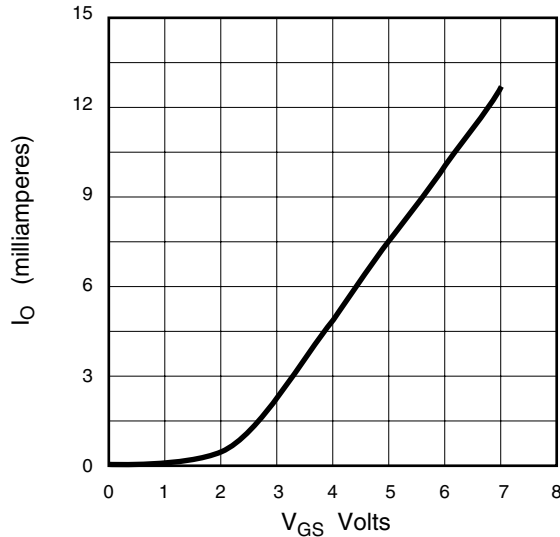


Typical Performance Curves

Source Output Characteristics



Sink Output Characteristics



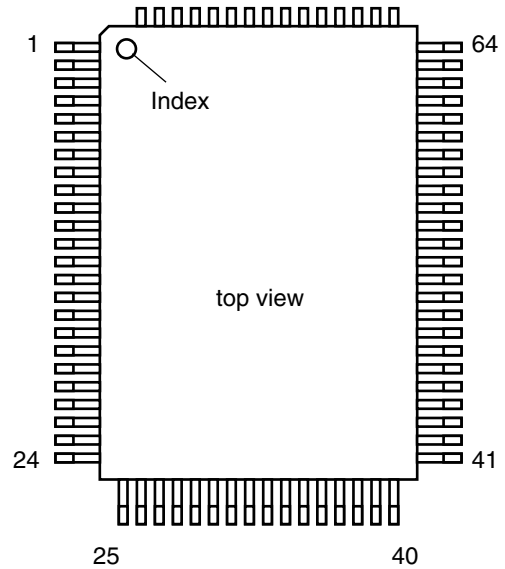
Pin Configuration

64-Pin PG Package

| Pin | Function | Pin | Function | Pin | Function |
|-----|---------------------------|-----|----------------------------|-----|----------------------|
| 1 | HV _{OUT} 1 | 23 | N/C | 45 | V _{PP} |
| 2 | HV _{OUT} 2 | 24 | V _{CTL} | 46 | N/C |
| 3 | HV _{OUT} 3 | 25 | R _{CTL} | 47 | V _R |
| 4 | HV _{OUT} 4 | 26 | SC (Shift Clock) | 48 | HVGND |
| 5 | HV _{OUT} 5 | 27 | LVGND | 49 | HV _{OUT} 17 |
| 6 | HV _{OUT} 6 | 28 | DIR | 50 | HV _{OUT} 18 |
| 7 | HV _{OUT} 7 | 29 | V _{DD} (Digital)* | 51 | HV _{OUT} 19 |
| 8 | HV _{OUT} 8 | 30 | D ₇ | 52 | HV _{OUT} 20 |
| 9 | HV _{OUT} 9 | 31 | D ₆ | 53 | HV _{OUT} 21 |
| 10 | HV _{OUT} 10 | 32 | D ₅ | 54 | HV _{OUT} 22 |
| 11 | HV _{OUT} 11 | 33 | D ₄ | 55 | HV _{OUT} 23 |
| 12 | HV _{OUT} 12 | 34 | D ₃ | 56 | HV _{OUT} 24 |
| 13 | HV _{OUT} 13 | 35 | D ₂ | 57 | HV _{OUT} 25 |
| 14 | HV _{OUT} 14 | 36 | D ₁ | 58 | HV _{OUT} 26 |
| 15 | HV _{OUT} 15 | 37 | N/C | 59 | HV _{OUT} 27 |
| 16 | HV _{OUT} 16 | 38 | LVGND | 60 | HV _{OUT} 28 |
| 17 | HVGND | 39 | N/C | 61 | HV _{OUT} 29 |
| 18 | V _R | 40 | LC (Load Count) | 62 | HV _{OUT} 30 |
| 19 | V _{PP} | 41 | N/C | 63 | HV _{OUT} 31 |
| 20 | N/C | 42 | CC (Count Clock) | 64 | HV _{OUT} 32 |
| 21 | V _{DD} (Analog)* | 43 | CSO | | |
| 22 | CSI | 44 | N/C | | |

* Analog V_{DD} and digital V_{DD} may be connected separately for better noise immunity.

Package Outlines



3-Sided Plastic QFP 64-pin Gullwing Package

Theory of Operation

The HV633 has two primary functions:

- 1) Loading data from the data bus and,
- 2) Gray-shade conversion (converting latched data to output voltages).

Since the device was developed initially for flat panel displays, the operation will be described in terms that pertain to that technology. As shown by the Typical Drive Scheme, several HV633 packages are mounted at the top and bottom of a display panel. Data exists on a 7-bit bus (adjacent PC board traces) at top and bottom. The D1 through D7 inputs of each chip take data from the bus when either a CSI or CSO pulse is present at the chip. These pulses therefore act as a combination CHIP SELECT and LOCATION STROBE. Because of the way the chip HV_{OUT} pins are sequenced, data on the bus at the bottom of the display panel will be entered into the left-most chip as HV_{OUT}1, HV_{OUT}2, etc. up to HV_{OUT}32. The CSI pulse will accomplish this with DIR = High.

Loading Data from Data Bus

Here is the full data-entry sequence:

- 1) The microcontroller puts data on the bus (7 bits)
- 2) To enter the data into the 32 sets of 7 latches on the first chip, the shift clock rises. This positive transition is combined with the CSI pulse and is generated only once to strobe the data into the first set of latches. (These latches eventually send data to the HV_{OUT}1). The data on the bus then changes, the shift clock falls, and this negative transition is combined with the CSI pulse, which is now propagated internally, to strobe the new data into the next set of 7 latches (which will end up as HV_{OUT}2). This internal CSI pulse therefore runs at twice the shift clock rate.
- 3) When the last set of 7 latches in the first chip has been loaded (HV_{OUT}32), the CSI pulse leaves chip 1 and enters chip 2. The exit pin is called CSO and the chip 2 entry pin is CSI. For chips at the top of the panel things are reversed: DIR is low, entry pins are CSO and exit pins are CSI, because the data-into-latches sequence is in descending order, HV_{OUT}32 down to HV_{OUT}1.
- 4) The buses may of course be separate, and data can be strobed in on an interleaved basis, etc., but those complications will be left to systems designers.

When data has been loaded into all 32 outputs of all chips (top and bottom of the display panel), the load count pin is pulsed. On its rising transition, all output levels are reset to zero and all the data in the input latches is transferred to a like number of comparator latches, (thus leaving the data latches ready to receive new data during the following operations). After the transfer, the load count pin is brought low. This transition begins the events that convert the binary data into a gray-shade level.

Gray-shade Conversion

- 1) The COUNT CLOCK is started. An external signal is applied to the COUNT CLOCK pin, causing the counter on each chip to increment from binary 000 0000 to 111 1111 (0 to 127).
- 2) At the same time, the V_R voltage is applied to all chips, via charging transistors, causing the HOLD CAPACITOR (C_H) on each output to experience a rise in voltage.
- 3) The logic control compares the count in the comparator latch to the count clock. The gate voltage of Q_1 and the output voltage HV_{OUT} will ramp up at the same rate as V_R .
- 4) Once V_R has reached the maximum voltage, then all the pixels will be at the final value. (See Output Gray Scale Voltage.)

Output Voltage Variation

The output voltage of the HV633 is determined by the logic and the ramp voltage V_R . It is possible that the output voltage may be coupled to an unacceptable level due to its adjacent outputs through the panel. In order to solve this problem, internal logic (refer to Output Stage Detail) is integrated in the IC to minimize the effect.

Two external pins V_{CTL} and R_{CTL} allow the feasibility to control the current flowing through Q_2 . The V_{CTL} pin is connected to a voltage source and the R_{CTL} pin is connected to ground through a resistor (2V and 56K Ω are used for a particular panel). The internal bias circuit will drive the resistor to a voltage level that is equal to the V_{CTL} voltage at steady state through an operational amplifier. The current flowing through Q_1 and Q_2 will be limited to V_{CTL}/R_{CTL} . This combination of V_{CTL} and R_{CTL} will reduce the output voltage variation to less than $\pm 0.2V$ of delta voltage for each gray shade, independent of its adjacent output voltages.