PIC24F16KL402 Family
Silicon Errata and Data Sheet Clarification

The PIC24F16KL402 family devices that you have received conform functionally to the current Device Data Sheet (DS31037**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24F16KL402 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A0**).

Data Sheet clarifications and corrections start on Page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24F16KL402 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A0	A1			A0	A1
PIC24F04KL100	4B01h	0000h	0001h	PIC24F08KL302	4B00h	0000h	0001h
PIC24F04KL101	4B02h			PIC24F08KL401	4B0Eh		
PIC24F08KL200	4B05h			PIC24F08KL402	4B04h		
PIC24F08KL201	4B06h			PIC24F16KL401	4B1Eh		
PIC24F08KL301	4B0Ah			PIC24F16KL402	4B14h		

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FXXKL1XX/2XX/3XX/4XX Flash Programming Specifications"* (DS30625) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]	
				A0	A1
UART	Transmit	1.	UxTXBF flag may not indicate correctly.	X	
Oscillator	REFO	2.	REFO output unavailable at higher frequencies.	X	X
HLVD	Band Gap Reference	3.	BGVST and IRVST bits may not become set at extremely low temperatures	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: UART (Transmit)

The Transmit Buffer Full Flag, UTXBF (UxSTA<9>), may become cleared before data starts moving out of the full buffer. If the flag is used to determine when data can be written to the buffer, new data may not be accepted, and data may not be transmitted.

Work around

Poll the Transmit Buffer Empty Flag (TRMT, UxSTA<8>) to determine when the transmit buffer is empty and can be written to.

Alternatively, configure the UART to set the Transmit Interrupt Flag (UxTXIF) whenever a character is shifted into the Transmit Shift Register (UTXISEL<1:0> = 00). When a transmit interrupt occurs, this indicates that at least one buffer position is open and that the buffer can be written to.

Affected Silicon Revisions

A0	A1						
X							

2. Module: Oscillator (REFO)

When output frequencies above 16 MHz are selected for the Reference Clock Output (REFO), the peak output voltage on the REFO pin may be too low to be properly detected by external devices.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

3. Module: HLVD (Band Gap Reference)

At the extreme low end of the operating temperature range (near -40°C), the BGVST and IRVST flag bits (HLVDCON<6,5>) may not become set when the voltage references are stable and ready to use.

Work around

For applications that run at extremely cold temperatures, do not use the BGVST and IRVST bits as the sole indicator of band gap readiness. Include a time-out of 750 µs between enabling and using a reference.

Affected Silicon Revisions

A0	A1						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS31037**B**):

Note:	Corrections and additions are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Front Matter (Device Features)

Under the heading: **"Power Management Modes"** on Page 1, the bullet entry for Run mode current in "Low-Power Consumption" is corrected to read:

"Run mode current **of 150 µA/MHz, 1.8V** typical"

2. Module: Pin Diagrams

The pin diagrams for all 20-pin DIP devices (Pages 4 and 5 of the data sheet) are PDIP packages, and not Skinny PDIP (SPDIP), as indicated. SPDIP packaging is not available for 20-pin devices in this device family.

References to SPDIP packaging for 28-pin DIP devices are corrected as shown.

3. Module: Overview

In Table 1-2 ("Device Features for PIC24F16KL40X/30X Devices"), references in the "Packages" row to 20-Pin SPDIP are to be read as "20-Pin **PDIP**". In addition, references to 28-Pin PDIP are to be read as "28-Pin **SPDIP**".

In Table 1-3 ("Device Features for the PIC24F16KL20X/10X Devices"), references in the "Packages" row to 20-Pin SPDIP are to be read as "20-Pin **PDIP**".

4. Module: I/O Ports

The following is appended to the end of **Section 11.2.1 "Analog Selection Register"**:

"On devices which do not have an A/D Converter, it is still necessary to configure the ANSx registers in order to enable digital input buffers. Any I/O pins with an ANx function listed in red in the device pinout diagrams (Pages 3 through 5) will default to have the digital input buffer disabled."

5. Module: Master Synchronous Serial Port (MSSP)

A new footnote (4) is added to Register 17-3 (SSPxCON1, SPI Mode) to clarify an exception condition for a particular bit state. The definition of the state itself is unchanged. The new footnote is shown in Register 17-3 (below).

REGISTER 17-3: SSPxCON1:MSSPx CONTROL REGISTER 1 (PARTIAL PRESENTATION)

bit 3-0 **SSPM<3:0>:** Master Synchronous Serial Port Mode Select bits(3)

1010 = SPI Master mode, Clock = FOSC/(2 * ([SSPxADD] + 1))(4)
0101 = SPI Slave mode, Clock = SCKx pin; $\overline{SSx}$ pin control is disabled, $\overline{SSx}$ can be used as an I/O pin
0100 = SPI Slave mode, Clock = SCKx pin; $\overline{SSx}$ pin control is enabled
0011 = SPI Master mode, Clock = TMR2 output/2
0010 = SPI Master mode, Clock = FOSC/32
0001 = SPI Master mode, Clock = FOSC/8
0000 = SPI Master mode, Clock = FOSC/2

Note 1: In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPxBUF register.

2: When enabled, these pins must be properly configured as input or output.

3: Bit combinations not specifically listed here are either reserved or implemented in I^2C mode only.

4: **An SSPxADD value of 00h is not supported when the Baud Rate Generator is used in SPI mode.**

6. Module: Comparator

For Register 20-1 (CMxCON), the definitions of the EVPOLx bits (CMxCON<7:6>) have been clarified. Specifically, the definitions for states, '10' and '01', are simplified; the other states, as well as the overall functionality of the bits, are unchanged. The new definitions are shown in Register 20-1 (below).

REGISTER 20-1: CMxCON: COMPARATOR x CONTROL REGISTER (PARTIAL PRESENTATION)

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits

11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt is generated on **the high-to-low transition of the** comparator output
01 = Trigger/event/interrupt is generated on **the low-to-high transition of the** comparator output
00 = Trigger/event/interrupt generation is disabled

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (11/2011)

Initial release of this document; issued for revision A0. Includes silicon issues 1 (UART, Transmit) and 2 (Oscillator, REFO).

Rev B Document (4/2012)

Adds silicon issue 3 (HLVD, Band Gap Reference) to revision A0.

Adds data sheet clarifications 1 (Front Matter, Device Features), 2 (Pin Diagrams), 3 (Overview), 4 (I/O Ports), 5 (Master Synchronous Serial Port – MSSP) and 6 (Comparator).

Rev C Document (4/2013)

Adds silicon revision A1.

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