DDR2 VLP Registered MiniDIMM

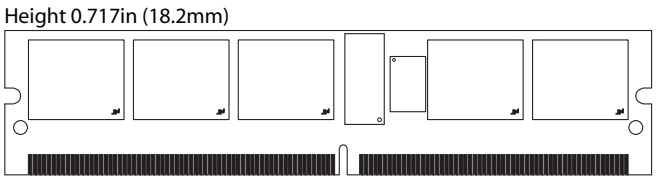
MT9HVF3272(P)K – 256MB
MT9HVF6472(P)K – 512MB
MT9HVF12872(P)K – 1GB (Advance)

For the latest data sheet, refer to the Micron's Web site: www.micron.com/products/modules

Features

- 244-pin, very low profile mini dual in-line memory module (VLP MiniDIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, or PC2-5300
- Supports ECC error detection and correction
- 256MB (32 Meg x 72), 512MB (64 Meg x 72)
  1GB (128 Meg x 72)
- V_{DD} = $V_{DD}Q$ = +1.8V
- V_{DDSPD} = +1.7V to +3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency (WL) = READ latency (RL) - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Single rank

Figure 1: 244-Pin VLP MiniDIMM



Options

Options	Marking
• Register parity	P
• Package	
244-pin DIMM (lead-free)	Y
• Frequency/CAS latency[1]	
3ns @ CL = 5 (DDR2-667)[2]	-667
3.75ns @ CL = 4 (DDR2-533)	-53E
5.0ns @ CL = 3 (DDR2-400)	-40E
• PCB height	
0.717in (18.2mm)	

Notes: 1. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
2. Contact Micron for product availability.

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Table 1: Address Table

	256MB	512MB	1GB
Refresh count	8K	8K	8K
Row addressing	8K (A0–A12)	16K (A0–A13)	16K (A0–A13)
Device bank addressing	4 (BA0, BA1)	4 (BA0, BA1)	8 (BA0, BA1, BA2)
Device page size per bank	1KB	1KB	1KB
Device configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column addressing	1K (A0–A9)	1K (A0–A9)	1K (A0–A9)
Module rank addressing	1 (S0#)	1 (S0#)	1 (S0#)

Table 2: Key Timing Parameters

Speed Grade	Data Rate (MT/s)			^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
	CL = 3	CL = 4	CL = 5			
-667	–	533	667	15	15	55
-53E	400	533	–	15	15	55
-40E	400	400	–	15	15	55

Table 3: Part Numbers and Timing Parameters

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT9HVF3272(P)KY-667__	256MB	32 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HVF3272(P)KY-53E__	256MB	32 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HVF3272(P)KY-40E__	256MB	32 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9HVF6472(P)KY-667__	512MB	64 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HVF6472(P)KY-53E__	512MB	64 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HVF6472(P)KY-40E__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9HVF12872(P)KY-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HVF12872(P)KY-53E__	1GB	128 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HVF12872(P)KY-40E__	1GB	128 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes: 1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT9HVF6472Y-40EC2.

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Pin Assignments and Descriptions

Table 4: Pin Assignments

244-Pin MiniDIMM Front								244-Pin MinDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	32	VSS	63	VDDQ	94	DQS5#	123	VSS	154	DQ28	185	A3	216	NC/RDQS#5
2	VSS	33	DQ24	64	A2	95	DQS5	124	DQ4	155	DQ29	186	A1	217	VSS
3	DQ0	34	DQ25	65	VDD	96	VSS	125	DQ5	156	VSS	187	VDD	218	DQ46
4	DQ1	35	VSS	66	VSS	97	DQ42	126	VSS	157	DM3/RDQS3	188	CK0	219	DQ47
5	VSS	36	DQS3#	67	VSS	98	DQ43	127	DM0/RDQS0	158	NC/RDQS#3	189	CK0#	220	VSS
6	DQS0#	37	DQS3	68	PAR_IN/NC	99	VSS	128	NC/RDQS#0	159	VSS	190	VDD	221	DQ52
7	DQS0	38	VSS	69	VDD	100	DQ48	129	VSS	160	DQ30	191	A0	222	DQ53
8	VSS	39	DQ26	70	A10/AP	101	DQ49	130	DQ6	161	DQ31	192	BA1	223	VSS
9	DQ2	40	DQ27	71	BA0	102	VSS	131	DQ7	162	VSS	193	VDD	224	RFU
10	DQ3	41	VSS	72	VDD	103	SA2	132	VSS	163	CB4	194	RAS#	225	RFU
11	VSS	42	CB0	73	WE#	104	NC (Test)	133	DQ12	164	CB5	195	VDDQ	226	VSS
12	DQ8	43	CB1	74	VDDQ	105	VSS	134	DQ13	165	VSS	196	S0#	227	DM6/RDQS6
13	DQ9	44	VSS	75	CAS#	106	DQS6#	135	VSS	166	DM8/RDQS8	197	VDDQ	228	NC/RDQS#6
14	VSS	45	DQS8#	76	VDDQ	107	DQS6	136	DM1/RDQS1	167	NC/RDQS#8	198	ODT0	229	VSS
15	DQS1#	46	DQS8	77	NC	108	VSS	137	NC/RDQS#1	168	VSS	199	NC/A13	230	DQ54
16	DQS1	47	VSS	78	NC	109	DQ50	138	VSS	169	CB6	200	VDD	231	DQ55
17	VSS	48	CB2	79	VDDQ	110	DQ51	139	RFU	170	CB7	201	NC	232	VSS
18	Reset#	49	CB3	80	NC	111	VSS	140	RFU	171	VSS	202	VSS	233	DQ60
19	NC	50	VSS	81	VSS	112	DQ56	141	VSS	172	NC	203	DQ36	234	DQ61
20	VSS	51	NC	82	DQ32	113	DQ57	142	DQ14	173	VDDQ	204	DQ37	235	VSS
21	DQ10	52	VDDQ	83	DQ33	114	VSS	143	DQ15	174	NC	205	VSS	236	DM7/RDQS7
22	DQ11	53	CKE0	84	VSS	115	DQS7#	144	VSS	175	VDD	206	DM4/RDQS4	237	NC/RDQS#7
23	VSS	54	VDD	85	DQS4#	116	DQS7	145	DQ20	176	NC	207	NC/RDQS#4	238	VSS
24	DQ16	55	NC/BA2	86	DQS4	117	VSS	146	DQ21	177	NC	208	VSS	239	DQ62
25	DQ17	56	ERR_OUT/NC	87	VSS	118	DQ58	147	VSS	178	VDDQ	209	DQ38	240	DQ63
26	VSS	57	VDDQ	88	DQ34	119	DQ59	148	DM2/RDQS2	179	A12	210	DQ39	241	VSS
27	DQS2#	58	A11	89	DQ35	120	VSS	149	NC/RDQS#2	180	A9	211	VSS	242	SDA
28	DQS2	59	A7	90	VSS	121	SA0	150	VSS	181	VDD	212	DQ44	243	SCL
29	VSS	60	VDD	91	DQ40	122	SA1	151	DQ22	182	A8	213	DQ45	244	VDDSPD
30	DQ18	61	A5	92	DQ41			152	DQ23	183	A6	214	VSS		
31	DQ19	62	A4	93	VSS			153	VSS	184	VDDQ	215	DM5/RDQS5		

Note: Pin 199 is NC for 256MB or A13 for 512MB and 1GB.

Figure 2: Pin Locations

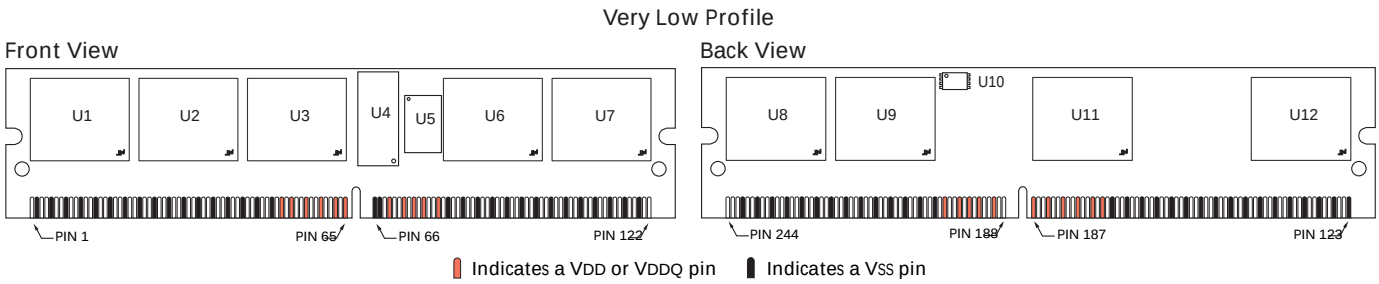

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Table 5: Pin Descriptions

Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 6 for more information

Pin Numbers	Symbol	Type	Description
198	ODT0	Input	On-Die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, RDQS, RDQS#, CB, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
188, 189	CK0, CK0#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
53	CKE0	Input	Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all device banks idle), or ACTIVE power-down (row ACTIVE in any device bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF REFRESH operation V_{REF} must be maintained to this input.
196	S0#	Input	Chip select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
73, 75, 194	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
55 (1GB), 71, 192	BA0, BA1, BA2 (1GB)	Input	Bank address inputs: BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.
58, 59, 61, 62, 64, 70, 179, 180, 182, 183, 185, 186, 191, 199 (512MB, 1GB)	A0–A12 (256MB) A0-A13 (512MB, 1GB)	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for Read/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.

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Table 5: Pin Descriptions

Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 6 for more information

Pin Numbers	Symbol	Type	Description
3, 4, 9, 10, 12, 13, 21, 22, 24, 25, 30, 31, 33, 34, 39, 40, 82, 83, 88, 89, 91, 92, 97, 98, 100, 101, 109, 110, 112, 113, 118, 119, 124, 125, 130, 131, 133, 134, 142, 143, 145, 146, 151, 152, 154, 155, 160, 161, 203, 204, 209, 210, 212, 213, 218, 219, 221, 222, 230, 231, 233, 234, 239, 240	DQ0–DQ63	I/O	Data input/output: Bidirectional data bus.
6, 7, 15, 16, 27, 28, 36, 37, 45, 46, 85, 86, 94, 95, 106, 107, 115, 116	DQS0–DQS8	I/O	Data strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
127, 136, 148, 157, 166, 206, 215, 227, 236	DM0/RDQS0–DM8/RDQS8	I/O	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. If RDQS is disabled, DQS0–DQS17 become DM0–DM8 and DQS#9–DQS#17 are not used (NC).
128, 137, 149, 158, 167, 207, 216, 228, 237	RDQS#0–RDQS#8	I/O	Redundant DQS: If RDQS is disabled, DQS0–DQS17 become DM0–DM8 and DQS#9–DQS#17 are not used (NC).
42, 43, 48, 49, 163, 164, 169, 170	CB0–CB7	I/O	Check bits.
68 (NC for non-parity)	PAR_IN	Input	Parity bit for the address and control bus.
56 (NC for non-parity)	ERR_OUT	Output	Parity error found on the address and control bus.
243	SCL	Input	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
103, 121, 122	SA0–SA2	Input	Presence-Detect address inputs: These pins are used to configure the presence-detect device.
242	SDA	I/O	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
18	Reset#	Input	Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.
54, 60, 65, 69, 72, 175, 181, 187, 190, 193, 200	VDD	Supply	Power supply: 1.8V ±0.1V.
52, 57, 63, 74, 76, 79, 173, 178, 184, 195, 197	VDDQ	Supply	DQ power supply: 1.8V ±0.1V.
1	VREF	Supply	SSTL_18 reference voltage.

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Table 5: Pin Descriptions

Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 6 for more information

Pin Numbers	Symbol	Type	Description
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 66, 67, 81, 84, 87, 90, 93, 96, 99, 102, 105, 108, 111, 114, 117, 120, 123, 126, 129, 132, 135, 138, 141, 144, 147, 150, 153, 156, 159, 162, 165, 168, 171, 202, 205, 208, 211, 214, 217, 220, 223, 226, 229, 232, 235, 238, 241	V_{SS}	Supply	Ground.
244	V_{DDSPD}	Supply	Serial EEPROM positive power supply: +1.7V to +3.6V.
19, 51, 55, 77, 78, 80, 104, 128, 137, 149, 158, 167, 172, 174, 176, 177, 199 (256MB), 201, 207, 216, 228, 237	NC	–	No connect: These pins should be left unconnected.
139, 140, 224, 225	RFU	–	Reserved for future use.

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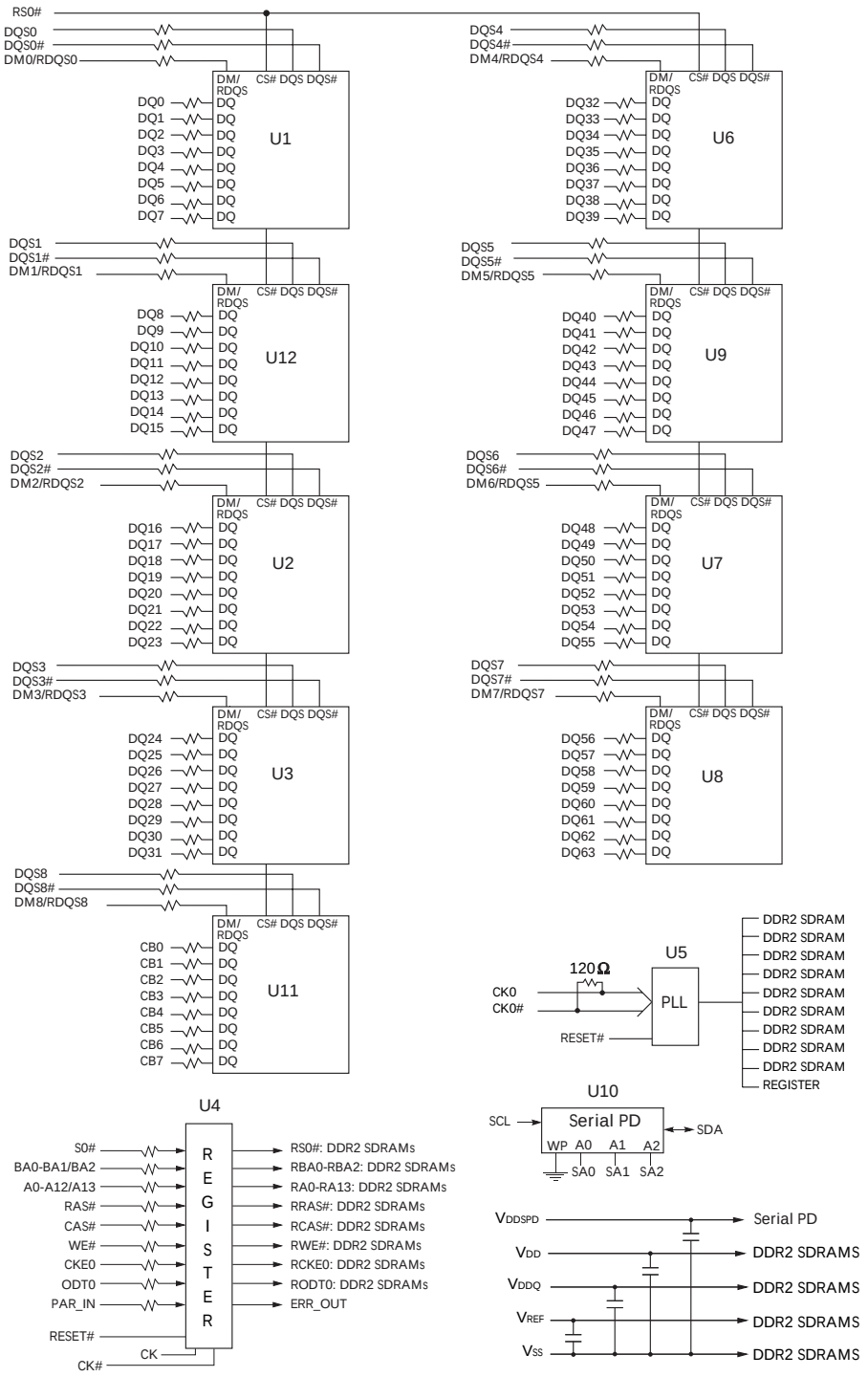
Functional Block Diagram

Unless otherwise noted, resistor values are 22Ω. Micron module part numbers are explained in the Module Part Numbering Guide at www.micron.com/numberguide. Modules use the following DDR2 SDRAM devices: MT47H32M8BP (256MB); MT47H64M8BT (512MB); and MT47H128M8BT (1GB).

Figure 3: Functional Block Diagram



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General Description

The MT9HVF3272(P)K, MT9HVF6472(P)K, and MT9HVF12872(P)K DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 256MB, 512MB, and 1GB memory modules organized in x72 configuration. DDR2 SDRAM modules use internally configured quad-bank DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to DDR2 SDRAM modules are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting column location for the burst access.

DDR2 SDRAM modules provide for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM devices support interrupting a burst read of eight with another read, or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR2 SDRAM devices allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

PLL and Register Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The registers and PLL minimize system and clock loading. Registered mode will add one clock cycle to CL.

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Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Initialization

The following sequence is required for power-up and initialization and is shown in Figure 4 on page 13.

1. Apply power; if CKE is maintained below 20 percent of $V_{DD}Q$, outputs remain disabled. To guarantee R_{TT} (ODT resistance) is off, V_{REF} must be valid and LOW must be applied to the ODT pin (all other inputs may be undefined). The time from when V_{DD} first starts to power up to the completion of $V_{DD}Q$ must be equal to or less than 20ms. At least one of the following two sets of conditions (A or B) must be met:
   A. V_{DD}, $V_{DD}L$ and $V_{DD}Q$ are driven from a single power converter output
      - V_{TT} is limited to 0.95V MAX
      - V_{REF} tracks $V_{DD}Q/2$
   B. Apply V_{DD} before or at the same time as $V_{DD}L$.
      - Apply $V_{DD}L$ before or at the same time as $V_{DD}Q$
      - Apply $V_{DD}Q$ before or at the same time as V_{TT} and V_{REF}
2. The voltage difference between any V_{DD} supply can not exceed 0.3V. For a minimum of 200µs after stable power and clock (CK, CK#), apply NOP or DESELECT commands and take CKE HIGH.
3. Wait a minimum of 400ns, then issue a PRECHARGE ALL command.
4. Issue a LOAD MODE command to the EMR(2) register. (To issue an EMR(2) command, provide LOW to BA0 and BA2, provide HIGH to BA1.)
5. Issue a LOAD MODE command to the EMR(3) register. (To issue an EMR(3) command, provide HIGH to BA0 and BA1, provide LOW to BA2.)
6. Issue a LOAD MODE command to the EMR register to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1, BA2, and A0, provide HIGH to BA0. Bits E7, E8, and E9 must all be set to 0.
7. Issue a LOAD MODE command for DLL reset. 200 cycles of clock input is required to lock the DLL. (To issue a DLL reset, provide HIGH to A8 and provide LOW to BA2, BA1 and BA0.) CKE must be HIGH the entire time.
8. Issue PRECHARGE ALL command.
9. Issue two or more REFRESH commands.
10. Issue a LOAD MODE command with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL).
11. Issue a LOAD MODE command to the EMR to enable OCD default by setting Bits E7, E8, and E9 to 1 and set all other desired parameters.
12. Issue a LOAD MODE command to the EMR to enable OCD exit by setting Bits E7, E8, and E9 to 0 and set all other desired parameters.

The DDR2 SDRAM device is now intialized and ready for normal operation 200 clocks after DLL reset in step 7.

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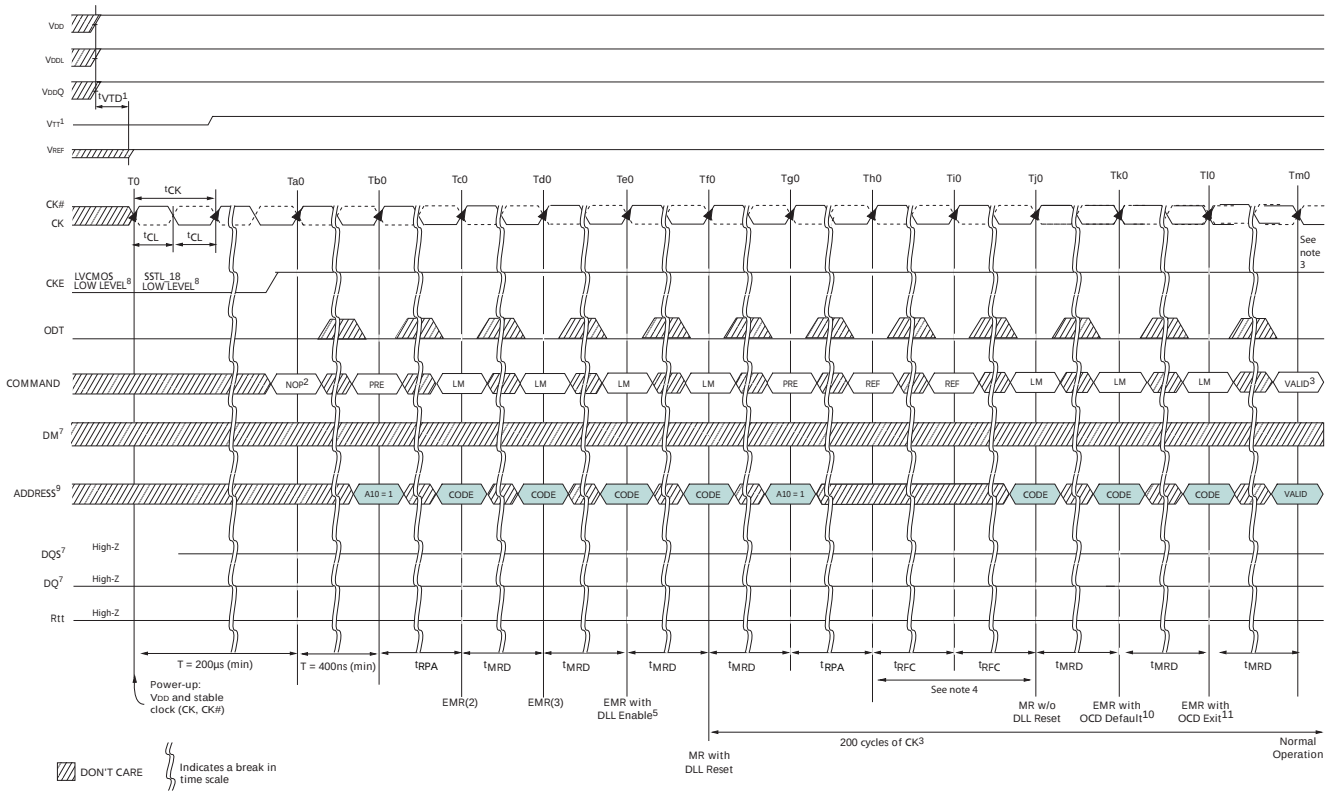
Figure 4: DDR2 Power-Up and Initialization



Notes:
1. VTT is not applied directly to the device; however, tVTD should be greater than or equal to zero to avoid device latch-up.
   The time from when VDD first starts to power-up to the completion of VDDQ must be equal to or less than 20ms. One of the following two conditions (A or B) MUST be met:
   A. VDD, VDDL, and VDDQ are driven from a single power converter output.
      VTT may be 0.95V maximum during power up.
      VREF tracks VDDQ/2.
   B. Apply VDD before or at the same time as VDDL.
      Apply VDDL before or at the same time as VDDQ.
      Apply VDDQ before or at the same time as VTT and VREF. The voltage difference between any VDD supply can not exceed 0.3V.
2. Either a NOP or DESELECT command may be applied.
3. 200 cycles of clock (CK, CK#) are required before a READ command can be issued. CKE must be HIGH the entire time.
4. Two or more REFRESH commands are required.
5. Bits E7, E8, and E9 must all be set to 0 with all other operating parameters of EMRS set as required.
6. PRE = PRECHARGE command, LM = LOAD MODE command, REF = REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Bank Address.
7. DM represents all DM. DQS represents all DQS, DQS#, RDQS,and RDQS# (RDQS/RDQS# only functional on RDIMMs using x8 components). DQ represents all DQ.
8. CKE pin uses LVCMOS input levels prior to state T0. After state T0, CKE pin uses SSTL_18 input levels.
9. A10 should be HIGH at states Tb0 and Tg0 to ensure a PRECHARGE (all banks) command is issued.
10. Bits E7, E8, and E9 must be set to 1 to set OCD default.
11. Bits E7, E8, and E9 must be set to 0 to set OCD exit and all other operating parameters of EMRS set as required.

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Mode Register (MR)

The mode register is used to define the specific mode of operation of the DDR2 SDRAM device. This definition includes the selection of a burst length (BL), burst type, CAS latency (CL), operating mode, DLL reset, write recovery, and power-down mode as shown in Figure 5, Mode Register (MR) Definition. Contents of the mode register can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables (M0–M14) must be programmed when the LOAD MODE command is issued.

The mode register is programmed via the LM command (bits BA0–BA1/BA2 all = 0) and other bits (M0–M13 or will retain the stored information until it is programmed again or the device loses power (except for bit M8, which is self-clearing). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The LOAD MODE command can only be issued (or reissued) when all banks are in the precharged state. The controller must wait the specified time ^{t}MRD before initiating any subsequent operations such as an ACTIVE command. Violating either of these requirements will result in unspecified operation.

Burst Length

Burst length is defined by bits M0–M2 as shown in Figure 5 on page 15. Read and write accesses to the DDR2 SDRAM device are burst-oriented, with BL being programmable to either four or eight. The BL determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to BL is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–A*i* when BL = 4 and by A3–A*i* when BL = 8 (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed BL applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3 as shown in Figure 5 on page 15. The ordering of accesses within a burst is determined by BL, the burst type, and the starting column address as shown in Table 6 on page 16. DDR2 SDRAM devices support 4-bit burst and 8-bit burst modes only. For 8-bit burst mode, full interleave address ordering is supported; however, sequential address ordering is nibble-based.

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Figure 5: Mode Register (MR) Definition

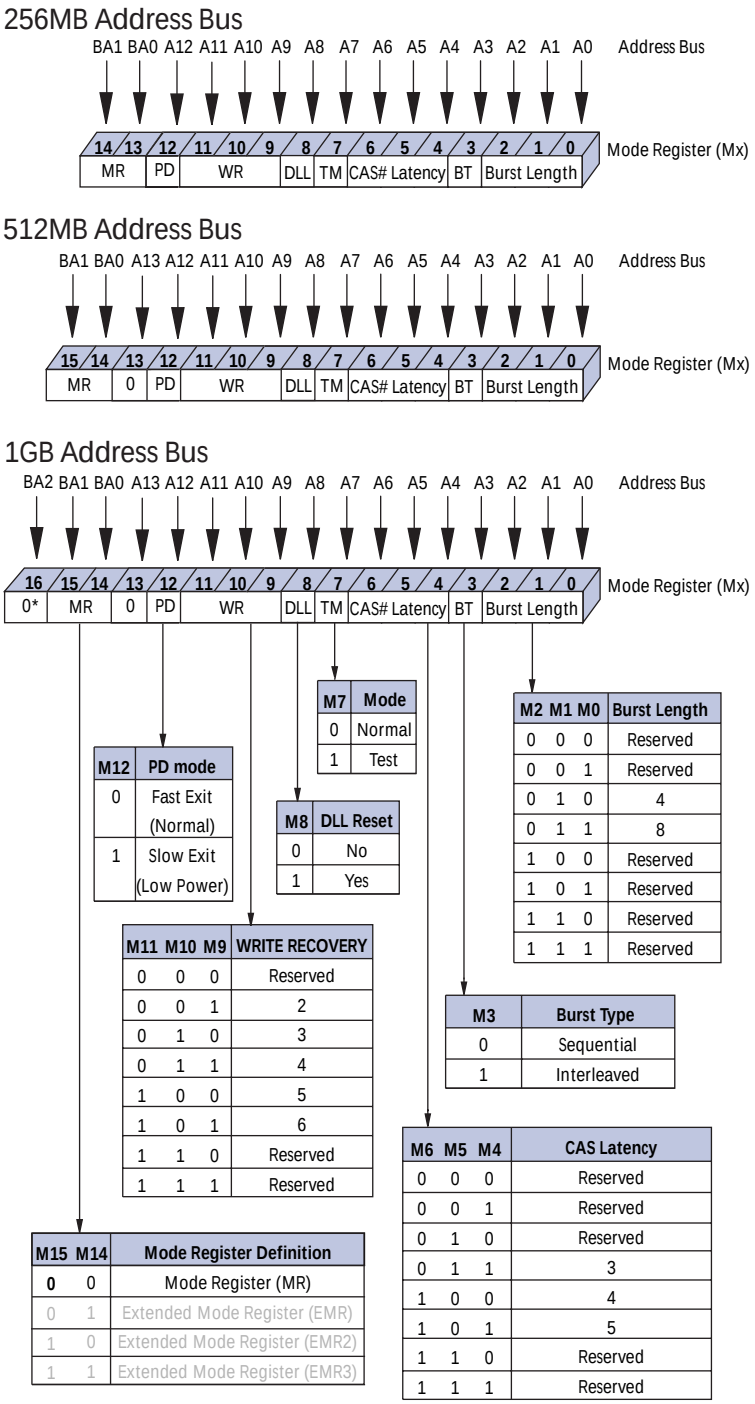

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Table 6: Burst Definition

BursT Length	Starting Column Address (A2, A1, A0)	Order of Accesses Within a Burst	
		Burst Type = Sequential	burst type = Interleaved
4	0 0 0	0,1,2,3	0,1,2,3
	0 0 1	1,2,3,0	1,0,3,2
	0 1 0	2,3,0,1	2,3,0,1
	0 1 1	3,0,1,2	3,2,1,0
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6
	0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5
	0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4
	1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2
	1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1
	1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0

Operating Mode

The normal operating mode is selected by issuing a LOAD MODE command with bit M7 set to zero, and all other bits set to the desired values as shown in Figure 5 on page 15. When bit M7 is ‘1,’ no other bits of the mode register are programmed. Programming bit M7 to ‘1’ places the DDR2 SDRAM device into a test mode that is only used by the Manufacturer and should NOT be used. No operation or functionality is guaranteed if M7 bit is ‘1.’

DLL Reset

DLL reset is defined by bit M8 as shown in Figure 5. Programming bit M8 to ‘1’ will activate the DLL RESET function. Bit M8 is self-clearing, meaning it returns back to a value of ‘0’ after the DLL RESET function has been issued.

Anytime the DLL RESET function is used, 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Write Recovery

Write recovery (WR) time is defined by bits M9–M11 as shown in Figure 5. The WR Register is used by the DDR2 SDRAM device during WRITE with AUTO PRECHARGE operation. During WRITE with AUTO PRECHARGE operation, the DDR2 SDRAM device delays the internal AUTO PRECHARGE operation by WR clocks (programmed in bits M9–M11) from the last data burst.

Write Recovery (WR) values of 2, 3, 4, 5, or 6 clocks may be used for programming bits M9–M11. The user is required to program the value of write recovery, which is calculated by dividing ^{t}WR (in ns) by ^{t}CK (in ns) and rounding up a noninteger value to the next integer; WR [cycles] = ^{t}WR [ns] / ^{t}CK [ns]. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

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Power-Down Mode

Active power-down (PD) mode is defined by bit M12 as shown in Figure 5 on page 15. PD mode allows the user to determine the active power-down mode, which determines performance vs. power savings. PD mode bit M12 does not apply to precharge power-down mode.

When bit M12 = 0, standard active power-down mode or 'fast-exit' active power-down mode is enabled. The ^{t}XARD parameter is used for 'fast-exit' active power-down exit timing. The DLL is expected to be enabled and running during this mode.

When bit M12 = 1, a lower power active power-down mode or 'slow-exit' active power-down mode is enabled. The ^{t}XARDS parameter is used for 'slow-exit' active power-down exit timing. The DLL can be enabled, but 'frozen' during active power-down mode since the exit-to-READ command timing is relaxed. The power difference expected between PD 'normal' and PD 'low-power' mode is defined in the IDD table.

CAS Latency

The CL is defined by bits M4–M6 as shown in Figure 5. CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The CL can be set to 3, 4, or 5 clocks. CL of 6 clocks is a JEDEC optional feature and may be enabled in future speed grades. DDR2 SDRAM devices do not support any half-clock latencies. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

DDR2 SDRAM devices also support a feature called posted CAS additive latency (AL). This feature allows the READ command to be issued prior to ^{t}RCD(MIN) by delaying the internal command to the DDR2 SDRAM device by AL clocks. The AL feature is described in more detail in the Extended Mode Register (EMR) and Operational sections.

Examples of CL = 3 and CL = 4 are shown in Figure 6, CAS Latency; both assume AL = 0. If a READ command is registered at clock edge *n*, and the CAS latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m* (this assumes AL = 0).

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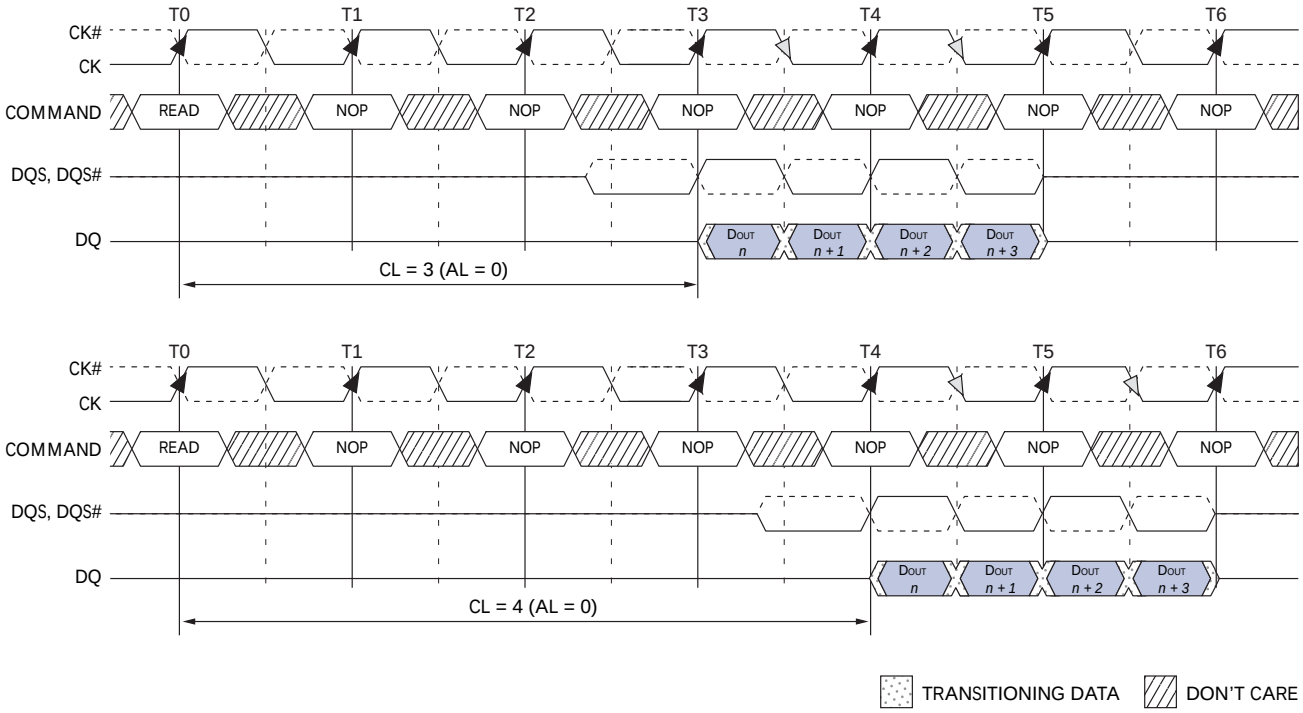
Figure 6: CAS Latency



Notes: 1. BL = 4.
2. Posted CAS additive latency (AL = 0).
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ

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Extended Mode Register (EMR)

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, ODT (RTT), posted CAS additive latency (AL), off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and OUTPUT disable/enable. These functions are controlled via the bits shown in Figure 7 on page 20. The extended mode register is programmed via the LOAD MODE (LM) command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

DLL Enable/Disable

The DLL may be enabled or disabled by programming bit E0 during the LOAD MODE command as shown in Figure 7 on page 20. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using a LOAD MODE command.

The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled and reset upon exit of self refresh operation.

Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Output Drive Strength

The output drive strength is defined by bit E1 as shown in Figure 7, Extended Mode Register Definition. The normal drive strength for all outputs are specified to be SSTL_18. Programming bit E1 = 0 selects normal (100 percent) drive strength for all outputs. Selecting a reduced drive strength option (bit E1 = 1) will reduce all outputs to approximately 60 percent of the SSTL_18 drive strength. This option is intended for the support of the lighter load and/or point-to-point environments.

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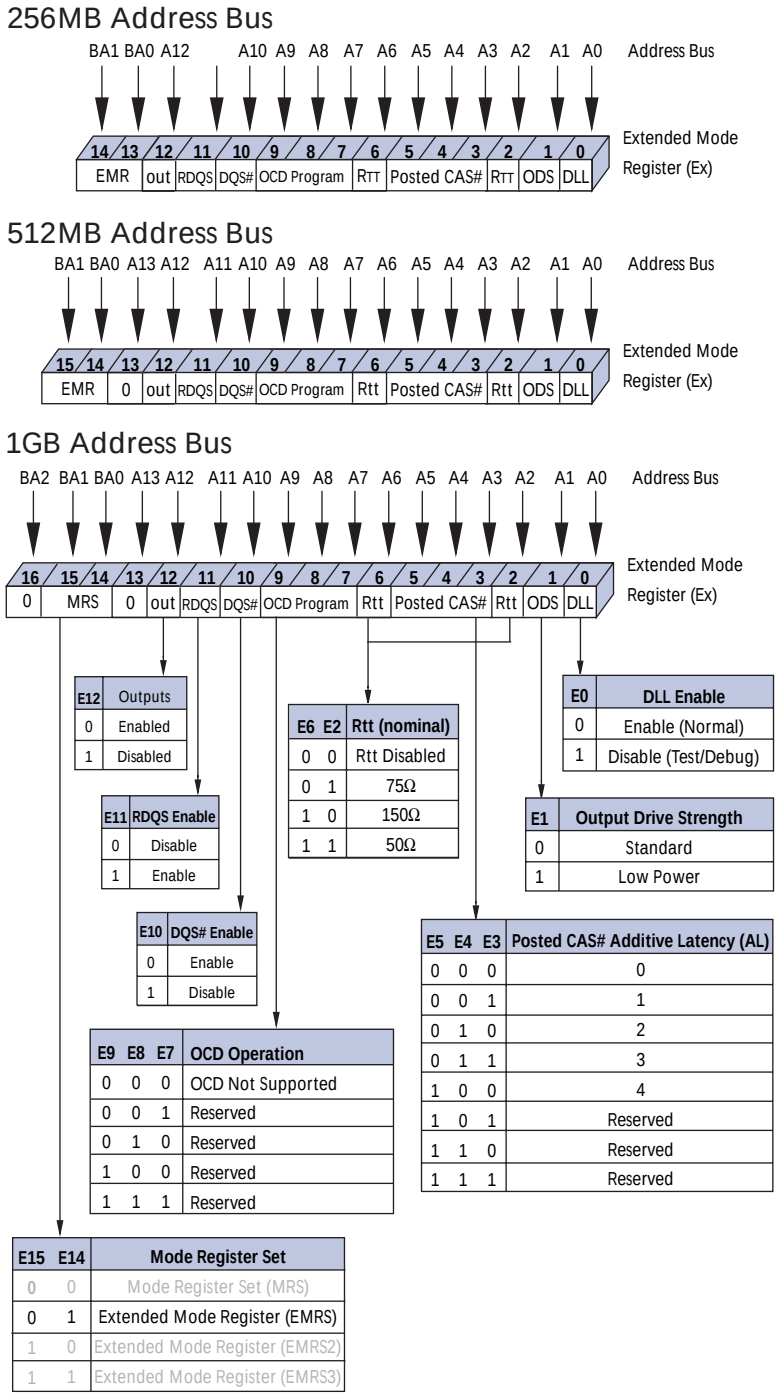
Figure 7: Extended Mode Register Definition



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DQS# Enable/Disable

The DQS# enable function is defined by bit E10. When enabled (bit E10 = 0), DQS# is the complement of the differential data strobe pair DQS/DQS#. When disabled (bit E10 = 1), DQS is used in a single-ended mode and the DQS# pin is disabled. This function is also used to enable/disable RDQS#. If RDQS is enabled (E11 = 1) and DQS# is enabled (E10 = 0), then both DQS# and RDQS# will be enabled. RDQS/RDQS# is supported only on RDIMMs using x8 DDR2 SDRAM devices.

RDQS Enable/Disable

RDQS/RDQS# is supported only on RDIMMs using x8 DDR2 SDRAM devices. The RDQS enable function is defined by bit E11 as shown in Figure 7 on page 20. When enabled (E11 = 1), RDQS is identical in function and timing to data strobe DQS during a READ. During a WRITE operation, RDQS is ignored by the DDR2 SDRAM device.

Output Enable/Disable

The OUTPUT enable function is defined by bit E12 as shown in Figure 7. When enabled (E12 = 0), all outputs (DQs, DQS, DQS#, RDQS, RDQS#) function normally. When disabled (E12 = 1), all DDR2 SDRAM device outputs (DQs, DQS, DQS#, RDQS, RDQS#) are disabled removing output buffer current. The OUTPUT disable feature is intended to be used during I_{DD} characterization of read current.

On Die Termination (ODT)

ODT effective resistance $R_{TT(EFF)}$ is defined by bits E2 and E6 of the EMR as shown in Figure 7. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DDR2 SDRAM device controller to independently turn on/off ODT for any or all devices. R_{TT} effective resistance values of 75Ω and 150Ω are selectable and apply to each DQ, DQS/DQS#, RDQS/RDQS#, and DM signals. Additionally, the -667 speed modules offer a third option of 50Ω. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

The ODT control pin is used to determine when $R_{TT(EFF)}$ is turned on and off, assuming ODT has been enabled via bits E2 and E6 of the EMR. The ODT feature and ODT input pin are only used during active, active power-down (both fast-exit and slow-exit modes), and precharge power-down modes of operation. If SELF REFRESH operation is used, $R_{TT(EFF)}$ should *always* be disabled and the ODT input pin is disabled by the DDR2 SDRAM device. During power-up and initialization of the DDR2 SDRAM device, ODT should be disabled until the EMR command is issued to enable the ODT feature, at which point the ODT pin will determine the $R_{TT(EFF)}$ value. Refer to the 256Mb, 512Mb, or 1Gb DDR2 SDRAM discrete data sheet for ODT timing diagrams.

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Off-Chip Driver (OCD) Impedance Calibration

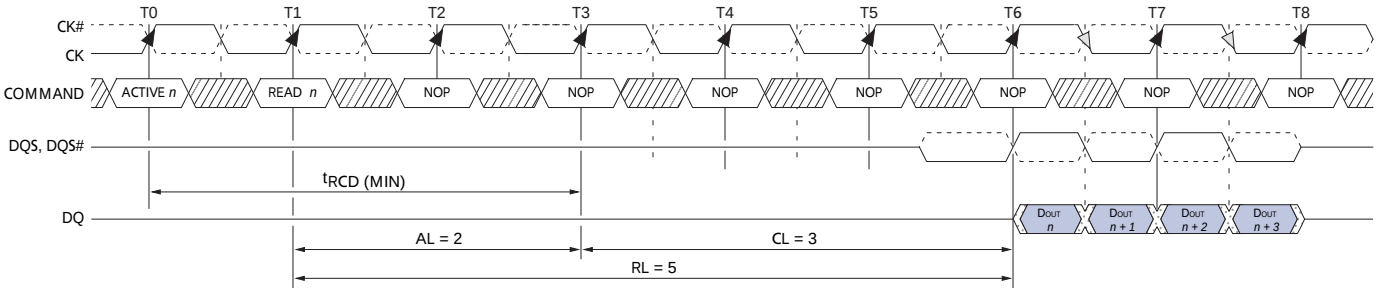
The OCD function is not supported and must be set to the default state. See "Initialization" on page 12, to properly set OCD defaults.

Posted CAS Additive Latency

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR2 SDRAM device. Bits E3–E5 define the value of AL as shown in Figure 7 on page 20. Bits E3–E5 allow the user to program the DDR2 SDRAM device with an AL of 0, 1, 2, 3, or 4 clocks. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

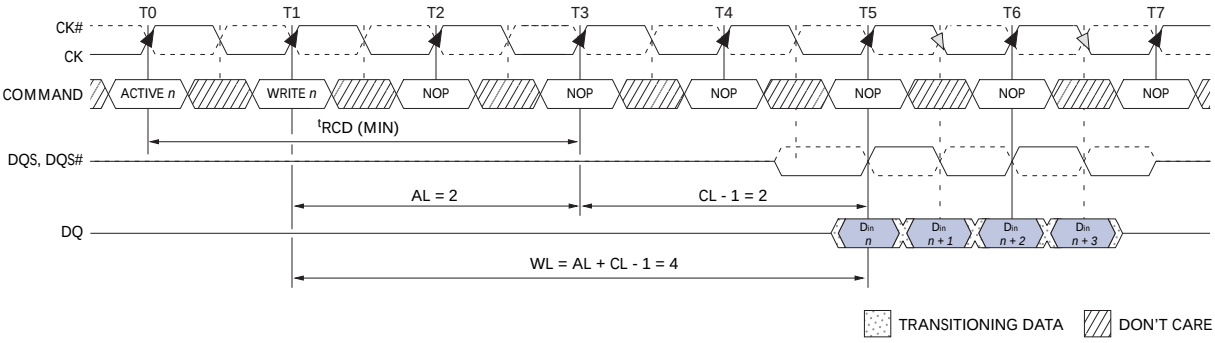
In this operation, the DDR2 SDRAM device allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) with the requirement that AL ≤ ^{t}RCD(MIN). A typical application using this feature would set AL = ^{t}RCD (MIN) - 1 × ^{t}CK. The READ or WRITE command is held for the time of the additive latency (AL) before it is issued internally to the DDR2 SDRAM device. RL is controlled by the sum of the posted AL and CL; RL = AL + CL. Write latency (WL) is equal to RL minus one clock; WL = AL + CL - 1 × ^{t}CK. An example of RL is shown in Figure 8. An example of WL is shown in Figure 9.

Figure 8: READ Latency



Notes: 1. BL = 4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
2. CL = 3
AL = 2
RL = AL + CL = 5.

Figure 9: Write Latency



Notes: 1. BL = 4.
2. CL = 3
AL = 2
WL = AL + CL -1 = 4.

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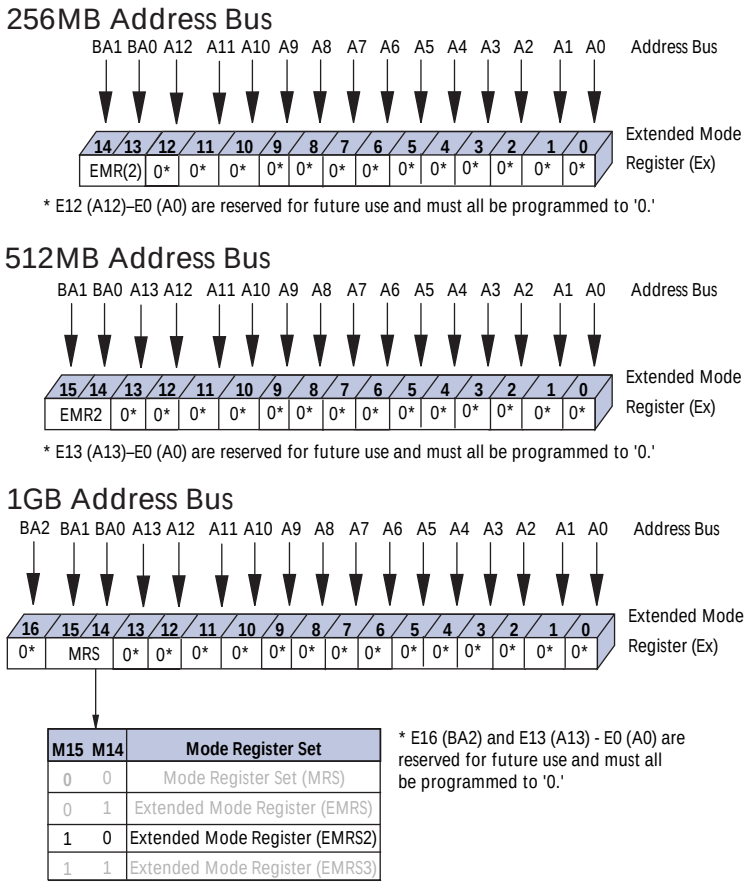
Extended Mode Register 2 (EMR2)

The extended mode register 2 (EMR2) controls functions beyond those controlled by the mode register. Currently all bits in EMR2 are reserved as shown in Figure 10. The EMR2 is programmed via the LOAD MODE command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 10: Extended Mode Register 2 (EMR2) Definition



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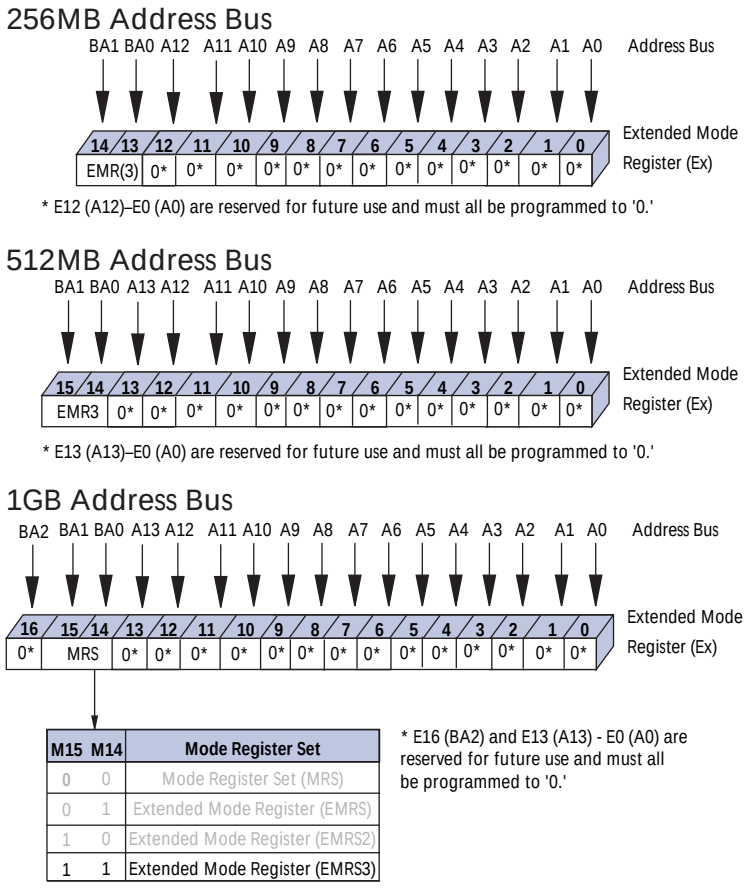
Extended Mode Register 3 (EMR3)

The extended mode register 3 (EMR3) controls functions beyond those controlled by the mode register. Currently all bits in EMR3 are reserved as shown in Figure 11. The EMR3 is programmed via the LOAD MODE command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 11: Extended Mode Register 3 (EMR3) Definition



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Command Truth Tables

Table 7 provides a quick reference of DDR2 SDRAM device available commands. Refer to the 256Mb, 512Mb, or 1Gb DDR2 SDRAM component data sheet for more Truth Table definitions, including CKE power-down modes and device bank-to-bank commands.

Table 7: Commands Truth Table
Notes: 1, 5, 6

Function	CKE		S#	RAS#	CAS#	WE#	BA2[8], BA1, BA0	A13[8]–A11	A10	A9–A0	Notes
	Previous Cycle	Current Cycle									
Mode Register Set	H	H	L	L	L	L	BA	OP Code			2
Refresh	H	H	L	L	L	H	X	X	X	X	
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	
Self Refresh Exit	L	H	X	X	X	X	X	X	X	X	7
			L	H	H	H	X	X	X	X	
Single Device Bank Precharge	H	H	L	L	H	L	BA	X	L	X	2
ALL Device Banks Precharge	H	H	L	L	H	L	X	X	H	X	
Device Bank Activate	H	H	L	L	H	H	BA	Row Address			2
Write	H	H	L	H	L	L	BA	Column Address	L	Column Address	2, 3
Write with Auto Precharge	H	H	L	H	L	L	BA	Column Address	H	Column Address	2, 3
Read	H	H	L	H	L	H	BA	Column Address	L	Column Address	2, 3
Read with Auto Precharge	H	H	L	H	L	H	BA	Column Address	H	Column Address	2, 3
No Operation	H	X	L	H	H	H	X	X	X	X	
Device Deselect	H	X	H	X	X	X	X	X	X	X	
Power-Down Entry	H	L	H	X	X	X	X	X	X	X	4
			L	H	H	H	X	X	X	X	
Power-Down Exit	L	H	H	X	X	X	X	X	X	X	4
			L	H	H	H	X	X	X	X	

Notes:
1. All DDR2 SDRAM device commands are defined by states of S#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock.
2. Device Bank addresses (BA) BA0–BA1/BA2 determine which device bank is to be operated upon. For EMR, BA selects an extended mode register.
3. Burst reads or writes at BL = 4 cannot be terminated or interrupted. Refer to the 256Mb, 512Mb, or 1Gb DDR2 SDRAM discrete data sheet for other restrictions or details.
4. The Power Down Mode does not perform any refresh operations. The duration of power-down is therefore limited by the refresh requirements outlined in the AC parametric section.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh. Refer to the 256Mb, 512Mb, or 1Gb DDR2 SDRAM discrete data sheet for other restrictions or details.
6. "X" means "H or L" (but a defined logic level).
7. Self refresh exit is asynchronous.
8. BA2 valid for 1GB only; A13 valid for 512MB and 1GB only.

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Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 8: Absolute Maximum DC Ratings

Parameter		Symbol	Min	Max	Units
V_{DD} supply voltage relative to V_{SS}		V_{DD}	-1.0	2.3	V
V_{DDQ} supply voltage relative to V_{SS}		V_{DDQ}	-0.5	2.3	V
V_{DDL} supply voltage relative to V_{SS}		V_{DDL}	-0.5	2.3	V
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	-0.5	2.3	V
Storage temperature		T_{STG}	-55	100	°C
DDR2 SDRAM device operating temperature (ambient)		T_{case}	0	85	°C
Operating temperature (ambient)		T_{OPR}	0	55	°C
Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤0.95V; (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE# S#, CKE, CK, CK#, DM	I_I	-5	5	µA
Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQs and ODT are disabled	DQ, DQS, DQS#	I_{OZ}	-5	5	µA
V_{REF} leakage current; V_{REF} = Valid V_{REF} level		I_{VREF}	-18	18	µA

Table 9: Recommended DC Operating Conditions
All voltages referenced to V_{SS}

Parameter	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V_{DD}	1.7	1.8	1.9	V	1
V_{DDL} Supply Voltage	V_{DDL}	1.7	1.8	1.9	V	4
I/O Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	4
I/O Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.50 × V_{DDQ}	0.51 × V_{DDQ}	V	2
I/O Termination Voltage (system)	V_{TT}	V_{REF} - 40	V_{REF}	V_{REF} + 40	mV	3

Notes:
1. V_{DD} and V_{DDQ} must track each other. V_{DDQ} must be less than or equal to V_{DD}.
2. V_{REF} is expected to equal V_{DDQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±1percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of $V_{REF(DC)}$. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
4. V_{DDQ} tracks with V_{DD}; V_{DDL} tracks with V_{DD}.

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Table 10: Input DC Logic Levels
All voltages referenced to VSS

Parameter	Symbol	Min	Max	Units
Input high (Logic 1) voltage	VIH(DC)	VREF + 125	VDDQ + 300	mV
Input low (Logic 0) voltage	VIL(DC)	-300	VREF - 125	mV

Table 11: Input AC Logic Levels
All voltages referenced to VSS

Parameter	Symbol	Min	Max	Units
Input high (Logic 1) voltage (-40E/-53E)	VIH(AC)	VREF + 250	–	mV
Input high (Logic 1) voltage (-667)	VIH(AC)	VREF + 200	–	mV
Input low (Logic 0) voltage	VIL(AC)	–	VREF - 250	mV

IDD Specifications and Conditions

IDD specifications are tested after the device is properly initialized. 0°C ≤ T_{CASE} ≤ +85°C. VDD = VDDQ = VDDL = +1.8V ±0.1V; VREF=VDDQ/2.

Input slew rate is specified by AC Parametric Test Conditions. IDD parameters are specified with ODT disabled. Data bus consists of DQ, DM, DQS, DQS#. IDD values must be met with all combinations of EMR bits 10 and 11.

Definitions for IDD Conditions:

- LOW is defined as VIN ≤ VIL(AC) (MAX)
- HIGH is defined as VIN ≥ VIH(AC) (MIN)
- STABLE is defined as inputs stable at a HIGH or LOW level
- FLOATING is defined as inputs at VREF = VDDQ/2
- SWITCHING is defined as inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals
- Switching is defined as inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes

Table 12: General IDD Parameters

IDD Parameter		-667	-53E	-40E	Units
CL (IDD)		5	4	3	tCK
tRCD (IDD)		15	15	15	ns
tRC (IDD)		55	55	55	ns
tRRD (IDD)		7.5	7.5	7.5	ns
tCK (IDD)		3	3.75	5	ns
tRAS MIN (IDD)		45	45	40	ns
tRAS MAX (IDD)		70,000	70,000	70,000	ns
tRP (IDD)		15	15	15	ns
tRFC (IDD)	256MB	75	75	75	ns
	512MB	105	105	105	ns
	1GB	127.5	127.5	127.5	ns

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IDD7 Conditions

Table 13, and Table 14, specify detailed timing requirements for IDD7. Changes will be required if timing parameter changes are made to the specification.

Legend: A = active; RA = read auto precharge; D = deselect. All banks are being interleaved at minimum ^{t}RC (IDD) without violating ^{t}RRD (IDD) using a BL = 4. Control and address bus inputs are STABLE during DESELECTs. IOUT = 0mA.

Table 13: IDD7 Timing Patterns – 256MB and 512MB
All bank interleave READ operation

Speed Grade	IDD7 Timing Patterns
-40E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D
-53E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D
-667	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D

Table 14: IDD7 Timing Patterns – 1GB
All bank interleave READ operation

Speed Grade	IDD7 Timing Patterns
-40E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 A4 RA4 A5 RA5 A6 RA6 A7 RA7
-53E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D
-667	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D

Capacitance

At DDR2 data rates, Micron encourages designers to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

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Table 15: IDD Specifications and Conditions – 256MB
Values shown for DDR2 SDRAM components only

Parameter/Condition		Symbol	-667	-53E	-40E	Units
Operating one bank active-precharge current; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD0	810	720	675	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		IDD1	900	810	765	mA
Precharge power-down current; All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		IDD2P	45	45	45	mA
Precharge quiet standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		IDD2Q	360	315	225	mA
Precharge standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD2N	360	315	270	mA
Active power-down current; All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN exit MR[12] = 0	IDD3P	270	225	180	mA
	Slow PDN exit MR[12] = 1		54	54	54	mA
Active standby current; All device banks open; tCK = tCK(IDD), tRAS = tRAS MAX (IDD), tRP = tRP(IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD3N	450	360	270	mA
Operating burst write current; All device banks open, Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD4W	1,710	1,440	1,125	mA
Operating burst read current; All device banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD4R	1,620	1,350	1,035	mA
Burst refresh current; tCK = tCK (IDD); Refresh command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD5	1,620	1,530	1,485	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.		IDD6	45	45	45	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD)-1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = tRCD(IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See "IDD7 Conditions" on page 28 for details.		IDD7	2,340	2,160	2,070	mA

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Table 16: IDD Specifications and Conditions – 512MB
Values shown for DDR2 SDRAM components only

Parameter/Condition		Symbol	-667	-53E	-40E	Units
Operating one bank active-precharge current; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD0	810	720	720	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		IDD1	945	855	810	mA
Precharge power-down current; All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		IDD2P	45	45	45	mA
Precharge quiet standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		IDD2Q	450	360	315	mA
Precharge standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD2N	495	405	360	mA
Active power-down current; All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN exit MR[12] = 0	IDD3P	315	270	225	mA
	Slow PDN exit MR[12] = 1		90	90	90	mA
Active standby current; All device banks open; tCK = tCK(IDD), tRAS = tRAS MAX (IDD), tRP = tRP(IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD3N	585	495	405	mA
Operating burst write current; All device banks open, Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD4W	1,395	1,170	990	mA
Operating burst read current; All device banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD4R	1,575	1,305	1,035	mA
Burst refresh current; tCK = tCK (IDD); Refresh command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD5	1,890	1,800	1,710	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.		IDD6	45	45	45	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD)-1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = tRCD(IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See "IDD7 Conditions" on page 28 for details.		IDD7	2,520	2,340	2,070	mA

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Table 17: IDD Specifications and Conditions – 1GB
Values shown for DDR2 SDRAM components only

Parameter/Condition		Symbol	-667	-53E	-40E	Units
Operating one bank active-precharge current; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD0	900	720	720	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		IDD1	1,305	855	855	mA
Precharge power-down current; All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		IDD2P	63	45	45	mA
Precharge quiet standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		IDD2Q	540	369	315	mA
Precharge standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD2N	585	405	315	mA
Active power-down current; All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN exit MR[12] = 0	IDD3P	360	270	225	mA
	Slow PDN exit MR[12] = 1		45	45	45	mA
Active standby current; All device banks open; tCK = tCK(IDD), tRAS = tRAS MAX (IDD), tRP = tRP(IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD3N	630	450	360	mA
Operating burst write current; All device banks open, Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD4W	1,620	1,170	1,080	mA
Operating burst read current; All device banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD4R	1,845	1,305	1,215	mA
Burst refresh current; tCK = tCK (IDD); Refresh command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD5	2,430	2,250	2,160	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.		IDD6	63	45	45	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD)-1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = tRCD(IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See "IDD7 Conditions" on page 28 for details.		IDD7	3,060	2,655	2,655	mA

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AC Operating Specifications

Table 18: AC Operating Conditions (Sheet 1 of 4)

Notes: 1–5; notes appear on page 36; 0°C ≤ T_{CASE} ≤ +85°C; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V

AC Characteristics				-667		-53E		-40E		Units	Notes
Parameter			Symbol	Min	Max	Min	Max	Min	Max		
Clock	Clock cycle time	CL = 5	^tCK (5)	3,000	8,000	–	–	–	–	ps	16, 25
		CL = 4	^tCK (4)	3,750	8,000	3,750	8,000	5,000	8,000	ps	16, 25
		CL = 3	^tCK (3)	5,000	8,000	5,000	8,000	5,000	8,000	ps	16, 25
	CK high-level width		^tCH	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	19
	CK low-level width		^tCL	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	19
	Half clock period		^tHP	MIN (^tCH, ^tCL)		MIN (^tCH, ^tCL)		MIN (^tCH, ^tCL)		ps	20
	Clock jitter		^tJIT	-125	125	-125	125	-125	125	ps	18
Data	DQ output access time from CK/CK#		^tAC	-450	+450	-500	+500	-600	+600	ps	
	Data-out High-Z window from CK/CK#		^tHZ		^tAC (MAX)		^tAC (MAX)		^tAC (MAX)	ps	8, 9
	Data-out Low-Z window from CK/CK#		^tLZ	^tAC (MIN)	^tAC (MAX)	^tAC (MIN)	^tAC (MAX)	^tAC (MIN)	^tAC (MAX)	ps	8, 10
	DQ and DM input setup time relative to DQS		^tDS_a	300		350		400		ps	7, 15, 22
	DQ and DM input hold time relative to DQS		^tDH_a	300		350		400		ps	7, 15, 22
	DQ and DM input setup time relative to DQS		^tDS_b	100		100		150		ps	7, 15, 22
	DQ and DM input hold time relative to DQS		^tDH_b	175		225		275		ps	7, 15, 22
	DQ and DM input pulse width (for each input)		^tDIPW	0.35		0.35		0.35		^tCK	
	Data hold skew factor		^tQHS		340		400		450	ps	
	DQ–DQS hold, DQS to first DQ to go nonvalid, per access		^tQH	^tHP - ^tQHS		^tHP - ^tQHS		^tHP - ^tQHS		ps	15, 17
	Data valid output window (DVW)		^tDVW	^tQH - ^tDQSQ		^tQH - ^tDQSQ		^tQH - ^tDQSQ		ns	15, 17

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Table 18: AC Operating Conditions (Sheet 2 of 4)

Notes: 1–5; notes appear on page 36; 0°C ≤ T_{CASE} ≤ +85°C; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V

AC Characteristics			-667		-53E		-40E		Units	Notes
	Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Data Strobe	DQS input high pulse width	^{t}DQSH	0.35		0.35		0.35		^{t}CK	
	DQS input low pulse width	^{t}DQSL	0.35		0.35		0.35		^{t}CK	
	DQS output access time from CK/CK#	^{t}DQSCK	-400	+400	-450	+450	-500	+500	ps	
	DQS falling edge to CK rising – setup time	^{t}DSS	0.2		0.2		0.2		^{t}CK	
	DQS falling edge from CK rising – hold time	^{t}DSH	0.2		0.2		0.2		^{t}CK	
	DQS–DQ skew, DQS to last DQ valid, per group, per access	^{t}DQSQ		240		300		350	ps	15, 17
	DQS read preamble	^{t}RPRE	0.9	1.1	0.9	1.1	0.9	1.1	^{t}CK	36
	DQS read postamble	^{t}RPST	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	36
	DQS write preamble setup time	^{t}WPRES	0		0		0		ps	12, 13, 37
	DQS write preamble	^{t}WPRE	0.35		0.25		0.25		^{t}CK	
	DQS write postamble	^{t}WPST	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	11
	Write command to first DQS latching transition	^{t}DQSS	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	^{t}CK	

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Table 18: AC Operating Conditions (Sheet 3 of 4)

Notes: 1–5; notes appear on page 36; 0°C ≤ T_{CASE} ≤ +85°C; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC Characteristics			-667		-53E		-40E		Units	Notes
	Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Command and Address	Address and control input pulse width for each input	^tIPW	0.6		0.6		0.6		^tCK	
	Address and control input setup time	^tIS_a	400		500		600		ps	6, 22
	Address and control input hold time	^tIH_a	400		500		600		ps	6, 22
	Address and control input setup time	^tIS_b	200		250		350		ps	6, 22
	Address and control input hold time	^tIH_b	275		375		475		ps	6, 22
	CAS# to CAS# command delay	^tCCD	2		2		2		^tCK	
	ACTIVE to ACTIVE (same bank) command	^tRC	55		55		55		ns	34
	ACTIVE bank *a* to ACTIVE bank *b* command	^tRRD	7.5		7.5		7.5		ns	28
	ACTIVE to READ or WRITE delay	^tRCD	15		15		15		ns	
	Four Bank Activate period	^tFAW	37.5		37.5		37.5		ns	31
	ACTIVE to PRECHARGE command	^tRAS	40	70,000	40	70,000	40	70,000	ns	21, 34
	Internal READ to precharge command delay	^tRTP	7.5		7.5		7.5		ns	24, 28
	Write recovery time	^tWR	15		15		15		ns	28
	Auto precharge write recovery + precharge time	^tDAL	$^tWR + ^tRP$		$^tWR + ^tRP$		$^tWR + ^tRP$		ns	23
	Internal WRITE to READ command delay	^tWTR	10		7.5		10		ns	28
	PRECHARGE command period	^tRP	15		15		15		ns	32
	PRECHARGE ALL command period	^tRPA	$^tRP + ^tCK$		$^tRP + ^tCK$		$^tRP + ^tCK$		ns	32
	LOAD MODE command cycle time	^tMRD	2		2		2		^tCK	
	CKE low to CK,CK# uncertainty	^tDELAY	$^tIS + ^tCK + ^tIH$		$^tIS + ^tCK + ^tIH$		$^tIS + ^tCK + ^tIH$		ns	29
Self Refresh	REFRESH to Active or Refresh to Refresh command interval	^tRFC (256MB)	75	70,000	75	70,000	75	70,000	ns	14
		^tRFC (512MB)	105	70,000	105	70,000	105	70,000	ns	14
		^tRFC (1GB)	127.5	70,000	127.5	70,000	127.5	70,000	ns	14
	Average periodic refresh interval	^tREFI		7.8		7.8		7.8	µs	14
	Exit self refresh to non-READ command	^tXSNR	^tRFC (MIN) + 10		^tRFC (MIN) + 10		^tRFC (MIN) + 10		ns	
	Exit self refresh to READ command	^tXSRD	200		200		200		^tCK	
	Exit self refresh timing reference	^tISXR	^tIS		^tIS		^tIS		ps	6, 30

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Table 18: AC Operating Conditions (Sheet 4 of 4)

Notes: 1–5; notes appear on page 36; 0°C ≤ T_{CASE} ≤ +85°C; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V

AC Characteristics			-667		-53E		-40E		Units	Notes
	Parameter	Symbol	Min	Max	Min	Max	Min	Max		
ODT	ODT turn-on delay	^{t}AOND	2	2	2	2	2	2	^{t}CK	
	ODT turn-on	^{t}AON	^{t}AC (MIN)	^{t}AC (MAX) + 700	^{t}AC (MIN)	^{t}AC (MAX) + 1,000	^{t}AC (MIN)	^{t}AC (MAX) + 1000	ps	26
	ODT turn-off delay	^{t}AOFD	2.5	2.5	2.5	2.5	2.5	2.5	^{t}CK	
	ODT turn-off	^{t}AOF	^{t}AC (MIN)	^{t}AC (MAX) + 600	^{t}AC (MIN)	^{t}AC (MAX) + 600	^{t}AC (MIN)	^{t}AC (MAX) + 600	ps	27
	ODT turn-on (power-down mode)	^{t}AONPD	^{t}AC (MIN) + 2,000	2 × ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2000	2 × ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2 × ^{t}CK + ^{t}AC (MAX) + 1000	ps	
	ODT turn-off (power-down mode)	^{t}AOFPD	^{t}AC (MIN) + 2,000	2.5 × ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2.5 × ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2.5 × ^{t}CK + ^{t}AC (MAX) + 1,000	ps	
	ODT to power-down entry latency	^{t}ANPD	3		3		3		^{t}CK	
	ODT power-down exit latency	^{t}AXPD	8		8		8		^{t}CK	
Power-Down	Exit active power-down to READ command, MR[bit12 = 0]	^{t}XARD	2		2		2		^{t}CK	
	Exit active power-down to READ command, MR[bit12 = 1]	^{t}XARDS	7 - AL		6 - AL		6 - AL		^{t}CK	
	Exit precharge power-down to any non-READ command.	^{t}XP	2		2		2		^{t}CK	
	CKE minimum HIGH/LOW time	^{t}CKE	3		3		3		^{t}CK	35

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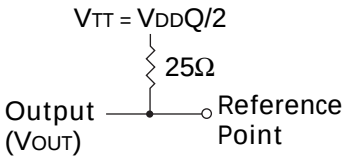
Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.0V in the test environment and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1.0V/ns for signals in the range between V_{IL}(AC) and V_{IH}(AC). Slew rates less than 1.0V/ns require the timing parameters to be derated as specified.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. Command/Address minimum input slew rate is at 1.0V/ns. Command/Address input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated using ^{t}ISb and the Setup and Hold Time Derating Values tables from the component data sheet. ^{t}IS timing ($^{t}IS_b$) is referenced from V_{IH}(AC) for a rising signal and V_{IL}(AC) for a falling signal. ^{t}IH timing ($^{t}IH_b$) is referenced from V_{IH}(AC) for a rising signal and V_{IL}(DC) for a falling signal. The timing table also lists the $^{t}IS_b$ and $^{t}IH_b$ values for a 1.0V/ns slew rate; these are the "base" values.
7. Data minimum input slew rate is at 1.0V/ns. Data input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated if the timing is referenced from the logic trip points. ^{t}DS timing ($^{t}DS_b$) is referenced from V_{IH}(AC) for a rising signal and V_{IL}(AC) for a falling signal. ^{t}IH timing ($^{t}IH_b$) is referenced from V_{IH}(DC) for a rising signal and V_{IL}(DC) for a falling signal. The timing table lists the $^{t}DS_b$ and $^{t}DH_b$ values for a 1.0V/ns slew rate. If the DQS/DQS# differential strobe feature is not enabled, timing is no longer referenced to the crosspoint of DQS/DQS#. Data timing is now referenced to V_{REF}, provided the DQS slew rate is not less than 1.0V/ns. If the DQS slew rate is less than 1.0V/ns, then data timing is now referenced to V_{IH}(AC) for a rising DQS and V_{IL}(DC) for a falling DQS.
8. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (^{t}HZ) or begins driving (^{t}LZ).
9. This maximum value is derived from the referenced test load. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition.
10. ^{t}LZ (MIN) will prevail over a ^{t}DQSCK (MIN) + ^{t}RPRE (MAX) condition.
11. The intent of the "Don't Care" state after completion of the postamble is the DQS-driven signal should either be HIGH, LOW or High-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions HIGH (above V_{IH}[DC]MIN), then it must not transition LOW (below V_{IH}[DC] prior to ^{t}DQSH[MIN]).

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12. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
13. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
14. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs. However, a REFRESH command must be asserted at least once every 70.3µs or ^{t}RFC (MAX). To ensure all rows of all banks are properly refreshed, 8,192 REFRESH commands must be issued every 64ms.
15. Each byte lane has a corresponding DQS.
16. CK and CK# input slew rate must be ≥ 1V/ns (≥ 2 V/ns if measured differentially).
17. The data valid window is derived by achieving other specifications - ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
18. The period jitter ($^{t}JIT_{per}$) is the maximum deviation in the clock period from the average or nominal clock allowed in either the positive or negative direction. JEDEC specifies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent less than noted in the table (DLL locked). Refer to the 256Mb, 512Mb, or 1Gb DDR2 SDRAM discrete data sheet for full jitter specifications.
19. MIN(^{t}CL, ^{t}CH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e., this value can be greater than the minimum specification limits for ^{t}CL and ^{t}CH). For example, ^{t}CL and ^{t}CH are = 50 percent of the period, less the half period jitter [^{t}JIT(HP)] of the clock source, and less the half period jitter due to cross talk [^{t}JIT(cross talk)] into the clock traces.
20. ^{t}HP (MIN) is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK# inputs.
21. READs and WRITEs with auto precharge *are* allowed to be issued before ^{t}RAS (MIN) is satisfied since ^{t}RAS lockout feature is supported in DDR2 SDRAM devices.
22. VIL/VIH DDR2 overshoot/undershoot. Refer to the 256Mb, 512Mb, or 1Gb DDR2 SDRAM data sheet for more detail.
23. ^{t}DAL = (nWR) + (^{t}RP/^{t}CK): For each of the terms above, if not already an integer, round to the next highest integer. ^{t}CK refers to the application clock period; nWR refers to the ^{t}WR parameter stored in the MR[11,10,9]. Example: For -53E at ^{t}CK = 3.75ns with ^{t}WR programmed to four clocks. ^{t}DAL = 4 + (15 ns/3.75 ns) clocks = 4 +(4) clocks = 8 clocks.
24. The minimum READ to internal PRECHARGE time. This parameter is only applicable when ^{t}RTP/(2 × ^{t}CK) > 1. If ^{t}RTP/(2 × ^{t}CK) ≤ 1, then equation AL + BL/2 applies. Notwithstanding, ^{t}RAS (MIN) has to be satisfied as well. The DDR2 SDRAM device will automatically delay the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.
25. Operating frequency is only allowed to change during self refresh mode, precharge power-down mode, and system reset condition.
26. ODT turn-on time ^{t}AON (MIN) is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time ^{t}AON (MAX) is when the ODT resistance is fully on. Both are measured from ^{t}AOND.
27. ODT turn-off time ^{t}AOF (MIN) is when the device starts to turn off ODT resistance. ODT turn off time ^{t}AOF (MAX) is when the bus is in High-Z. Both are measured from ^{t}AOFD.
28. This parameter has a two clock minimum requirement at any ^{t}CK.

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29. ^{t}DELAY is calculated from ^{t}IS + ^{t}CK + ^{t}IH so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system RESET condition.
30. ^{t}ISXR is equal to ^{t}IS and is used for CKE setup time during self refresh exit.
31. No more than 4 bank ACTIVE commands may be issued in a given ^{t}FAW(MIN) period. ^{t}RRD(MIN) restriction still applies. The ^{t}FAW(MIN) parameter applies to all 8-bank DDR2 devices, regardless of the number of banks already open or closed.
32. ^{t}RPA timing applies when the PRECHARGE(ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued, ^{t}RP timing applies. ^{t}RPA (MIN) applies to all 8-bank DDR2 devices.
33. Value is minimum pulse width, not the number of clock registrations.
34. Applicable to READ cycles only. WRITE cycles generally require additional time due to WRITE recovery time (^{t}WR) during auto precharge.
35. ^{t}CKE (MIN) of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + 2 × ^{t}CK + ^{t}IH.
36. This parameter is not referenced to a specific voltage level, but specified when the device output is no longer driving (^{t}RPST) or beginning to drive (^{t}RPRE).
37. When DQS is used single-ended, the minimum limit is reduced by 100ps.

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PLL and Register Specifications

Table 19: Register Timing Requirements and Switching Characteristics

Symbol	Parameter	Condition	0°C ≤ T_{OPR} ≤ +55°C, V_{DD} = +1.8V ±0.1V		Units
			Min	Max	
V_{OH}		I_{OH} = -6 mA	1.2	–	V
V_{OL}		I_{OL} = 6 mA	–	.05	V
I_I	All inputs	V_I = V_{DD} or GND	–	5	µA
I_{DD}	Static standby	RESET# = GND	–	100	µA
	Static operating	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_0 = 0	–	40	mA
I_{DDD}	Dynamic operating – clock only	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_0 = 0; CK and CK# switching 50% duty cycle	Varies by mfr	Varies by mfr	µA
	Dynamic operating – per each data input, 1:1 mode	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_0 = 0; CK and CK# switching 50% duty cycle; One data input switching at $^tCK/2$, 50% duty cycle	Varies by mfr	Varies by mfr	
	Dynamic operating – per each data input, 1:2 mode	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_0 = 0; CK and CK# switching 50% duty cycle; One data input switching at $^tCK/2$, 50% duty cycle	Varies by mfr	Varies by mfr	
C_I	Data inputs	V_I = V_{REF} ±250mV	2.5	3.5	pF
	CK and CK#	V_{ICR} = 0.9V, V_{ID} = 600mV	2	3	
	RESET	V_I = V_{DD} or GND	Varies	Varies	

Table 20: Register Electrical Characteristics
Note: 1

Register	Symbol	Parameter	Condition	0°C ≤ T_{OPR} ≤ +55°C, V_{DD} = +1.8V ±0.1V		Units	Notes
				Min	Max		
SSTL (bit pattern by JESD82)	f_{clock}	Clock frequency		–	270	MHz	
	t_w	Pulse duration		1	–	ns	
	t_{act}	Differential inputs active time		–	10	ns	2, 3
	t_{inact}	Differential inputs inactive time		–	15	ns	2, 4
	t_{su}	Setup time	Data before CK HIGH, CK# LOW	0.7	–	ns	
			Data before CK HIGH, CK# LOW	0.5	–	ns	
			ODT, CKE, and data before CK HIGH, CK# LOW	0.5	–		
	t_h	Hold time	OKE, CKE, and data after CK HIGH, CK# LOW	0.50	–	ns	

Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC Standard JESD82.
2. This parameter is not necessarily production tested.
3. Data inputs must be LOW a minimum time of t_{act} (MAX), after RESET# is taken HIGH.
4. Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} (MAX), after RESET# is taken LOW.

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Table 21: PLL Clock Driver Electrical Characteristics

Symbol	Parameter	Test Condition	$0°C \le T_{OPR} \le +55°C$, $V_{DD} = +1.8V \pm 0.1V$			Units	Notes
			Min	Nominal	Max		
V_{IK}	All inputs	I_I = -18mA	–	–	-1.2	V	
V_{OH}	High output voltage	I_{OH} = -100µA	V_{DDQ}/2 - 0.2	–	–	V	
		I_{OH} = -9mA	1.1	–	–	V	
V_{OL}	Low output voltage	I_{OL} = 100µA		–	0.1	µA	
		I_{OL} = 9mA			0.6	V	
I_{ODL}	Output disabled low current	OE = L, V_{ODL} = 100mV	100	–	–	µA	
V_{OD}	Output differential voltage, the magnitude of the difference between the true and complimentary outputs		0.6	–	–	V	
I_I	CK, CK#	V_I = V_{DDQ} or GND	–	–	±250	µA	
I_{DDLD}	Static supply current: I_{DDQ} + I_{ADD}	CK and CK# = L	–	–	500	µA	
I_{DD}	Dynamic supply current: I_{DDQ} + I_{ADD}	CK and CK# = 270 MHz, all outputs are open (not connected to a PCB)	–	–	300	mA	1
C_I	CI and CK#	V_I = V_{DDQ} or GND	2	–	3	pF	
$C_{I(\Delta)}$	CI and CK#	V_I = V_{DDQ} or GND	V_{DDQ}/2 - 0.2	–	0.25	pF	

Notes: 1. Total $I_{DD} = I_{DDQ} = I_{ADD} = F_{CK} \times C_{PD} \times V_{DDQ}$, solving for $C_{PD} = (I_{DDQ} + I_{ADD})/(F_{CK} \times V_{DDQ})$ where F_{CK} is the input frequency, V_{DDQ} is the power supply and C_{PD} is the power dissipation capacitance.

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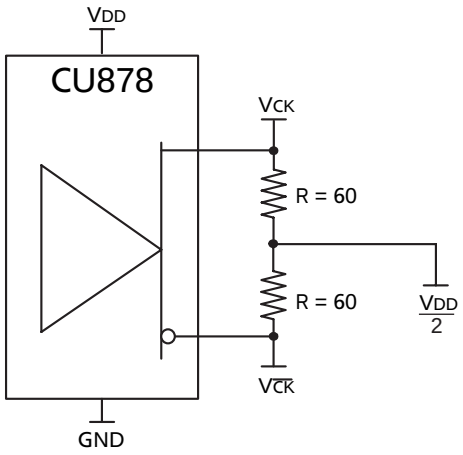
Table 22: PLL Clock Driver Timing Requirements and Switching Characteristics
Note: 1

Parameter	Symbol	0°C ≤ T_{OPR} ≤ +55°C, V_{DD} = +1.8V ±0.1V			Units	Notes
		Min	Nominal	Max		
Output Enable to any Y/Y#	^{t}EN	–	–	8	ns	
Output Enable to any Y/Y#	^{t}DIS	–	–	8	ns	
Cycle to Cycle Jitter	$^{t}JIT_{CC}$	-40	–	40	ps	
Static Phase Offset	$^{t}\varnothing$	-50	0	50	ps	2
Dynamc Phase Offset	$^{t}\varnothing_{dyn}$	-50	0	50	ps	2
Output Clock Skew	$^{t}SK_{O}$	–	–	40	ps	
Period Jitter	$^{t}JIT_{PER}$	-40	–	40	ps	3, 4
Half-Period Jitter	$^{t}JIT_{HPER}$	-75	–	75	ps	3
Input Clock Slew Rate	$^{t}LS_{I}$	1.0	2.5	4	V/ns	
Output Clock Slew Rate	$^{t}LS_{O}$	1.5	2.5	3	V/ns	6
Output Differential-Pair Cross-Voltage	V_{OX}	$V_{DD}Q/2$ - 0.1	–	$V_{DD}Q/2$ + 0.1	V	5
SSC Modulation Frequency		30	–	33	kHZ	
SSC Clock Input Frequency Deviation		0.0	–	-0.50	%	
PLL Loop Bandwidth (-3dB from unity gain)		2.0	–	–	MHz	

Notes:
1. Timing and switching specifications for the PLL listed above are critical for proper operation of the DDR2 SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this PLL is available in JEDEC Standard JESD82.
2. Static phase offset does not include Jitter.
3. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.
4. Design target is 60ps, unless it is unachievable.
5. V_{OX} specified at the DRAM clock input, or the test load.
6. The output slew rate is determined from the IBIS model:



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Serial Presence-Detect

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figure 12, and Figure 13 on page 43).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting 8 bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the 8 bits of data (Figure 14 on page 43).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent 8-bit word. In the read mode the SPD device will transmit 8 bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 12: Data Validity

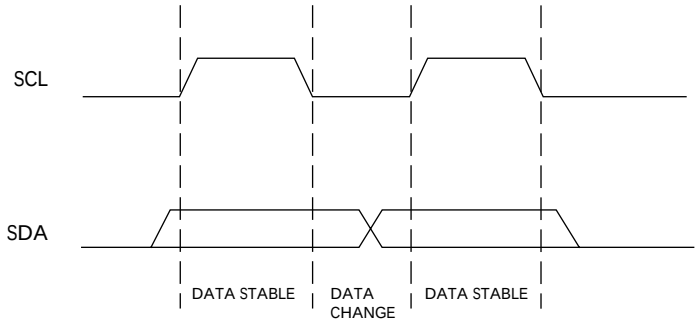

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Figure 13: Definition of Start and Stop

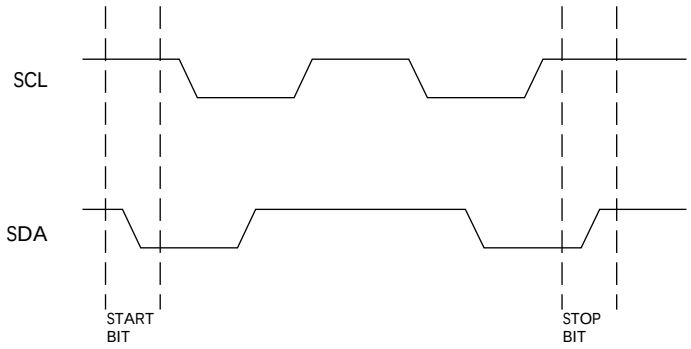

Figure 14: Acknowledge Response From Receiver

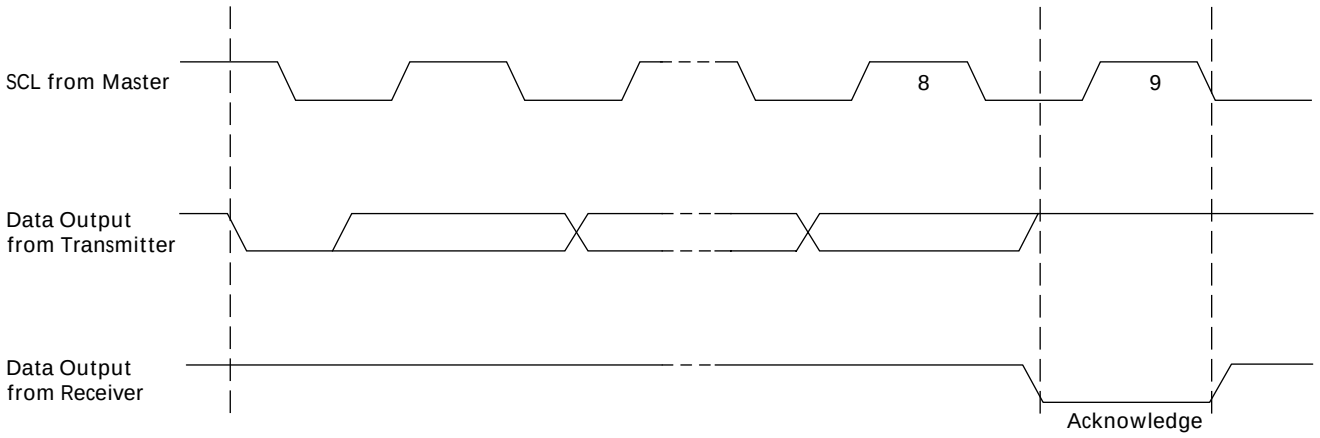

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Table 23: EEPROM Device Select Code

The most significant bit (b7) is sent first

Select Code	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory area select code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection register select code	0	1	1	0	SA2	SA1	SA0	RW

Table 24: EEPROM Operating Modes

Mode	RW Bit	WC	Bytes	Initial Sequence
Current address read	1	VIH or VIL	1	START, Device select, RW = '1'
Random address read	0	VIH or VIL	1	START, Device select, RW = '0', Address
	1	VIH or VIL	1	reSTART, Device select, RW = '1'
Sequential read	1	VIH or VIL	≥ 1	Similar to current or random address read
Byte write	0	VIL	1	START, Device select, RW = '0'
Page write	0	VIL	≤ 16	START, Device select, RW = '0'

Figure 15: SPD EEPROM Timing Diagram

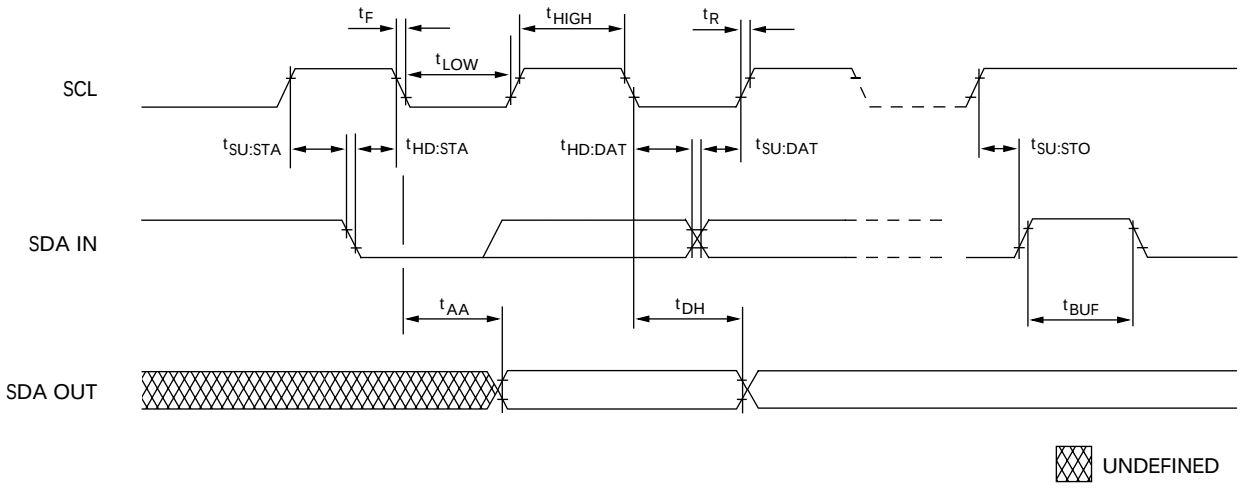

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Table 25: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	-0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DDSPD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DDSPD}	I_{LO}	0.05	3	µA
Standby current	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 KHz	ICC_R	0.4	1	mA
Powr supply current, WRITE: SCL clock frequency = 100 KHz	ICC_W	2	3	mA

Table 26: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3		µs	
Data-out hold time	^tDH	200		ns	
SDA and SCL fall time	^tF		300	ns	2
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	0.6		µs	
Clock HIGH period	^tHIGH	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		50	ns	
Clock LOW period	^tLOW	1.3		µs	
SDA and SCL rise time	^tR		0.3	µs	2
SCL clock frequency	^fSCL		400	KHz	
Data-in setup time	$^tSU:DAT$	100		ns	
Start condition setup time	$^tSU:STA$	0.6		µs	3
Stop condition setup time	$^tSU:STO$	0.6		µs	
WRITE cycle time	^tWRC		10	ms	4

Notes:
1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a write cycle.
4. The SPD EEPROM write cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the write cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

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Table 27: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 47

Byte	Description	Entry (Version)	MT9HVF3272K/ MT9HVF3272(P)K	MT9HVF6472K/ MT9HVF6472(P)K	MT9HVF12872K/ MT9HVF12872(P)K
0	Number of SPD bytes used by Micron	128	80	80	80
1	Total number of bytes in SPD device	256	08	08	08
2	Fundamental memory type	DDR2 SDRAM	08	08	08
3	Number of row addresses on assembly	13, 14	0D	0E	0E
4	Number of column addresses on assembly	10	0A	0A	0A
5	DIMM height and module ranks	0.72in, Single rank	00	00	00
6	Module data width	72	48	48	48
7	Module data width (continued)	0	00	00	00
8	Module voltage interface levels	SSTL 1.8V	05	05	05
9	SDRAM cycle time, ^{t}CK (CL = maximum value, see byte 18)	-667 -53E -40E	30 3D 50	30 3D 50	30 3D 50
10	SDRAM access from clock, ^{t}AC (CL = maximum value, see byte 18)	-667 -53E -40E	45 50 60	45 50 60	45 50 60
11	Module configuration type	ECC/ECC and parity	02/06	02/06	02/06
12	Refresh rate/type	7.81µs/SELF	82	82	82
13	SDRAM device width (primary SDRAM)	8	08	08	08
14	Error-checking SDRAM data width	8	08	08	08
15	Minimum clock delay, back-to-back random column access	1 clock	00	00	00
16	Burst lengths supported	4, 8	0C	0C	0C
17	Number of banks on SDRAM device	4 or 8	04	04	08
18	CAS latencies supported	-667 (5, 4, 3) -53E/-40E (4, 3)	38 18	38 18	38 18
19	Module thickness		01	01	01
20	DDR2 DIMM type	Reg. MiniDIMM	10	10	10
21	SDRAM module attributes		04	04	04
22	SDRAM device attributes: Weak driver (01) and 50Ω ODT (03)	-667 -53E/-40E	03 01	03 01	03 01
23	SDRAM cycle time, ^{t}CK, MAX CL - 1	-667 -53E/-40E	3D 50	3D 50	3D 50
24	SDRAM access from CK, ^{t}AC, MAX CL - 1	-667 -53E -40E	45 50 60	45 50 60	45 50 60
25	SDRAM cycle time, ^{t}CK, MAX CL - 2	-667 -53E/-40E(N/A)	50 00	50 00	50 00
26	SDRAM access from CK, ^{t}AC, MAX CL - 2	-667 -53E/-40E(N/A)	45 00	45 00	45 00
27	Minimum row precharge time, ^{t}RP		3C	3C	3C
28	Minimum row active to row active, ^{t}RRD		1E	1E	1E
29	Minimum RAS#-to-CAS# delay, ^{t}RCD		3C	3C	3C
30	Minimum RAS# pulse width, ^{t}RAS (see note 1)	-667/-53E -40E	2D 28	2D 28	2D 28
31	Module rank density	256MB, 512MB, 1GB	40	80	01

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Table 27: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 47

Byte	Description	Entry (Version)	MT9HVF3272K/ MT9HVF3272(P)K	MT9HVF6472K/ MT9HVF6472(P)K	MT9HVF12872K/ MT9HVF12872(P)K
32	Address and command setup time, $^{t}IS_{b}$	-667 -53E -40E	20 25 35	20 25 35	20 25 35
33	Address and command hold time, $^{t}IH_{b}$	-667 -53E -40E	27 37 47	27 37 47	27 37 47
34	Data/ Data mask input setup time, $^{t}DS_{b}$	-667/-53E -40E	10 15	10 15	10 15
35	Data/ Data mask input hold time, $^{t}DH_{b}$	-667 -53E -40E	17 22 27	17 22 27	17 22 27
36	Write recovery time, ^{t}WR		3C	3C	3C
37	Write-to-read CMD delay, ^{t}WTR	-667/-53E -40E	1E 28	1E 28	1E 28
38	Read-to-precharge CMD delay, ^{t}RTP		1E	1E	1E
39	Memory analysis probe		00	00	00
40	Extension for bytes 41 and 42		00	00	06
41	Minimum active auto refresh time, ^{t}RC	-667/-53E -40E	3C 37	3C 37	3C 37
42	Minimum auto refresh to active/ AUTO REFRESH command period, ^{t}RFC		4B	69	7F
43	SDRAM device MAX cycle time, $^{t}CKMAX$		80	80	80
44	SDRAM device MAX DQS-DQ skew time, $^{t}DQSQ$	-667 -53E -40E	18 1E 23	18 1E 23	18 1E 23
45	SDRAM device MAX read data hold skew factor, ^{t}QHS	-667 -53E -40E	22 28 2D	22 28 2D	22 28 2D
46	PLL relock time		0F	0F	0F
47–61	Optional features, not supported		00	00	00
62	SPD revision	Release 1.2	12	12	12
63	Checksum For bytes 0–62 ECC/ECC and parity	-667 -53E -40E	BF/C3 6A/6E D1/D5	1E/22 C9/CD 30/34	BF/C3 6A/6E D1/D5
64	Manufacturer's JEDEC ID code	MICRON	2C	2C	2C
65–71	Manufacturer's JEDEC ID code	(Continued)	FF	FF	FF
72	Manufacturing location	01–12	01–0C	01–0C	01–0C
73–90	Module part number (ASCII)		Variable data	Variable data	Variable data
91	PCB identification code	1–9	01–09	01–09	01–09
92	Identification code (continued)	0	00	00	00
93	Year of manufacture in BCD		Variable data	Variable data	Variable data
94	Week of manufacture in BCD		Variable data	Variable data	Variable data
95–98	Module serial number		Variable data	Variable data	Variable data
99–127	Manufacturer-Specific data (RSVD)		–	–	–

Notes: 1. The ^{t}RAS SPD value shown is based on the JEDEC standard value of 45ns; the actual device specification is ^{t}RAS = 40ns.

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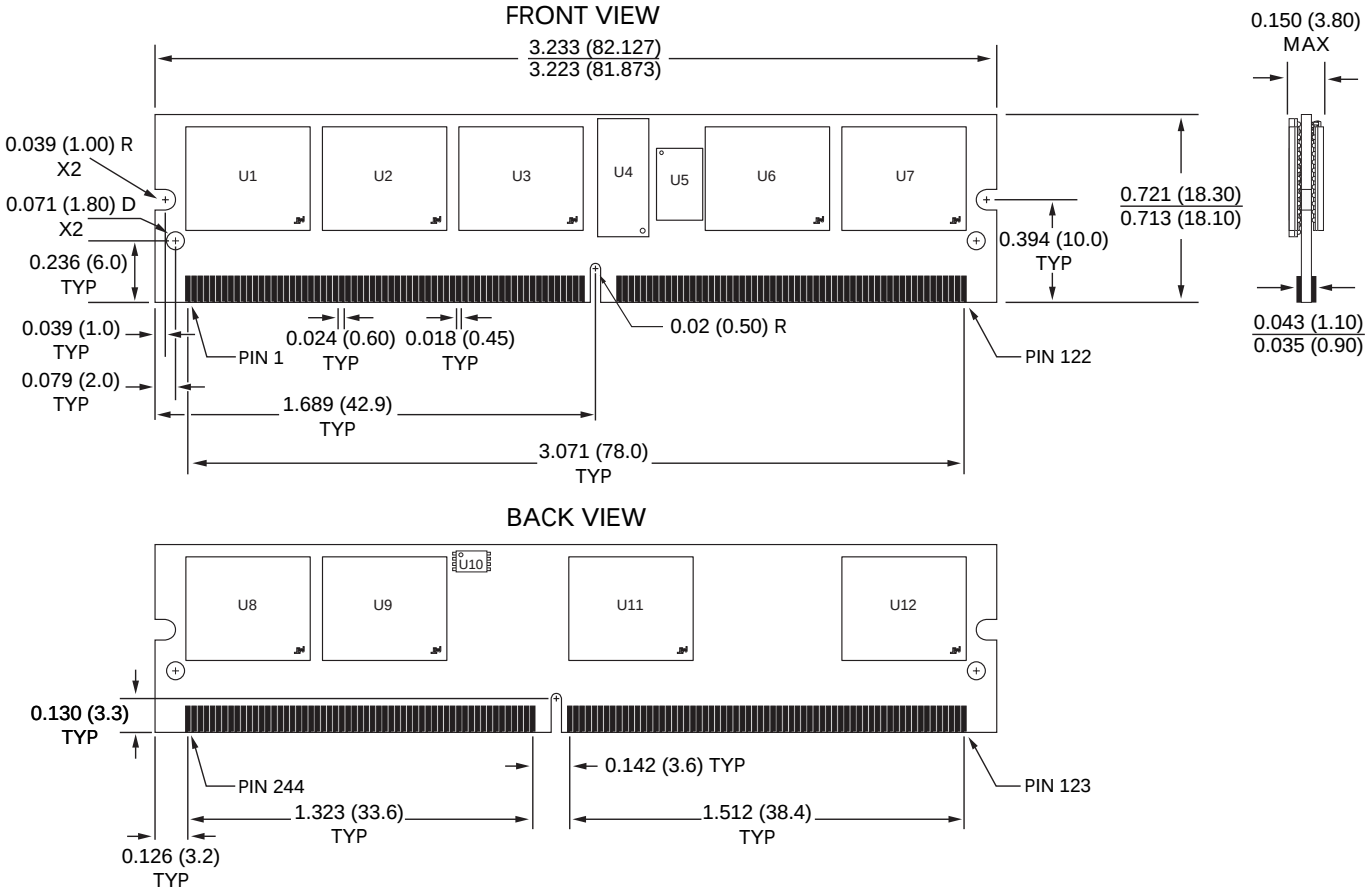
Package Dimensions

All dimensions are in inches (millimeters); $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.

Figure 16: 244-Pin VLP Registered MiniDIMM Dimensions



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Data Sheet Designation

Advance: This data sheet contains initial descriptions of products still under development. Advance applies to MT9HVF12872(P)K only.

Released (No Mark): This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur. Released (no mark) applies to MT9HVF3272(P)K and MT9HVF6472(P)K only.

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