Actel
POWER MATTERS

Product Catalog

May 2009

Now, more than ever, **power matters.**

Whether you're designing at the board or system level, **Actel's low-power and mixed-signal FPGAs are your best choice.** The unique, flash-based technology of Actel FPGAs, coupled with their history of reliability, sets them apart from traditional FPGAs.

Design for today's rapidly growing markets of consumer and portable medical devices, or tomorrow's environmentally friendly data centers and industrial controls. Take your designs to 30,000 feet or even millions of miles into space. Only Actel can meet the power, size, cost, and reliability targets that reduce time-to-market and enable long-term profitability.

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Please refer to www.actel.com and appropriate product datasheets for the latest device information and valid ordering codes. More information regarding previous generations of flash and antifuse FPGAs is also available on Actel's website.

IGLOO/e

The ultra-low-power programmable solution

The Actel IGLOO family of reprogrammable, full-featured flash FPGAs is designed to meet the demanding power, area, and cost requirements of today's portable electronics. Based on Actel's nonvolatile flash technology, the 1.2 V to 1.5 V operating voltage family offers the industry's lowest power consumption—as low as 5 µW. The IGLOO family supports up to 3,000,000 system gates with up to 504 Kbits of true dual-port SRAM, up to 6 embedded PLLs, and up to 620 user I/Os. Low-power applications that require 32-bit processing can use the ARM® Cortex™-M1 processor without license fee or royalties in M1 IGLOO devices. Developed specifically for implementation in FPGAs, Cortex-M1 offers an optimal balance between performance and size to minimize power consumption.

- Ultra-low-power FPGAs
- Flash*Freeze technology for lowest power consumption
- 1.2 V core and I/O voltage
- 5 µW Flash*Freeze mode
- Reprogrammable
- Live at power-up
- Secure in-system programming (ISP)
- User nonvolatile FlashROM

IGLOO/e Devices

IGLOO Devices	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	AGLE600	AGLE3000
Cortex-M1 Devices					M1AGL250		M1AGL600	M1AGL1000		M1AGLE3000
System Gates	15,000	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	3,000,000
Typical Equivalent Macrocells	128	256	512	1,024	2,048	—	—	—	—	—
VersaTiles (D-flip-flops)	384	768	1,536	3,072	6,144	9,216	13,824	24,576	13,824	75,264
Flash*Freeze Mode (typical, µW)	5	5	10	16	24	32	36	53	49	137
RAM (1,024 bits)	—	—	18	36	36	54	108	144	108	504
RAM Blocks (4,608 bits)	—	—	4	8	8	12	24	32	24	112
FlashROM (Kbits)	1	1	1	1	1	1	1	1	1	1
Secure (AES) ISP[1]	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLLs with CCC	—	—	1	1	1	1	1	1	6	6
VersaNet Globals[2]	6	6	18	18	18	18	18	18	18	18
I/O Banks	2	2	2	2	4	4	4	4	8	8
Maximum User I/Os (packaged device)	49	81	96	133	143	194	235	300	270	620
Package Pins UC CS QFN VQFP FBGA	QN68	UC81 CS81 QN48 QN68 QN132 VQ100	CS121 QN132 VQ100 FG144[4]	CS196 QN132 VQ100 FG144	CS196[3] QN132[3,4] VQ100 FG144	CS196 FG144 FG256 FG484	CS281 FG144 FG256 FG484	CS281 FG144 FG256 FG484	 FG256 FG484	 FG484 FG896

Notes:
1. *AES is not available for Cortex-M1 IGLOO devices.*
2. *Six chip (main) and twelve quadrant global networks are available for AGL060 devices and above.*
3. *The M1AGL250 device does not support this package.*
4. *Device/package support TBD.*

I/Os Per Package

IGLOO Devices	AGL015	AGL030	AGL060	AGL125	AGL250		AGL400		AGL600		AGL1000		AGLE600		AGLE3000	
Cortex-M1 Devices					M1AGL250[1]				M1AGL600		M1AGL1000				M1AGLE3000	
I/O Type	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs
QN48	—	34	—	—	—	—	—	—	—	—	—	—	—	—	—	—
QN68	49	49	—	—	—	—	—	—	—	—	—	—	—	—	—	—
UC81	—	66	—	—	—	—	—	—	—	—	—	—	—	—	—	—
CS81	—	66	—	—	—	—	—	—	—	—	—	—	—	—	—	—
CS121	—	—	96	—	—	—	—	—	—	—	—	—	—	—	—	—
VQ100	—	77	71	71	68	13	—	—	—	—	—	—	—	—	—	—
QN132	—	81	80	84	87[2]	19[2]	—	—	—	—	—	—	—	—	—	—
CS196	—	—	—	133	143	35	143	35	—	—	—	—	—	—	—	—
FG144	—	—	96[2]	97	97	24	97	25	97	25	97	25	—	—	—	—
FG256	—	—	—	—	—	—	178	38	177	43	177	44	165	79	—	—
CS281	—	—	—	—	—	—	—	—	215	53	215	53	—	—	—	—
FG484	—	—	—	—	—	—	194	38	235	60	300	74	270	135	341	168
FG896	—	—	—	—	—	—	—	—	—	—	—	—	—	—	620	310

Notes:
1. *The M1AGL250 device does not support QN132 or CS196 packages.*
2. *Device/package support TBD.*

IGLOO nano

The industry's lowest-power, smallest-size solution

Actel's IGLOO nano products offer groundbreaking possibilities in power, size, lead-times, operating temperature, and cost. Available in logic densities from 10,000 to 250,000 gates, the 1.2 V to 1.5 V IGLOO nano devices have been designed for high-volume applications where power and size are key decision criteria. IGLOO nano devices are perfect ASIC or ASSP replacements, yet retain the historical FPGA advantages of flexibility and quick time-to-market in low-power and small footprint profiles.

- Ultra-low power in Flash*Freeze mode, as low as 2 µW
- Variety of small footprint packages as small as 3x3 mm
- Zero lead-time on selected devices
- Known good die supported
- Enhanced commercial temperature
- Reprogrammable flash technology
- 1.2 V to 1.5 V single voltage operation
- Enhanced I/O features
- Clock conditioning circuits (CCCs) and PLLs
- Embedded SRAM and nonvolatile memory (NVM)
- ISP and security

IGLOO nano Devices

IGLOO nano Devices	AGLN010	AGLN015	AGLN020	AGLN030	AGLN060	AGLN125	AGLN250
System Gates	10,000	15,000	20,000	30,000	60,000	125,000	250,000
Typical Equivalent Macrocells	86	128	172	256	512	1,024	2,048
VersaTiles (D-flip-flops)	260	384	520	768	1,536	3,072	6,144
Flash*Freeze Mode (typical, µW)	2	4	4	5	10	16	24
RAM (1,024 bits)	—	—	—	—	18	36	36
RAM Blocks (4,608 bits)	—	—	—	—	4	8	8
FlashROM (Kbits)	1	1	1	1	1	1	1
Secure (AES) ISP	—	—	—	—	Yes	Yes	Yes
Integrated PLLs with CCC	—	—	—	—	1	1	1
VersaNet Globals	4	4	4	6	18	18	18
I/O Banks	2	3	3	2	2	2	4
Maximum User I/Os (packaged device)	34	49	52	77	71	71	68
Known Good Die User I/Os	34	—	52	83	71	71	68
Package Pins UC CS QFN VQFP	 UC36 QN48	 QN68	 UC81 CS81 QN68	 UC81 CS81 QN48, QN68 VQ100	 CS81 VQ100	 CS81 VQ100	 CS81 VQ100

I/Os Per Package

IGLOO nano Devices	AGLN010	AGLN015	AGLN020	AGLN030	AGLN060	AGLN125	AGLN250
Known Good Die	34	—	52	83	71	71	68
UC36	23	—	—	—	—	—	—
QN48	34	—	—	34	—	—	—
QN68	—	49	49	49	—	—	—
UC81	—	—	52	66	—	—	—
CS81	—	—	52	66	60	60	60
VQ100	—	—	—	77	71	71	68

IGLOO PLUS

The low-power FPGA with enhanced I/O capabilities

Actel's IGLOO PLUS products deliver unrivaled low power and I/O features in a feature-rich programmable device, offering up to 64 percent more I/Os than the award-winning IGLOO products and supporting independent Schmitt trigger inputs, hot-swapping, and Flash*Freeze bus hold. Ranging from 30,000 to 125,000 gates, the 1.2 V to 1.5 V IGLOO PLUS devices have been optimized to meet the needs of I/O-intensive, power-conscious applications that require exceptional features.

- I/O-optimized FPGA
- Ultra-low power in Flash*Freeze mode, as low as 5 µW
- Low-power active capability
- Small footprint and low-cost packages
- Reprogrammable flash technology
- 1.2 V to 1.5 V single voltage operation
- Enhanced I/O features
- CCCs and PLLs
- Embedded SRAM NVM
- ISP and security

IGLOO PLUS Devices

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
System Gates	30,000	60,000	125,000
Typical Equivalent Macrocells	256	512	1,024
VersaTiles (D-flip-flops)	792	1,584	3,120
Flash*Freeze Mode (typical, µW)	5	10	16
RAM (1,024 bits)	—	18	36
RAM Blocks (4,608 bits)	—	4	8
FlashROM (Kbits)	1	1	1
Secure (AES) ISP	—	Yes	Yes
Integrated PLLs with CCC	—	1	1
VersaNet Globals	6	18	18
I/O Banks	4	4	4
Maximum User I/Os (packaged device)	120	157	212
Package Pins CS VQFP	 CS201, CS289 VQ128	 CS201, CS289 VQ176	 CS281, CS289

I/Os Per Package

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
I/O Type	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O
CS201	120	157	—
CS281	—	—	212
CS289	120	157	212
VQ128	101	—	—
VQ176	—	137	—

ProASIC3/E

The low-power, low-cost FPGA solution

The ProASIC3 series of flash FPGAs offers a breakthrough in power, price, performance, density, and features for today's most demanding high-volume applications. ProASIC3 devices support the ARM Cortex-M1 processor, offering the benefits of programmability and time-to-market at low cost. ProASIC3 devices are based on nonvolatile flash technology and support 15,000 to 3,000,000 gates and up to 620 high-performance I/Os. For automotive applications, selected ProASIC3 devices are qualified to the AEC-Q100 specification and are available with AEC T1 screening and PPAP documentation.

- Low power
- Single chip, single voltage
- Nonvolatile, reprogrammable
- Low cost
- Live at power-up
- Maximum design security
- Firm-error immune
- Clock management
- Advanced I/O standards
- User nonvolatile FlashROM
- Secure ISP
- High performance

ProASIC3/E Devices

ProASIC3/E Devices	A3P015	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000	A3PE600	A3PE1500	A3PE3000
Cortex-M1 Devices					M1A3P250	M1A3P400	M1A3P600	M1A3P1000		M1A3PE1500	M1A3PE3000
System Gates	15,000	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	1,500,000	3,000,000
Typical Equivalent Macrocells	128	256	512	1,024	2,048	—	—	—	—	—	—
VersaTiles (D-flip-flops)	384	768	1,536	3,072	6,144	9,216	13,824	24,576	13,824	38,400	75,264
RAM (1,024 bits)	—	—	18	36	36	54	108	144	108	270	504
RAM Blocks (4,608 bits)	—	—	4	8	8	12	24	32	24	60	112
FlashROM (Kbits)	1	1	1	1	1	1	1	1	1	1	1
Secure (AES) ISP[1]	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLLs with CCC	—	—	1	1	1	1	1	1	6	6	6
VersaNet Globals	6	6	18	18	18	18	18	18	18	18	18
I/O Banks	2	2	2	2	4	4	4	4	8	8	8
Maximum User I/Os (packaged device)	49	81	96	133	157	194	235	300	270	444	620
Package Pins QFN VQFP TQFP PQFP FBGA	QN68	QN48 QN68 QN132 VQ100	QN132 VQ100[2] TQ144 FG144[2]	QN132[2] VQ100[2] TQ144 PQ208 FG144[2]	QN132[3] VQ100[2] PQ208 FG144[2] FG256[2, 3]	 PQ208 FG144 FG256 FG484	 PQ208 FG144 FG256 FG484	 PQ208 FG144[2] FG256[2] FG484[2]	 PQ208 FG256 FG484	 PQ208 FG484 FG676	 PQ208 FG324 FG484 FG896

Notes:

1. *AES is not available for Cortex-M1 ProASIC3 devices.*
2. *Available as automotive "T" grade*
3. *The M1A3P250 device does not support this package.*

I/Os Per Package

ProASIC3 Devices	A3P015	A3P030	A3P060	A3P125	A3P250		A3P400		A3P600		A3P1000		A3PE600		A3PE1500		A3PE3000	
Cortex-M1 Devices					M1A3P250		M1A3P400		M1A3P600		M1A3P1000				M1A3PE1500		M1A3PE3000	
I/O Type	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs
QN48	—	34	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
QN68	49	49	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
QN132	—	81	80	84	87	19	—	—	—	—	—	—	—	—	—	—	—	—
VQ100	—	77	71	71	68	13	—	—	—	—	—	—	—	—	—	—	—	—
TQ144	—	—	91	100	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PQ208	—	—	—	133	151	34	151	34	154	35	154	35	147	65	147	65	147	65
FG144	—	—	96	97	97	24	97	25	97	25	97	25	—	—	—	—	—	—
FG256	—	—	—	—	157	38	178	38	177	43	177	44	165	79	—	—	—	—
FG324	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	221	110
FG484	—	—	—	—	—	—	194	38	235	60	300	74	270	135	280	139	341	168
FG676	—	—	—	—	—	—	—	—	—	—	—	—	—	—	444	222	—	—
FG896	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	620	310

ProASIC3 nano

The lowest-cost solution with enhanced I/O capabilities

Actel's innovative ProASIC3 nano devices bring a new level of value and flexibility to high-volume markets. When measured against the typical project metrics of performance, cost, flexibility, and time-to-market, ProASIC3 nano devices provide an attractive alternative to ASICs and ASSPs in fast moving or highly competitive markets. Customer-driven total system cost reduction was a key design criteria for the ProASIC3 nano program. Reduced device cost, availability of known good die, a single-chip implementation, and a broad selection of small footprint packages all contribute to lower total system costs.

- 1.5 V core for low power
- Known good die supported
- 350 MHz system performance
- Embedded SRAM NVM
- Firm-error immune
- Enhanced commercial temperature
- Enhanced I/O features
- ISP and security
- Reprogrammable flash technology
- Zero lead-time on selected devices
- CCCs and PLLs

ProASIC3 nano Devices

ProASIC3 nano Devices	A3PN010	A3PN015	A3PN020	A3PN030	A3PN060	A3PN125	A3PN250
System Gates	10,000	15,000	20,000	30,000	60,000	125,000	250,000
Typical Equivalent Macrocells	86	128	172	256	512	1,024	2,048
VersaTiles (D-flip-flops)	260	384	520	768	1,536	3,072	6,144
RAM (1,024 bits)	—	—	—	—	18	36	36
RAM Blocks (4,608 bits)	—	—	—	—	4	8	8
FlashROM (Kbits)	1	1	1	1	1	1	1
Secure (AES) ISP	—	—	—	—	Yes	Yes	Yes
Integrated PLLs with CCC	—	—	—	—	1	1	1
VersaNet Globals	4	4	4	6	18	18	18
I/O Banks	2	3	3	2	2	2	4
Maximum User I/Os (packaged device)	34	49	49	77	71	71	68
Known Good Die User I/Os	34	—	52	83	71	71	68
Package Pin QFN VQFP	QN48	QN68	QN68	QN48, QN68 VQ100	VQ100	VQ100	VQ100

I/Os Per Package

ProASIC3 nano Devices	A3PN010	A3PN015	A3PN020	A3PN030	A3PN060	A3PN125	A3PN250
Known Good Die	34	—	52	83	71	71	68
QN48	34	—		34	—	—	—
QN68	—	49	49	49	—	—	—
VQ100	—	—	—	77	71	71	68

ProASIC3L

Balancing low power, performance, and low cost

ProASIC3L FPGAs feature 40 percent lower dynamic power and 90 percent lower static power than the previous generation ProASIC3 FPGAs and orders of magnitude lower power than SRAM competitors, combining dramatically reduced power consumption with up to 350 MHz operation. The ProASIC3L family also supports the free implementation of an FPGA-optimized 32-bit ARM Cortex-M1 processor, enabling system designers to select the Actel flash FPGA solution that best meets their speed and power design requirements, regardless of application or volume. Optimized software tools using power-driven layout (PDL) provide instant power reduction capabilities.

- Low-power 1.2 V to 1.5 V core operation
- 700 Mbps DDR, LVDS capable I/Os
- Up to 350 MHz system performance
- Enhanced I/O features
- Embedded SRAM and NVM
- Firm-error immune
- ISP and security
- Flash*Freeze technology for lowest power
- Reprogrammable flash technology
- CCCs and PLLs

ProASIC3L Low-Power Devices

ProASIC3L Devices	A3P250L	A3P600L	A3P1000L	A3PE3000L
Cortex-M1 Devices		M1A3P600L	M1A3P1000L	M1A3PE3000L
System Gates	250,000	600,000	1,000,000	3,000,000
VersaTiles (D-flip-flops)	6,144	13,824	24,576	75,264
RAM (1,024 bits)	36	108	144	504
RAM Blocks (4,608 bits)	8	24	32	112
FlashROM (Kbits)	1	1	1	1
Secure (AES) ISP*	Yes	Yes	Yes	Yes
Integrated PLLs with CCC	1	1	1	6
VersaNet Globals	18	18	18	18
I/O Banks	4	4	4	8
Maximum User I/Os (packaged device)	157	235	300	620
Package Pins VQFP PQFP FBGA	 VQ100 PQ208 FG144, FG256	 PQ208 FG144, FG256, FG484	 PQ208 FG144, FG256, FG484	 PQ208 FG324, FG484, FG896

Note:

** AES is not available for Cortex-M1 ProASIC3L devices.*

I/Os Per Package

ProASIC3L Devices	A3P250L		A3P600L		A3P1000L		A3PE3000L	
Cortex-M1 Devices			M1A3P600L		M1A3P1000L		M1A3PE3000L	
I/O Type	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs
VQ100	68	13	—	—	—	—	—	—
PQ208	151	34	154	35	154	35	147	65
FG144	97	24	97	25	97	25	—	—
FG256	157	38	177	43	177	44	—	—
FG324	—	—	—	—	—	—	221	110
FG484	—	—	235	60	300	74	341	168
FG896	—	—	—	—	—	—	620	310

Fusion

The world's first mixed-signal FPGA

Actel Fusion integrates configurable analog, large flash memory blocks, comprehensive clock generation and management circuitry, and high-performance, flash-based programmable logic in a monolithic device. Actel's innovative Fusion architecture can be used with the Actel soft MCU core as well as the performance-maximized 32-bit ARM Cortex-M1 cores. Fusion is the definitive mixed-signal FPGA platform.

- Integrated A/D converter (ADC) with 8-, 10-, and 12-bit resolution and 30 scalable analog input channels
- ADC accuracy better than 1 percent
- Current and voltage monitoring blocks
- In-system configurable analog supports a wide variety of applications
- Up to 8 Mbits of user flash memory
- Extensive clocking resources
- Analog PLLs
- 1 percent RC oscillator
- Crystal oscillator circuit
- Real-time counter (RTC)
- Flash FPGA fabric
- Reprogrammable
- Live at power-up
- Maximum design security
- Ultra-low power
- Firm-error immune
- Clock management
- Advanced I/O standards
- User nonvolatile FlashROM

Fusion Devices

Fusion Devices		AFS090	AFS250	AFS600	AFS1500
Cortex-M1 Devices*			M1AFS250	M1AFS600	M1AFS1500
General Information	System Gates	90,000	250,000	600,000	1,500,000
	Tiles (D-flip-flops)	2,304	6,144	13,824	38,400
	Secure (AES) ISP	Yes	Yes	Yes	Yes
	PLLs	1	1	2	2
	Globals	18	18	18	18
Memory	Flash Memory Blocks (2 Mbits)	1	1	2	4
	Total Flash Memory (2 Mbits)	2	2	4	8
	FlashROM (Kbits)	1	1	1	1
	RAM Blocks (4,608 bits)	6	8	24	60
	RAM (Kbits)	27	36	108	270
Analog and I/Os	Analog Quads	5	6	10	10
	Analog Input Channels	15	18	30	30
	Gate Driver Outputs	5	6	10	10
	I/O Banks (+ JTAG)	4	4	5	5
	Maximum Digital I/Os	75	114	172	252
	Analog I/Os	20	24	40	40

Note:
** Refer to the Cortex-M1 product brief for more information.*

Package I/Os: Single-/Double-Ended (Analog)

Fusion Devices	AFS090	AFS250	AFS600	AFS1500
Cortex-M1 Devices		M1AFS250	M1AFS600	M1AFS1500
QN108[1]	37/9 (16)			
QN180[1]	60/16 (20)	65/15 (24)		
PQ208[2]		93/26 (24)	95/46 (40)	
FG256[3]	75/22 (20)	114/37 (24)	119/58 (40)	119/58 (40)
FG484[3]			172/86 (40)	223/109 (40)
FG676[3]				252/126 (40)

Notes:
1. These packages are available only as RoHS-compliant (QNG package specifier).
2. AFS250 and AFS600 PQ208 devices are not pin-compatible.
3. Available in RoHS-compliant and standard leaded packages.

IGLOO and ProASIC3 I/O Table

IGLOO/e		AGL015		AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	AGLE600		AGLE3000
IGLOO nano	AGLN010	AGLN015	AGLN020	AGLN030	AGLN060	AGLN125	AGLN250						
IGLOO PLUS				AGLP030	AGLP060	AGLP125							
ProASIC3/E		A3P015		A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000	A3PE600	A3PE1500	A3PE3000
ProASIC3 nano	A3PN010	A3PN015	A3PN020	A3PN030	A3PN060	A3PN125	A3PN250						
ProASIC3L							A3P250L		A3P600L	A3P1000L			A3PE3000L
Tiles	260	384	520	768	1,536	3,072	6,144	9,216	13,824	24,576	13,824	38,400	75,264
RAM (Kbits)	—	—	—	—	18	36	36	54	108	144	108	270	504
PLLs	—	—	—	—	1	1	1	1	1	1	6	6	6
I/Os	Std, Hot-Swap	Std, Hot-Swap	Std, Hot-Swap	Std, Hot-Swap	Std+	Std+	Std+/LVDS	Std+/LVDS	Std+/LVDS	Std+/LVDS	Pro	Pro	Pro
I/O Banks	2	3	3	2	2	2	4	4	4	4	8	8	8
Size (mm) Name Pitch (mm)													
3x3 UC36 0.40	23												
4x4 UC81 0.40			52	66									
5x5 CS81 0.50			52	66	60	60	60						
6x6 CS121 0.50					96								
6x6 QN48 0.40	34			34									
8x8 CS196 0.50						133	143/35	143/35					
8x8 QN68 0.40		49	49	49									
8x8 QN108 0.50													
8x8 QN132 0.50				81	80	84	87/19						
8x8 CS201 0.50				120	157								
10x10 CS281 0.50						212			215/53	215/53			
10x10 QN180 0.50													
13x13 FG144 1.00					96	97	97/24	97/25	97/25	97/25			
14x14 CS289 0.80				120	157	212							
14x14 VQ100 0.50				77	71	71	68/13						
14x14 VQ128 0.40				101									
17x17 FG256 1.00							157/38	178/38	177/43	177/44	165/79		
19x19 FG324 1.00													221/110
20x20 TQ144 0.50					91	100							
20x20 VQ176 0.40					137								
23x23 FG484 1.00								194/38	235/60	300/74	270/135	280/139	341/168
27x27 FG676 1.00												444/222	
28x28 PQ208 0.50						133	151/34	151/34	154/35	154/35	147/65	147/65	147/65
31x31 FG896 1.00													620/310

Notes: *# / # structure shows single-ended/double-ended I/Os.*
Please refer to the Actel website and appropriate product datasheets for the latest device information and valid ordering codes.

Refer to www.actel.com for information regarding previous generations of flash and antifuse FPGAs.

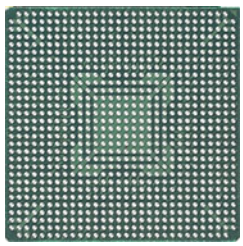
I/O Table

FPGA Packages

Key: **f** – family **bs** – package body size excluding leads **ps** – overall package dimensions including package leads **h** – package thickness **p** – pin pitch / ball pitch

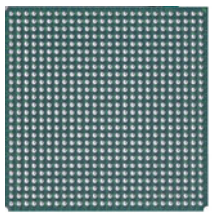
FG896

f IGLOOe
ProASIC3E*
ProASIC3L*
ps 31x31 mm
h 2.23 mm
p 1.00 mm



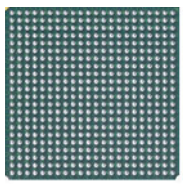
FG676

f ProASIC3E
Fusion*
ps 27x27 mm
h 2.23 mm
p 1.00 mm



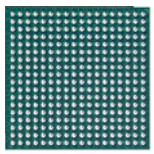
FG484

f IGLOO*
IGLOOe*
ProASIC3*†
ProASIC3E*†
ProASIC3L*
Fusion
ps 23x23 mm
h 2.23 mm
p 1.00 mm



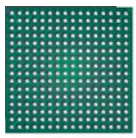
FG324

f ProASIC3E*
ProASIC3L*
ps 19x19 mm
h 1.63 mm
p 1.00 mm



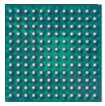
FG256

f IGLOO*
IGLOOe
ProASIC3*†
ProASIC3E†
ProASIC3L
Fusion*
ps 17x17 mm
h 1.60 mm
p 1.00 mm



FG144

f IGLOO*
ProASIC3*
ProASIC3L*
ps 13x13 mm
h 1.45 mm
p 1.00 mm



PQ208

f ProASIC3*
ProASIC3E*
ProASIC3L*
Fusion*
bs 28x28 mm
ps 30.6x30.6 mm
h 3.40 mm
p 0.50 mm

TQ144

f ProASIC3
bs 20x20 mm
ps 22x22 mm
h 1.40 mm
p 0.50 mm

VQ176

f IGLOO PLUS
bs 20x20 mm
ps 22x22 mm
h 1.00 mm
p 0.40 mm

VQ128

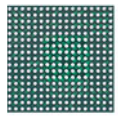
f IGLOO PLUS
bs 14x14 mm
ps 16x16 mm
h 1.00 mm
p 0.40 mm

VQ100

f IGLOO*
IGLOO nano
ProASIC3*
ProASIC3 nano
ProASIC3L
bs 14x14 mm
ps 16x16 mm
h 1.00 mm
p 0.50 mm

CS289

f IGLOO PLUS
ps 14x14 mm
h 1.20 mm
p 0.80 mm



CS281

f IGLOO
IGLOO PLUS
ps 10x10 mm
h 1.05 mm
p 0.50 mm

CS201

f IGLOO PLUS
ps 8x8 mm
h 0.89 mm
p 0.50 mm

CS196

f IGLOO
ps 8x8 mm
h 1.11 mm
p 0.50 mm

CS121

f IGLOO
ps 6x6 mm
h 0.90 mm
p 0.50 mm

CS81

f IGLOO
IGLOO nano
ps 5x5 mm
h 0.80 mm
p 0.50 mm

UC81

f IGLOO
IGLOO nano
ps 4x4 mm
h 0.80 mm
p 0.40 mm

UC36

f IGLOO nano
ps 3x3 mm
h 0.80 mm
p 0.40 mm

QN180

f Fusion
ps 10x10 mm
h 0.75 mm
p 0.50 mm

QN132

f IGLOO
ProASIC3
ps 8x8 mm
h 0.75 mm
p 0.50 mm

QN108

f Fusion
ps 8x8 mm
h 0.75 mm
p 0.50 mm

QN68

f IGLOO
IGLOO nano
ProASIC3
ProASIC3 nano
ps 8x8 mm
h 0.90 mm
p 0.40 mm

QN48

f IGLOO
IGLOO nano
ProASIC3
ProASIC3 nano
ps 6x6 mm
h 0.90 mm
p 0.40 mm

The **bs** dimension is the package body dimension *exclusive* of leads. The **ps** dimension is the overall package dimension *inclusive* of leads. Refer to the Actel Package Mechanical Drawings document located at **http://www.actel.com/documents/PckgMechDrwngs.pdf** for more information concerning package dimensions.

* Includes Cortex-M1 devices. † FG256 and FG484 are footprint-compatible for ProASIC3 and ProASIC3E.

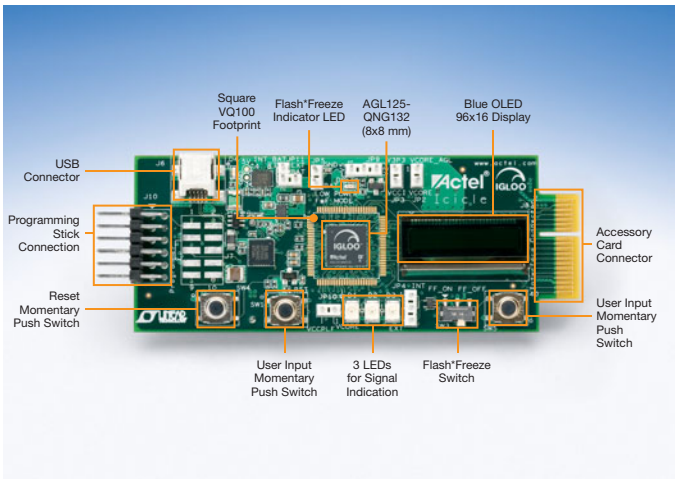
Libero IDE Tools and Editions

	Function			Tool	Editions			
					Evaluation	Gold	Platinum	Standalone
LIBERO IDE TOOLS*	Project Manager Tools	Device Support		Libero IDE	All Devices	Through 1,500,000 Gates	All Devices	All Devices
		Design Flow and File Management		Project Manager	✓	✓	✓	✓
		Pin Assignment / I/O Attributes		Project Manager	✓	✓	✓	✓
		Design Entry	Block System Design	SmartDesign	✓	✓	✓	✓
			Configurable Cores	Catalog	✓	✓	✓	✓
			HDL Editor	HDL Editor	✓	✓	✓	✓
			Schematic	ViewDraw® AE	✓	✓	✓	✓
		Synthesis		Synplify® AE	✓	✓	✓	
				Synplify Pro AE	✓		✓	
		Simulation		ModelSim® AE	✓	✓	✓	
		Testbench Generator		WaveFormer Lite™	✓	✓	✓	
		Testbench Generator Advanced Tools		WaveFormer Lite	✓		✓	
	Designer Tools	Floorplanning		MultiView Navigator	✓	✓	✓	✓
		Pin Assignment / I/O Attributes		MultiView Navigator	✓	✓	✓	✓
		Place-and-Route		Designer	✓	✓	✓	✓
		Timing Constraints		SmartTime	✓	✓	✓	✓
		Timing Analysis		SmartTime	✓	✓	✓	✓
		Power Analysis		SmartPower	✓	✓	✓	✓
		Program File Generation		Designer		✓	✓	✓
		Debug		SmartDebug	✓	✓	✓	✓
	Flash Programming			FlashPro		✓	✓	✓
	Flash Debug			Identify AE	✓	✓	✓	
	Antifuse Debug			Silicon Sculptor	✓	✓	✓	

Note:

** Windows® OS version. See www.Actel.com for details, operating system support, and other available tools.*

IGLOO Icicle Evaluation Kit

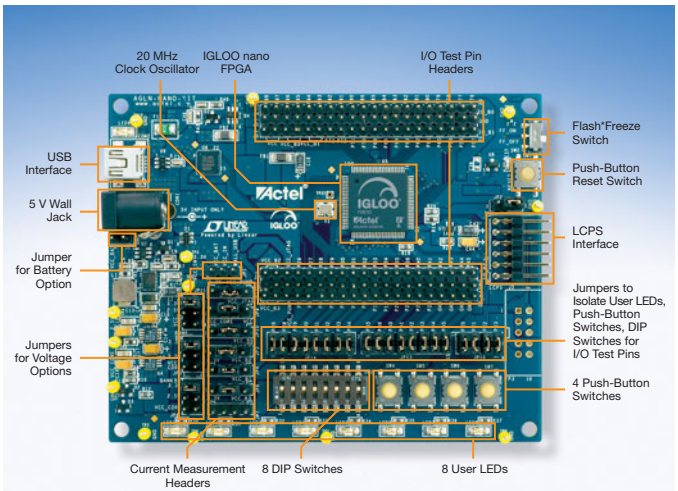


- **Supports IGLOO low-power FPGA demonstration and evaluation, including Flash*Freeze mode**
- **Free one-year Libero IDE software and Gold license**
- **FlashPro3 compatible low-cost programming stick**
- **Battery powered via included lithium-ion battery and built-in charger from USB cable**
- **Kit user's guide, Libero IDE tutorial, and design examples**
- **PCB schematics, layout files, and BOM**

- **Board features**
  - 96x16 OLED display
  - On-board current sensor to demonstrate low power
  - Full current measurement capability of independent I/O banks and V_{CC}
  - 20 MHz resistor-set oscillator
  - Reset, LEDs, and switches for simple inputs and outputs
  - Ability to switch V_{CC} from 1.2 V to 1.5 V
  - RoHS compliant

Ordering Code	Supported Device
AGL-ICICLE-KIT	AGL125-QNG132

IGLOO nano Starter Kit

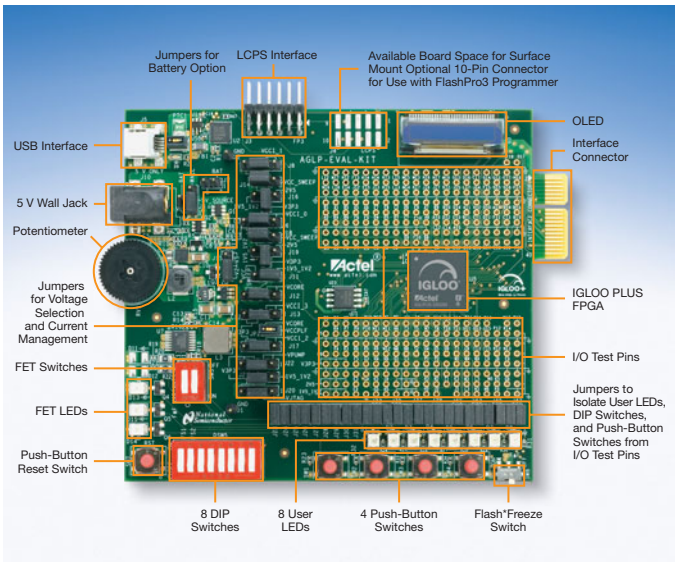


- **Supports basic IGLOO nano low-power FPGA design, including Flash*Freeze mode**
- **Free one-year Libero IDE software and Gold license**
- **FlashPro3 compatible low-cost programming stick**
- **International power supply and USB cables**
- **Kit user's guide, Libero IDE tutorial, and design examples**
- **PCB schematics, layout files, and BOM**

- **Board features**
  - 96x16 OLED display
  - All I/Os available for external connections
  - Full current measurement capability of independent I/O banks and V_{CC}
  - USB connection for USB-to-serial (RS232) interface for HyperTerminal or power
  - 20 MHz clock oscillator
  - LEDs and switches for simple inputs and outputs
  - Ability to switch V_{CORE} from 1.2 V to 1.5 V
  - RoHS compliant

Ordering Code	Supported Device
AGLN-Z-NANO-KIT	AGLN250V2-ZVQG100

IGLOO PLUS Starter Kit

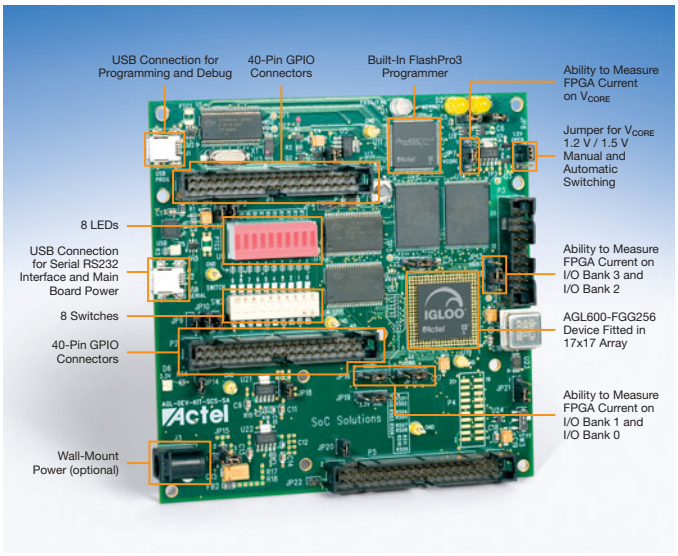


- **Supports basic IGLOO PLUS low-power FPGA design, including Flash*Freeze mode**
- **Free one-year Libero IDE software and Gold License**
- **FlashPro3 compatible low-cost programming stick**
- **International power supply and two USB cables**
- **Kit user's guide, Libero IDE tutorial, and design examples**
- **PCB schematics, layout files, and BOM**

- **Board features**
  - 96x16 OLED display
  - All I/Os available for external connection
  - Full current measurement capability of independent I/O banks
  - LEDs and switches for simple inputs and outputs
  - USB connection for USB-to-serial (RS232) interface for HyperTerminal or power
  - 20 MHz clock oscillator
  - LEDs and switches for simple inputs and outputs
  - Ability to switch V_{CORE} from 1.2 V to 1.5 V
  - RoHS compliant

Ordering Code	Supported Device
AGLP-EVAL-KIT	AGLP125V2-CSG289

ARM Cortex-M1 IGLOO Development Kit

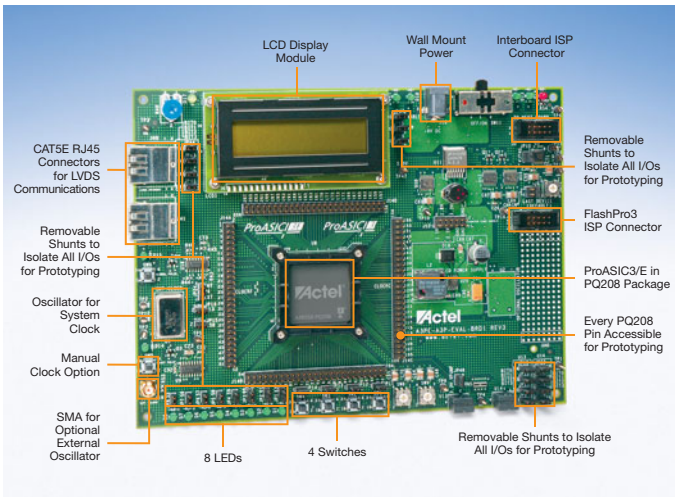


- **Supports royalty-free, industry-standard ARM Cortex-M1 development ***
- **Free one-year Libero IDE software and Gold license**
- **SoftConsole for program and debug**
- **FlashPro3-compatible built-in programmer**
- **International power supply and two USB cables**
- **Kit user's guide, Libero IDE tutorial, and design examples**
- **PCB schematics, layout files, and BOM**

- **Board features**
  - 1 MB of SRAM and 16 MB of flash memory provided on board
  - USB connection used for program and debug
  - USB connection for USB-to-serial (RS232) interface for HyperTerminal or power
  - Full current measurement capability of independent I/O banks and V_{CC}
  - Socketed 48 MHz system clock
  - LEDs and switches for simple inputs and outputs
  - RoHS compliant

Ordering Codes	Supported Devices
AGL-DEV-KIT-SCS	AGL600V2-FGG256
M1AGL-DEV-KIT-SCS*	M1AGL600V2-FGG484

ProASIC3 Starter Kit

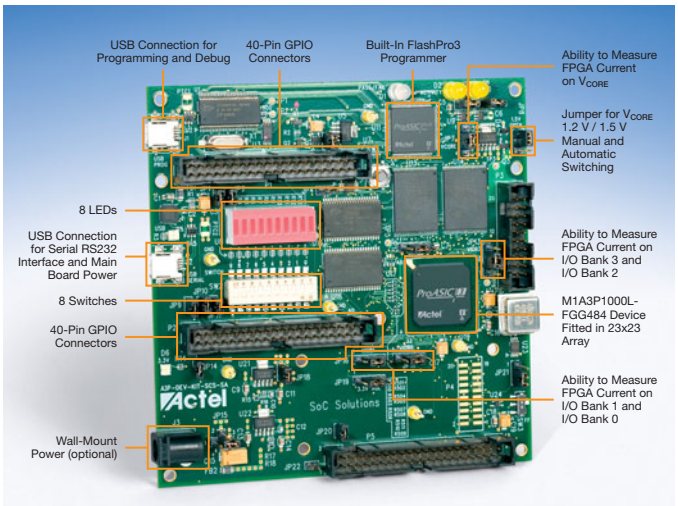


- **Supports basic ProASIC3 FPGA design and LVDS I/O usage**
- **Free one-year Libero IDE software and Gold license**
- **FlashPro3 Programmer***
- **Power supply and cables***
- **Kit user's guide, Libero IDE tutorial, and design examples**
- **PCB schematics, layout files, and BOM**

- **Board features**
  - Eight I/O banks with variety of voltage options
  - Oscillator for system clock or manual clock option
  - LEDs and switches for simple inputs and outputs
  - LCD display module
  - Two CAT5E RJ45 connectors for high-speed LVDS communications
  - All I/Os available for external connections
  - Not RoHS compliant

Ordering Codes	Supported Devices
A3PE-PROTO-KIT	A3PE1500-PQ208
A3PE-BRD1500-SKT*	A3PE1500-PQ208

ARM Cortex-M1 ProASIC3L Development Kit

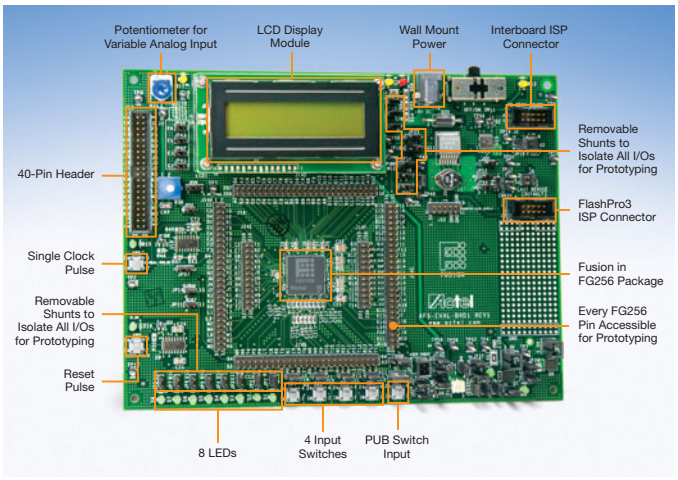


- **Supports royalty-free, industry-standard ARM Cortex-M1 development**
- **Free one-year Libero IDE software and Gold license**
- **SoftConsole for program and debug**
- **FlashPro3 compatible built-in programmer**
- **International power supply and two USB cables**
- **Kit user's guide, Libero IDE tutorial, and design examples**
- **PCB schematics, layout files, and BOM**

- **Board features**
  - 1 MB of SRAM and 16 MB of flash memory provided on board
  - USB connection used for program and debug
  - USB connection for USB-to-serial (RS232) interface for HyperTerminal or power
  - Full current measurement capability of independent I/O banks and V_{CC}
  - Socketed 48 MHz system clock
  - LEDs and switches for simple inputs and outputs
  - RoHS compliant

Ordering Code	Supported Device
M1A3PL-DEV-KIT	M1A3P1000L-FGG484

Fusion Starter Kit

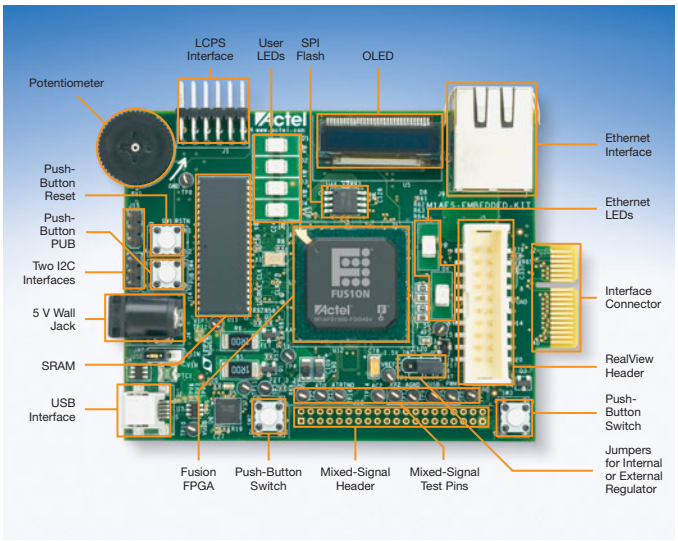


- **Supports basic ProASIC3 FPGA design and LVDS I/O usage**
- **Free one-year Libero IDE software and Gold license**
- **FlashPro3 programmer**
- **Power supply and cables**
- **Kit user's guide, Libero IDE tutorial, and design examples**
- **PCB schematics, layout files, and BOM**

- **Board features**
  - Independent variable I/O bank settings
  - On-chip 1 percent RC oscillator, a crystal oscillator circuit, and PLLs support system clock generation
  - LEDs and switches for simple inputs and outputs
  - LCD display module
  - Multi-color LED illustrates temperature changes and pulse width modulation (PWM) fan control
  - RoHS compliant

Ordering Code	Supported Device
AFS-EVAL-KIT	AFS600-FG256

Fusion Embedded Development Kit

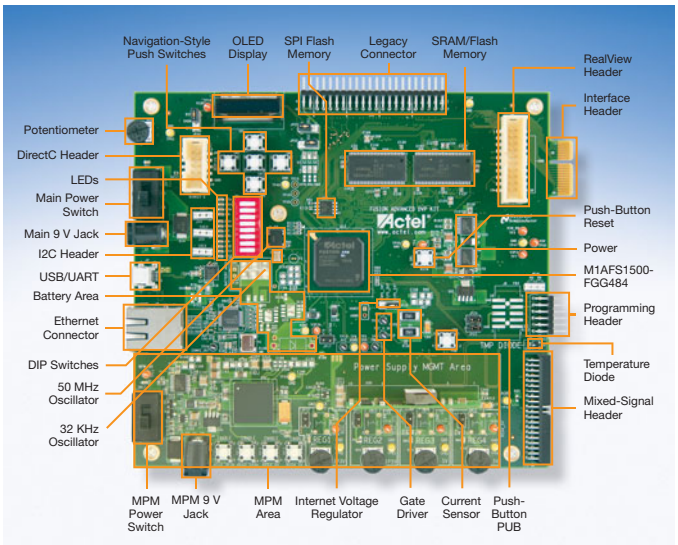


- **Supports royalty-free, industry-standard ARM Cortex-M1 or 8051 development**
- **Free one-year Libero IDE software and Gold license**
- **SoftConsole for program and debug**
- **FlashPro3 compatible low-cost programming stick**
- **International power supply and two USB cables**
- **Kit user's guide, Libero IDE tutorial, and design examples**
- **PCB schematics, layout files, and BOM**

- **Board features**
  - 512 KB SRAM, 2 MB SPI flash memory provided on board
  - 10/100 Ethernet and I2C interfaces
  - USB-to-UART connection for HyperTerminal on a PC
  - Built-in voltage, current, and temperature monitor and voltage potentiometer
  - Mixed-signal interface
  - Blue OLED 96x16 pixel display
  - Dynamic reconfigurable analog and flash memory
  - FlashPro3 and RealView® debug interface
  - RoHS compliant

Ordering Code	Supported Device
M1AFS-EMBEDDED-KIT	M1AFS1500-FGG484

Fusion Advanced Development Kit



- **Supports royalty-free, industry-standard ARM Cortex-M1 or 8051 development**
- **Free one-year Libero IDE software and Gold license**
- **SoftConsole for program and debug**
- **FlashPro3 compatible built-in programmer**
- **Order two 9 V power pack or combined kit***
- **Kit user's guide, Libero IDE tutorial, and design examples**
- **PCB schematics, layout files, and BOM**

- **Board features**
  - 16 MB SRAM, 2 MB SPI flash, 128-Mbit parallel flash
  - 10/100 Ethernet, USB-to-UART and I2C interfaces
  - Built-in voltage, current, and temperature monitor
  - Mixed-signal interface
  - Blue OLED 96x16 pixel display
  - Dynamic reconfigurable analog and flash memory
  - FlashPro3 and RealView debug interface
  - RoHS compliant

Ordering Codes	Supported Devices
M1AFS-ADV-DEV-KIT	M1AFS1500-FGG484
M1AFS-ADV-DEV-KIT-PWR*	M1AFS1500-FGG484

FlashPro3 In-System FPGA Programmer

- **Supports in-system programming**
- **Supports IEEE 1149 JTAG programming through STAPL**
- **Supports IEEE 1532**
- **Free software updates**
- **Self-test option**
- **Connections to parallel port and USB port available**
- **Operating systems:**
  - Windows XP Professional (SP2 recommended)
  - Windows 2000 Professional (SP4 recommended)

Ordering Code
FLASHPRO 3

Silicon Sculptor 3 FPGA Programmer

- **Programs all Actel packages, including PLCC, PQFP, VQFP, VQFP, QFN, BGA, FBGA, and CSP**
- **Universal Actel socket adapters**
- **Use with Silicon Sculptor software**
- **Security fuse can be programmed to secure the devices**
- **Includes self-test to test its own hardware**
- **Protection features:**
  - Overcurrent shutdown
  - Power failure shutdown
  - ESD protection
  - ESD wrist straps with banana jacks (included as standard)
- **Operating systems:**
  - Windows XP Professional (SP2 recommended)
  - Windows 2000 Professional (SP4 recommended)

Ordering Code
SILICON-SCULPTOR 3

For adapter modules, refer to *www.actel.com/products/hardware/program_debug/ss/modules.aspx.*

Programming Devices In-System Using a Microprocessor

Although the FlashPro3 programmer can perform in-system programming, it does require a specific header to be connected externally. For example, if your system already has external communication available through a microprocessor interface, you may prefer to have the processor perform the in-system programming. This can be done in two ways.

DirectC

DirectC v2.3 is a set of C code designed to support embedded microprocessor–based in-system programming for IGLOO, ProASIC3, and Fusion families. To use DirectC v2.3, you must make some minor modifications to the provided source code, add the necessary API, and compile the source code and the API together to create a binary executable. The target system must contain a microprocessor with a minimum 256 bytes of RAM, a JTAG interface to the target device from the microprocessor, and access to the programming data to be used for programming the FPGA. Access to programming data could be provided by a telecommunications link for most remote systems.

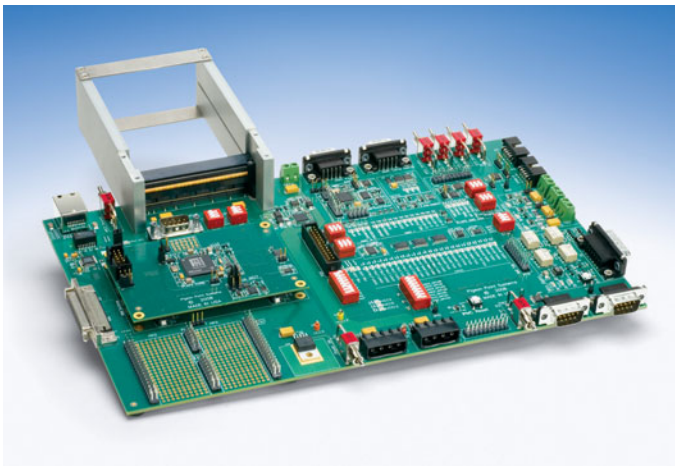
Download DirectC source files and the complete user's guide:
http://www.actel.com/products/hardware/program_debug/directc/default.aspx

STAPL Player

The STAPL Player may be used to program third-generation flash devices such as IGLOO, ProASIC3, and Fusion, and interprets the contents of a STAPL file, which is generated by Actel's Libero IDE software tools. The file contains information about the programming of Actel flash-based devices, as well as the JTAG scan chain for a single device. The data format is a JEDEC standard known as the Standard Test and Programming Language (STAPL) format. For third-generation devices, note that the STAPL Player will not support serialization of the FlashROM nor will it support Smart Erase-enabled silicon. The STAPL Player reads the STAPL file and executes the file's programming instructions. Because all programming details are in the STAPL file, the STAPL Player itself is completely device-independent. In other words, the system does not need to implement any programming algorithm details; the STAPL file provides all of the details.

The key differences between the DirectC and the STAPL player methods are in the memory footprint in the microprocessor and amount of data to transmit. The DirectC option requires more code space on the processor but as a result less data has to be transmitted to perform programming. On the other hand the STAPL player communicates both the information to be programmed and the intelligence needed to perform programming. So the code footprint is smaller but the amount of data to transmit will be larger. One advantage of the STAPL player method is that if updates are required to the programming algorithm, the STAPL method does not require new code in the processor, but the DirectC would require new code for the processor.

Pigeon Point Systems Products



Pigeon Point Systems AdvancedTCA and AdvancedMC Carrier Board Management Reference (BMR) Starter Kits

- **AdvancedTCA® (ATCA) and AdvancedMC™ (AMC) benchtop development board implementing an IPM Controller (IPMC) and Carrier IPMC**
- **Pigeon Point™ ShMM-500R-based benchtop Shelf Manager board**
- **Complete Libero IDE design for Fusion mixed-signal FPGA**
- **Comprehensive user's guide, hardware and software architecture documentation**
- **Pigeon Point firmware, including source code**
- **Support for FGG256 or FGG484 package, with or without external SRAM**
- **Benchtop development board features**
  - AdvancedMC slot with connector and guide to attach a customer AdvancedMC for development and testing
  - Complete on-board AVR-based Module Management Controller (MMC) simulating a second AMC site
  - Mezzanine-implemented P1 Fusion core IPMC for future flexibility
  - LEDs and switches for configuration, state signaling, and control
  - FPGA prototyping area for testing FPGA extensions
  - RoHS compliant

Ordering Code	Supported Devices	Price
Contact Pigeon Point Systems	P1AFS600-2FGG256I P1AFS600-2FGG484I P1AFS1500-2FGG256I P1AFS1500-2FGG484I	Contact Pigeon Point Systems

Pigeon Point Shelf Management Mezzanine Products

Products	Supported Devices	Descriptions
Pigeon Point ShMM-500R and Shelf Manager	MIPS-32	Core of an AdvancedTCA Shelf Manager, complete with a 333 MHz 32-bit RISC processor, SDRAM, and flash, plus dual IPMB, Ethernet, and serial interfaces
Pigeon Point Shelf Manager Source Code	All ShMM Processors	Enables sophisticated users or developers of ShMM-based shelves to replace the Shelf Manager on their ShMMs with a customized or extended version.

Other Pigeon Point Board Management Reference Products

Products	Supported Devices	Descriptions
AdvancedTCA IPM Controller	H8S	A complete hardware and firmware solution for the mandatory IPMC on all ATCA boards and other intelligent FRUs, such as fan trays or PEMs
AdvancedMC Carrier IPM Controller Add-on	H8S	Augments a Pigeon Point ATCA IPMC with the additional hardware and firmware needed to implement the Carrier IPMC on an AMC carrier board.
AdvancedMC Module Management Controller	AVR	A complete hardware and firmware solution for the mandatory MMC on all AMC modules, compatible with either ATCA carriers or MicroTCA® shelves
MicroTCA Carrier Management Controller	H8S	A complete hardware and firmware solution for the mandatory MicroTCA Carrier Management Controller (MCMC) on a MicroTCA Carrier Hub (MCH), which includes the MCMC, Carrier Manager, and an optionally installed Shelf Manager, all executing on a single microcontroller
Enhanced Module Management Controller	H8S	A complete hardware and firmware solution for the mandatory Enhanced Module Management Controller (EMMC) on MicroTCA modules such as OEM modules or Cooling Units

You May Be Interested In:

IGLOO Product Brochure: http://www.actel.com/documents/IGLOO_PIB.pdf
ProASIC3 Product Brochure: http://www.actel.com/documents/PA3_E_PIB.pdf
Fusion Product Brochure: http://www.actel.com/documents/Fusion_PIB.pdf

For more information regarding Actel products, please contact your local Actel sales representative.

Actel is the leader in low-power and mixed-signal FPGAs and offers the most comprehensive portfolio of system and power management solutions. Power Matters. Learn more at www.actel.com

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