Short Form Data Sheet
February 2013

MAX24605, MAX24610
5- or 10-Output Clock Multiplier / Jitter Attenuator ICs

General Description

The MAX24605 and MAX24610 are flexible, high-performance clock multiplier and jitter attenuator ICs that include a DPLL and two independent APLLs. When locked to one of two input clock signals, the device performs any-to-any frequency conversion. From any input clock frequency 2kHz to 750MHz the device can produce frequency-locked APLL output frequencies up to 750MHz and as many as 10 output clock signals that are integer divisors of the APLL frequencies. Input jitter can be attenuated by an internal low-bandwidth DPLL. The DPLL also provides glitchless switching between input clocks and numerically controlled oscillator capability. Input switching can be manual or automatic. Using only a low-cost crystal or oscillator, the device can also serve as a frequency synthesizer IC. Output jitter is typically 0.18 to 0.3ps RMS for an APLL-only integer multiply and 0.25 to 0.4ps RMS for APLL-only fractional multiply or DPLL+APLL operation.

Applications

Jitter Attenuation, Frequency Conversion and Frequency Synthesis Applications in a Wide Variety of Equipment Types

Ordering Information

PART	OUTPUTS	TEMP RANGE	PIN-PACKAGE
MAX24605EXG+	5	-40 to +85	81-CSBGA
MAX24610EXG+	10	-40 to +85	81-CSBGA

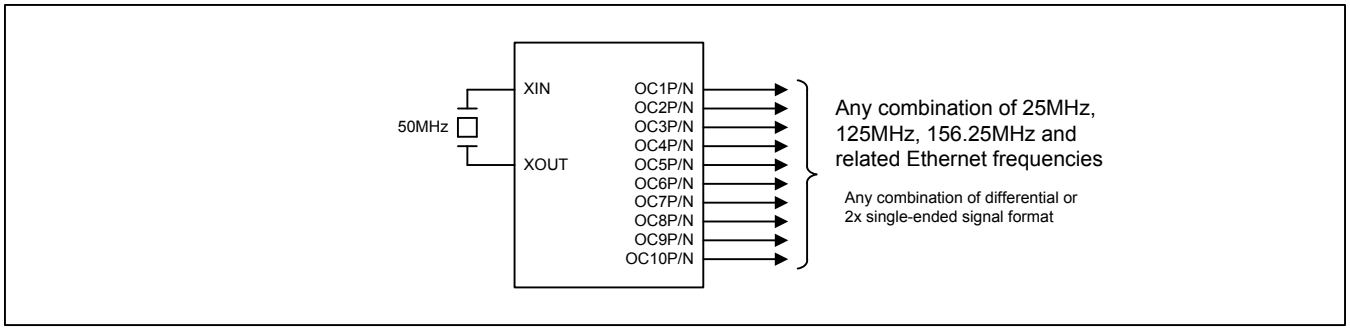
+Denotes a lead(Pb)-free/RoHS-compliant package.

Features

- **Input Clocks**
  - One Crystal Input
  - Two Differential or CMOS/TTL Inputs
  - Differential to 750MHz, CMOS/TTL to 160MHz
  - Continuous Input Clock Quality Monitoring
  - Automatic or Manual Clock Selection
  - Glitchless Reference Switching
- **Low-Bandwidth DPLL**
  - Programmable Bandwidth, 4Hz to 400Hz
  - Attenuates Input Jitter up to Several UI
  - Manual Phase Adjustment
- **Two APLLs Plus 5 or 10 Output Clocks**
  - APLLs Perform High Resolution Fractional-N Clock Multiplication
  - Any Output Frequency from <1Hz to 750MHz
  - Each Output Has an Independent Divider
  - Output Jitter Typically 0.18 to 0.3ps RMS for APLL-Only Integer Multiply and 0.25 to 0.4ps RMS for Other Modes (12kHz to 20MHz)
  - Outputs are CML or 2xCMOS, Can Interface to LVDS, LVPECL, HSTL, SSTL and HCSL
  - CMOS Output Voltage from 1.5V to 3.3V
- **General Features**
  - Automatic Self-Configuration at Power-Up from External EEPROM Memory
  - Uses External Crystal, Oscillator or Clock Signal As Master Clock
  - Internal Compensation for Local Oscillator Frequency Error
  - SPI Processor Interface
  - 1.8V + 3.3V Operation (5V Tolerant)
  - -40 to +85°C Operating Temp. Range
  - 10mm x 10mm CSBGA Package

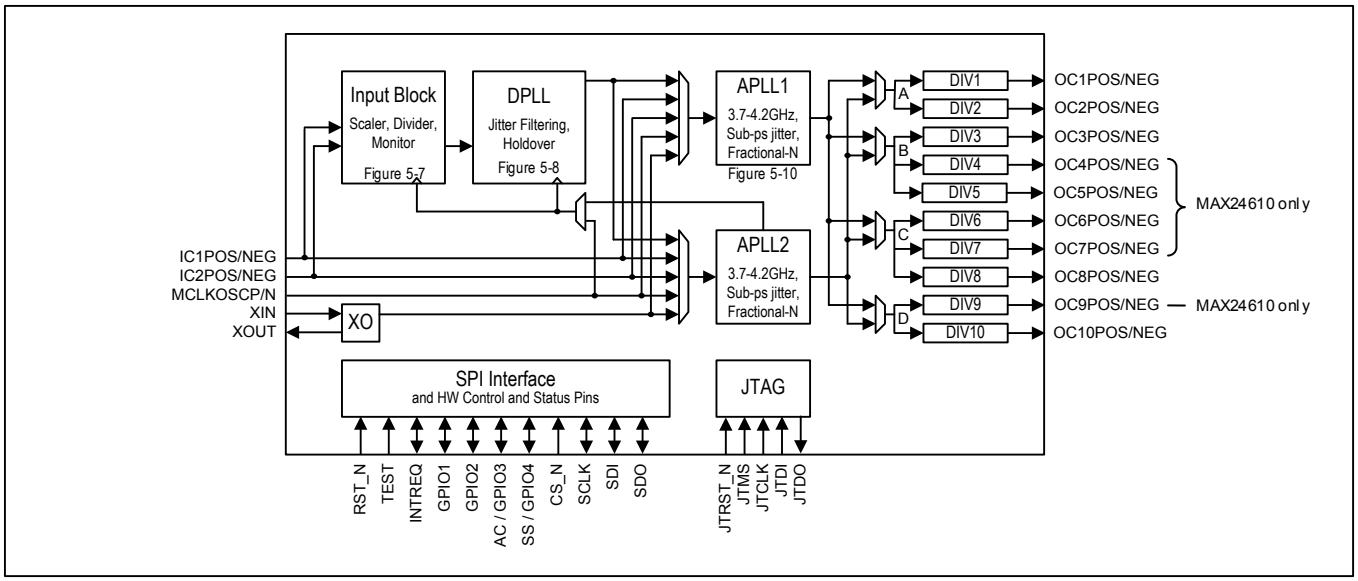
1. Application Examples

Figure 1-1. Frequency Multiplication and Fanout of Ethernet Clocks



2. Block Diagram

Figure 2-1. Block Diagram



3. Detailed Features

3.1 Input Block Features

- Two input clocks, differential or CMOS/TTL signal format
- Input clocks can be any frequency from 1Hz up to 750MHz
- Per-input fractional scaling (i.e. multiplying by N÷D where N is a 16-bit integer and D is a 32-bit integer and N<D) to undo 64B/66B and FEC scaling (e.g. 64/66, 238/255, 237/255, 236/255)
- All inputs constantly monitored by programmable activity monitors and frequency monitors
- Fast activity monitor can disqualify the selected reference after a few missing clock cycles
- Frequency measurement with 1.25ppm resolution
- Frequency monitor thresholds with 1.25ppm or 5ppb resolution

3.2 DPLL Features

- Very high-resolution DPLL architecture
- Sophisticated state machine automatically transitions between free-run, locked, and digital hold states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 4Hz to 400Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10 or 20
- Multiple phase detectors: phase/frequency and multicycle
- Phase/frequency locking (±360° capture) or nearest-edge phase locking (±180° capture)
- Multicycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- Output phase adjustment up to ±200ns in 6ps steps with respect to selected input reference
- High-resolution frequency and phase measurement
- Numerically controlled oscillator (NCO) mode allows system software to steer DPLL frequency

3.3 APLL Features

- Two independent APLLs simultaneously product two frequency families from the same reference clock or different reference clocks
- Very high-resolution fractional scaling (i.e. non-integer multiplication)
- Output jitter is typically 0.18 to 0.3ps RMS for APLL-only integer multiply and 0.25 to 0.4ps RMS for APLL-only fractional multiply or DPLL+APLL operation (12kHz to 20MHz integration band, for output frequencies >100MHz)
- Bypass mode for each APLL supports system testing and allows device to be used in fanout applications

3.4 Output Clock Features

- Ten low-jitter output clocks
- Each output can be one differential output or two CMOS/TTL outputs
- Outputs easily interface with CML, LVDS, LVPECL, HSTL, SSTL, HCSL components
- Each output can be any integer divisor of either APLL output clock
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can also produce clock frequencies for microprocessors, ASICs, FPGAs and other components
- Per-output delay adjustment
- Per-output enable/disable

3.5 General Features

- SPI serial microprocessor interface
- Optional automatic self-configuration at power-up from external EEPROM memory
- Four general-purpose I/O pins
- Register set can be write-protected
- Can operate as DPLL+APLL for jitter filtering or as APLL only
- Local oscillator can be nearly any frequency from 10MHz to 210MHz
- Internal compensation for local oscillator frequency error

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