VCC6-1320-156M250000

LVDS Crystal Oscillator Data Sheet

Description

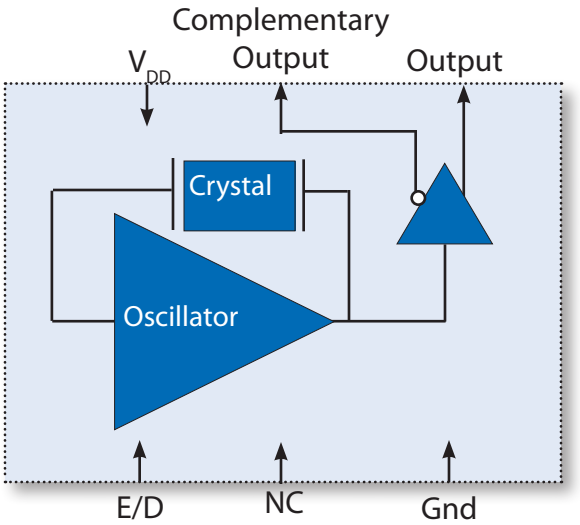
Vectron's VCC6 Crystal Oscillator is a quartz stabilized, differential output oscillator, operating off a 3.3 volt supply, hermetically sealed 5x7 ceramic package.

Features

- Ultra Low Jitter Performance, Fundamental Oscillator Design
- 156.25 MHz Output Frequency
- <1 ps RMS jitter, 12kHz-20MHz
- Differential Output
- Enable/Disable
- -55/105°C Operation
- Hermetically Sealed 5x7 Ceramic Package
- Product is compliant to RoHS directive and fully compatible with lead free assembly

Applications

Block Diagram



Performance Specifications

Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	3.165	3.3	3.465	V
Current (No Load)	I_{DD}			60	mA
Frequency					
Nominal Frequency	f_N		156.25		MHz
Stability[2,]				±50	ppm
Outputs					
Output Logic Levels[3] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 0.9	 1.43 1.10	 1.6	V
Differential Output		247	350	454	mV
Differential Output Error			50		mV
Offset Voltage		1.125	1.25	1.375	V
Offset Voltage Error			150		mV
Output Leakage Current				10	uA
Output Rise and Fall Time[3] Rise Time Fall Time	t_R/t_F			 600 600	 ps ps
Load, Connected Differential			100		ohms
Duty Cycle[4]		45	50	55	%
Jitter (12 kHz - 20 MHz BW)[5] Phase Noise[5] 10 100 1kHz 10kHz 100kHz 1MHz 10MHz 20MHz	ϕJ		0.3 -68 -100 -125 -140 -142 -142 -142 -142	1	ps dBc/Hz
Period Jitter rms[6] Period Jitter peak-peak[6]	ϕJ		2.4 22		ps ps
Spurious Response[1,5], 12kHz-20MHz				-110	dBc
Enable/Disable					
Output Enabled[7] Output Disabled	V_{IH} V_{IL}	$0.7*V_{DD}$		 $0.3*V_{DD}$	V V
Disable Time	t_D			200	ns
Enable/Disable Leakage Current				±200	uA
Start-Up Time	t_{SU}			10	ms
Operating Temp	T_{OP}	-55		105	°C
Package Size			5.0 x 7.0 x 1.8		mm

1. The VCC6 power supply pin should be filtered, eg, a 10uF, 0.1uF and 0.01uf capacitor.
2. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
3. Figure 1 defines these parameters.
4. Duty Cycle is defines as the On Time / Period.
5. Measured using an Agilent E5052, AC coupled (passive connection)
6. Measured using a Wavecrest SIA330C, 90K samples, AC coupled (passive connection).
7. Outputs will be Enabled if Enable/Disable is left open.

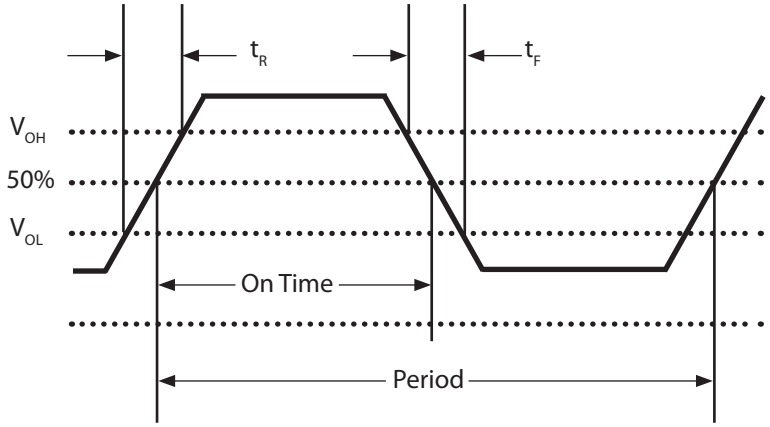


Figure 1

Package and Pinout

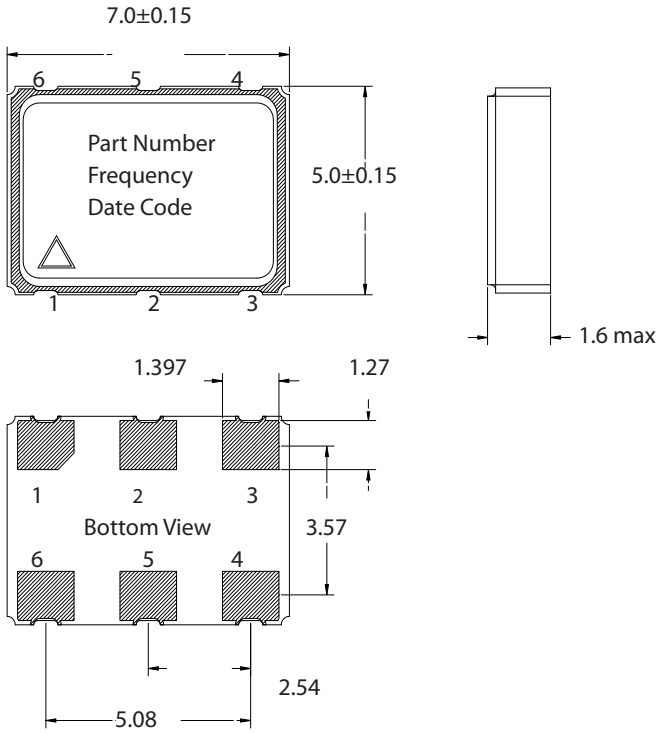


Figure 2 Package Outline Drawing

Table 2. Pinout

Pin #	Symbol	Function
1	E/D	Enabale Disable
2	NC	No Connection
3	GND	Electrical and Lid Ground
4	f_O	Output Frequency
5	Cf_O	Complementary Output Frequency
6	V_{DD}	Supply Voltage

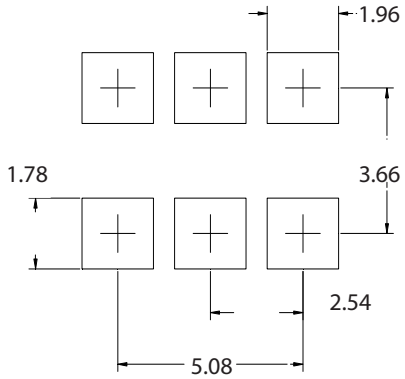


Figure 3 Pad Layout

LVDS Application Diagrams

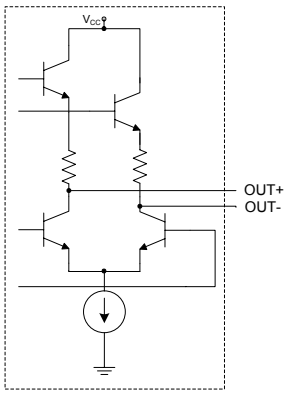


Figure 4 Standard LVDS Output Configuration

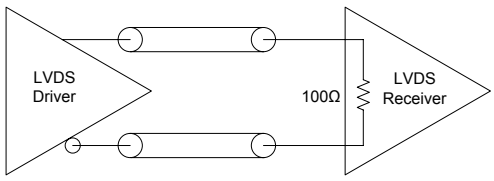


Figure 5 LVDS to LVDS Connection, Internal 100ohm
Some LVDS structures have an internal 100 ohm resistor on the input and do not need additional components.

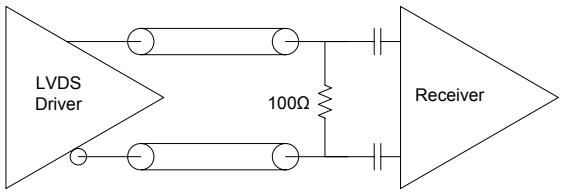


Figure 6 LVDS to LVDS Connection External 100ohm and AC blocking caps
Some input structures may not have an internal 100 ohm resistor on the input and will need an external 100ohm resistor for impedance matching. Also, the input may have an internal DC bias which may not be compatible with LVDS levels, AC blocking capacitors can be used.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

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Environmental and IR Compliance

Table 3. Environmental Compliance

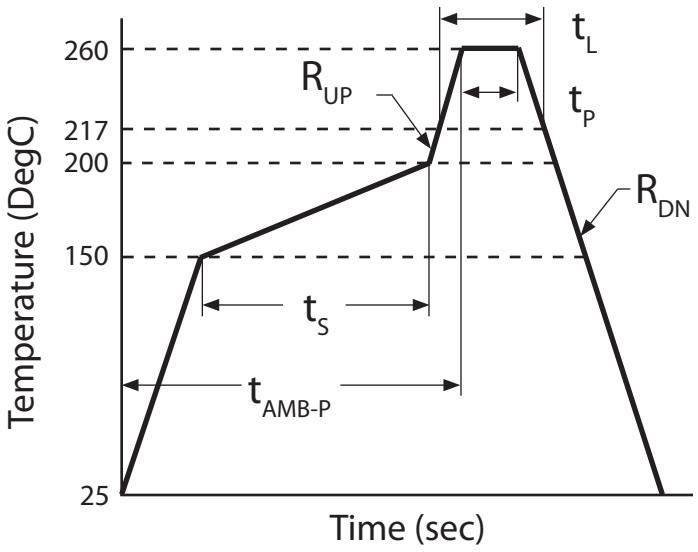
Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Fine and Gross Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-883 Method 2015
Moisture Sensitivity Level	MSL1
Contact Pads	Gold (0.3um min - 1.0um max) over Nickel

IR Compliance

Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 5. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220C.

Table 4. Reflow Profile		
Parameter	Symbol	Value
PreHeat Time	ts	200 sec Max
Ramp Up	R_{UP}	3°C/sec Max
Time above 217°C	tL	150 sec Max
Time to Peak Temperature	tAMB-P	480 sec Max
Time at 260°C	tP	10 sec Max
Time at 240°C	tP2	60 sec Max
Ramp down	R_{DN}	6°C/sec Max



Maximum Ratings, Tape & Reel

Absolute Maximum Ratings and Handling Precautions

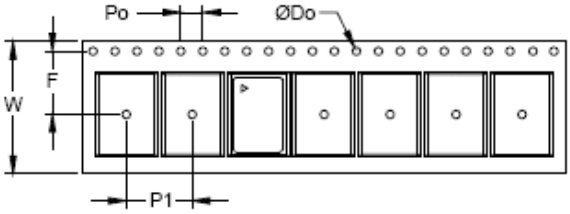
Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

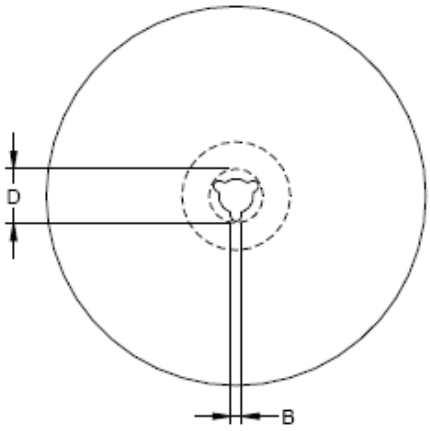
Although ESD protection circuitry has been designed into the VCC6, proper precautions should be taken when handling and mounting, VI employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation.
ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

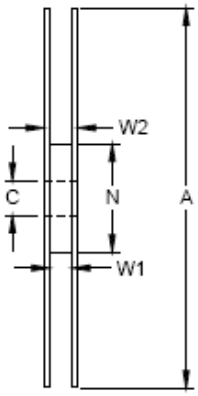
Table 5. Maximum Ratings			
Parameter	Symbol	Rating	Unit
Storage Temperature	T_{STORE}	-57/125	°C
Supply Voltage		-0.5 to 5.0	V
Enable Disable Voltage		-0.5 to V_{DD}+0.5	
ESD, Human Body Model		1000	V
ESD, Charged Device Model		1000	V

Table 6. Tape and Reel Information

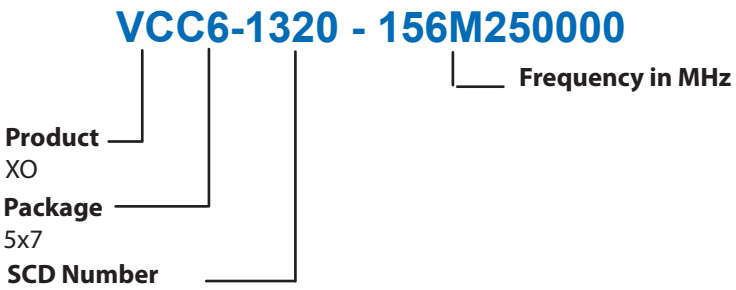
Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
16	7.5	1.5	4	8	180	2	13	21	50	17	21	200







Ordering Information



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