ZL70250 Ultra-Low-Power Sub-GHz RF Transceiver

Features

- Ultralow Power
  - Typical TX Current (at 50-Ω match): <2mA at −13dBm;<5mA at −2dBm
  - Typical RX Current: <1.9mA
  - Sleep Current: <500nA
  - Supply: 1.2V to 1.8V
- Radio Operating Frequency Range: 795 to 965MHz
  - North American ISM Band: 902 to 928MHz
  - European SRD Bands: 863 to 870MHz
- Radio Performance
  - Raw Data Rate: 186kbit/s
  - TX Power: up to 0dBm
  - RX Sensitivity: −90dBm Typical at 186kbit/s
- Very Few External Components
  - Only Crystal and Bias Resistor
- Standard Interfaces
  - SPIbus Master for Packet Data
  - Two-Wire for Status and Control
- MAC
  - Clear Channel Assessment
  - Sniff with Automatic Receive or Sleep
  - Automatic Clear-to-Send, Turn-Around, and Sleep
  - Receiver AGC
  - Packetization
  - Preamble and Frame Sync
  - Whitening
- RoHS Compliant

Applications

- Body-Area Network
- Energy Harvesting
- Wireless Sensor Network
- Remote Control
- Voice/Compressed Audio Communication
- RF Switch
- Active RFID
- Inventory Management

Description

The ZL70250 ultra-low-power RF transceiver provides a wireless link in applications where power consumption is of primary importance. The transceiver's ultralow power requirements allow the use of a coin-cell battery or energy-harvesting methods, enabling devices with extremely small form factors.

The ultra-low-power device operates in unlicensed frequency bands between 795 and 965MHz with a data rate of 186kbit/s to support voice/compressed audio communication. Duty cycling can be employed for applications that require lower average payload to further reduce power consumption.

Ordering Information

36-Pin CSP, SAC405, in Tray – ZL70250UEJ2
36-Pin CSP, SAC405, in T&R – ZL70250UEB2

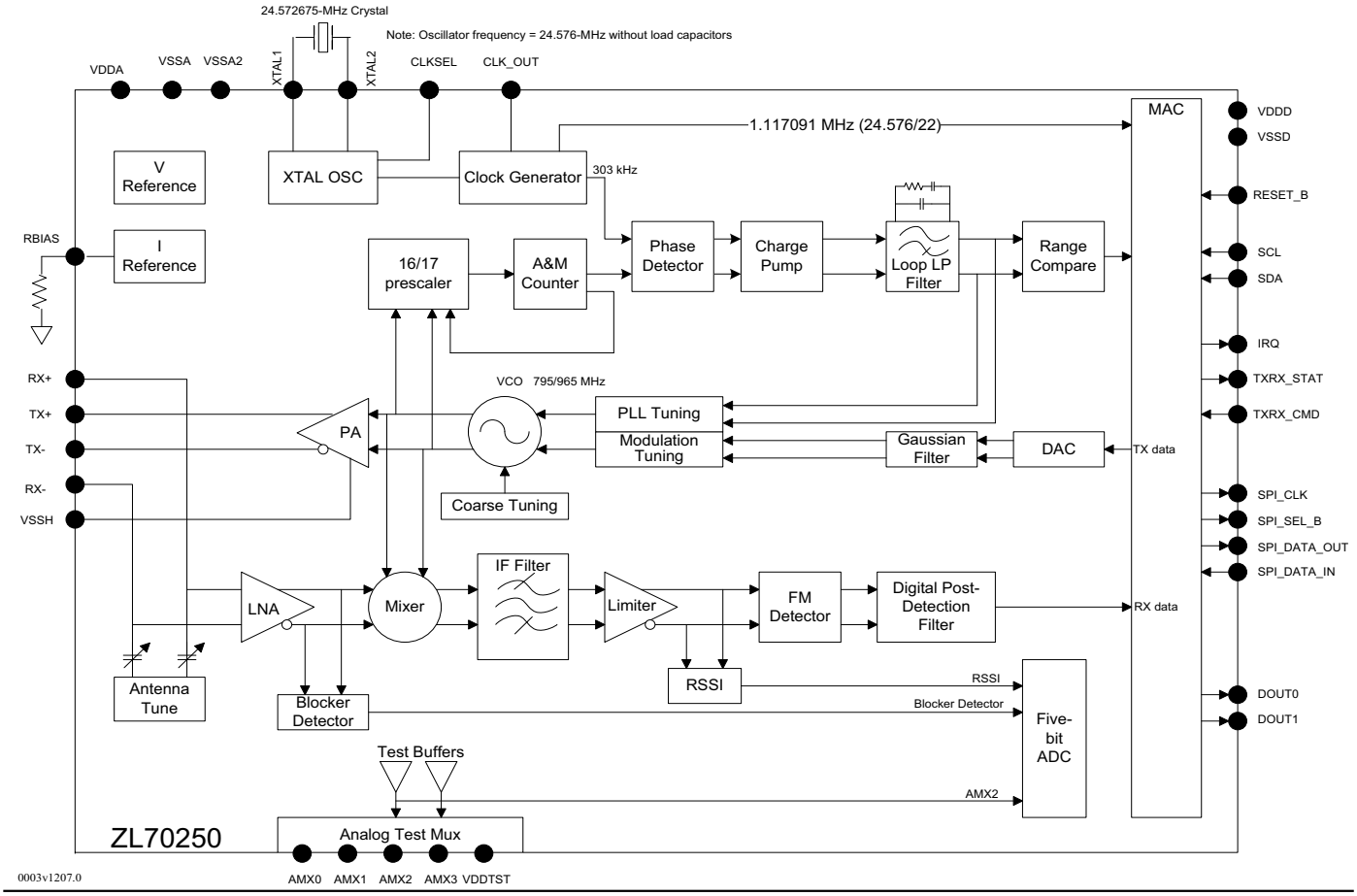


Figure 1 • **ZL70250 Block Diagram**

Table of Contents

List of Figures

List of Tables

1 – Overview

The ultra-low-power ZL70250 RF transceiver enables RF telemetry in applications powered by coin-cell batteries or energy harvesting, where wireless telemetry was previously unfeasible. End applications may include wireless sensors, body-area networks (principally on-body sensors), or voice communication.

With a typical peak/average current consumption below 2 mA in both transmit and receive, and with a data rate of 186 kbit/s, the ZL70250 enables bidirectional RF links with an impressive efficiency of 13 nJ/bit over a range of up to 100 meters.

The output power is programmable and can be reduced to −25 dBm to save power in cases where the link budget allows it, or can be increased up to 0 dBm for more range or to allow for system losses such as a very small antenna or body tissue absorption.

To achieve the minimum possible power consumption, the ZL70250 offers many optimization parameters, all available to the user via the control interface. To streamline the setup and optimization process, most parameters have an on-chip automatic trim capability. The frequency tuning is also highly automated.

In addition to its very low power consumption, the ZL70250 also includes a highly flexible Media Access Controller (MAC) that offers all the basic functions needed to implement a link layer with the minimum amount of data transfer between the ZL70250 and its controller. Some of the capabilities are:

- Digital RSSI and blocker indicator
- Clear channel assessment
- Transmit with automatic clear-to-send
- Sniff with automatic receive or sleep
- Receiver AGC (programmable)
- Preamble and frame sync generation and detection
- Whitening
- Packetization with programmable size for both transmit and receive
- Automatic sleep after receive
- Automatic turnaround for bidirectional data transfer

The ZL70250 is also highly integrated. Besides the antenna and, in some cases, its matching network, only a crystal and a bias resistor are required.

The ZL70250 is an ultra-low-power RF transceiver operating in unlicensed frequency bands between 795 and 965 MHz. It offers a data rate of 186 kbit/s in 300-kHz-wide channels.

The ZL70250 includes a frequency synthesizer, transmit and receive RF circuitry (shown in Figure 1 on page I), and a MAC for performing bit and frame synchronization, transmit and receive control, and other digital functions.

The ZL70250 transceiver transmits and receives GFSK-modulated digital data over one 300-kHz-wide channel using time-division multiplexing. The channel frequency and other features are configurable via registers that must be programmed over the control interface.

Registers control selective shutdown of the device in order to conserve power. The device does not contain any timing circuits necessary for periodic wake-up and channel sniffing; this is left to the system host.

The system host initiates and controls Clear Channel Assessment (CCA) at a high level. CCA consists of the RSSI level and mixer peak detector output (blockers) for the currently programmed receiver channel. CCA of other channels requires the host to set the receiver for those channels one at a time and to request and read the RSSI and blocker registers.

Although many different channel frequencies can be selected by programming the synthesizer dividers, the IF has been chosen such that six adjacent channels can operate within the same range without interference in both the US and Europe, assuming there are vacant bands that are four channels wide both above and below the six used channels. The vacant bands are necessary because— due to limitations on power, size, and external components— the architecture does not include image cancellation or image filtering. The polarity of the receiver data output is programmable to allow for a high-side LO or a low-side LO.

The ZL70250 is configurable for operation with minimal external components. In some applications the only necessary external components are an antenna, a crystal, and a resistor (49.9kΩ ±1%) to set the nominal bias current. The capacitors for antenna tuning and crystal oscillator trimming reside on the chip. The transmit power amplifier has a separate ground pin and is able to drive the antenna such that the voltage at its end points swings above the VDD supply.

The MAC handles the received and transmitted data. The MAC also includes the programming interface, trim and test modes, transmit and receive switching, and any other controllable functions on the chip. The transmitted and received data is exchanged with the system host or other devices via dedicated pins. No conversion to or from encoded audio data formats is done on the chip. Transmit and receive timing is controlled by the system host via a single pin. The TX-RX turnaround timing is programmable and resides in the ZL70250.

2 – Functional Description

Control Interface

Functional Description

The control interface in the MAC is used to program the ZL70250 RF transceiver.

At the bit level the ZL70250 interface is a standard two-wire control interface with a maximum speed of 400kHz. The bit-level protocol is shown in "Bit-Level Protocol" below.

The ZL70250 control interface differs slightly from the standard two-wire protocol at the byte sequencing level due to the addition of some extra functionality as shown in "Byte Sequencing" on page 2-2.

Bit-Level Protocol

Figure 2-1 shows the basic bit protocol for a transfer on the two-wire bus. The first byte provides a seven-bit device ID and one bit for read/write indication. All byte transfers are nine bits, with the ninth bit being the acknowledge bit. At the bit level, the ZL70250 two-wire protocol is identical to a standard two-wire protocol.

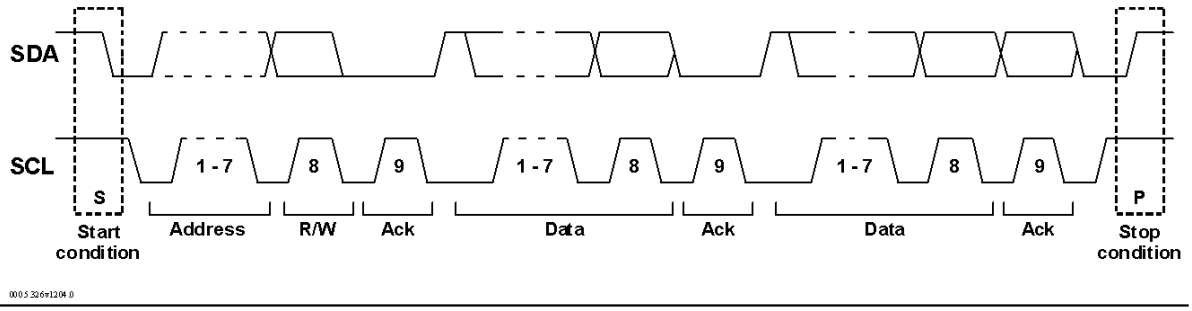


Figure 2-1 • **Bit-Level Protocol**

Byte Sequencing

The byte sequence required to control the ZL70250 is specific to the ZL70250, and is defined below. All byte definitions are shown with the MSB ([D7]) first.

Write operations are performed in one sequence of bytes (see Table 2-1). One or more bytes can be written in a write command: first (in byte 5) to the address that was specified in byte 4, then continuing to autoincrement to the next address for each of the remaining bytes.

Table 2-1 • **Write Command Sequence**

Bits	Description
Byte 1, bits [D7:D1]	Device ID for ZL70250 = 7'b1000101
Byte 1, bit [D0]	R/W bit; 0 = Write
Byte 2, bits [D7:D0]	Write command byte = 8'b00000010
Byte 3, bits [D7:D0]	Upper address bits [15:8] = 8'b00000000
Byte 4, bits [D7:D0]	Lower address bits [7:0] = Register address
Byte 5, bits [D7:D0]	First data byte to be written
Byte 5+N, bits [D7:D0]	Nth data byte to be written

Read operations are performed in two sequences of bytes. The first sequence is the read setup operation (see Table 2-2), which provides the first address to be read. The second sequence is the actual read operation (see Table 2-3). One or more bytes can be read in a read operation: first (in byte 2) from the address that was specified during the setup operation, then continuing to autoincrement to the next address for each of the remaining bytes.

Table 2-2 • **Read Setup Command Sequence**

Bits	Description
Byte 1, bits [D7:D1]	Device ID for ZL70250 = 7'b1000101
Byte 1, bit [D0]	R/W bit, 0 = Write
Byte 2, bits [D7:D0]	Read setup command byte = 8'b00000001
Byte 3, bits [D7:D0]	Upper address bits [15:8] = 8'b00000000
Byte 4, bits [D7:D0]	Lower address bits [7:0] = Register address

Table 2-3 • **Read Operation Sequence**

Bits	Description
Byte 1, bits [D7:D1]	Device ID for ZL70250 = 7'b1000101
Byte 1, bit [D0]	R/W bit, 1 = Read
Byte 2, bits [D7:D0]	First data byte read
Byte 2+N, bits [D7:D0]	Nth data byte read

Data Interface

Functional Description

The data interface in the MAC controls the transfer of data between the ZL70250 RF transceiver and the external microcontroller.

The data interface can be configured in either SPI or PCM mode. For PCM, both wide and narrow frame sync are supported. In PCM mode, the clock and frame sync can be any polarity. In both SPI and PCM modes, the ZL70250 is the master, and data is clocked in and out at the fixed bit rate of the RF interface.

The data interface supports five basic modes of operation:

- bidirectional transmit/receive multiple packets
- transmit one packet
- transmit multiple packets
- receive one packet
- receive multiple packets

In both SPI and PCM mode, SPI_DATA_OUT is not tristated. This implies that outgoing and incoming traffic needs to happen on separate lines.

Table 2-4 • **Data Interface, SPI Timing Specifications**

Parameter	Sym.	Conditions	Min.	Nom	Max.	Unit
Rise time (20% to 80%)	T_R	C_{LOAD} = 200 pF R_{PULLUP} = 8 kΩ			50	ns
Fall time (80% to 20%)	T_F	C_{LOAD} = 200 pF I_{LOAD} = 1 mA			50	ns
Clock period	T_{CP}	Receive mode	4.45	5.37	6.30	µs
Clock low	T_{CL}	Receive mode	2.63	2.68	2.73	µs
Clock high	T_{CH}	Receive mode	1.73	2.68	3.63	µs
RX data setup	T_{RSU}	Receive mode	1.50	2.68		µs
RX data hold	T_{RH}	Receive mode	−100			ns
RX data out	T_{RCO}	Receive mode			200	ns
TX data setup	T_{TSU}	Transmit mode	200			ns
TX data out	T_{TCO}	Transmit mode			1000	ns
TX data hold	T_{TH}	Transmit mode	−1000			ns

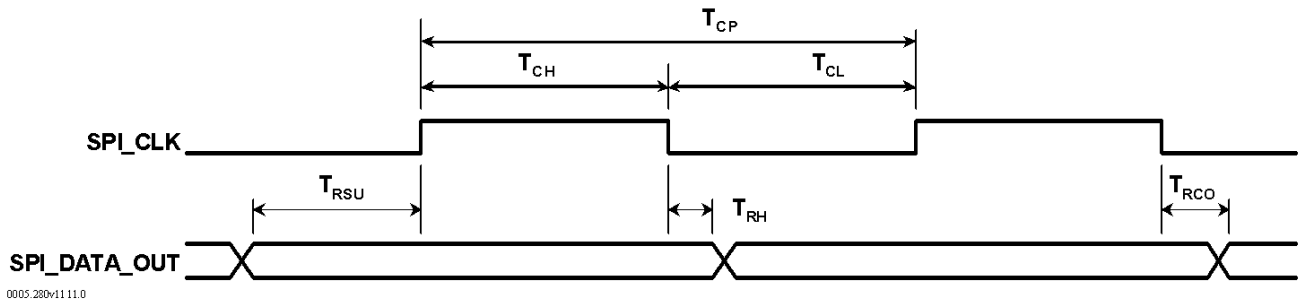


Figure 2-2 • **SPI Receive Timing, ZL70250 to External Microcontroller**

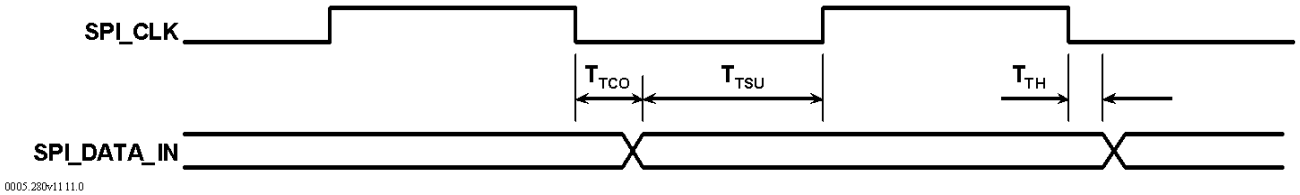
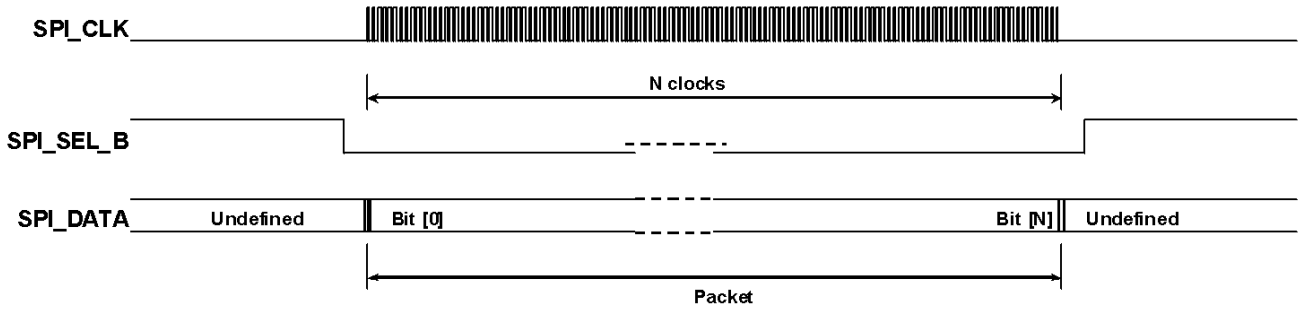


Figure 2-3 • **SPI Transmit Timing, External Microcontroller to ZL70250**

SPI Data Packet

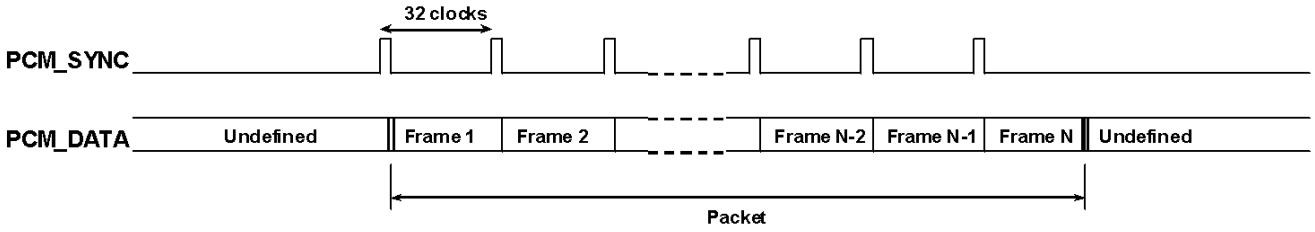


- A packet is composed of N contiguous bits, with no data before or after packet boundaries.
- For RX, the first bit of the packet arrives on the first SPI_CLK.
- For RX, the last bit of the packet arrives on the last SPI_CLK.
- For TX, the PCM interface buffer is preloaded transmit data.
- For TX, the first bit of the first packet is transmitted on the first SPI_CLK.
- For TX, the last bit of the packet is transmitted on the last SPI_CLK.
- Data bits before the first bit of the packet , and after the last bit of the packet , are undefined and should have no effect on the SPI interface buffer for either TX or RX.
- There are no frames in SPI mode.

0005.325v 1111.0

Figure 2-4 • **SPI Data Packet**

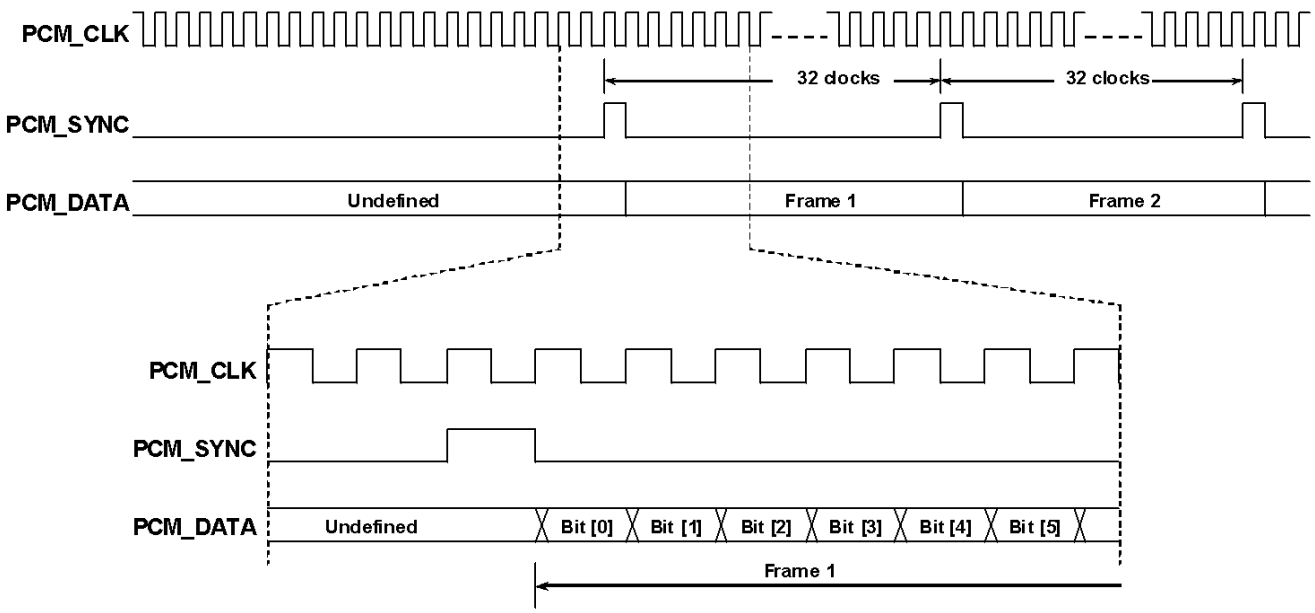
PCM Data Packet



- A packet is composed of N contiguous frames, with no data before or after packet boundaries.
- For RX, the first bit of the frame arrives during the bit-period following the PCM_SYNC.
- For RX, the last bit of the frame arrives 32 bit-periods after the last PCM_SYNC.
- For TX, the PCM interface buffer is preloaded with 8 x 32 bits.
- For TX, the first bit of the first frame is transmitted on the bit-period following the PCM_SYNC.
- For TX, the last bit of the frame is transmitted 32 bit-periods after the last PCM_SYNC.
- Data bits before the first bit of the frame, and after the last bit of the frame, are undefined and should have no effect on the PCM interface buffer for either TX or RX.

0005318rv1111.0

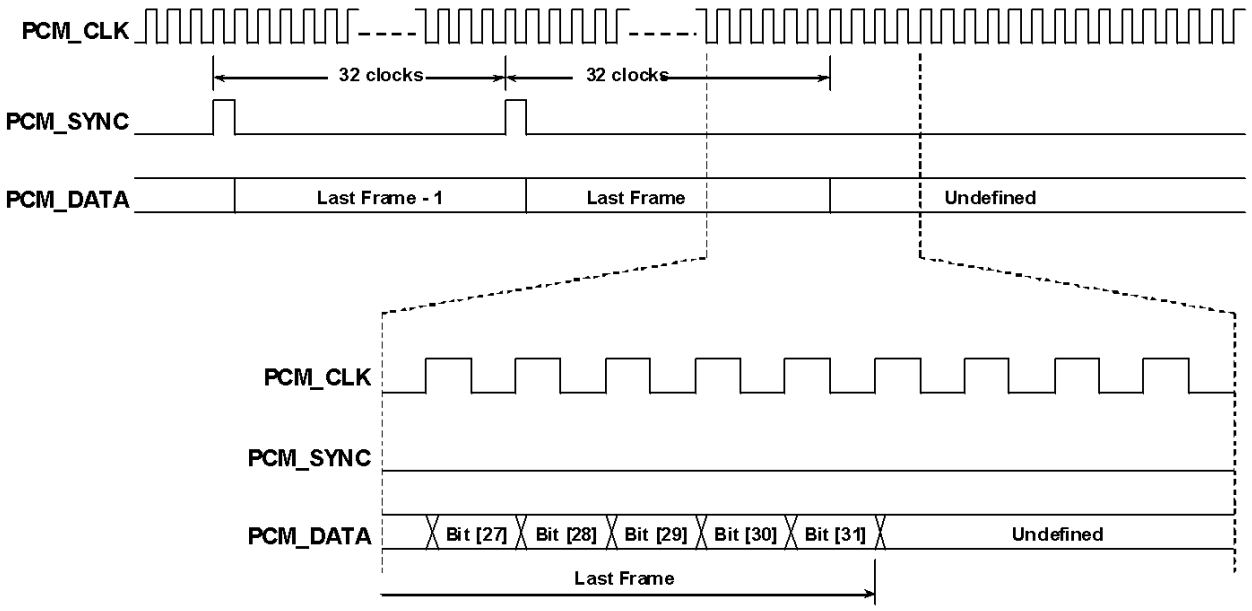
Figure 2-5 • **PCM Data Packet with 32-Bit Frame**



Note: Bit [0] is the first bit of the packet. No PCM_SYNC pulses occur prior to the pulse immediately preceding bit [0].

0005311rv1111.0

Figure 2-6 • **PCM Start of Packet**



Note: Bit [31] is the last bit of the packet. No PCM_SYNC pulses following the PCM_SYNC pulse prior to the last frame.

000531 6v111 1.0

Figure 2-7 • **PCM End of Packet**

3 – Electrical Specifications

Absolute Maximum Ratings

Table 3-1 • **Absolute Maximum Ratings**

Characteristics	Symbol	Minimum Rating	Maximum Rating	Unit	Notes
Supply voltage	VDD		1.98	V	Note 1
Reverse supply voltage			0.3	V	At least 20mA at −1.5V
Input voltage (digital and analog)	Vin	VSS − 0.3	VDD + 0.3	V	
RF I/O voltage	Vio	VSS − 0.3	2 × VDD	V	
Storage temperature	Tstg	−40	+85	°C	
Electrostatic discharge	ESD		RF pads: 500 All others: 1.5k	V	Note 2

Notes:

1. *A DC voltage above 1.98 will begin to degrade the life of the part.*
2. *Applied one at a time. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Human body model.*

Recommended Operating Conditions

Table 3-2 • **Recommended Operating Conditions**

Characteristics	Symbol	Min.	Max.	Unit	Notes
Supply voltage	VDD_op	1.1	1.9	V	
Operating temperature	Top	−10	70	°C	

Digital I/O DC Specifications

Table 3-3 • **Digital I/O DC Specifications**

Parameter	Sym.	Conditions	Min.	Nom	Max.	Unit
Output high	V_{OH}	DOUTB = VSS R_{PULLUP} = 8kΩ	VDD − 0.01			V
Output low	V_{OL}	DOUTB = VDD I_{LOAD} = 1mA			VSS + 0.1	
Input high	V_{IH}		(VDD − VSS) × 0.8			V
Input low	V_{IL}				(VDD − VSS) × 0.2	V

Dynamic Characteristics

The specified performance of the ZL70250 is valid over a supply range of 1.1 to 1.9V. The ZL70250 continues to operate such that it can receive and transmit at some range over a supply range of 1.0 to 1.9V. Additionally, all other functions operate correctly over the same supply voltage range. See Table 3-4.

Table 3-4 • **Dynamic Characteristics**

Parameter	Min.	Typ.	Max.	Units and Notes
Operating frequency range	795		965	MHz
Sleep state		0.5		µA All circuits disabled
Reference frequency		24.576		MHz See Note 1
Symbol rate		186.182		ksps (24.576MHz / 22 / 6)
Channel separation		303.407		kHz (24.576MHz / 81)
Power up		3	5	ms From RESET_B release, assuming VDD is settled
External clock output	0.8192		6.144	MHz (24.576MHz / N, where 4 ≤ N ≤ 30)
Receiver Parameters				
Sensitivity at 25°C		−90		dBm Input level resulting in BER of 10^{-3}; minimum depends on load conditions
1-dB compression point		4		mVrms Input at LNA/mixer gain of 30dB
Cascaded voltage gain		30		dB LNA and mixer; programmable, with five settings in 4-dB steps
Current consumption		1.9		mA Continuous RX mode
IF		606.814		kHz (303.407kHz × 2)
RSSI range		40		dB Digital, 32 levels of 2dB
Adjacent channel rejection		11		dB Desired channel 3dB above the sensitivity limit; 303.407-kHz channel spacing
Alternate channel rejection		25		dB Desired channel 3dB above the sensitivity limit; 606.814-kHz channel spacing

1. *In order to save power, the crystal oscillator has a 3-pF load instead of a typical 8-pF or 10-pF load.*
2. *The achievable output voltage swing depends on the supply voltage: Vswing = ±Min[VDD-0.4, 1.5]. For VDD = 1.8V, the single-ended voltage swing can be up to ±1.4V centered around VDD. For VDD = 1.2V, it is reduced to ±0.8V.*
3. *The PA has been optimized for a 1-kΩ load. However, for efficiency, the higher the load impedance the better.*
4. *Test performed was with specified load of 50Ω with the transmitter operating. See section 8.8.2 of ETSI EN 300 220.*

Table 3-4 • **Dynamic Characteristics (continued)**

Parameter	Min.	Typ.	Max.	Units and Notes
Transmitter Parameters				
Current consumption		2.0		mA Continuous TX mode; with PA trim code of 8'h08, 1 kΩ load
Maximum output power		−2		dBm, 1 kΩ load
Output voltage range of PA	0.4		2 × VDD	V Each single-ended output; DC bias to VDD required (see Note 2)
Output current range of PA	100	320	1500	µArms Nominal 100-µA steps
Matching impedance	500	1000	2000	ohms See Note 3
Spurious emissions		−68	−36	dBm See Note 4 862 MHz to 1 GHz (Maximum figure is the limit per ETSI EN 300 220 section 8.8.5)
		−33	−30	dBm See Note 4 Above 1 GHz (Maximum figure is the limit per ETSI EN 300 220 section 8.8.5)
Modulation index	0.45	0.5	0.55	(±10%) A transmitted 1 is a shift to a higher frequency, 0 a shift to a lower
TX-RX or RX-TX turnaround time		1.8		ms Programmable

1. *In order to save power, the crystal oscillator has a 3-pF load instead of a typical 8-pF or 10-pF load.*
2. *The achievable output voltage swing depends on the supply voltage: Vswing = ±Min[VDD-0.4, 1.5]. For VDD = 1.8 V, the single-ended voltage swing can be up to ±1.4 V centered around VDD. For VDD = 1.2 V, it is reduced to ±0.8 V.*
3. *The PA has been optimized for a 1-kΩ load. However, for efficiency, the higher the load impedance the better.*
4. *Test performed was with specified load of 50 Ω with the transmitter operating. See section 8.8.2 of ETSI EN 300 220.*

Programmable Transmit Power Characteristics

Measurement results for characterizing the transmitter power were taken from a typical device, at room temperature and VDD = 1.8V. Measurements were made using the ZL70250 Application Development Kit (ADK) at the 50-Ω SMA connector (after matching network); refer to Figure 5-1 on page 5-1. IC transmit power results were extrapolated assuming a 3-dB loss in the matching network.

Transmit Power vs. PA trim Value

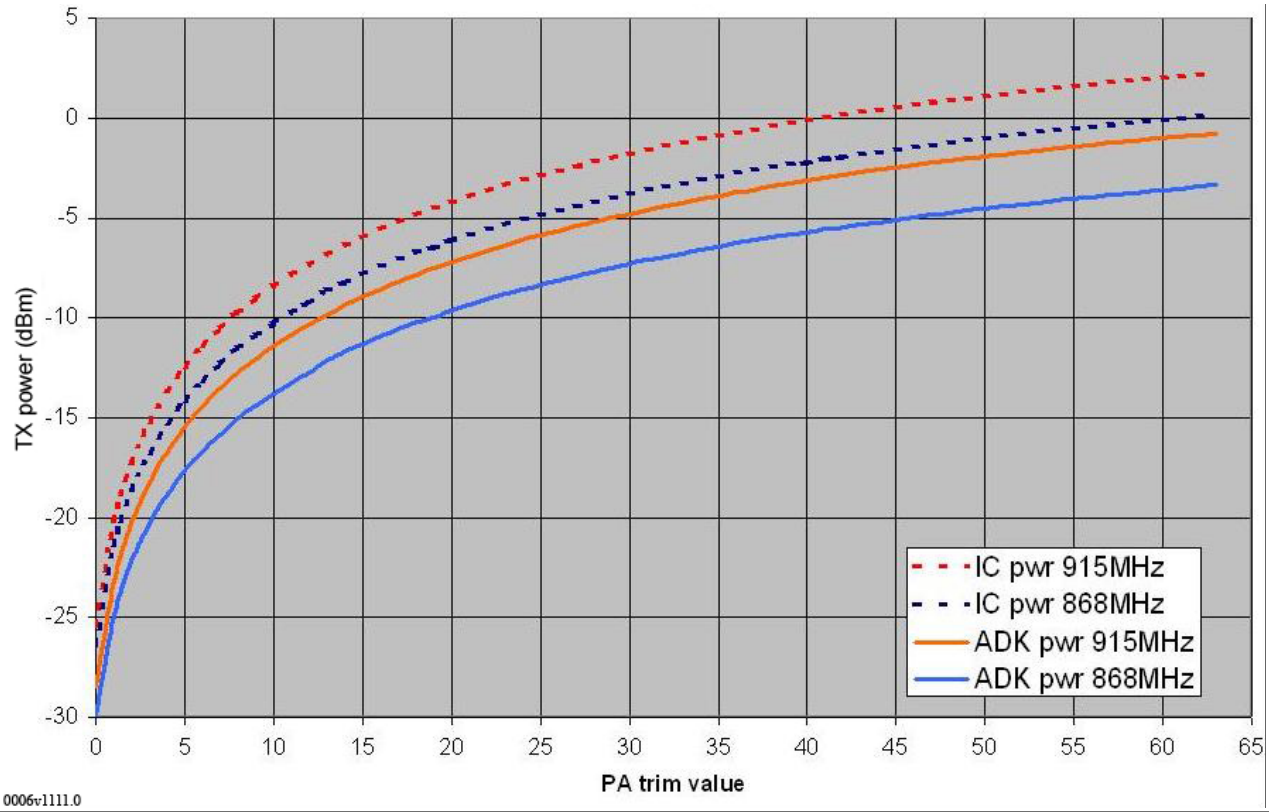


Figure 3-1 • **TX Power vs. PA Trim Value**

Current Consumption vs. Transmit Power

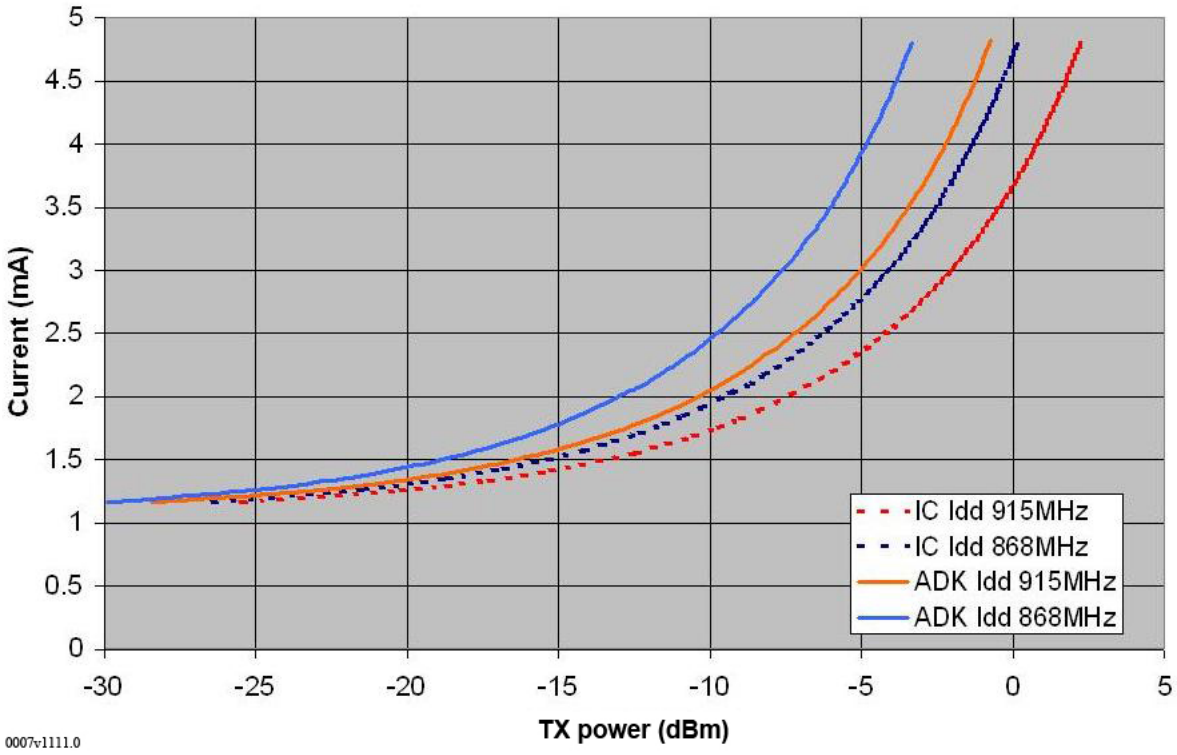


Figure 3-2 • **Current Consumption vs. TX Power**

Crystal Specifications

All frequency-related specifications are based on the crystal oscillator performance, which, in turn, is dependent on the crystal specifications. The ZL70250 specifications assume that the crystal specifications listed in Table 3-5 are met or exceeded.

Table 3-5 • **Crystal Specifications**

Parameter	Min.	Typ.	Max.	Units and Notes
Frequency		24.576		MHz
Frequency tolerance			±25	ppm
Stability with temperature			±20	ppm (over operating temp)
Operating temperature range	−10		70	°C
Equivalent series resistance	50	63	110	ohms
Shunt capacitance		2		pF (Note 1)
Motional capacitance		1.5		fF (Note 1)
Load capacitance		3		pF (Note 2)
Drive level			50	µW

1. *A low shunt capacitance and high motional capacitance is best as it result in a larger trim range. It is particularly important when external capacitors are used, as those reduce the trim range.*
2. *In order to save power, the crystal oscillator presents a 3-pF load instead of the typical 8-pF or 10-pF load. A slight frequency pull, on the order of 100 to 150ppm, would result if using a standard crystal without additional external load capacitors. Such a deviation has no effect on the operation of the device and is generally not a problem for most applications, providing all ZL70250s have the same frequency pull (within trimmable range). If the deviation is not acceptable and power is critical, a special cut crystal would need to be ordered (that is, slightly slower to compensate for the pull). Alternatively, if power is not as critical, external capacitors can be added, as shown in Figure 3-3 below, to bring the total load capacitance to the crystal load specification. For instance, for a crystal with an 8-pF load specification (CL), CLext = 8pF − 3pF = 5pF, so two 10-pF capacitors need to be added, one on each end of the crystal. It must be noted, however, that this results in a reduced trim range. The frequency tolerance should therefore be tighter to compensate.*

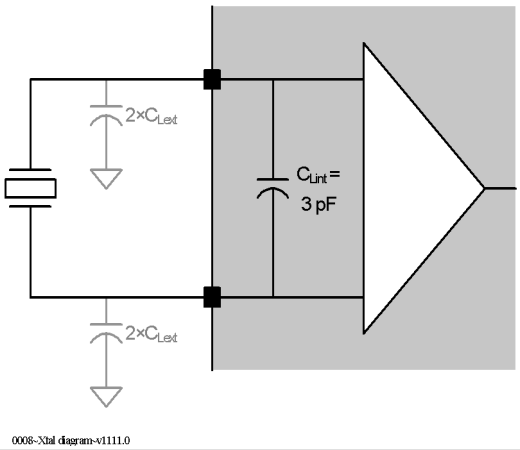


Figure 3-3 • **Crystal Oscillator with Additional External Load Capacitors**

4 – Mechanical Specifications

36-Pin Chip Scale Package (CSP)

Pinout

Table 4-1 • **CSP Pinout**

CSP Pin #	Pin Name	I/O	A/D	Function	Connection
A1	XTAL1	I	A	Crystal connection or external clock input when CLKSEL is high	Connect to crystal.
A2	XTAL2	I	A	Crystal connection, leave open when using external clock source	Connect to crystal.
A3	RESET_B	I	D	Reset when low, all circuits off (including the CLK_OUT, so do not use CLK_OUT for microprocessor and then control the RESET_B with the microprocessor). When the chip comes out of reset, the programmable registers are at default conditions— crystal oscillator and CLK_OUT on, everything else off.	Connect to microprocessor or other reset network. Internal 1-MΩ pull-down when driven high, 100-kΩ pull-down when low.
A4	CLK_OUT	O	D	Programmable clock output for normal operation is crystal frequency/N, where 4≤N≤30	Can be used to clock microprocessor (minimize load capacitance) or leave open and disable through SSI port.
A5	NC			Reserved: do not use; do not connect	
B1	VDDTEST	PWR	A	Supply voltage for test buffers	Supply, connect to VDDA.
B2	NC			Reserved: do not use; do not connect	
B3	TXRX_STAT	O	D	Transmit/receive mode indicator for controlling a TX-RX switch during normal operation	Connect to TX-RX switch or leave open.
B4	SCL	I	D	Serial clock (similar to two-wire); ZL70250 is slave	External pull-up resistor required, value depends on load capacitance.
B5	SDA	I/O	D	Data input or open drain output for serial port data (similar to two-wire); ZL70250 is slave	External pull-up resistor required, value depends on load capacitance.
C1	AMX2	O	A	Analog test bus output	Leave open for normal operation.
C2	AMX3	O	A	Analog test bus output	Leave open for normal operation.

Table 4-1 • **CSP Pinout (continued)**

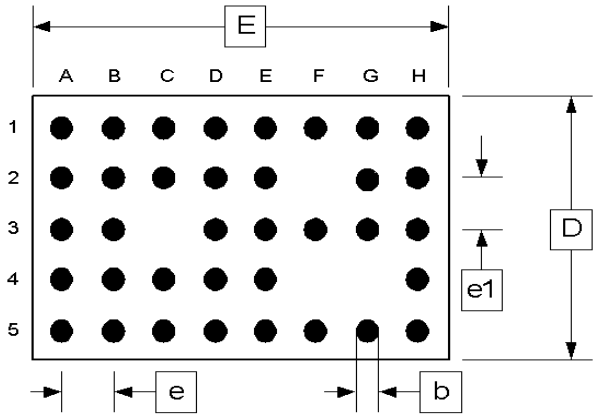
CSP Pin #	Pin Name	I/O	A/D	Function	Connection
C4	SPI_CLK	O	D	SPI master clock. Can be configured for PCM clock. See programmer's manual.	Connects to SPI or PCM interface.
C5	SPI_DATA_IN	I	D	SPI data input. Can be configured for PCM data input. See programmer's manual.	Connects to SPI or PCM interface.
D1	AMX0	I	A	Analog test bus input	Leave open for normal operation.
D2	AMX1	I	A	Analog test bus input	Leave open for normal operation.
D3	TXRX_CMD	I	D	Transmit/receive control (see programmer's manual)	Output from microprocessor.
D4	SPI_DATA_OUT	O	D	SPI data output. Can be configured for PCM data output (see programmer's manual)	Connects to SPI or PCM interface.
D5	SPI_SEL_B	O	D	SPI frame output. Can be configured for PCM frame output (see programmer's manual)	Connects to SPI or PCM interface.
E1	VDDA	PWR	A	Analog supply voltage	Supply, 1.2V to 1.9V.
E2	RBIAS	I	A	Bias resistor used in trim	Connect external 50 kΩ to ground.
E3	DOUT0	O	D	Digital test output	Leave open or connect to test point.
E4	VDDD	PWR	A	Digital supply voltage	Supply, 1.2V to 1.9V.
E5	IRQ	O	D	Interrupt to microprocessor	
F1	VSSA	PWR	A	Analog ground	Ground.
F3	NC			Reserved: do not use; do not connect	
F5	VSSD	PWR	A	Ground for digital section	Ground.
G1	VSSH	PWR	A	Ground for power amplifier	Ground.
G2	TX−	O	A	RF transmitter PA minus output	
G3	VSSA2	PWR	A	Analog ground	Ground.
G5	DOUT1	O	D	Digital test output	Leave open or connect to test point.

Table 4-1 • **CSP Pinout (continued)**

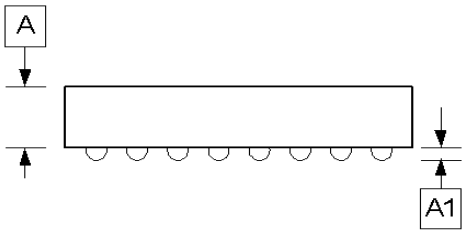
CSP Pin #	Pin Name	I/O	A/D	Function	Connection
H1	RX−	I	A	RF receiver amplifier minus input (differential high impedance, internal AC coupled); internally connected to antenna tuning capacitor bank	
H2	RX+	I	A	RF receiver amplifier plus input (differential high impedance, internal AC coupled); internally connected to antenna tuning capacitor bank	
H3	TX+	O	A	RF transmitter PA plus output	
H4	NC			Reserved: do not use; do not connect	
H5	CLKSEL	I	D	Selects crystal oscillator when low and external clock signal when high (bypasses internal oscillator)	Internal 1-MΩ pull-down when driven high, 100-kΩ pull-down when low, leave open or tie to ground for normal operation.

Note: **Regarding pull-downs:** Most of the digital input pads have built-in pull-down resistors so that, if the pin is not used for normal operation, then no connection to the pin is required, thus reducing the traces on small hybrid assemblies. If the input is used, then the pull-down resistor value is switched depending on the input state. If the pin is driven high, the resistor is switched to 1 MΩ to reduce the amount of pull-down current. If the input is driven low or left unconnected, the pull-down resistor value is 100 kΩ.

Package Mechanical Specifications



BOTTOM VIEW



SIDE VIEW

Note: Pin F3 is a dummy pin. No pad should be placed on substrate to accommodate this pin.

0016v1204.0

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	0.292		
A1	0.085	0.100	0.115	
b	-	0.115	-	
D	-	1.898	-	
E	-	3.125	-	
e		0.387 BSC		
e1		0.371 BSC		
N		36		

Figure 4-1 • **ZL70250 CSP Bottom View**

5 – Typical Application Example

Figure 5-1 is representative of a 50-Ω single-ended implementation. The matching network might be different, or even unnecessary, for other types of antennas. In addition, the matching component values assume a particular FR4 substrate. Those values might be different with another substrate type or with FR4 with different characteristics.

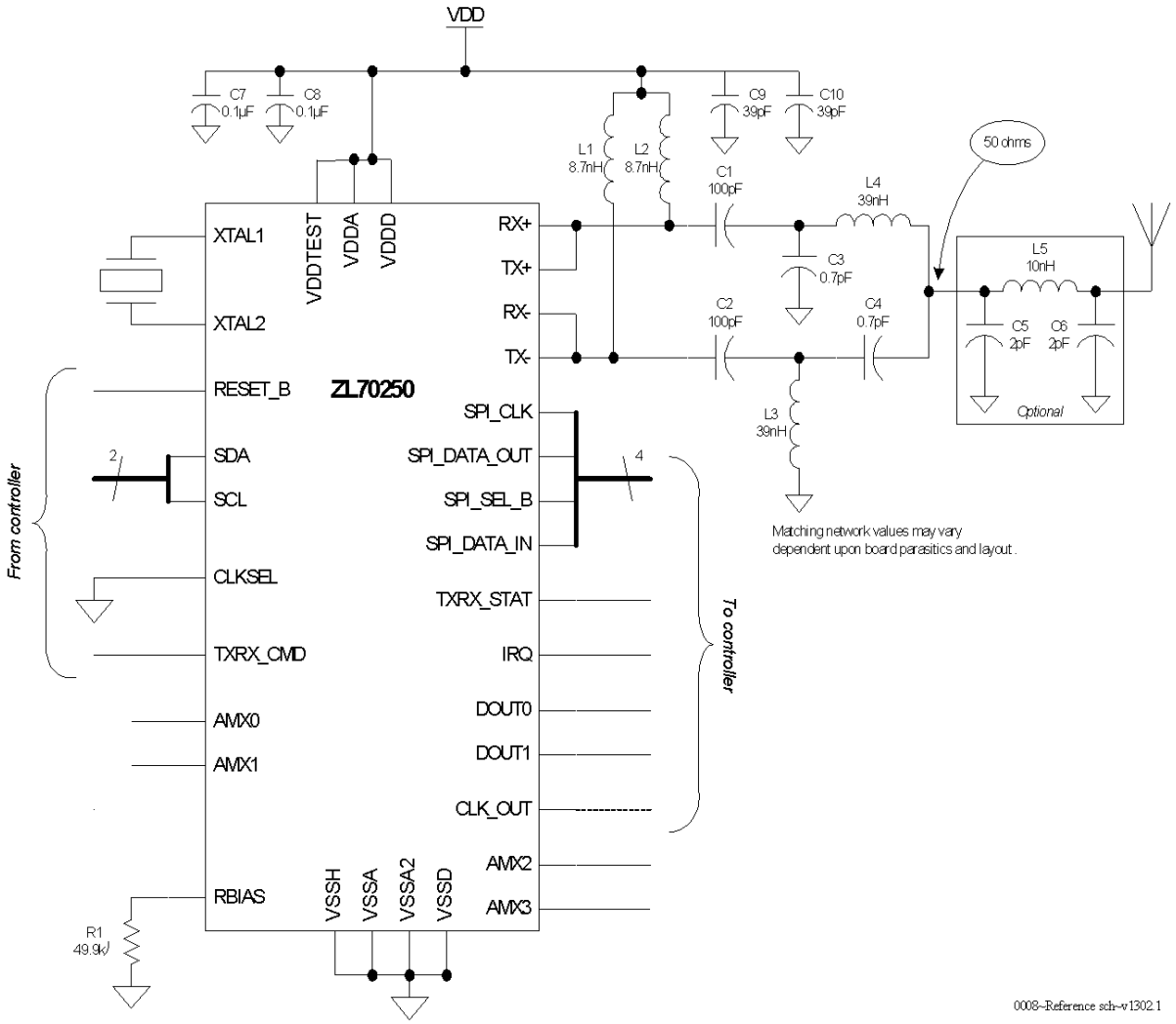


Figure 5-1 • **50-Ω Single-Ended Implementation Schematic**

6 – Glossary

Term	Explanation
A	Analog
A/D	Analog/digital
AC	Alternating current
ACK	Acknowledgement
ADC	Analog-to-digital converter
addr	Address
ADK	Application development kit
AGC	Automatic gain control
ANT	Antenna
BER	Bit error ratio
CCA	Clear channel assessment
Clk	Clock
cmd	Command
CODEC	Coder/decoder
CSP	Chip Scale Package
Ctrl	Control
D	Digital
DAC	Digital-to-analog converter
DC	Direct current
EEPROM	Electrically erasable and programmable read-only memory
EMC	Electromagnetic compatibility
EN	European Standard (French: Norme)
ESD	Electrostatic discharge
ETS	European Telecommunications Standard
ETSI	European Telecommunications Standards Institute
Ext	External
FCC	Federal Communications Commission (US)
FM	Frequency modulation
FR4	Flame retardant 4 (printed circuit board)
Freq	Frequency
Gen	Generator
GMFK	Gaussian frequency shift keying
GPIO	General-purpose input/output

Term	Explanation
I	Current; Input
I/O	Input/output
IC	Integrated circuit
ID	Identification
IF	Intermediate frequency
ISM	Industrial, Scientific, and Medical
ksps	Thousand (or kilo) symbols per second
LO	Local oscillator
LNA	Low-noise amplifier
LP	Low pass
MAC	Media access controller
Max	Maximum
MSB	Most significant bit
Min	Minimum
mux	Multiplexer
OSC	Oscillator
NC	No connect
Nom	Nominal
P	Stop
PA	Power amplifier
PCM	Pulse code modulation
PLL	Phase-locked loop
ppm	Parts per million
pwr	Power
R/W	Read/write
ref	Reference
RF	Radio frequency
rms	Root mean square
RSSI	Received signal strength indicator
RX	Receive
S	Start
SMA	Subminiature A
SPI	Serial peripheral interface
SRD	Short-range device
SSI	Synchronous serial interface
Sym	Symbol

Term	Explanation
sync	Synchronization
synth	Synthesizer
T&R	Tape and reel
TX	Transmit
Typ	Typical
US	United States
USB	Universal serial bus
V	Voltage; Volt(s)
VCO	Voltage-controlled oscillator
VDD	Supply voltage
VDDA	Supply voltage, analog
VDDD	Supply voltage, digital
vs	Versus
VSS	Ground
Wr	Write
XTAL	Crystal

7 – Datasheet Information

List of Changes

The following table lists substantive changes that were made in the ZL70250 Ultra-Low-Power Sub-GHz RF Transceiver datasheet.

Revision	Changes	Page
Revision 4 (February 2013)	In "Features"list added bullet for RoHS compliance.	I
	In "Ordering Information" specified SAC405.	I
	In Table 4-1, changed comment in Connection column for VDDTEST.	4-1
	Modified Figure 5-1 to: (1) show VDDTEST connected to VDDA. (2) show AMX0..3 left open. (3) change capacitance for C3 and C4 to 0.7pF. (4) adjust brackets to and from controller such that they exclude AMX0..3 (5) add note regarding matching network values (located below L3 inductor).	5-1
	Changed datasheet category from Preliminary to Production.	All
Preliminary Revision 3 (August 2012)	Removed -ENG suffix from part numbers in "Ordering Information".	I
	In Table 3-1, corrected supply voltage and RF I/O voltage, and added a relevant footnote to the table.	3-1
	In Table 3-3, removed input current row.	3-1
	Corrected recommended supply range in paragraph introducing table.	3-2
	In Table 3-4: (1) replaced standby current row with sleep state, including changes to specs and note. (2) clarified temperature for sensitivity parameter, and moved value to "Typ" column. (3) changed note for current consumption row. (4) corrected output voltage range of PA. (5) replaced output power row with maximum output power, including changes to specs and note.	3-2
	In Table 3-5, corrected operating temperature range.	3-6
	Replaced Figure 5-1.	5-1
	Changed terminology to be consistent with other documents: (1) changed "standby" to "sleep" state in tables and text. (2) changed WCLK to CLK_OUT in Figure 1 and in text.	I, 1-1, 3-2, 4-1, 5-1
	Corrected link range.	1-1
Advance Revision 2 (April 2012)	Changed part number in "Ordering Information" from -ENG1 suffix to -ENG2 suffix, plus related changes to specifications throughout document (e.g., removed all references to 24.000-MHz crystal, and changed the recommended operating voltage to 1.1 to 1.9V).	I, various
	Name change from Zarlink to Microsemi. Included changing document format and chapter structure. Spelling and grammar were also corrected throughout the document.	All

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in an advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi CMPG Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the CMPG Products Group’s products is available from Microsemi upon request. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

ZL70250CSP-DS/142423-4/02.13