BLAZAR BE3-RMW Accelerator Engine
Intelligent In-Memory Computing
1Gb Memory

PRODUCT BRIEF

Acceleration Engines give Software and Hardware System Architects Acceleration Options not previously available

BANDWIDTH ENGINE (BE) INTRODUCTION

The **BLAZAR Family of Accelerator Engines** support high bandwidth, fast random memory access rates and *embedded **I**n-**M**emory **F**unctions (**IMF**)* that solve critical memory access challenges for memory bottlenecked applications like network search, statistics, buffering, security, firewall, 8k video, anomaly detect, genomics, ML random forest of trees, graph/tree/list walking, traffic monitoring.

The ***Bandwidth Engine 3 RMW (BE3-RMW)*** combines the high speed serial memory with the

- ***In-memory BURST functions***
- ***In-memory RMW functions***
    - RMW functions are a family of functions that modify memory locations utilizing an ALU on the device to perform Read/Modify/Write operations.
- The BE3 BURST and RMW functions include all the BE2 functions plus many more.

System benefits

- **FPGA Acceleration for Xilinx and Intel**
- **QDR comparison**
    - ***Replaces up to 8 QDR/RLDRAM memory devices***
    - ***Equal to or outperforms QDR memories***
    - ***Equivalent system latency***
- Memory architecture allows 32 simultaneous accesses
- ***Accelerates FPGA application by providing fast, efficient, single function for***
    - ***Burst for Data Movement***
    - ***RMW for Compute and Decision***
    - ***Over 50 Burst and RMW Functions.***
- The devices support application acceleration for aggregate throughput rates up to 380 Gb/s (190 Gb/s full duplex)

KEY FEATURES / PRODUCT OPTIONS

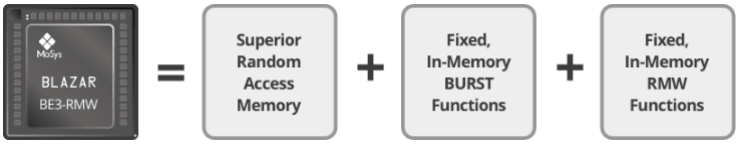
- High Bandwidth, low pin count serial interface
    - Highly efficient reliable transport command and data protocol optimized for 90% efficiency
    - Eases board layout and signal integrity, minimal trace length matching required, operates over connectors
- 1 Gb SRAM (16M x 72b)
    - User defined WORD length
    - Typical 8x, 16x, 32x, 36x, … 72x
- High access rate SRAM class memory
    - Up to 6.5 Billion transactions/sec
    - 3.2 ns tRC
- **In-Memory Bandwidth Functions**
    - **BURST** sequential read and write functions for Data Movement
    - Burst length: 1, 2, 4, 8 words
    - Can double or triple QDR bandwidth
    - Reduction of I/O pins up to 7X
- **In-Memory Compute and Decision Functions**
    - **RMW** for Applications of Compute and Decision focused on *Read/Modify/Write* operations for *Data Modification* that execute by issuing a single command, saving the typical 3 operations normally required
- Highest Single Chip Bandwidth – up to 380 Gb/s throughput

APPLICATIONS FOCUS

- High bandwidth data access application where low latency and Movement of Data is a critical requirement.
- Applications needed large SRAMs.
- FPGA Acceleration for Xilinx and Intel

MoSys ACCELERATOR ENGINE Elements of BE3-RMW

MoSys Engines have a Unique Memory Architecture that can replace SyncRAM/RLDRAM memories and Embeds In Memory Functions (IMF) that execute many times faster. A single function replaces many traditional memory accesses.



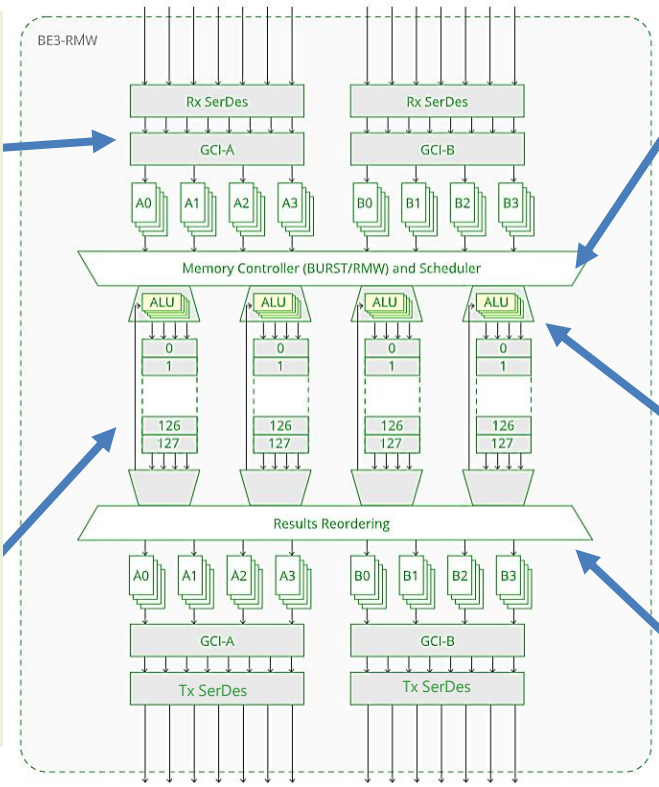
MoSys Bandwidth Engine RMW (BE3) Architecture

High speed serial I/O

- GCI serial I/O versions of 12.5, 15, 25 Gbps for high bandwidth (up to 640 Gbps)
- Device can operate with a minimum of 4 lanes.
- Has two, full duplex 8 lane ports that operate independently
- Reduces number of signal pins over traditional memories, increases signal integrity allowing longer board traces to ease board signal routing
- Operates across connectors

Main Memory

- 1Gb
  - 4 partitions/128 banks
  - 16 READ & 16 WRITE ports
- 2.7 ns tRC
- Allows parallel partition & Bank execution
- Up to 6.5 B access per sec



Memory/Function Controller

- Resolves localized bank conflicts
- operation by long latency operations
- Directs read/write function to selected bank of memory
- Manages all Burst functions
- Manages the sequence of operations to execute a RMW
  - 4-8x reduction in RMW accesses
  - Insures no stale data (mutec)
- Controls parallel function execution
- Four Domain levels for function execution priority setting
- Multiple scheduling domains minimize blocking short latency

ALU

- Embedded RMW Functions utilize ALUs for in memory computational functions
  - There are 16 ALUs
  - Simultaneous operations

Result Reordering

- Reorder buffers ensure that results are returned to the output of the submitted input port and tagged with priority Domain if used

Optional Use Advanced Acceleration Functions … In-Memory Functions – BURST and RMW

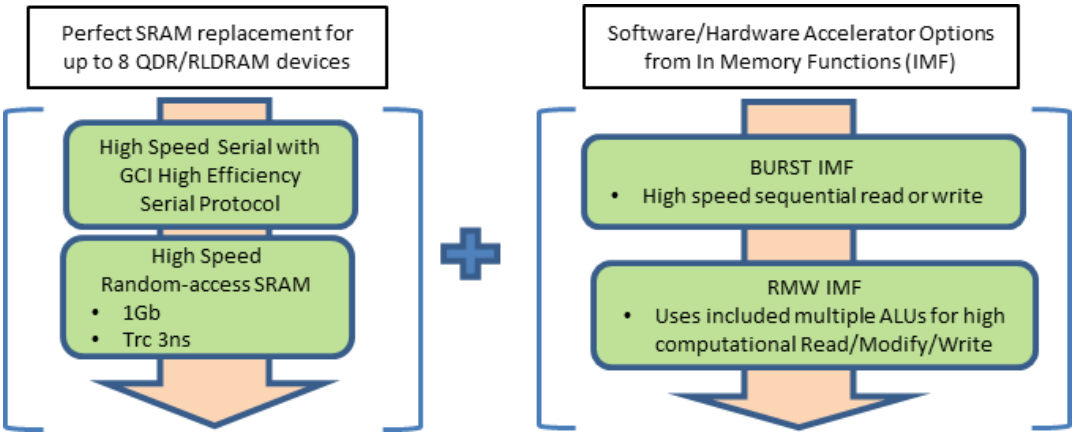
MoSys Engines Unique Memory Architectures that replace SyncSRAM/QDR/RLDRAM memories and embeds optional use In-Memory Functions (IMF) that replace traditional memory accesses with functions that execute faster, and some combine multiple traditional operations.

BURST In-Memory Functions

- Focused on DATA MOVEMENT to accelerate getting data in and out of the memory faster and more efficiently by reducing the number of command cycles.

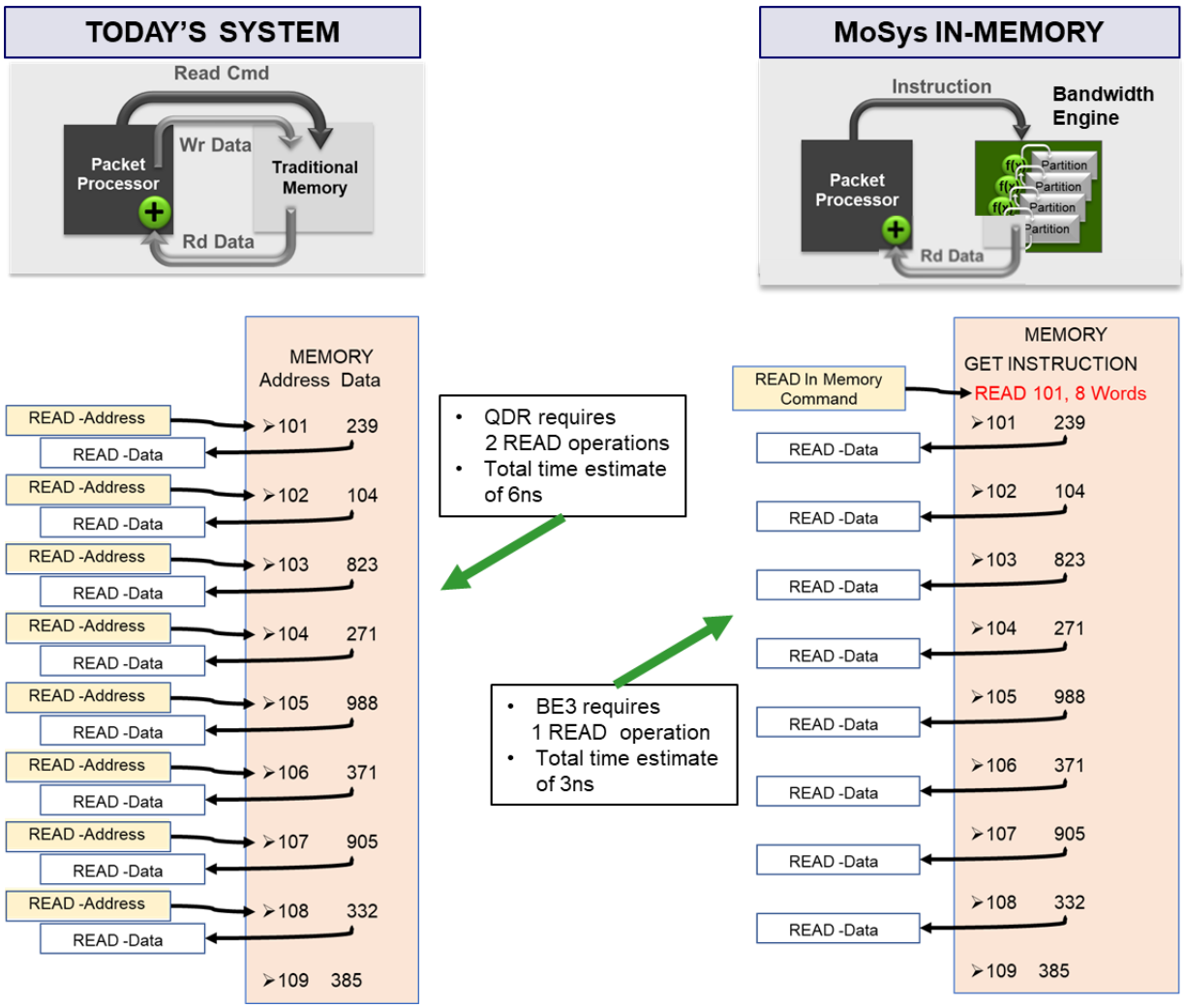
RMW (Read/Modify/Write) In-Memory Functions

- Focused on DATA COMPUTING AND DECISION where there is need for memory location modification involving RMW in applications such as metering, as well a single or dual counter update for statistics.



2309 Bering Drive, San Jose, CA 95131
Tel: 408-418-7500 Fax: 408-418-7501
www.mosys.com

In-Memory BURST Function - 8 Word READ Example



Example In-Memory BURST time saving comparing 1 QDR to 1 BE2

QDR…36b word width SINGLE READ

- Reads 144b/read
- **4 words of 36b**
- **Estimate of 3ns**

BE3...36b word width SINGLE READ

- BE has to 8 lane ports (A & B)
- Port A can READS 288b/read
  - **8 words of 36b**
- Port B can READS 288b/read
  - **8 words of 36b**

RESULT

- Total SINGLE READ "using" both A & B together
- **16 words of 36b**
- **Estimate of 3ns**
- **4 times a QDR Bandwidth**

MoSys In-Memory Functions

- BURST
  - Multiple Sequential READS
  - Multiple Sequential WRITES
  - Function types ~12

Save significant system time with higher bandwidth

2309 Bering Drive, San Jose, CA 95131
Tel: 408-418-7500 Fax: 408-418-7501
www.mosys.com

In-Memory RMW (Read/Modify/Write) Function Example

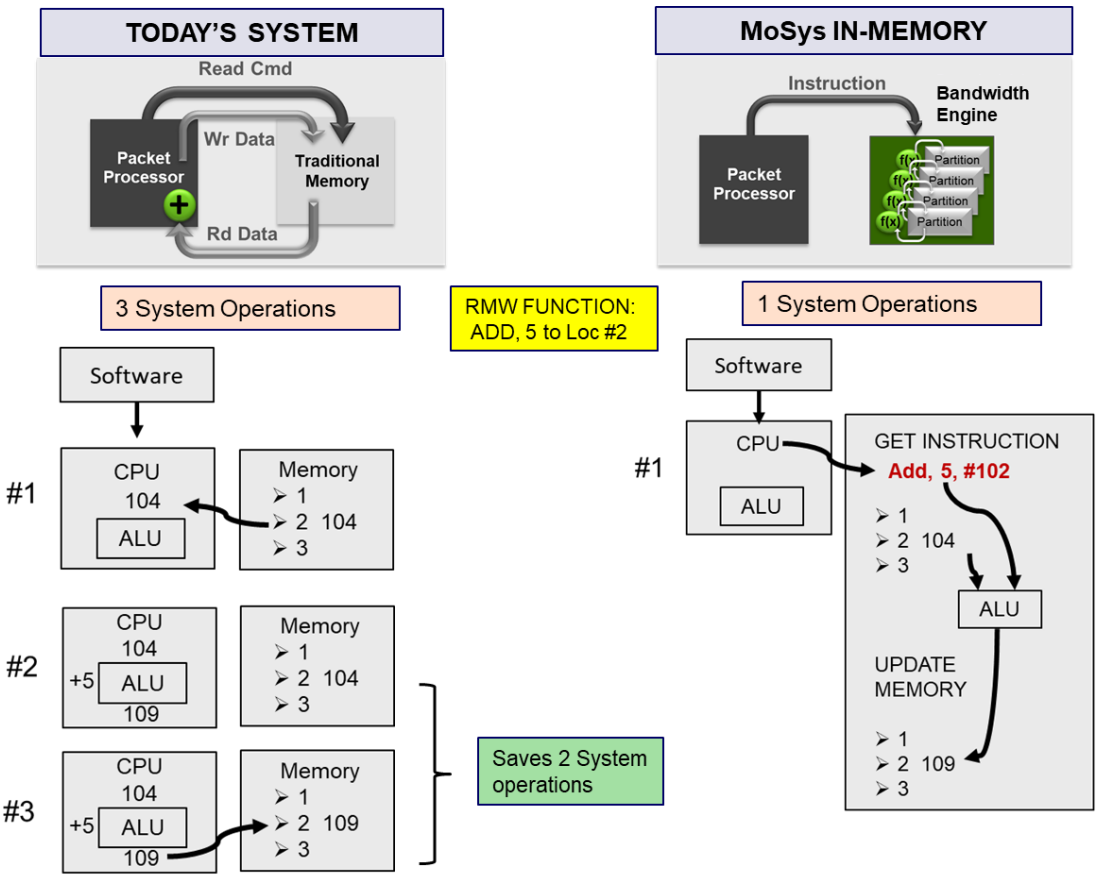
- Focused on DATA COMPUTING AND DECISION where there is need for memory location modification involving RMW in applications such as metering, as well a single or dual counter update for statistics.
- There are over 27 operations available such as add, subtract, compare, increment, etc.

The RMW function is done in one command, where traditional memory require 3 commands

- A location modification requires first, one command to READ a memory location, a second command to MODIFY the value, and a third command to WRITE the new value back to the memory location.

The RMW Functions provide at least two levels of speed acceleration.

- First, the RMW functions can be executed with a single command.
- Second, since the modification is executed within memory, there is no need to move the data out to be modified, and then back into memory to write. This removes all of the associated I/O latency.



Example In-Memory RMW time saving comparing 1 QDR to 1 BE

Add a number to a location

- Traditional Memory System
  - 3 operations Time Analysis
    - Read Cycle … 3ns
    - RTL/CPU "ADD" time ?
    - Write Cycle … 3 ns
  - **Calculation = 3ns + ADD + 3ns**
  - **Total Time = 6ns + ADD**
- MoSys In Memory Function
  - 1 operations Time Analysis
    - Command to BE Memory…3ns
  - **Total Time = 3ns**

MoSys In-Memory Functions

- RMW (Read-Modify-Writes)
  - ADD, SUB, INC, Compare, etc.
  - Functions ~17

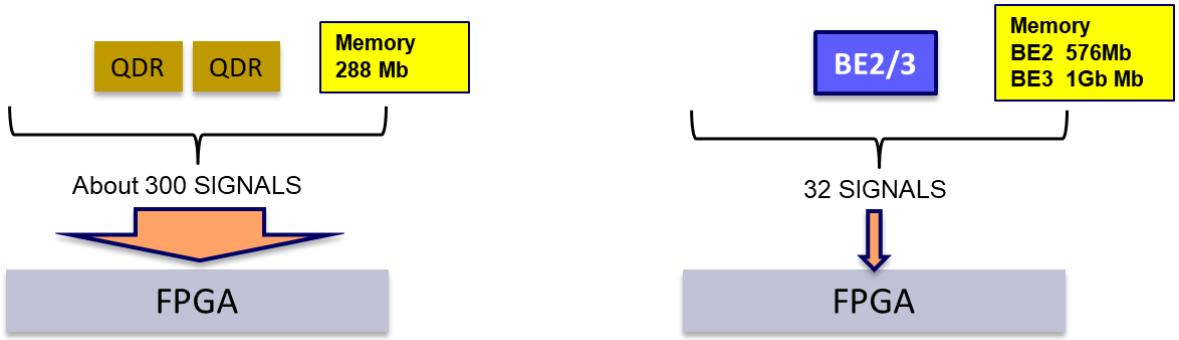
Save significant system time by eliminating many system operations freeing up the FPGA to do other operations

2309 Bering Drive, San Jose, CA 95131
Tel: 408-418-7500 Fax: 408-418-7501
www.mosys.com

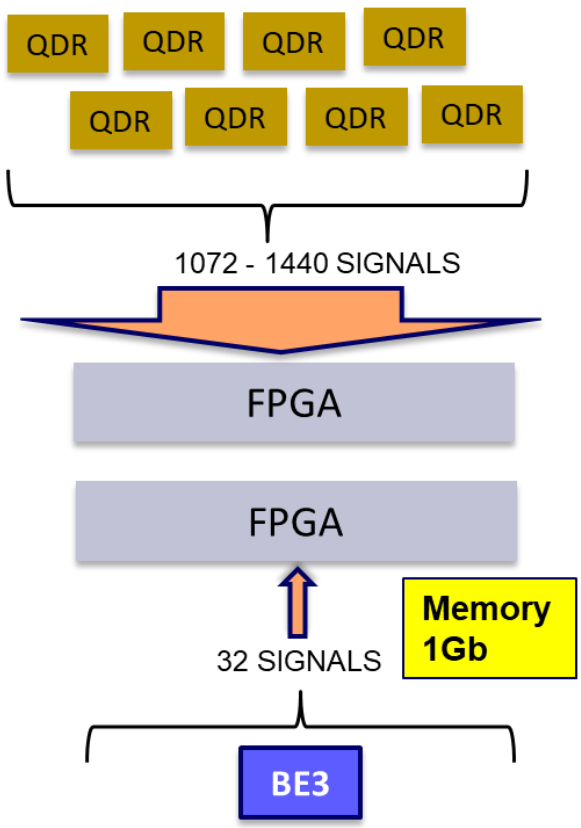
Benefits of Serial Memory vs QDR

Serial memories bring many advantage over traditional parallel signal memory device like QDRs.

Allows high bandwidth over a few pins



This is a typical 2 QDR design compared with a BE2 and BE3



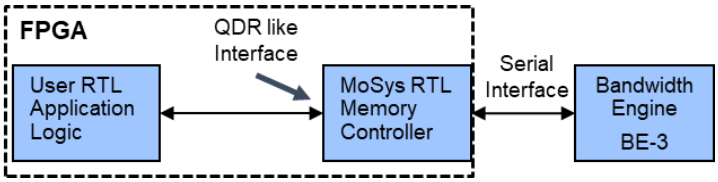
More High Speed memory generally allows acceleration options for software and hardware architects/Designers

Overview comparison of BE3 to QDR

- Memory size
  - BE3 with 1Gb equivalent to 8 QDR at 144Mb per device
- Device PCB board Space Saving
  - 1 BE3 device vs 8 QDR devices
- Signal Pins Reductions
  - 8 QDR…1Gb requires 1072-1440 pins/signals)
  - 1 BE3 …1Gb…BE3 requires 4 to 32 signal/pins
  - All BE devices have *Auto-Adaptation which handles on-board signal tuning*, eliminating the need for any external components to insure a clean, reliable signals
- Costs
  - One BE-3 is approx. the price of 3 QDR memories with 8x the memory of single QDR
- Benefits
  - Larger Buffers, High Bandwidth
  - Allows Realtime operations and analysis at Line rate
  - Eliminates need for complex parallel operations using RLDRAM, HBM, or slow DRAM

2309 Bering Drive, San Jose, CA 95131
Tel: 408-418-7500 Fax: 408-418-7501
www.mosys.com

Simplifying the User Interface to BE with MoSys RTL Controller



MoSys suppled RTL Controller simplifies the user interface with the BE.

MoSys can supply the FPGA RTL Memory Controller interfaces with the MoSys Bandwidth Engine. This controller is between the User Application logic and the BE device. It handles all the logic for the Serial GigaChip Interface (GCI) between the FPGA and BE as well as all memory addressing and commands and looks to the user like a QDR interface.

MEMORY CONTROLLER

- Converts the Bandwidth Engine serial protocol to a FPGA parallel QDR like interface to the user and is provided at NO COST TO THE USER.
- Signal interface to the user from the MoSys RTL Controller is a simple SRAM memory read/write operation.
- *Supports all of the In-Memory BURST and RMW commands to achieve higher performance than a QDR*

GRANULARITY OF MEMORY WORD WIDTH

Memory WORD width

- The RTL Memory controller allows the user to define a word width that best fits the application.
- Memory WORD width is user definable
    - Typical word sizes are 8, 16, 32, 36, 64 …
- While the memory on the BE2 is organized as 8Mx72b and the BE3 is 16Mx72b, the address conversion mapping from the selected WORD width to the BE memory is handled by the RTL.
    - Address translation to BE3 memory organization is transparent to the application

SERIAL HIGH SPEED GCI DEVICE INTERFACE

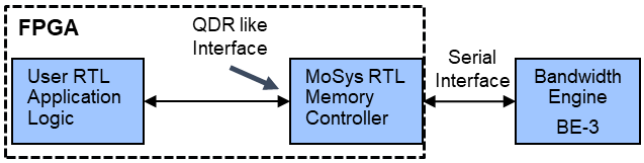
- MoSys RTL handles all serial protocol conversion in the FPGA from the BE resulting in a parallel like QDR interface
- Systems use up to 16 SerDes lanes. (Can use as few as 4 lanes on one port)
- Controller supports 4, 8 or 16 lanes depending FPGA pins available and application bandwidth requirement
- If user would like to writes their own controller, the GCI protocol is available.

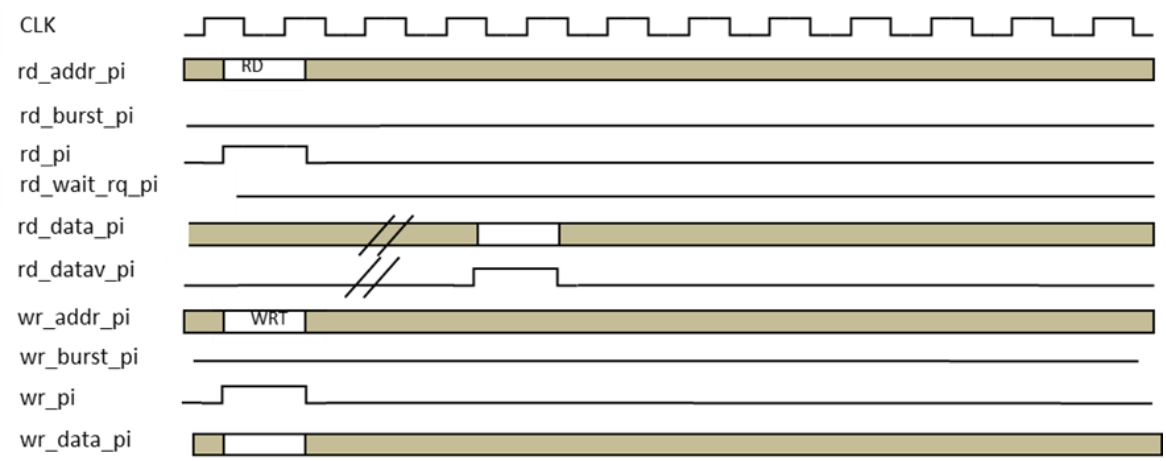
The signal interface at the User Application is a simple SRAM memory Address, Data, Control structure with burst capability. This simple interface shields the users from the BE2 commands, serial interface and the scheduling logic for Bandwidth Engine memory partition timing.

.

2309 Bering Drive, San Jose, CA 95131
Tel: 408-418-7500 Fax: 408-418-7501
www.mosys.com

High Speed GCI Serial Interface





SIGNAL NAME	WIDTH	DIR	DESCRIPTION
Read Interface			
rd_p	1	In	Assertion of this signal indicates that this is a read transaction.
rd_addr_p	32	In	Read address. Please refer to the Address section of this specification to see the detail of this address field.
rd_partsel_p	1	In	Indicates the BE-2 partition that this read command will be operated upon: 0 = Partition 0 for GCI port A, Partition 1 for GCI port B 1 = Partition 2 for GCI port A, Partition 3 for GCI port B
rd_data_p0	*	Out	Returned data from BE-2 memory. This data is qualified by the “rd_datav_p0” signal
rd_data_p1	*	Out	Returned data from BE-2 memory. This data is qualified by the “rd_datav_p1” signal. Note that rd_data_p1 will only have valid data if rd_data_p0 is valid as well. rd
rd_datav_p0	1	Out	The Memory Controller asserts this signal to indicate the current data in the “rd_data_p0” bus is valid
rd_datav_p1	1	Out	The Memory Controller asserts this signal to indicate the current data in the “rd_data_p1” bus is valid. Note that rd_data_p1 will only have valid data if rd_data_p0 is valid as well
rd_wait_rq_p	1	Out	The Memory controller asserts “rd_wait_rq_p” to indicate that it cannot accept the current read request from user. The User Application should hold all the request signals (rd_p, rd_addr_p …) until the de-assertion of this signal.

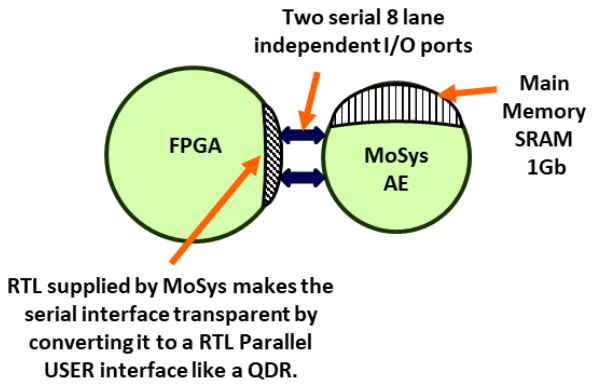
SIGNAL NAME	WIDTH	DIR	DESCRIPTION
Write Interface			
wr_p	1	In	Assertion of this signal indicates that this is a write transaction.
wr_addr_p	32	In	Write address of the memory for this transaction. Please refer to the Address section of this specification to see the detail of this address field.
wr_partsel_p	1	In	Indicates the BE-2 partition that this write command will be operated upon: 0=Partition 0 for GCI port A, Partition 1 for GCI port B 1=Partition 2 for GCI port A, Partition 3 for GCI port B
wr_data_p	*	In	Write data from the User Application logic.
wr_wait_rq_p	1	Out	The Memory controller asserts “wr_wait_rq_p” to indicate that it cannot accept the current write request. The User Application should hold all the request signals (wr_p, wr_addr_p …) until the de-assertion of this signal.

2309 Bering Drive, San Jose, CA 95131
Tel: 408-418-7500 Fax: 408-418-7501
www.mosys.com

Typical Applications

STANDARD MEMORY INTERFACE USE

REPLACE RLDram or UP TO 8 QDR SRAMS

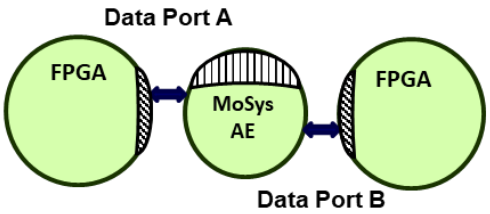


- Each Accelerator Engine Memory has two 8 lane serial Ports
- ***Typical QDR system needs only one port as shown***
- Each port has 8 Data Lanes which is 32 signals
- Typical QDR application requires only 1 port on a BE-2 which is 32 signals
- In addition the MoSys devices have *auto-adaptation which handles on-board signal tuning*
  - Eliminating the need for any external components to insure a clean, reliable signals

DUAL PORT MEMORY USE

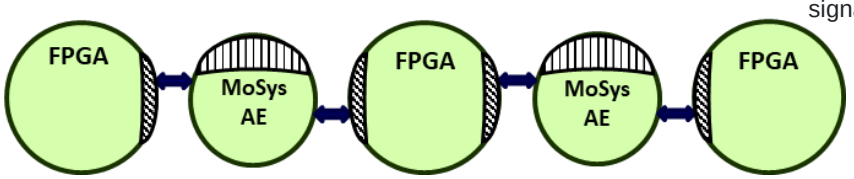
Traditional DUAL PORT MEMORY

- **True Dual Port operation**
- **Allows simultaneous memory access from each Port**

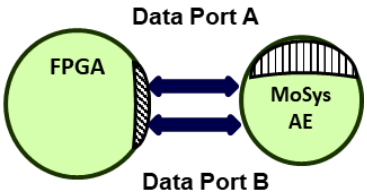


- Each Accelerator Engine Memory has two 8 lane serial Ports.
- Each port has 8 Data Lane which is 32 signals.
- A BE3 can operate as a true Dual Port with simultaneously memory access from each port.
- Also, each port is independent and can have different clock rates for each port
- In addition the MoSys devices have *auto-adaptation which handles on-board signal tuning*
  - Eliminating the need for any external components to insure a clean, reliable signals

Dual Port used in a PIPELINE MEMORY Application



SUPER HIGH BANDWIDTH MEMORY USE



- The devices support application acceleration for aggregate throughput rates up to 380 Gb/s (190 Gb/s full duplex)
- For extremely high bandwidth requirements, these two ports can be combined as one super high bandwidth port.
- Each Accelerator Engine Memory has two 8 lane ports. Using both ports, 64 signals
- In addition the MoSys devices have *auto-adaptation which handles on-board signal tuning*
  - Eliminating the need for any external components to insure a clean, reliable signals

2309 Bering Drive, San Jose, CA 95131
Tel: 408-418-7500 Fax: 408-418-7501
www.mosys.com

Accelerator Engine Family Overview

Software Define - Hardware Accelerated

Software and System Architects can improve application performance by accelerating the memory access and utilizing the In-Memory BURST and In-Memory RMW Functions.

BE2 with 576Mb or the **BE3 with 1Gb** of memory comes in two version with different In-Memory acceleration functions.

- **BURST Functions … High speed data movement and access functions**
- **RMW Functions … Computing and Decision functions**

The different Accelerator Engine devices allow application tuning to achieve increasing levels of performance up to our most powerful engine… the Programable HyperSpeed Engine (PHE).

The Programmable HyperSpeed Accelerator Engine (PHE) is essentially a BE3 with 1Gb of memory with BURST and RMW In-Memory Functions and has 32 RISC cores embedded in the device. *This is the ultimate in acceleration possibilities.*

- **User defined Functions**
- **Future- Standard functions from MoSys**

In-Memory	Part Number	Description	Package	Interface						Memory		Access Rate	In-Memory Functions		
			Pkg Size	Lanes	Rate per Lane Gb/s				BW	tRC	Size	Billion Transaction/s	BURST for Data Movement	RMW / ALU for Compute and Decision	Custom & User Functions with 32 RISC Cores
			mm	Tx/Rx	10.3	12.5	15.6	25	Gb	ns	Gb				
BURST	MSR622	Bandwidth Engine 2 Burst Serial 0.5Gb High Access Memory	FCBGA 19x19	16	✓	✓			320	3.2	0.5	3.3	✓		
BURST	MSR630	Bandwidth Engine 3 Burst Serial 1Gb High Access Memory	FCBGA 27x27	16		✓	✓	✓	380	2.7	1	6.5	✓		
RMW	MSR820	Bandwidth Engine 2 RMW Serial 0.5Gb High Access Memory with ALU for RMW functiions	FCBGA 19x19	16	✓	✓			320	3.2	0.5	3.3	✓	✓	
RMW	MSR830	Bandwidth Engine 3 RMW Serial 1Gb High Access Memory with ALU for RMW functiions	FCBGA 27x27	16		✓	✓	✓	380	2.7	1	6.5	✓	✓	
Program	MSPS30	Programmable Accelerator Engine Serial Interface, 1Gb Memory, 32 RISC Processor cores for custom algorithms, compute, functions	FCBGA 27x27	16		✓	✓	✓	717	2.7	1	24 Internal	✓	✓	✓

www.mosys.com LEARN MORE:
https://mosys.com/blazar-family-of-accelerator-engines/

2309 Bering Drive, San Jose, CA 95131
Tel: 408-418-7500 Fax: 408-418-7501
www.mosys.com