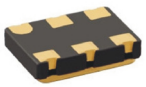
M630x Series

5x7 mm, 1.8/2.5/3.3 V, LVPECL/LVDS/CML/CMOS, TCXO/TCVCXO



RoHS Compliant

Features:

- Superior Jitter Performance (comparable to SAW based)
- Frequencies from 50 MHz to 1.4 GHz
- Designed for a short 2 week cycle time

Applications:

- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications

Ordering Information

M6300	2	J	B	V	P	N	00.0000 MHz

Product Series

M6300 = 3.3 V
M6301 = 2.5 V
M6302 = 1.8 V

Temperature Range

1: 0 °C to +70 °C
3: -55 °C to +105 °C
6: -20 °C to +70 °C
4: -55 °C to +125 °C
2: -40 °C to +85 °C

Stability

G: ±0.5 ppm
J: ±1.0 ppm
K: ±2.0 ppm
H: ±2.5 ppm
L: ±4.6 ppm
E: ±10 ppm

Enable/Disable Function

B: Enable High (Pad 1)
G: Enable High (Pad 2)
S: Enable Low (Pad 1)
M: Enable Low (Pad 2)
U: No Enable/Disable Function

Output Type

F: No Voltage Control (TCXO)
V: Voltage Control (TCVCXO)

Output Waveform

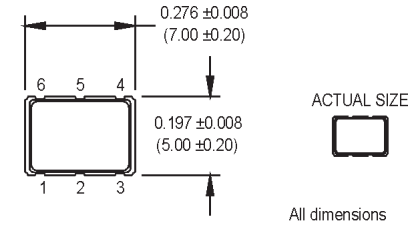
P: LVPECL
L: LVDS
M: CML
C: CMOS

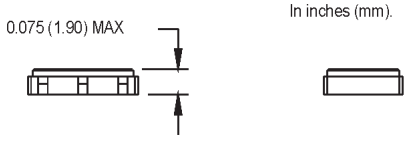
Package/Lead Configurations

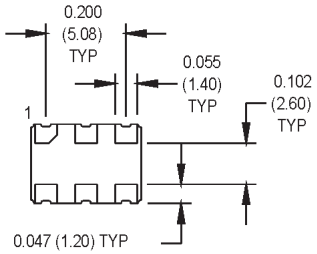
N: Leadless Ceramic (9 Pad)
C: Leadless Ceramic (6 Pad)

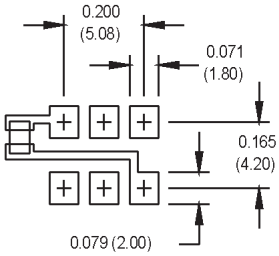
Frequency (customer specified)

M6300Sxxx, M6301Sxxx & M6302Sxxx - Custom datasheets.









PIN 1 ENABLE

Pad 1: Enable/Disable
Pad 2: N/C
Pad 3: GND
Pad 4: Output Q (LVPECL, LVDS, CML, CMOS)
Pad 5: Output Q̄ (LVPECL, LVDS, CML)
Pad 6: V_{cc}

PIN 2 ENABLE

Pad 1: N/C, V Control
Pad 2: Enable/Disable
Pad 3: GND
Pad 4: Output Q (LVPECL, LVDS, CML, CMOS)
Pad 5: Output Q̄ (LVPECL, LVDS, CML)
Pad 6: V_{cc}

Temperature vs. Stability

	±0.5 ppm	±1.0 ppm	±2.0 ppm	±2.5 ppm	±4.6 ppm
0 °C to +70 °C	A	A	A	A	A
-20 °C to +70 °C	N	A	A	A	A
-40 °C to +85 °C	N	A	A	A	A
-55 °C to +105 °C	N	N	N	N	A
-55 °C to +125 °C	N	N	N	N	A

A = Available
N = Contact Factory

M630x Series

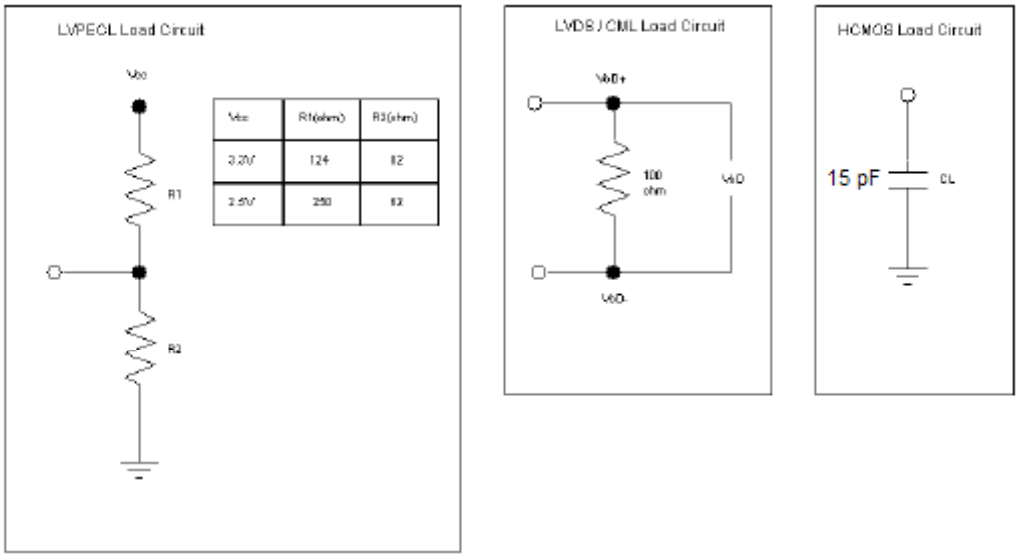
5x7 mm, 3.3/2.5/1.8 Volt, LVPECL/LVDS/CML/CMOS, TCXO/TCVCXO

	Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions/Notes
Electrical Specifications	Frequency Range	F_R	50		1400	MHz	LVPECL, LVDS, CML (See Note 1)
			50		135	MHz	CMOS
	Initial Accuracy	F_I	-1		+1	ppm	@ +25 °C
	Frequency Stability	$\Delta F_T/F$	See Ordering Information			ppm	(Fmax - Fmin)/2 (See Note 2)
	Frequency Vs. Aging	$\Delta F_{TIME}/F$	-3		+3	ppm	First year
			-1		+1	ppm	Thereafter (per year)
	Frequency Vs. Supply Voltage	$\Delta F_{VDD}/F$		±0.40		ppm	5% voltage variation
	Frequency Vs. Reflow			±0.75		ppm	2 reflows max.
	Frequency Vs. Load	$\Delta F_{LOAD}/F$		±0.20		ppm	5% supply voltage variation
	Operating Temperature	T_A	See Ordering Information			°C	
	Storage Temperature	T_{STG}	-55		+125	°C	
	Operating Voltage	$V_{CC}/V_S/V_{DD}$	3.135	3.3	3.465	V	M6300
			2.375	2.5	2.625	V	M6301
			1.71	1.8	1.89	V	M6302
	Operating Current	I_{CC}			125	mA	LVPECL
					100	mA	LVDS
					110	mA	CML
					90	mA	CMOS
	Rise/Fall Time	t_R/t_F			0.35	ns	LVPECL, LVDS, CML
					6	ns	CMOS
	Logic "1" Level	V_{OH}	V_{CC} - 1.02			V	LVPECL
			90			% V_{DD}	CMOS
	Logic "0" Level	V_{OL}			V_{CC} - 1.63	V	LVPECL
					10	% V_{DD}	CMOS
	Common Mode Output Voltage	V_{CM}		1.2		V	LVDS
	Symmetry (Duty Cycle)	t_{DC}	45		55	%	@ 50% V_{DD} (CMOS)
			45		55	%	@ 50% of waveform (LVPECL)
			45		55	%	@ 1.25 V (LVDS)
	Output Voltage Level		0.7	0.95	1.2	V_{pk-pk}	CML
	Tuning Range		±5			ppm	VCTCXO only (See Note 3)
	Voltage Control Range	V_C	0.18	0.90	1.62	V	@ 1.8 V supply (VCTCXO only - Pad 2)
			0.25	1.25	2.25	V	@ 2.5 V supply (VCTCXO only - Pad 2)
			0.30	1.65	3.00	V	@ 3.3 V supply (VCTCXO only - Pad 2)
	Output Skew			20		ps	LVPECL
				15		ps	CML
				20		ps	LVDS
	Output Load		50 Ω to (V_{CC} - 2)				LVPECL (See Note 4)
			V_{DC} 100 Ω Differential				LVDS, CML (See Note 4)
			15 pF				CMOS (See Note 4)
	Enable/Disable Function		80			%	Output Enabled
	(Option B or G)				0.5	V	Output Disabled
	Enable/Disable Function				0.5	V	Output Enabled
	(Option S or M)		80			%	Output Disabled
	Phase Noise (Typical)	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier
	@ 622.080 MHz (LVPECL)	-60	-90	-120	-127	-133	dBc/Hz
	@ 100.000 MHz (HCMOS)	-70	-103	-123	-131	-136	dBc/Hz
	@ 50.000 MHZ (HCMOS)	-77	-109	-129	-137	-141	dBc/Hz

Environmental	Shock	Per MIL-STD-202, Method 213, Condition C
	Vibration	Per MIL-STD-202, Methods 201 & 204
	Solderability	Per EIAJ-STD-002
	Hermeticity	1 X 10^{-8} atm cc/sec of helium (Crystal only)
	Thermal Shock	Per MIL-STD-883, Method 1011, Condition A
	Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B

Note 1: Contact factory for frequencies over 945 MHz.
Note 2: Contact factory for less than ±1 ppm frequency stability.
Note 3: Contact factory for other tuning range options.
Note 4: Refer to the load circuit diagram in this data sheet.

Load Circuit Diagrams



Lead Free Solder Profile