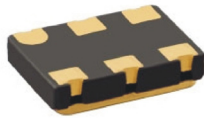
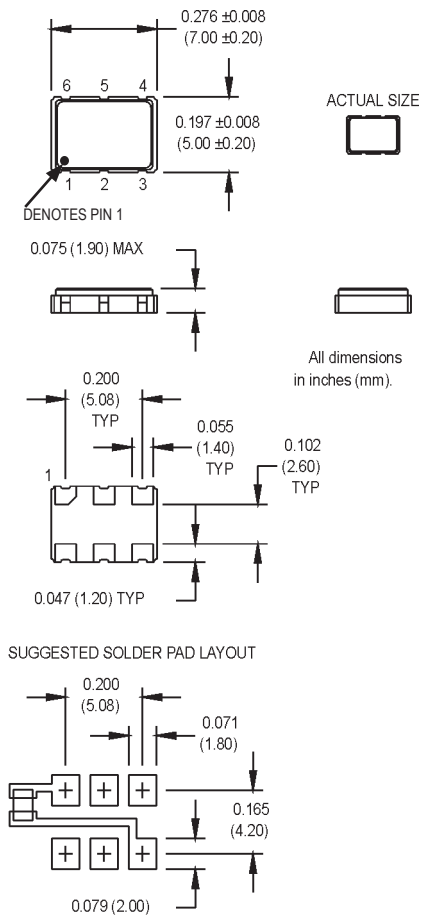


UVV Series

5x7 mm, 3.3 Volt, LVPECL/LVDS, VCXO



- Versatile VCXO to 800 MHz with good jitter (3 ps typical)
- Used in low jitter clock synthesizers and SONET applications



Ordering Information

UVV 1 0 R 1 L N 00.0000 MHz

Product Series _____

Temperature Range _____
 1: 0°C to +70°C 2: -40°C to +85°C
 6: -20°C to +70°C 8: 0°C to +50°C

Stability _____
 0: Nominal per APR selection

Output Type _____
 R: Complementary, Enable
 Z: Complementary, w/o Enable

Absolute Pull Range _____
 1: ±50 ppm (±35 ppm typ. Stability)
 2: ±100 ppm (±20 ppm typ. Stability)
 5: ±80 ppm (±25 ppm typ. Stability)
 8: ±25 ppm (±50 ppm typ. Stability)

Symmetry/Output Logic Type _____
 L: 45/55% LVDS P: 45/55% PECL
 H: 40/60% LVDS Q: 40/60% PECL

Package/Lead Configurations _____
 N: Leadless Ceramic (6 pads)

Frequency (customer specified) _____

M3013Sxxx - Contact factory for data sheet.

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition
Frequency Range	F	0.75		800	MHz	
Operating Temperature	TA	(See ordering information)				
Storage Temperature	TS	-55		+125	°C	
Frequency Stability	ΔF/F	(See ordering information)				
Aging						
1st Year		-3/-5		+3/+5	ppm	<52 MHz / ≥52 MHz
Thereafter (per year)		-1/-2		+1/+2	ppm	<52 MHz / ≥52 MHz
Pullability/APR		(See ordering information)				
Control Voltage	V _c	0.3	1.65	3	V	Pin 1 Voltage
Linearity			5	15	%	Positive Monotonic Slope
Modulation Bandwidth	f _m	10			kHz	-3 dB bandwidth
Input Impedance	Z _{in}	50k			Ohms	
Input Voltage	V _{cc}	3.135	3.3	3.456	V	
Input Current	I _{cc}					
0.75 MHz to 24 MHz				70/30	mA	PECL/LVDS
24 MHz to 96 MHz				100/60	mA	PECL/LVDS
96 MHz to 800 MHz				110/60	mA	PECL/LVDS
Output Type						PECL/LVDS
Load						
		50 Ohms to V _{cc} -2 VDC				See Note 3
		100 Ohms differential load				PECL waveform
Symmetry (Duty Cycle)						V _{cc} -1.3 VDC (PECL)
(Per Symmetry Code)		(See ordering information)				
Output Skew				200	ps	PECL
Differential Voltage	V _o	250	340	450	mV	LVDS
Logic "1" Level	V _{oh}	V _{cc} -1.02			V	PECL
Logic "0" Level	V _{ol}			V _{cc} -1.63	V	PECL
Rise/Fall Time	T _r /T _f		.35	.55	ns	@ 20/80% LVPECL
			.50	1.0	ns	@ 20/80% LVDS
Enable/Disable Logic		80% V _{cc} min or N/C: output active				Output Option R
		20% V _{cc} max: output disables to high-Z				
Start up Time			5		ms	
Phase Jitter	φ _J		3	5	ps RMS	Integrated 12 kHz - 20 MHz
Phase Noise (Typical)		10 Hz	100 Hz	1 kHz	10 kHz	Offset from carrier
@ 19.44 MHz		-60	-90	-112	-140	dBc/Hz
@ 155.52 MHz		-60	-90	-112	-123	dBc/Hz
Environmental						
Mechanical Shock	Per MIL-STD-202, Method 213, Condition C					
Vibration	Per MIL-STD-202, Method 201 & 204					
Max Soldering Conditions	See solder profiles, Figure 1					
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10 ⁻⁹ atm cc/s of helium)					
Solderability	Per MIL-STD-883, Method 2003					

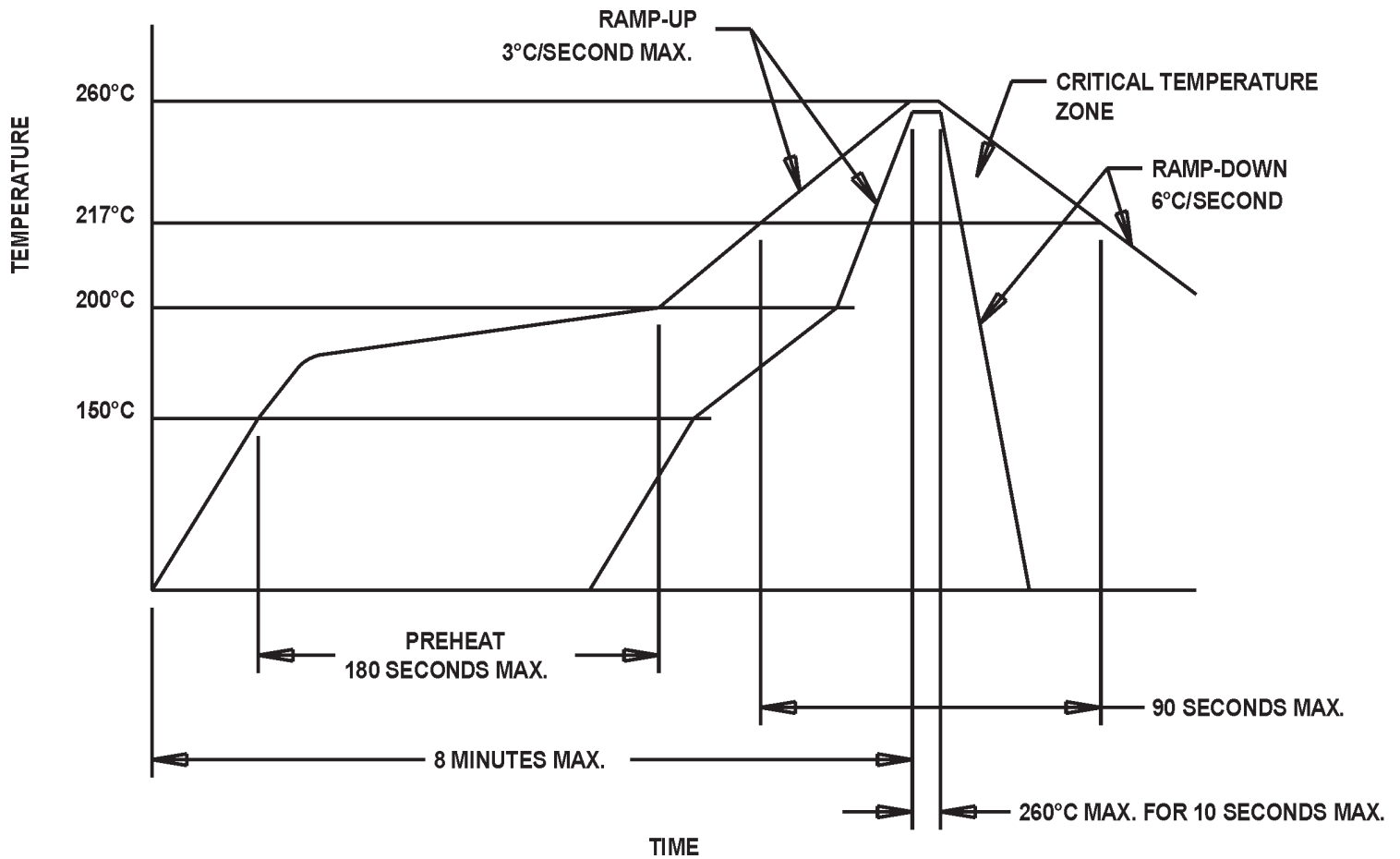
- Stability given for deviation over temperature
- APR specification inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging.
- PECL - See load circuit diagram #5. LVDS - See load circuit diagram #9.

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Please see www.mtronpti.com for our complete offering and detailed datasheets. Contact us for your application specific requirements: MtronPTI 1-800-762-8800.

Revision: 8-14-07

MtronPTI Lead Free Solder Profile



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