LP38512-ADJ

LP38512-ADJ 1.5A Fast-Transient Response Adjustable Low-Dropout Linear Voltage Regulator

Literature Number: SNVS546C

National Semiconductor

February 12, 2009

LP38512-ADJ

1.5A Fast-Transient Response Adjustable Low-Dropout Linear Voltage Regulator

General Description

The LP38512-ADJ Fast-Transient Response Low-Dropout Voltage Regulator offers the highest-performance in meeting AC and DC accuracy requirements for powering Digital Cores. The LP38512-ADJ uses a proprietary control loop that enables extremely fast response to change in line conditions and load demands. Output Voltage DC accuracy is guaranteed at 2.5% over line, load and full temperature range from -40°C to +125°C. The LP38512-ADJ is designed for inputs from the 2.5V, 3.3V, and 5.0V rail, is stable with 10 µF ceramic capacitors, and has an adjustable output voltage. The LP38512-ADJ provides excellent transient performance to meet the demand of high performance digital core ASICs, DSPs, and FPGAs found in highly-intensive applications such as servers, routers/switches, and base stations.

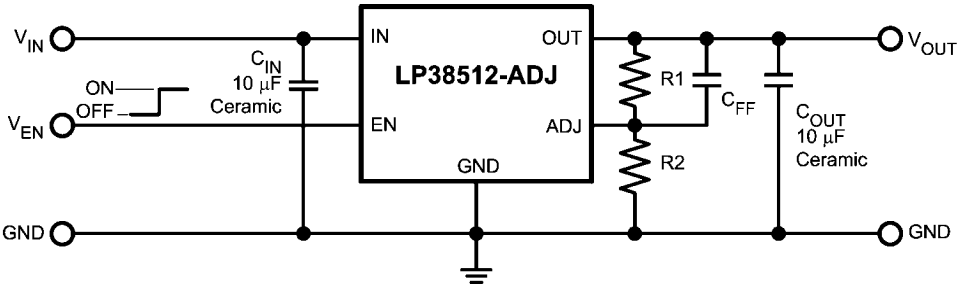
Features

- 2.25V to 5.5V Input Voltage Range
- Adjustable Output Voltage Range of 0.5V to 4.5V
- 1.5A Output Load Current
- ±2.0% Accuracy over Line, Load, and Full-Temperature Range from -40°C to +125°C
- Stable with tiny 10 µF ceramic capacitors
- Enable pin
- Typically less than 1uA of Ground pin current in when Enable pin is low
- 25dB of PSRR at 100 kHz
- Over-Temperature and Over-Current Protection
- PSOP-8 and TO263 THIN Surface Mount Packages

Applications

- Digital Core ASICs, FPGAs, and DSPs
- Servers
- Routers and Switches
- Base Stations
- Storage Area Networks
- DDR2 Memory

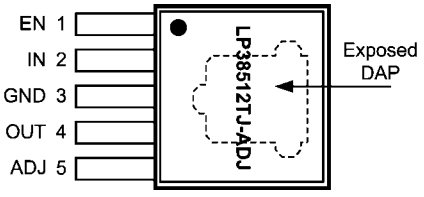
Typical Application Circuit



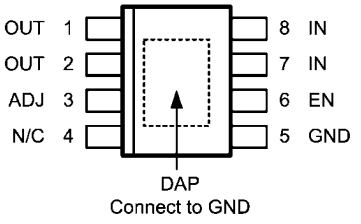
Ordering Information

Output Voltage	Order Number	Package Type	Package Marking	Supplie As
ADJ	LP38512MR-ADJ	PSOP-8	LP38512MR-ADJ	Rail
	LP38512MRX-ADJ	PSOP-8	LP38512MR-ADJ	Tape and Reel
	LP38512TJ-ADJ	TO263 THIN	LP38512TJ-ADJ	Tape and Reel

Connection Diagrams



Top View
TO-263 THIN 5-Pin Package



Top View
PSOP 8-Pin Package

Pin Descriptions for TO-263 THIN (TJ) Package

Pin #	Pin Name	Function
1	EN	Enable. Pull high to enable the output, low to disable the output. This pin has no internal bias and must be tied to the input voltage, or actively driven.
2	IN	Input Supply Pin
3	GND	Ground
4	OUT	Regulated Output Voltage Pin
5	ADJ	The feedback to the internal Error Amplifier to set the output voltage
DAP	DAP	The TJ-263 DAP is used as a thermal connection to remove heat from the device to an external heat-sink in the form of the copper area on the printed circuit board. The DAP is physically connected to backside of the die, but is not internally connected to device ground. The DAP should be soldered to the Ground Plane copper.

Pin Descriptions for PSOP-8 (MR) Package

Pin #	Pin Name	Function
1, 2	OUT	Regulated Output Voltage Pin. Pins share current and must be connected together.
3	ADJ	The feedback to the internal Error Amplifier to set the output voltage
4	N/C	No internal connection.
5	GND	Ground
6	EN	Enable. Pull high to enable the output, low to disable the output. This pin has no internal bias and must be tied to the input voltage, or actively driven.
7, 8	IN	Input Supply Pin. Pins share current and must be connected together.
DAP	DAP	The PSOP-8 DAP connection is used as a thermal connection to remove heat from the device to an external heat-sink in the form of the copper area on the printed circuit board. The DAP is physically connected to backside of the die, but is not internally connected to device ground. The DAP should be soldered to the Ground Plane copper.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Soldering Temperature (Note 3)	
Thin TO-263	260°C, 10s
PSOP-8	260°C, 10s
ESD Rating (Note 2)	±2 kV
Power Dissipation (Note 4)	Internally Limited
Input Pin Voltage (Survival)	-0.3V to +6.0V
Enable Pin Voltage (Survival)	-0.3V to +6.0V
Output Pin Voltage (Survival)	-0.3V to +6.0V
ADJ Pin Voltage (Survival)	-0.3V to +6.0V
I_{OUT} (Survival)	Internally Limited

Operating Ratings (Note 1)

Input Supply Voltage, V_{IN}	2.25V to 5.5V
Output Voltage, V_{OUT}	V_{ADJ} to 5V
Enable Input Voltage, V_{EN}	0.0V to 5.5V
Output Current (DC)	1 mA to 1.5A
Junction Temperature (Note 4)	−40°C to +125°C

Electrical Characteristics

Unless otherwise specified: V_{IN}= 2.50V, V_{OUT}= V_{ADJ}, I_{OUT}= 10 mA, C_{IN}= 10 µF, C_{OUT}= 10 µF, V_{EN}= 2.0V. Limits in standard type are for T_J= 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J= 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ADJ}	V_{ADJ} Accuracy (Note 7)	2.25V ≤ V_{IN} ≤ 5.5V 10 mA ≤ I_{OUT} ≤ 1.5A	495.0 **490.0**	500.	505.0 **510.0**	mV
I_{ADJ}	ADJ Pin Bias Current	2.25V ≤ V_{IN} ≤ 5.5V	-	1	-	nA
$\Delta V_{ADJ}/\Delta V_{IN}$	V_{ADJ} Line Regulation (Notes 5, 7)	2.25V ≤ V_{IN} ≤ 5.5V	-	0.03 **0.06**	-	%/V
$\Delta V_{ADJ}/\Delta I_{OUT}$	V_{ADJ} Load Regulation (Notes 6, 7)	10 mA ≤ I_{OUT} ≤ 1.5A	-	0.10 **0.20**	-	%/A
V_{DO}	Dropout Voltage (Note 8)	I_{OUT} = 1.5A	-	-	**300**	mV
I_{GND}	Ground Pin Current, Output Enabled	I_{OUT} = 10 mA	-	10	12 **15**	mA
		I_{OUT} = 1.5A	-	10	12 **14**	
	Ground Pin Current, Output Disabled	V_{EN} = 0.50V	-	60	100 **110**	µA
I_{SC}	Short Circuit Current	V_{OUT} = 0V	-	2.8	-	A
Enable Input						
$V_{EN(ON)}$	Enable ON Voltage Threshold	V_{EN} rising from < $V_{EN(OFF)}$ until V_{OUT} = ON	0.90 **0.80**	1.20	1.50 **1.60**	V
$V_{EN(OFF)}$	Enable OFF Voltage Threshold	V_{EN} falling from > $V_{EN(ON)}$ until V_{OUT} = OFF	0.60 **0.50**	1.00	1.40 **1.50**	V
$V_{EN(HYS)}$	Enable Voltage Hysteresis	$V_{EN(ON)}$ - $V_{EN(OFF)}$	-	200	-	mV
I_{EN}	Enable Pin Current	V_{EN} = V_{IN}	-	1	-	nA
		V_{EN} = 0V	-	-1	-	
$t_{d(OFF)}$	Turn-off delay	Time from V_{EN} < $V_{EN(TH)}$ to V_{OUT} = OFF, I_{LOAD} = 1.5A	-	5	-	µs
$t_{d(ON)}$	Turn-on delay	Time from V_{EN} >$V_{EN(TH)}$ to V_{OUT} = ON, I_{LOAD} = 1.5A	-	5	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AC Parameters						
PSRR	Ripple Rejection	V_{IN} = 2.5V f = 120Hz	-	73	-	dB
		V_{IN} = 2.5V f = 1 kHz	-	70	-	
$\rho_{n(l/f)}$	Output Noise Density	f = 120Hz	-	0.4	-	$\mu V/\sqrt{Hz}$
e_n	Output Noise Voltage	BW = 10Hz - 100kHz	-	25	-	μV_{RMS}
Thermal Characteristics						
T_{SD}	Thermal Shutdown	T_J rising	-	165	-	°C
ΔT_{SD}	Thermal Shutdown Hysteresis	T_J falling from T_{SD}	-	10	-	
θ_{J-A}	Thermal Resistance Junction to Ambient (Note 4)	PSOP-8	-	168	-	°C/W
		TO-263 THIN	-	67	-	
θ_{J-C}	Thermal Resistance Junction to Case	PSOP-8	-	11	-	°C/W
		TO-263 THIN	-	3	-	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD22-A114.

Note 3: Refer to JEDEC J-STD-020C for surface mount device (SMD) package reflow profiles and conditions. Unless otherwise stated, the temperatures and times are for Sn-Pb (STD) only.

Note 4: Device operation must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance (θ_{JA}).The typical θ_{JA} ratings given are worst case based on minimum land area on two-layer PCB (EIA/JESD51-3). See *POWER DISSIPATION/HEAT-SINKING* for details.

Note 5: Line regulation is defined as the change in V_{ADJ} from the nominal value due to change in the voltage at the input.

Note 6: Load regulation is defined as the change in V_{ADJ} from the nominal value due to change in the load current at the output.

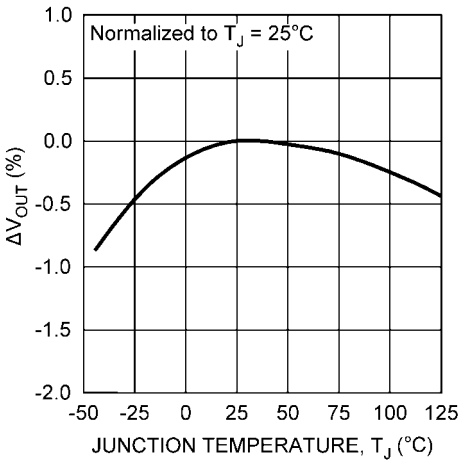
Note 7: The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.

Note 8: Dropout voltage (V_{DO}) is typically defined as the input to output voltage differential (V_{IN} - V_{OUT}) where the input voltage is low enough to cause the output voltage to drop 2%. For the LP38512-ADJ, the minimum operating voltage of 2.25V is the limiting factor when the programed output voltage is less than typically 1.80V.

Typical Performance Characteristics

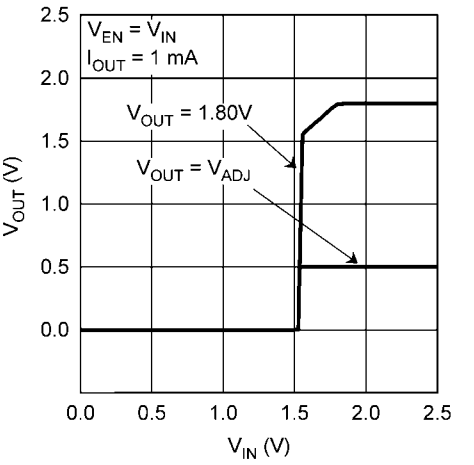
Unless otherwise specified: T_J = 25°C, V_{IN} = 2.50V, V_{OUT}= V_{ADJ}, V_{EN} = 2.0V, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA.

V_{ADJ} vs Temperature



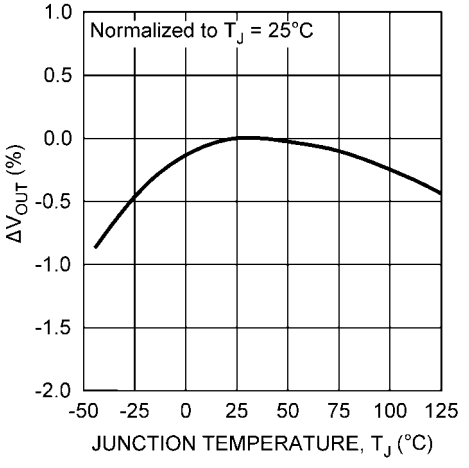
30040911

V_{OUT} vs V_{IN}



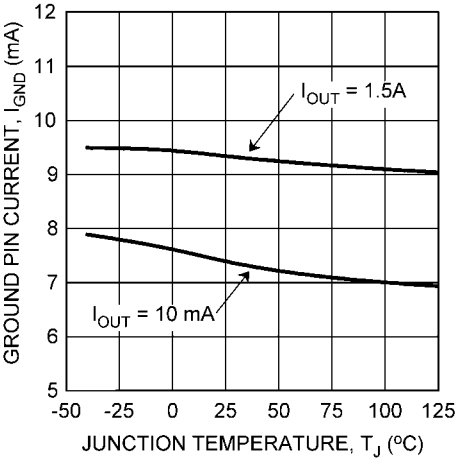
30040915

Ground Pin Current (I_{GND}) vs V_{IN}



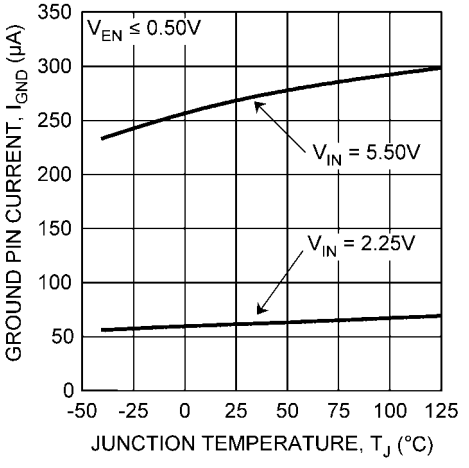
30040911

Ground Pin Current (I_{GND}) vs Temperature



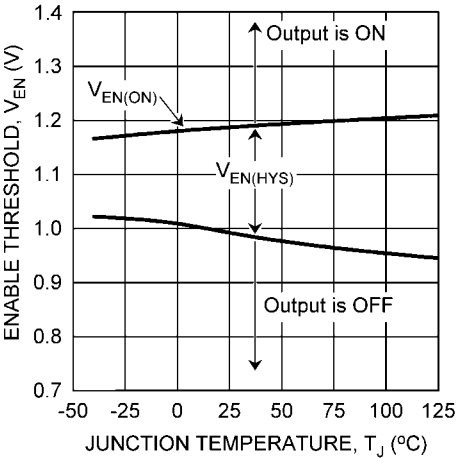
30040913

Ground Pin Current (I_{GND}) vs Temperature



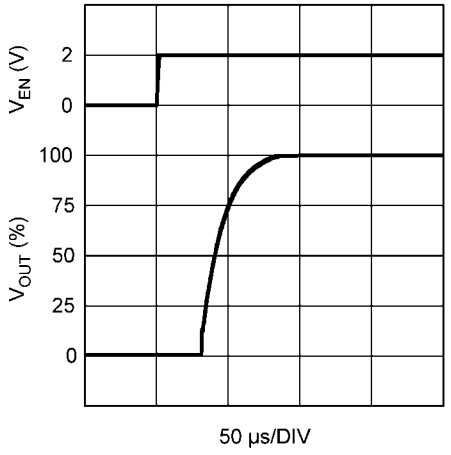
30040914

Enable Threshold vs Temperature



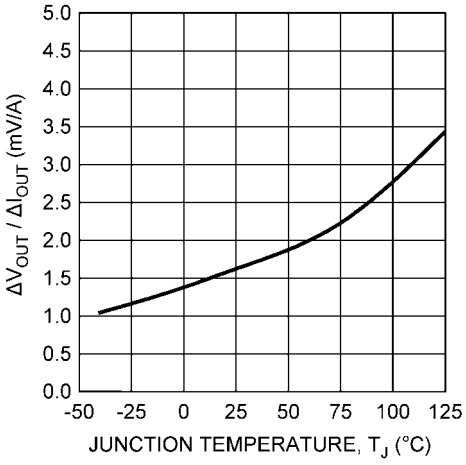
30040916

V_{OUT} vs V_{EN}



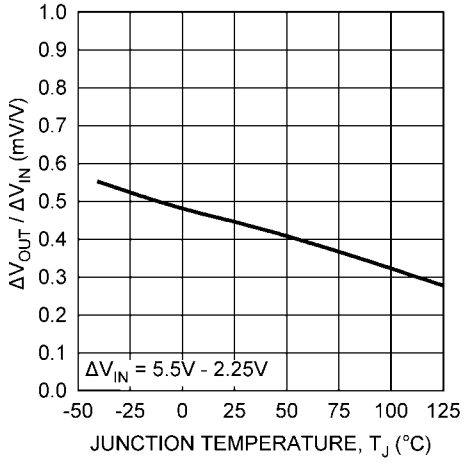
30040932

Load regulation vs Temperature



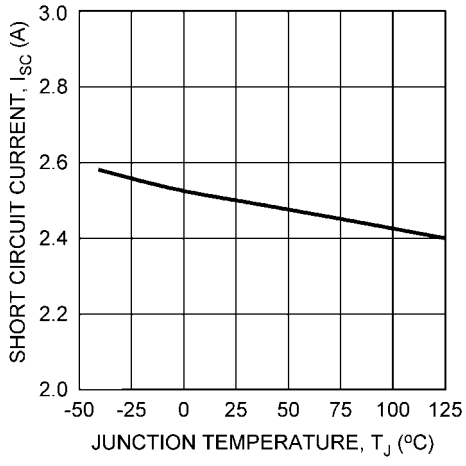
30040920

Line Regulation vs Temperature



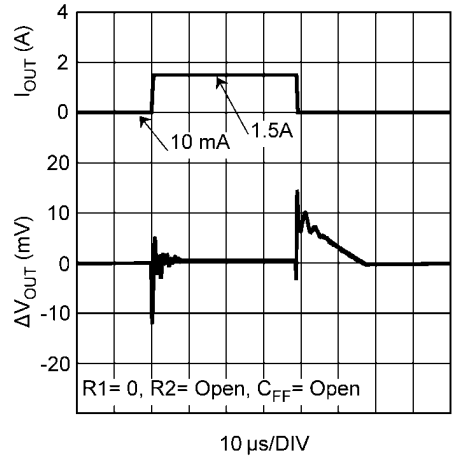
30040921

Current Limit vs Temperature



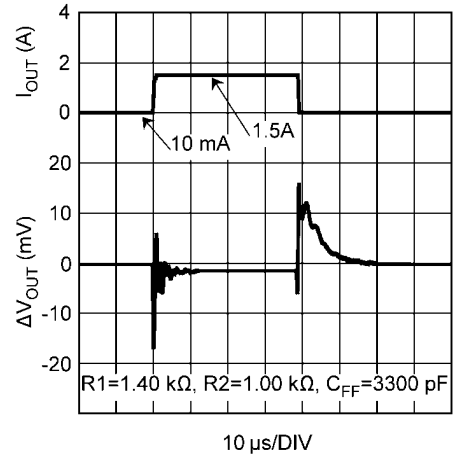
30040922

Load Transient 10 mA to 1.5A
V_{OUT} = V_{ADJ}, C_{OUT} = 10 µF Ceramic



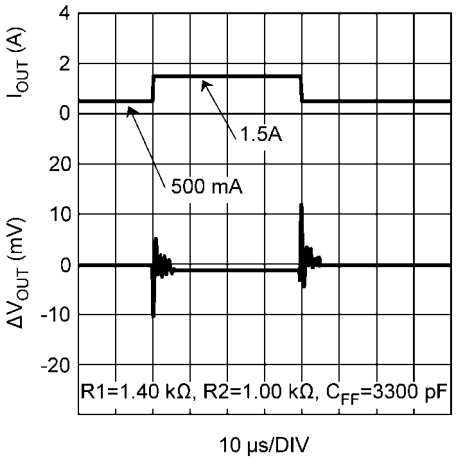
30040923

Load Transient, 10 mA to 1.5A
V_{OUT} = 1.20V, C_{OUT} = 10 µF Ceramic



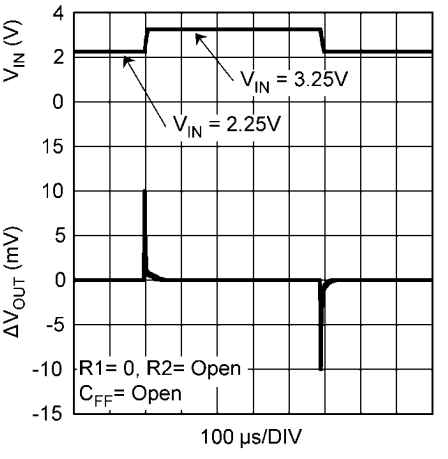
30040924

Load Transient, 500 mA to 1.5A
V_{OUT} = 1.20V, C_{OUT} = 10 µF Ceramic



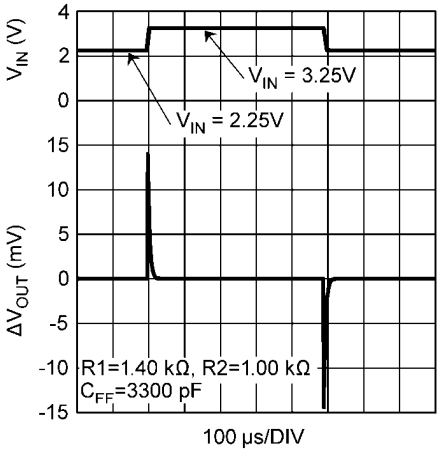
30040925

Line Transient
V_{OUT} = V_{ADJ}, C_{OUT} = 10 µF Ceramic



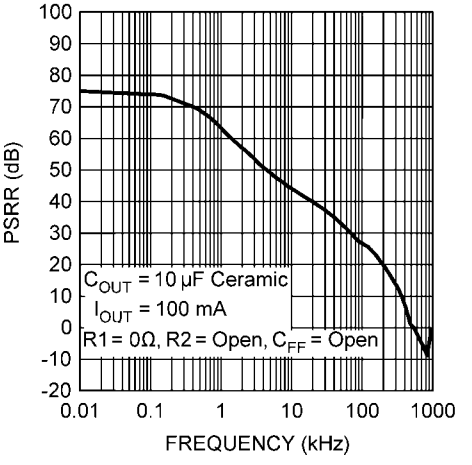
30040926

Line Transient
V_{OUT} = 1.20V, C_{OUT} = 10 µF Ceramic



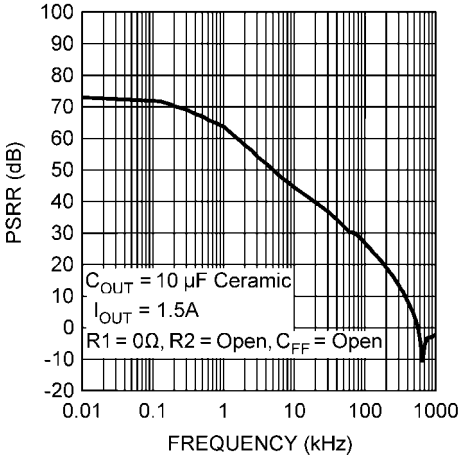
30040927

PSRR, I_{OUT} = 100 mA
V_{OUT} = V_{ADJ}, C_{OUT} = 10 µF Ceramic



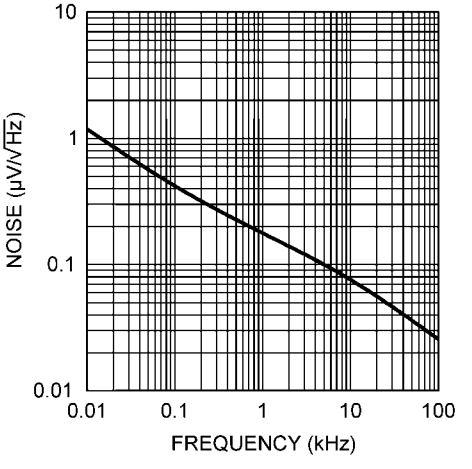
30040929

PSRR, I_{OUT} = 1.5A
V_{OUT} = V_{ADJ}, C_{OUT} = 10 µF Ceramic



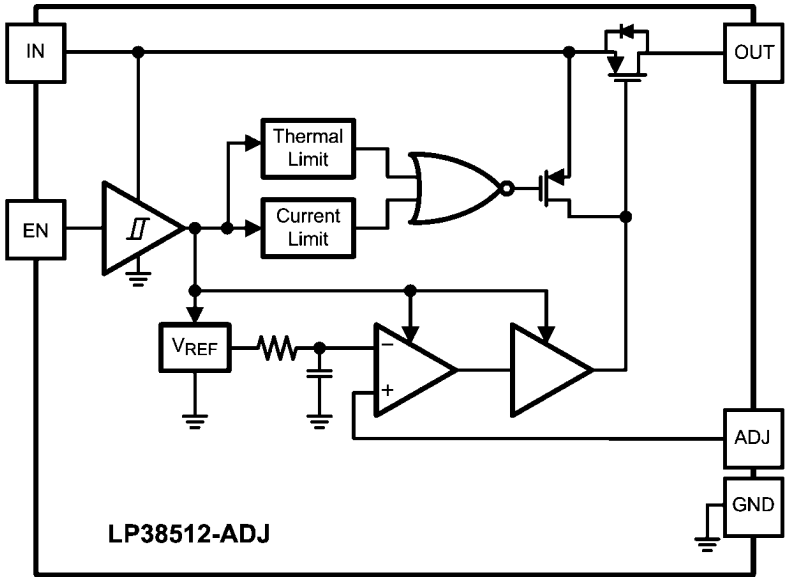
30040930

Output Noise Density
V_{OUT} = V_{ADJ}, C_{OUT} = 10 µF Ceramic



30040931

Block Diagram



30040907

Application Information

EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

Input Capacitor

A ceramic input capacitor of at least 10 µF is required. For general usage across all load currents and operating conditions, a 10 µF ceramic input capacitor will provide satisfactory performance.

Output Capacitor

A ceramic capacitor with a minimum value of 10 µF is required at the output pin for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pin using traces which have no other currents flowing through them. As long as the minimum of 10 µF ceramic is met, there is no limitation on any additional capacitance.

X7R and X5R dielectric ceramic capacitors are strongly recommended, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

Z5U and Y5V dielectric ceramics are not recommended as the capacitance will drop severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed. A less common condition is when an alternate voltage source is connected to the output.

There are two possible paths for current to flow from the output pin back to the input during a reverse voltage condition.

While V_{IN} is high enough to keep the control circuity alive, and the Enable pin is above the $V_{EN(ON)}$ threshold, the control circuitry will attempt to regulate the output voltage. Since the input voltage is less than the programmed output voltage, the control circuit will drive the gate of the pass element to the full on condition when the output voltage begins to fall. In this condition, reverse current will flow from the output pin to the input pin, limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. Discharging an output capacitor up to 1000 µF in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided. When the Enable is low this condition will be prevented.

The internal PFET pass element in the LP38512-ADJ has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output voltage to input voltage differential is more than 500 mV (typical) the parasitic diode becomes forward biased and current flows from the output pin to the input pin through the diode. The current in the parasitic diode should be limited to less than 1A continuous and 5A peak.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommended for this protective clamp.

SHORT-CIRCUIT PROTECTION

The LP38512-ADJ is short circuit protected, and in the event of a peak over-current condition the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation

causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to the *POWER DISSIPATION/HEAT-SINKING* section for power dissipation calculations.

SETTING THE OUTPUT VOLTAGE

The output voltage is set using the external resistive divider R1 and R2. The output voltage is given by the formula:

$$V_{OUT} = V_{ADJ} \times (1 + (R1/R2)) \quad (1)$$

The resistors used for R1 and R2 should be high quality, tight tolerance, and with matching temperature coefficients. It is important to remember that, although the value of V_{ADJ} is guaranteed, the final value of V_{OUT} is not. The use of low quality resistors for R1 and R2 can easily produce a V_{OUT} value that is unacceptable.

It is recommended that the values selected for R1 and R2 are such that the parallel value is less than 1.00 kΩ. This is to reduce the possibility of any internal parasitic capacitances on the ADJ pin from creating an undesirable phase shift that may interfere with device stability.

$$((R1 \times R2) / (R1 + R2)) \leq 1.00\ k\Omega \quad (2)$$

FEED FORWARD CAPACITOR, C_{FF}

When using a ceramic capacitor for C_{OUT}, the typical ESR value will be too small to provide any meaningful positive phase compensation, F_Z, to offset the internal negative phase shifts in the gain loop.

$$F_Z = 1 / (2 \times \pi \times C_{OUT} \times ESR) \quad (3)$$

A capacitor placed across the gain resistor R1 will provide additional phase margin to improve load transient response of the device. This capacitor, C_{FF}, in parallel with R1, will form a zero in the loop response given by the formula:

$$F_Z = 1 / (2 \times \pi \times C_{FF} \times R1) \quad (4)$$

For optimum load transient response select C_{FF} so the zero frequency, F_Z, falls between 20 kHz and 40 kHz.

$$C_{FF} = 1 / (2 \times \pi \times R1 \times F_Z) \quad (5)$$

The phase lead provided by C_{FF} diminishes as the DC gain approaches unity, or V_{OUT} approaches V_{ADJ}. This is because C_{FF} also forms a pole with a frequency of:

$$F_P = 1 / (2 \times \pi \times C_{FF} \times (R1 \parallel R2)) \quad (6)$$

It's important to note that at higher output voltages, where R1 is much larger than R2, the pole and zero are far apart in frequency. At lower output voltages the frequency of the pole and the zero mover closer together. The phase lead provided from C_{FF} diminishes quickly as the output voltage is reduced, and has no effect when $V_{OUT} = V_{ADJ}$. For this reason, relying on this compensation technique alone is adequate only for higher output voltages.

Table 1 lists some suggested, best fit, standard ±1% resistor values for R1 and R2, and a standard ±10% capacitor values for C_{FF}, for a range of V_{OUT} values. Other values of R1, R2, and C_{FF} are available that will give similar results.

TABLE 1.

V_{OUT}	R_1	R_2	C_{FF}	F_Z
0.80V	1.07 kΩ	1.78 kΩ	4700 pF	31.6 kHz
1.00V	1.00 kΩ	1.00 kΩ	4700 pF	33.8 kHz
1.20V	1.40 kΩ	1.00 kΩ	3300 pF	34.4 kHz
1.50V	2.00 kΩ	1.00 kΩ	2700 pF	29.5 kHz
1.80V	2.94 kΩ	1.13 kΩ	1500 pF	36.1kHz
2.00V	1.02 kΩ	340Ω	4700 pF	33.2 kHz
2.50V	1.02 kΩ	255Ω	4700 pF	33.2 kHz
3.00V	1.00 kΩ	200Ω	4700 pF	33.8 kHz
3.30V	2.00 kΩ	357Ω	2700 pF	29.5 kHz

Please refer to Application Note *AN-1378 Method For Calculating Output Voltage Tolerances in Adjustable Regulators* for additional information on how resistor tolerances affect the calculated V_{OUT} value.

ENABLE OPERATION

The Enable ON threshold is typically 1.2V, and the OFF threshold is typically 1.0V. To ensure reliable operation the Enable pin voltage must rise above the maximum $V_{EN(ON)}$ threshold and must fall below the minimum $V_{EN(OFF)}$ threshold. The Enable threshold has typically 200mV of hysteresis to improve noise immunity.

The Enable pin (EN) has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively.

If the Enable pin is driven from a single ended device (such as the collector of a discrete transistor) a pull-up resistor to V_{IN}, or a pull-down resistor to ground, will be required for proper operation. A 1 kΩ to 100 kΩ resistor can be used as the pull-up or pull-down resistor to establish default condition for the EN pin. The resistor value selected should be appropriate to swamp out any leakage in the external single ended device, as well as any stray capacitance.

If the Enable pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator output), the pull-up, or pull-down, resistor is not required.

If the application does not require the Enable function, the pin should be connected directly to the adjacent V_{IN} pin.

POWER DISSIPATION/HEAT-SINKING

A heat-sink may be required depending on the maximum power dissipation ($P_{D(MAX)}$), maximum ambient temperature ($T_{A(MAX)}$)of the application, and the thermal resistance (θ_{JA}) of the package. Under all possible conditions, the junction temperature (T_J) must be within the range specified in the Operating Ratings. The total power dissipation of the device is given by:

$$P_D = ((V_{IN} - V_{OUT}) \times I_{OUT}) + ((V_{IN}) \times I_{GND}) \quad (7)$$

where I_{GND} is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum expected ambient temperature ($T_{A(MAX)}$) of the application, and the maximum allowable junction temperature ($T_{J(MAX)}$):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (8)$$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} = \Delta T_J / P_{D(MAX)} \quad (9)$$

LP38512-ADJ is available in TO-263 THIN and PSOP-8 surface mount packages. For a comparison of the TO-263 THIN package to the standard TO-263 package see Application Note *AN-1797 TO-263 THIN Package*. The θ_{JA} thermal resistance depends on amount of copper area, or heat sink, attached to the DAP, and on air flow. See Application Note *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* for guidelines.

Heat-Sinking the TO-263 THIN Package

The DAP of the TO-263 THIN package is soldered to the copper plane for heat sinking. The TO-263 THIN package has a θ_{JA} rating of 67°C/W, and a θ_{JC} rating of 2°C/W. The θ_{JA} rating of 67°C/W includes the device DAP soldered to an area of 0.055 square inches (0.22 in x 0.25 in) of 1 ounce copper on a two sided PCB, with no airflow. See JEDEC standard EIA/JESD51-3 for more information.

Figure 1 shows a curve for the θ_{JA} of TO-263 THIN package for different thermal via counts under the exposed DAP, using a four layer PCB for heat sinking. The thermal vias connect the copper area directly under the exposed DAP to the first internal copper plane only. See JEDEC standards EIA/JESD51-5 and EIA/JESD51-7 for more information.

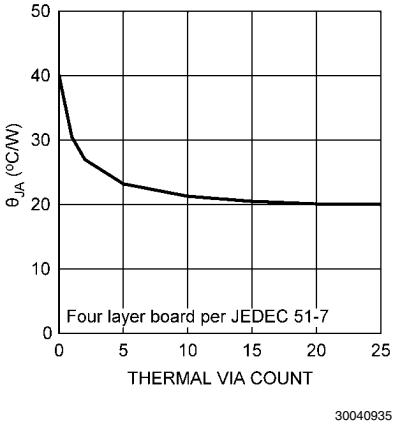


FIGURE 1. θ_{JA} vs Thermal Via Count for the TO-263 THIN Package on 4–Layer PCB

Figure 2 shows the thermal performance when the Thin TO-263 is mounted to a two layer PCB where the copper area is predominately directly under the exposed DAP.As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement.

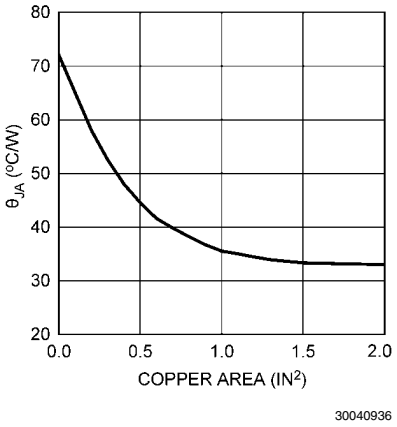


FIGURE 2. θ_{JA} vs Copper Area for the TO-263 THIN Package

Heat-Sinking The PSOP-8 Package

The DAP of the PSOP-8 package is soldered to the copper plane for heat sinking. The LP38512MR package has a θ_{JA} rating of 168°C/W, and a θ_{JC} rating of 11°C/W. The θ_{JA} rating of 168°C/W includes the device DAP soldered to an area of 0.008 square inches (0.09 in x 0.09 in) of 1 ounce copper on a two sided PCB, with no airflow. See JEDEC standard EIA/JESD51-3 for more information.

Figure 3 shows a curve for different thermal via counts under the exposed DAP, using a four layer PCB for heat sinking. The thermal vias connect the copper area directly under the exposed DAP to the first internal copper plane only. See JEDEC standards EIA/JESD51-5 and EIA/JESD51-7 for more information.

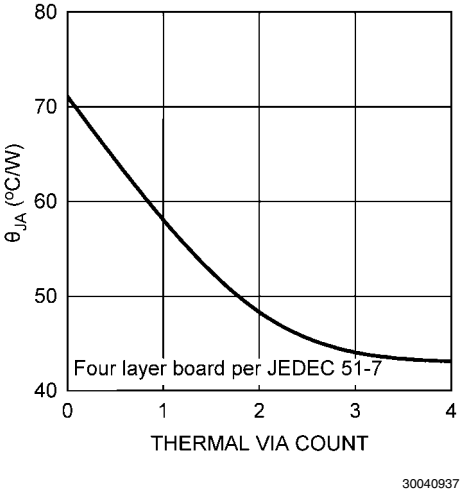


FIGURE 3. θ_{JA} vs Thermal Via Count for the PSOP-8 Package on 2–Layer PCB with Copper Area on Bottom-Side

Figure 4 shows thermal performance for a two layer board using thermal vias to a copper area on the bottom of the PCB. The copper area on the top of the PCB, which is soldered to the exposed DAP, is 0.10in x 0.20in, which is approximately the same dimensions as the body of the PSOP-8 package. The copper area on the bottom of the PCB is a square area and is centered directly under the PSOP-8 package.

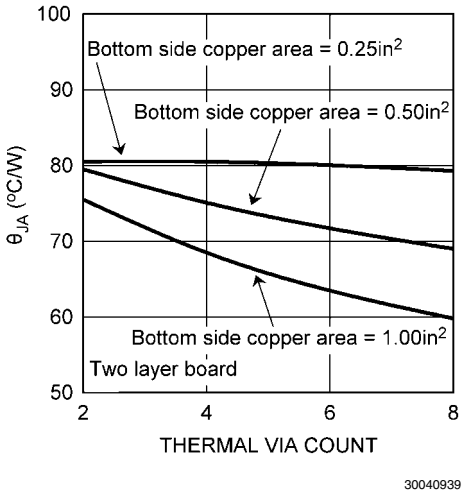


FIGURE 4. θ_{JA} vs Thermal Via Count for the PSOP-8 Package on 2–Layer PCB with Copper Area on Bottom-Side

Figure 5 shows thermal performance for a two layer board with the DAP soldered to copper area on the of the PCB only.

Increasing the copper area soldered to the DAP to 1 square inch of 1 ounce copper, using a dog-bone type layout, will produce a typical θ_{JA} rating of 98°C/W.

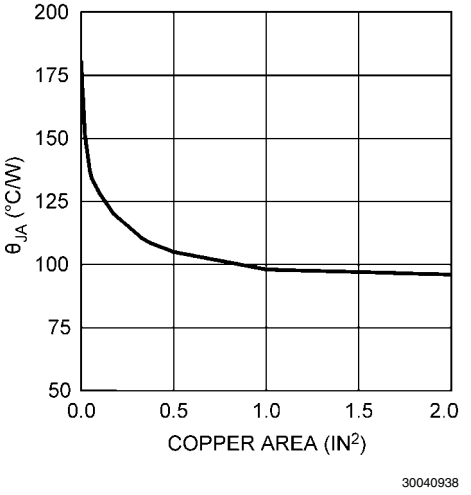
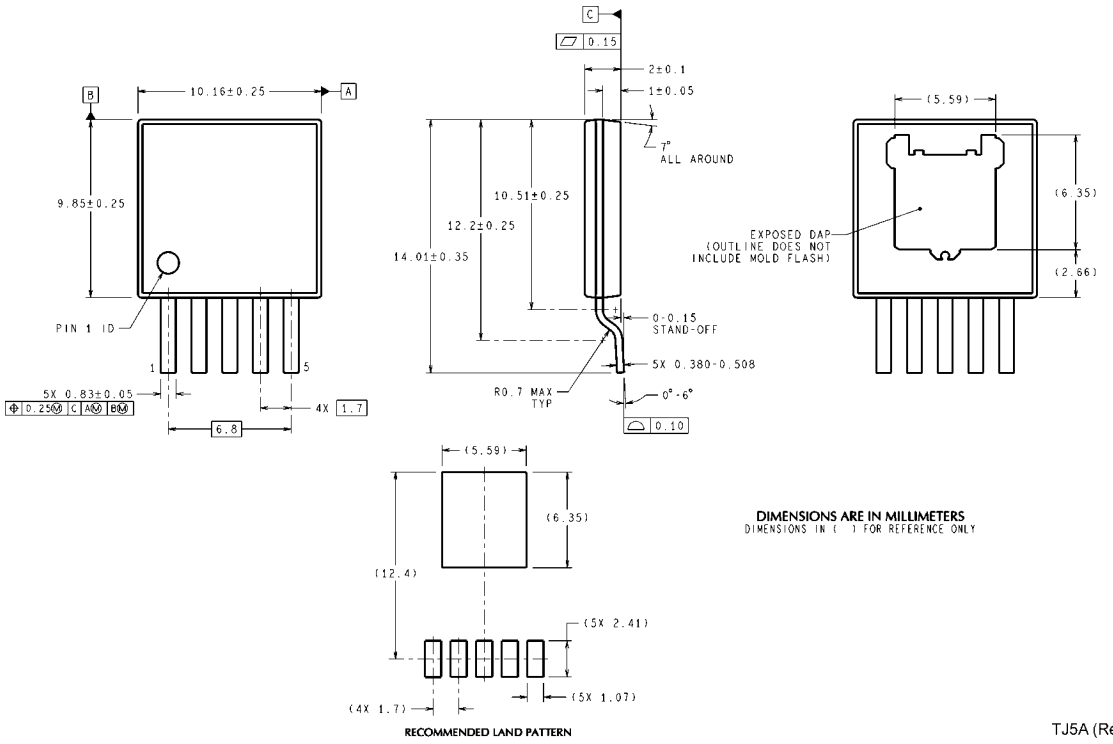


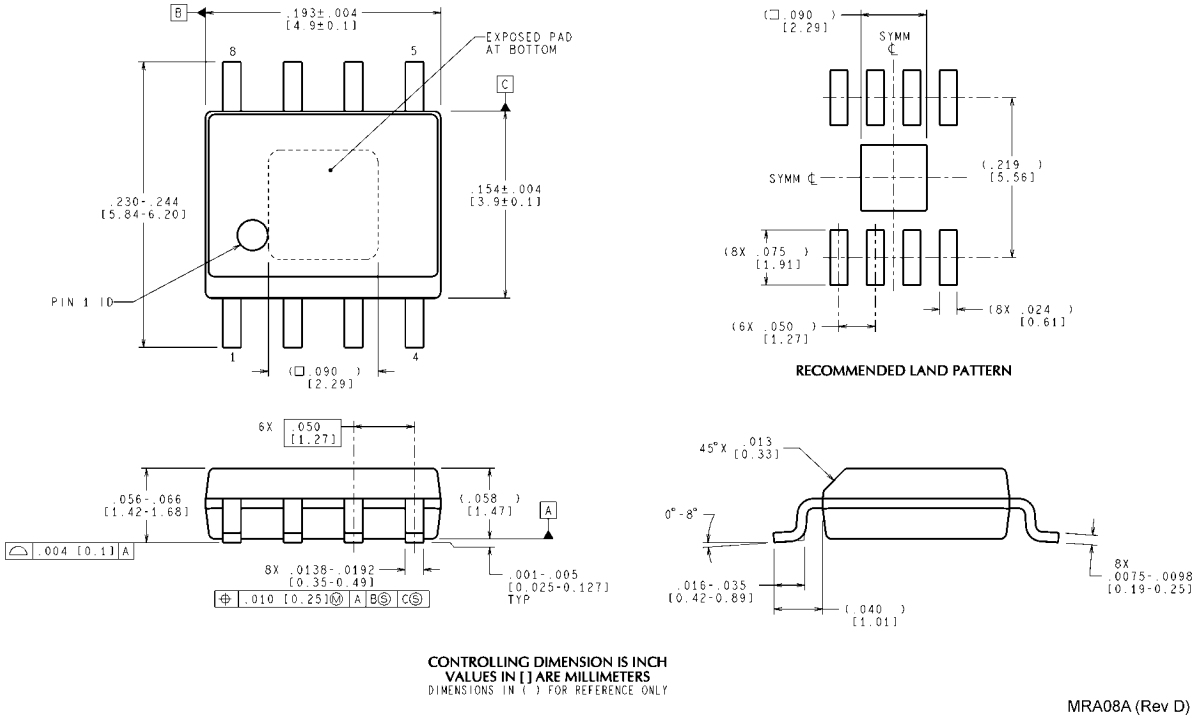
FIGURE 5. θ_{JA} vs Copper Area for the PSOP-8 Package on 2–Layer PCB with Copper Area on Top-Side

Physical Dimensions inches (millimeters) unless otherwise noted



TJ5A (Rev E)

TO-263 THIN, 5 Lead, Molded, 1.7mm Pitch, Surface Mount
NS Package Number TJ5A



MRA08A (Rev D)

PSOP, 8-Lead, Molded, 0.050in Pitch, Surface Mount
NS Package Number MRA08A

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
Wireless (PLL/VCO)	www.national.com/wireless	Analog University®	www.national.com/AU

National Semiconductor Americas Technical Support Center
Email: support@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
English Tel: +44 (0) 870 850 4288

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265