

## 12-stage binary ripple counter

## 74HC/HCT4040

## FEATURES

- Output capability: standard
- $I_{CC}$  category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT4040 are high-speed Si-gate CMOS devices and are pin compatible with "4040" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4040 are 12-stage binary ripple counters with a clock input ( $\overline{CP}$ ), an overriding asynchronous master reset input (MR) and twelve parallel outputs

( $Q_0$  to  $Q_{11}$ ). The counter advances on the HIGH-to-LOW transition of  $\overline{CP}$ .

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of  $\overline{CP}$ .

Each counter stage is a static toggle flip-flop.

## APPLICATIONS

- Frequency dividing circuits
- Time delay circuits
- Control counters

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $\overline{CP}$ to $Q_0$	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	14	16	ns
	$Q_n$ to $Q_{n+1}$		8	8	ns
$f_{max}$	maximum clock frequency		90	79	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1 and 2	20	20	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$

For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

## ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	$Q_0$ to $Q_{11}$	parallel outputs
10	$\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
11	MR	master reset input (active HIGH)
16	$V_{CC}$	positive supply voltage

