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# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT4094**

### **8-stage shift-and-store bus register**

Product specification  
File under Integrated Circuits, IC06

December 1990

## 8-stage shift-and-store bus register

## 74HC/HCT4094

## FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT4094 are high-speed Si-gate CMOS devices and are pin compatible with the “4094” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4094 are 8-stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input (D) to the parallel buffered 3-state outputs (QP<sub>0</sub> to QP<sub>7</sub>). The parallel outputs may be connected directly to common bus lines. Data is shifted on the positive-going clock (CP) transitions.

The data in each shift register stage is transferred to the storage register when the strobe input (STR) is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) signal is HIGH.

Two serial outputs (QS<sub>1</sub> and QS<sub>2</sub>) are available for cascading a number of “4094” devices. Data is available at QS<sub>1</sub> on the positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at QS<sub>2</sub> on the next negative-going clock edge and is for cascading “4094” devices when the clock rise time is slow.

## APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V			
	CP to QS <sub>1</sub>		15	19	ns
	CP to QS <sub>2</sub>		13	18	ns
	CP to QP <sub>n</sub>		20	21	ns
	STR to QP <sub>n</sub>		18	19	ns
f <sub>max</sub>	maximum clock frequency		95	86	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	83	92	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

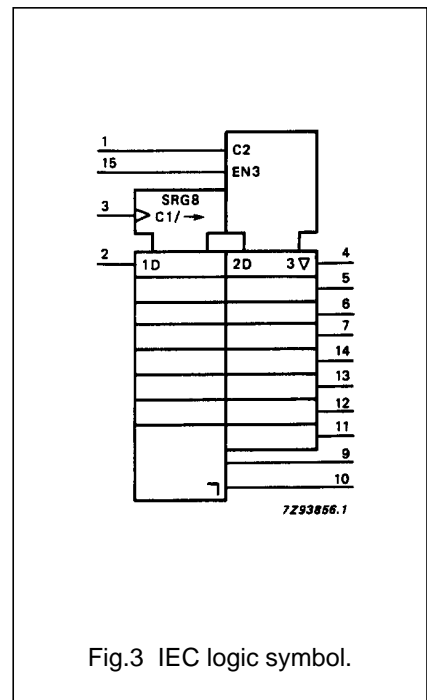
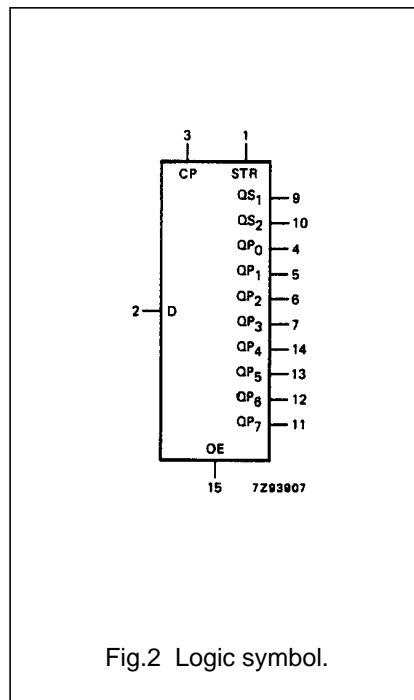
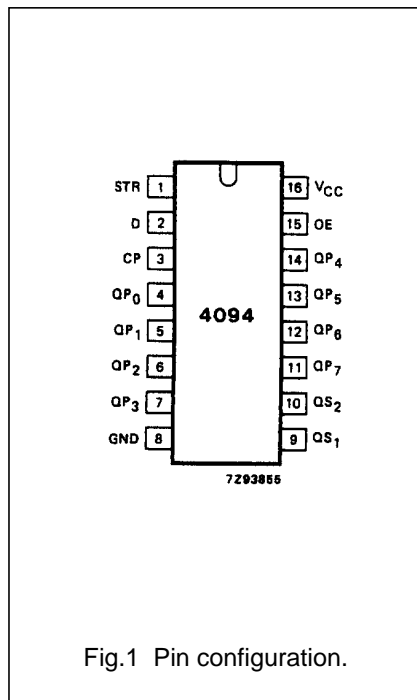
See “74HC/HCT/HCU/HCMOS Logic Package Information”.

# 8-stage shift-and-store bus register

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## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	STR	strobe input
2	D	serial input
3	CP	clock input
4, 5, 6, 7, 14, 13, 12, 11	QP <sub>0</sub> to QP <sub>7</sub>	parallel outputs
8	GND	ground (0 V)
9, 10	QS <sub>1</sub> , QS <sub>2</sub>	serial outputs
15	OE	output enable input
16	V <sub>CC</sub>	positive supply voltage



8-stage shift-and-store bus register

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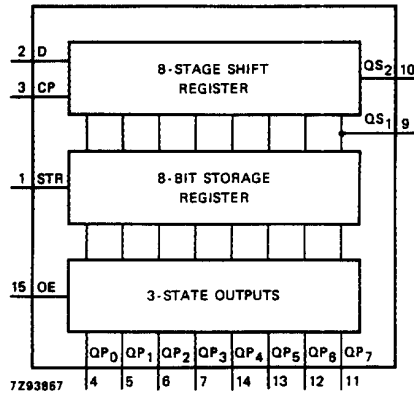


Fig.4 Functional diagram.

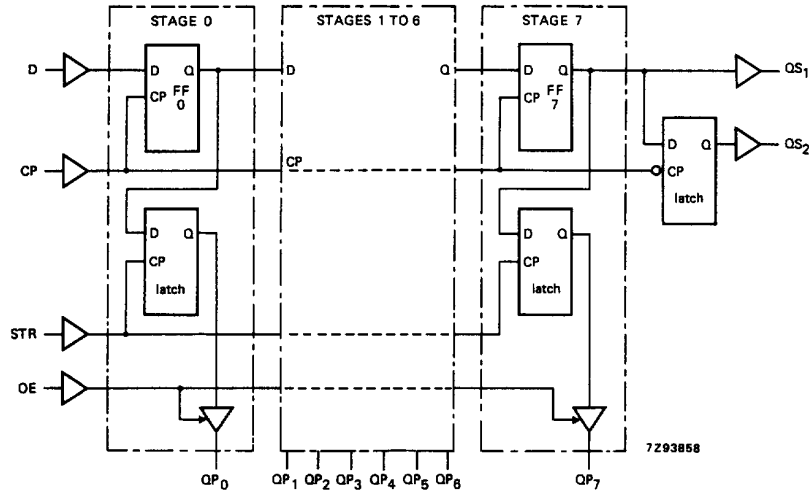


Fig.5 Logic diagram.

# 8-stage shift-and-store bus register

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## FUNCTION TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	OE	STR	D	QP <sub>0</sub>	QP <sub>n</sub>	QS <sub>1</sub>	QS <sub>2</sub>
↑	L	X	X	Z	Z	Q' <sub>6</sub>	NC
↓	L	X	X	Z	Z	NC	QP <sub>7</sub>
↑	H	L	X	NC	NC	Q' <sub>6</sub>	NC
↑	H	H	L	L	QP <sub>n-1</sub>	Q' <sub>6</sub>	NC
↑	H	H	H	H	QP <sub>n-1</sub>	Q' <sub>6</sub>	NC
↓	H	H	H	NC	NC	NC	QP <sub>7</sub>

### Notes

- H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 Z = high impedance OFF-state  
 NC = no change  
 ↑ = LOW-to-HIGH CP transition  
 ↓ = HIGH-to-LOW CP transition  
 Q'<sub>6</sub> = the information in the seventh register stage is transferred to the 8th register stage and QS<sub>n</sub> output at the positive clock edge

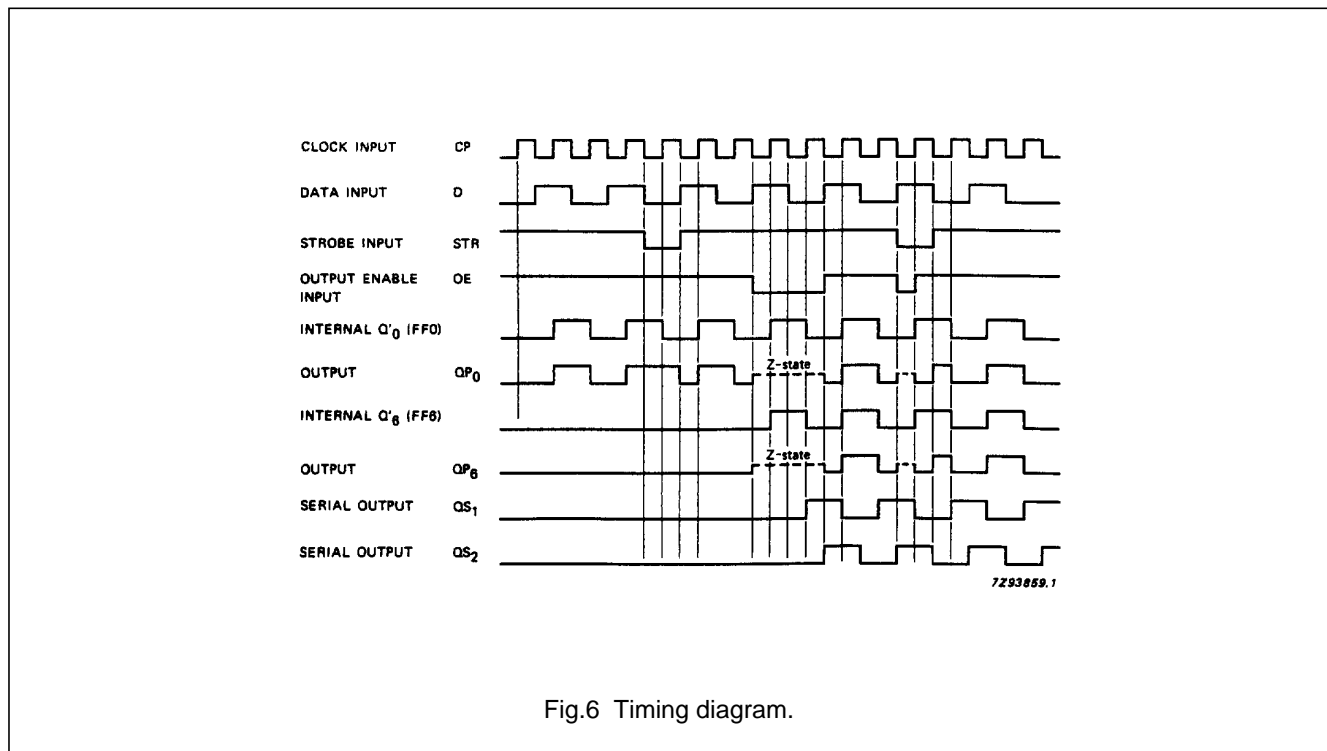


Fig.6 Timing diagram.

## 8-stage shift-and-store bus register

## 74HC/HCT4094

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to QS <sub>1</sub>		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to QS <sub>2</sub>		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to QP <sub>n</sub>		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay STR to QP <sub>n</sub>		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig.8
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to QP <sub>n</sub>		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to QP <sub>n</sub>		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5	Fig.7
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>W</sub>	strobe pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>su</sub>	set-up time D to CP	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.10
t <sub>su</sub>	set-up time CP to STR	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.8

## 8-stage shift-and-store bus register

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SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>h</sub>	hold time D to CP	3	-6		3		3		ns	2.0 4.5 6.0	Fig.10
		3	-2		3		3				
		3	-2		3		3				
t <sub>h</sub>	hold time CP to STR	0	-14		0		0		ns	2.0 4.5 6.0	Fig.8
		0	-5		0		0				
		0	-4		0		0				
f <sub>max</sub>	maximum clock pulse frequency	6.0	28		4.8		4.0		MHz	2.0 4.5 6.0	Fig.7
		30	87		24		20				
		35	103		28		24				

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**8-stage shift-and-store bus register****74HC/HCT4094**

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
OE, CP	1.50
D	0.40
STR	1.00

## 8-stage shift-and-store bus register

## 74HC/HCT4094

**AC CHARACTERISTICS FOR 74HCT**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to QS <sub>1</sub>		23	39		49		59	ns	4.5	Fig.7	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to QS <sub>2</sub>		21	36		45		54	ns	4.5	Fig.7	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to QP <sub>n</sub>		25	43		54		65	ns	4.5	Fig.7	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay STR to QP <sub>n</sub>		22	39		49		59	ns	4.5	Fig.8	
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to QP <sub>n</sub>		20	35		44		53	ns	4.5	Fig.9	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to QP <sub>n</sub>		21	35		44		53	ns	4.5	Fig.9	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.7	
t <sub>W</sub>	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.7	
t <sub>W</sub>	strobe pulse width HIGH	16	5		20		24		ns	4.5	Fig.8	
t <sub>su</sub>	set-up time D to CP	10	4		13		15		ns	4.5	Fig.10	
t <sub>su</sub>	set-up time CP to STR	20	9		25		30		ns	4.5	Fig.8	
t <sub>h</sub>	hold time D to CP	4	0		4		4		ns	4.5	Fig.10	
t <sub>h</sub>	hold time CP to STR	0	-4		0		0		ns	4.5	Fig.8	
f <sub>max</sub>	maximum clock pulse frequency	30	80		24		20		MHz	4.5	Fig.7	

# 8-stage shift-and-store bus register

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## AC WAVEFORMS

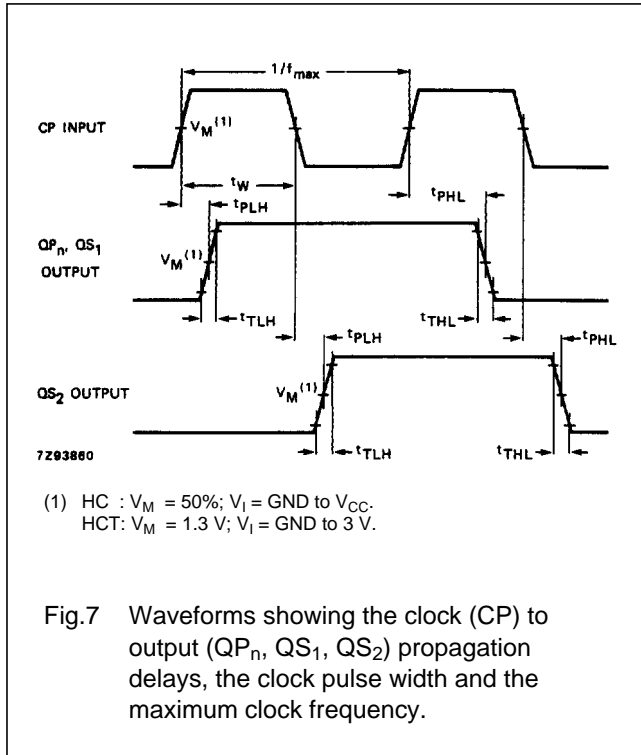


Fig.7 Waveforms showing the clock (CP) to output ( $QP_n$ ,  $QS_1$ ,  $QS_2$ ) propagation delays, the clock pulse width and the maximum clock frequency.

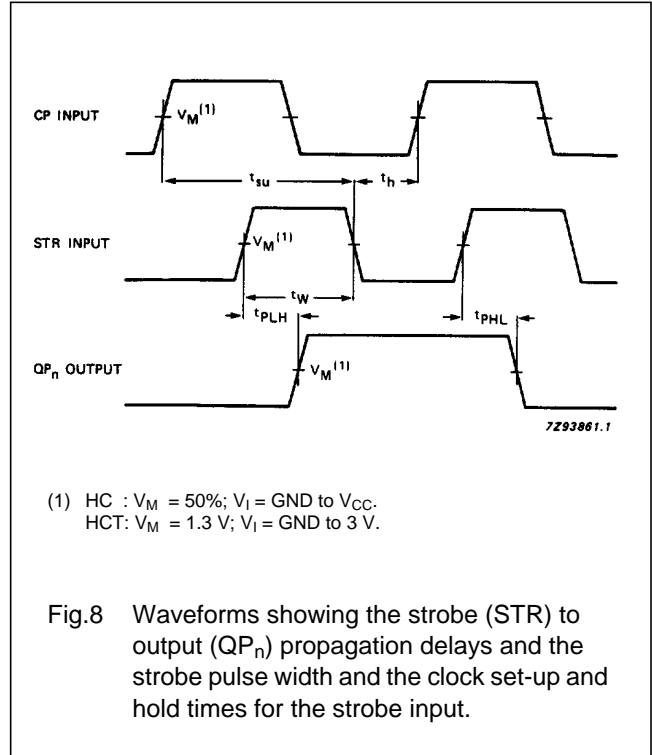


Fig.8 Waveforms showing the strobe (STR) to output ( $QP_n$ ) propagation delays and the strobe pulse width and the clock set-up and hold times for the strobe input.

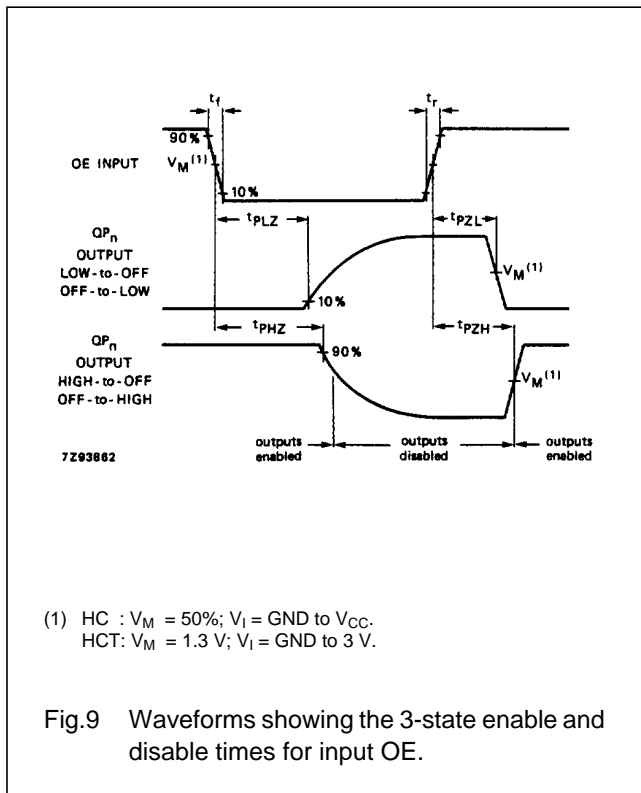


Fig.9 Waveforms showing the 3-state enable and disable times for input OE.

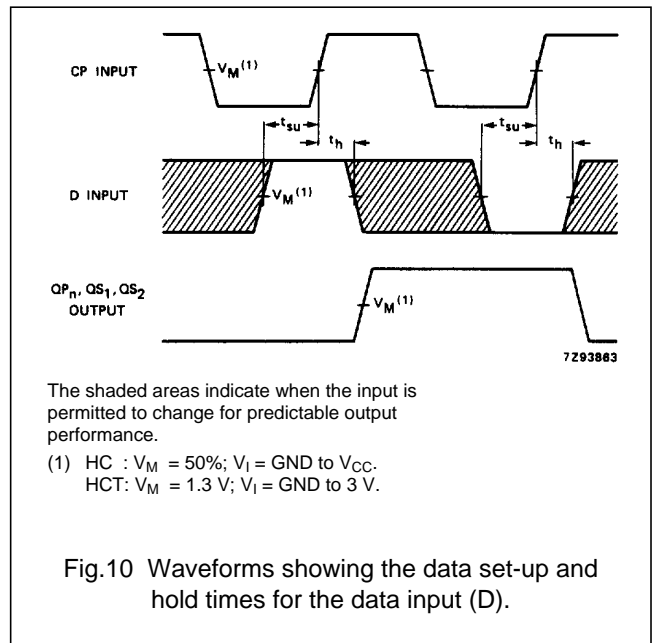


Fig.10 Waveforms showing the data set-up and hold times for the data input (D).

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".