

Octal buffer/line driver; 3-state

74HC/HCT541

FEATURES

- Non-inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

The 74HC/HCT541 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs \overline{OE}_1 and \overline{OE}_2 . A HIGH on \overline{OE}_n causes the outputs to assume a high impedance OFF-state.

The "541" is identical to the "540" but has non-inverting outputs.

GENERAL DESCRIPTION

The 74HC/HCT541 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay A _n to Y _n	C _L = 15 pF; V _{CC} = 5 V	10	12	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	37	39	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

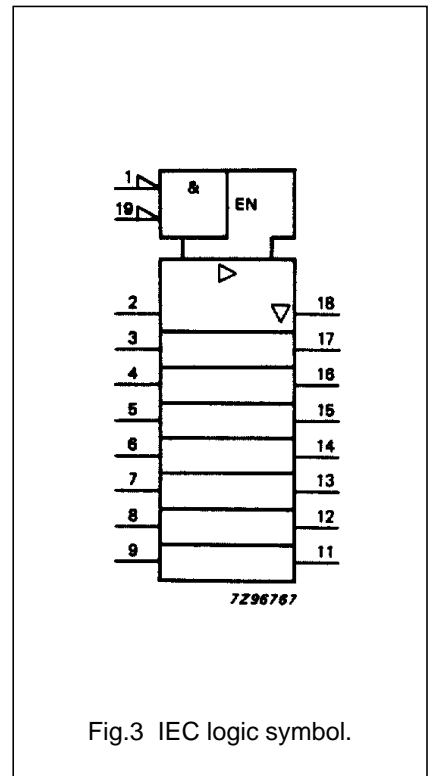
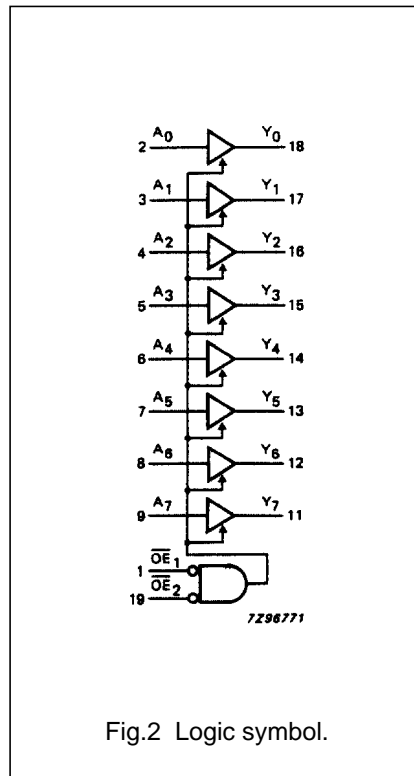
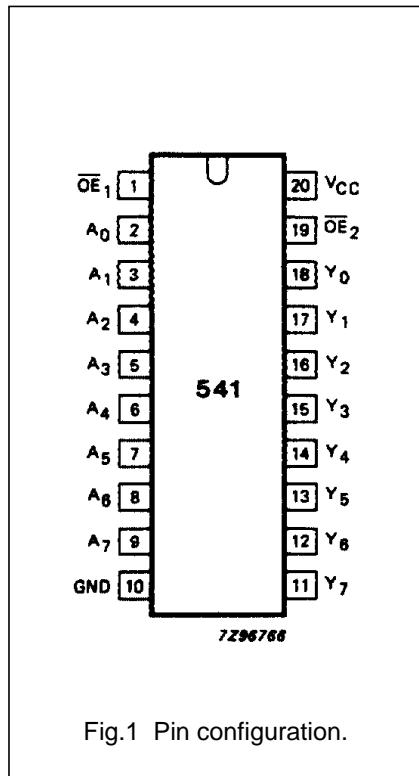
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Octal buffer/line driver; 3-state

74HC/HCT541

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1, \overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₇	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	Y ₀ to Y ₇	bus outputs
20	V _{CC}	positive supply voltage



Octal buffer/line driver; 3-state

74HC/HCT541

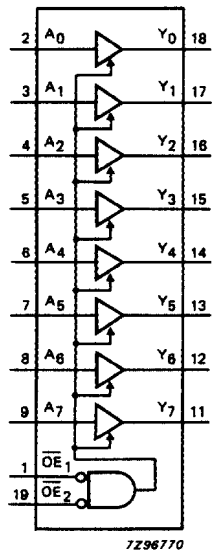


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUT
\overline{OE}_1	\overline{OE}_2	A_n	Y_n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

Notes

1. H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high impedance OFF-state

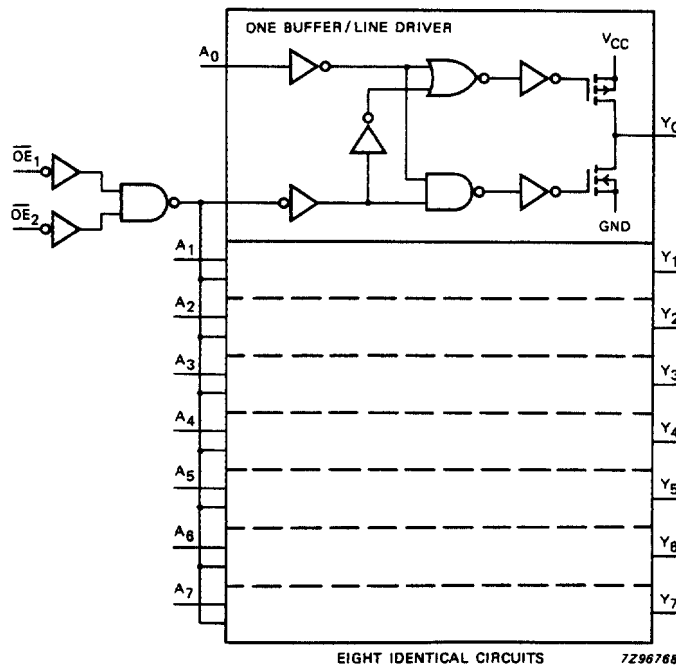


Fig.5 Logic diagram.

Octal buffer/line driver; 3-state

74HC/HCT541

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay A _n to Y _n		33 12 10	115 23 20		145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig.6
t _{PZH} / t _{PZL}	3-state output enable time OE to Y _n		55 20 16	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.7
t _{PHZ} / t _{PLZ}	3-state output disable time OE to Y _n		61 22 18	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.7
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6

Octal buffer/line driver; 3-state

74HC/HCT541

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
\overline{OE}_1	1.50
\overline{OE}_2	1.00
A_n	0.70

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HCT									V _{CC} (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay A _n to Y _n		15	28		35		42	ns	4.5	Fig.6	
t _{PZH} / t _{PZL}	3-state output enable time \overline{OE} to Y _n		21	35		44		53	ns	4.5	Fig.7	
t _{PHZ} / t _{PLZ}	3-state output disable time \overline{OE} to Y _n		21	35		44		53	ns	4.5	Fig.7	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6	