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Jameco Part Number 914806

DATA SHEET

74LVC244A; 74LVCH244A Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

Product specification
Supersedes data of 2003 May 20

2003 Oct 30

Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

74LVC244A; 74LVCH244A

FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when $V_{CC} = 0$ V
- Bushold on all data inputs (74LVCH244A only)
- Complies with JEDEC standard no. 8-1A
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 to $+85$ °C and -40 to $+125$ °C.

DESCRIPTION

The 74LVC244A/74LVCH244A is a high performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC244A/74LVCH244A is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

The 244 is functionally identical to the 240, but the 240 has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay 1An to 1Yn, 2An to 2Yn	$C_L = 50$ pF; $V_{CC} = 3.3$ V	2.8	ns
C_I	input capacitance		4.0	pF
C_{PD}	power dissipation capacitance per buffer	$V_{CC} = 3.3$ V; notes 1 and 2	10	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. The condition is $V_i = \text{GND to } V_{CC}$.

Octal buffer/line driver with 5 V tolerant
inputs/outputs (3-state)

74LVC244A; 74LVCH244A

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC244AD	-40 to +125 °C	20	SO20	plastic	SOT163-1
74LVCH244AD	-40 to +125 °C	20	SO20	plastic	SOT163-1
74LVC244ADB	-40 to +125 °C	20	SSOP20	plastic	SOT339-1
74LVCH244ADB	-40 to +125 °C	20	SSOP20	plastic	SOT339-1
74LVC244APW	-40 to +125 °C	20	TSSOP20	plastic	SOT360-1
74LVCH244APW	-40 to +125 °C	20	TSSOP20	plastic	SOT360-1
74LVC244ABQ	-40 to +125 °C	20	DHVQFN20	plastic	SOT764-1
74LVCH244ABQ	-40 to +125 °C	20	DHVQFN20	plastic	SOT764-1

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
\overline{nOE}	nAn	nYn
L	L	L
L	H	H
H	X	Z

Note

1. H = HIGH voltage level;
 - a) L = LOW voltage level;
 - b) X = don't care;
 - c) Z = high-impedance OFF-state.

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PINNING

PIN	SYMBOL	DESCRIPTION
1	$1\overline{OE}$	output enable input (active LOW)
2	1A0	data input
3	2Y0	bus output
4	1A1	data input
5	2Y1	bus output
6	1A2	data input
7	2Y2	bus output
8	1A3	data input
9	2Y3	bus output
10	GND	ground (0 V)

PIN	SYMBOL	DESCRIPTION
11	2A3	bus input
12	1Y3	bus output
13	2A2	bus input
14	1Y2	bus output
15	2A1	bus input
16	1Y1	bus output
17	2A0	bus input
18	1Y0	bus output
19	$2\overline{OE}$	output enable input (active LOW)
20	V _{CC}	supply voltage

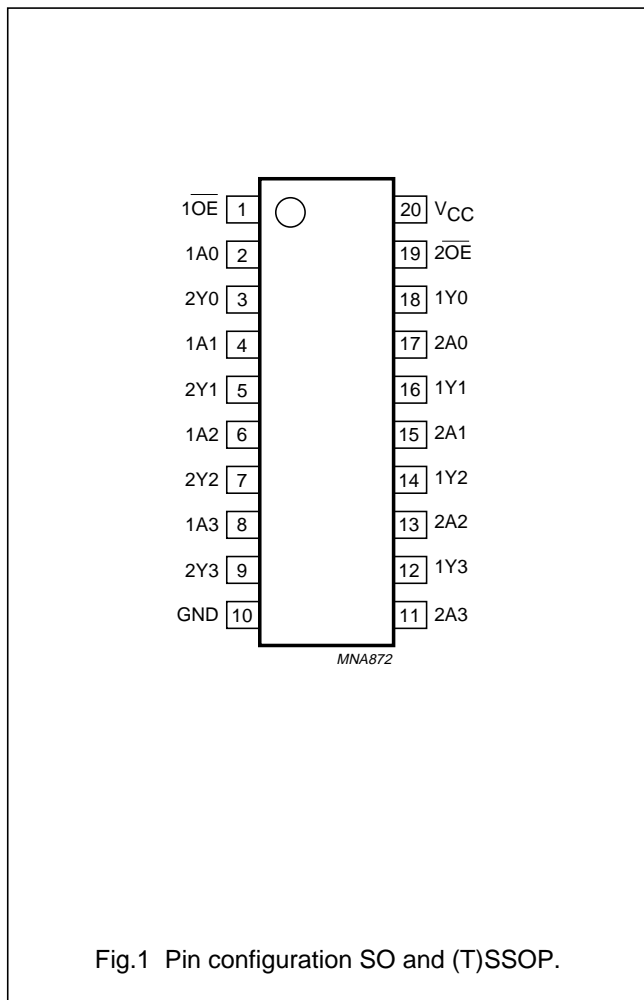
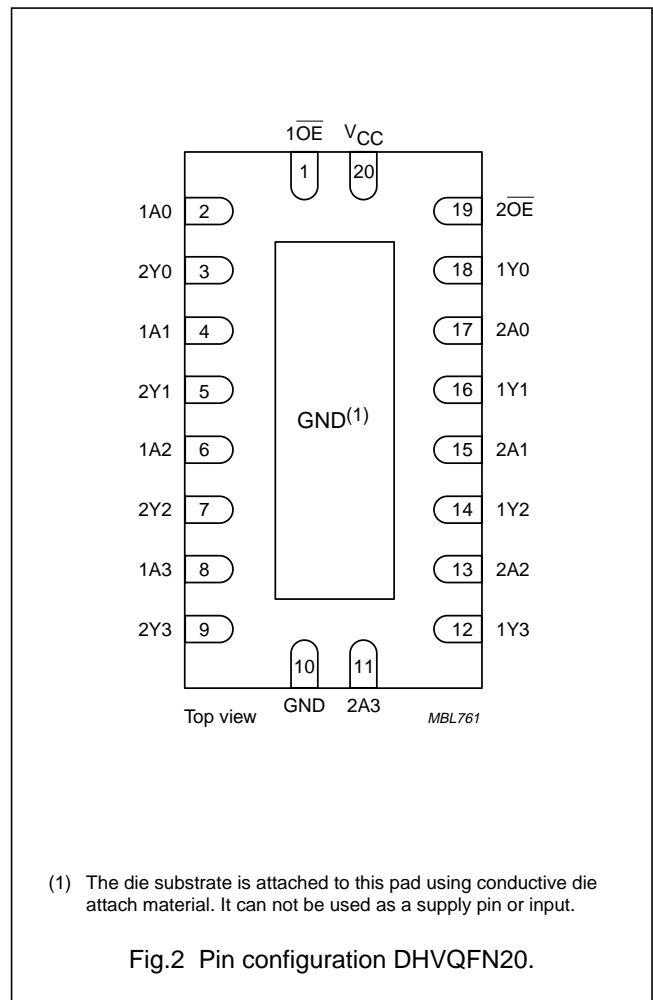


Fig.1 Pin configuration SO and (T)SSOP.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN20.

Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

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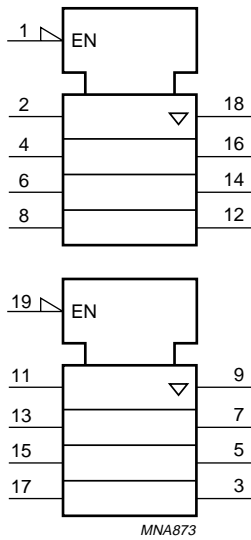


Fig.3 Logic symbol (IEEE/IEC).

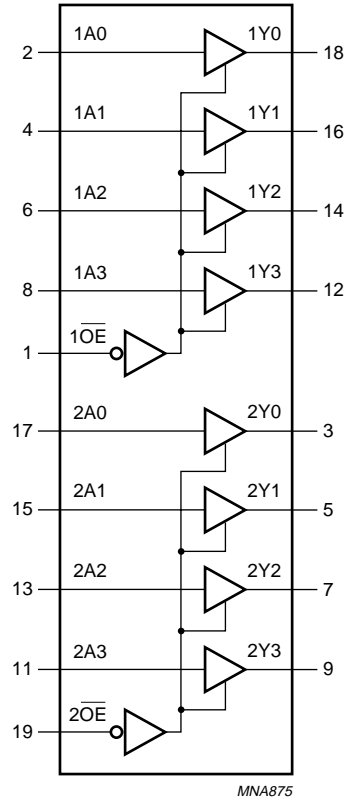


Fig.4 Functional diagram.

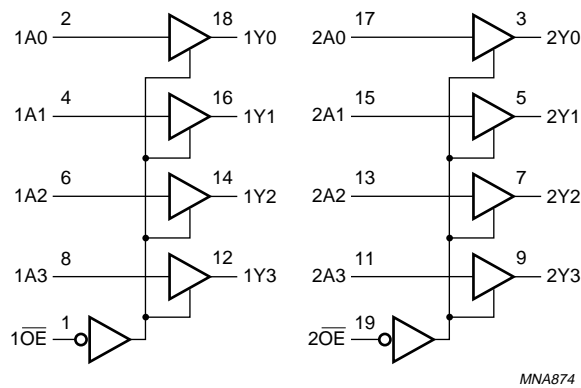


Fig.5 Logic symbol.

Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V _I	input voltage		0	5.5	V
V _O	output voltage	output HIGH or LOW state	0	V _{CC}	V
		output 3-state	0	5.5	V
T _{amb}	operating ambient temperature	in free air	-40	+125	°C
t _r , t _f	input rise and fall times	V _{CC} = 1.2 to 2.7 V	0	20	ns/V
		V _{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input diode current	V _I < 0	-	-50	mA
V _I	input voltage	note 1	-0.5	+6.5	V
I _{OK}	output diode current	V _O > V _{CC} or V _O < 0	-	±50	mA
V _O	output voltage	output HIGH or LOW state; note 1	-0.5	V _{CC} + 0.5	V
		output 3-state; note 1	-0.5	+6.5	V
I _O	output source or sink current	V _O = 0 to V _{CC}	-	±50	mA
I _{CC} , I _{GND}	V _{CC} or GND current		-	±100	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	power dissipation	T _{amb} = -40 to +125 °C; note 2	-	500	mW

Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO20 packages: above 70 °C derate linearly with 8 mW/K.
 - For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.
 - For DHVQFN20 packages: above 60 °C derate linearly with 5.5 mW/K.

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DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +85 °C							
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V _{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	2.7 to 3.6	V _{CC} – 0.2	V _{CC}	–	V
		I _O = –100 µA	2.7	V _{CC} – 0.5	–	–	V
		I _O = –12 mA	3.0	V _{CC} – 0.6	–	–	V
		I _O = –18 mA	3.0	V _{CC} – 0.8	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	2.7 to 3.6	–	GND	0.20	V
		I _O = 100 µA	2.7	–	–	0.40	V
		I _O = 12 mA	3.0	–	–	0.55	V
		I _O = 24 mA					
I _{LI}	input leakage current	V _I = 5.5 V or GND; notes 2	3.6	–	±0.1	±5	µA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; notes 2	3.6	–	0.1	±5	µA
I _{off}	power-off leakage supply current	V _I or V _O = 5.5 V	0.0	–	0.1	±10	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	3.6	–	0.1	10	µA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} – 0.6 V; I _O = 0	2.7 to 3.6	–	5	500	µA
I _{BH(L)}	bushold LOW sustaining current	V _I = 0.8 V; notes 3 and 4	3.0	75	–	–	µA
I _{BH(H)}	bushold HIGH sustaining current	V _I = 2.0 V; notes 3 and 4	3.0	–75	–	–	µA
I _{BH(LO)}	bushold LOW overdrive current	notes 3 and 5	3.6	500	–	–	µA
I _{BH(HO)}	bushold HIGH overdrive current	notes 3 and 5	3.6	–500	–	–	µA

Octal buffer/line driver with 5 V tolerant
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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V _{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	2.7 to 3.6	V _{CC} – 0.3	–	–	V
		I _O = –100 μA	2.7	V _{CC} – 0.65	–	–	V
		I _O = –12 mA	3.0	V _{CC} – 0.75	–	–	V
		I _O = –18 mA	3.0	V _{CC} – 1	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	2.7 to 3.6	–	–	0.3	V
		I _O = 100 μA	2.7	–	–	0.6	V
		I _O = 12 mA	3.0	–	–	0.8	V
		I _O = 24 mA					
I _{LI}	input leakage current	V _I = 5.5 V or GND; notes 2	3.6	–	–	±20	μA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; notes 2	3.6	–	–	±20	μA
I _{off}	power-off leakage supply current	V _I or V _O = 5.5 V	0.0	–	–	±20	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	3.6	–	–	40	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} – 0.6 V; I _O = 0	2.7 to 3.6	–	–	5000	μA
I _{BH(L)}	bushold LOW sustaining current	V _I = 0.8 V; notes 3 and 4	3.0	60	–	–	μA
I _{BH(H)}	bushold HIGH sustaining current	V _I = 2.0 V; notes 3 and 4	3.0	–60	–	–	μA
I _{BH(LO)}	bushold LOW overdrive current	notes 3 and 5	3.6	500	–	–	μA
I _{BH(HO)}	bushold HIGH overdrive current	notes 3 and 5	3.6	–500	–	–	μA

Notes

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. For bushold parts, the bushold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input pin.
3. Valid for data inputs of bushold parts (74LVCH244A) only. For data inputs only, control inputs do not have a bushold circuit.
4. The specified sustaining current at the data inputs do not have a bushold circuit.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.

Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

74LVC244A; 74LVCH244A

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 to +85 °C							
t _{PHL} /t _{PLH}	propagation delay 1An to 1Yn, 2An to 2Yn	see Figs 6 and 8	1.2	–	17.0	–	ns
			2.7	1.5	3.3	6.9	ns
			3.0 to 3.6	1.5	2.8 ⁽¹⁾	5.9	ns
t _{PZH} /t _{PZL}	3-state output enable time 1 $\overline{O\bar{E}}$ to 1Yn, 2 $\overline{O\bar{E}}$ to 2Yn	see Figs 7 and 8	1.2	–	24.0	–	ns
			2.7	1.5	3.3	8.6	ns
			3.0 to 3.6	1.0	3.4 ⁽¹⁾	7.6	ns
t _{PHZ} /t _{PLZ}	3-state output disable time 1 $\overline{O\bar{E}}$ to 1Yn, 2 $\overline{O\bar{E}}$ to 2Yn	see Figs 7 and 8	1.2	–	9.0	–	ns
			2.7	1.5	3.2	6.8	ns
			3.0 to 3.6	1.5	2.9 ⁽¹⁾	5.8	ns
t _{sk(0)}	skew	note 2		–	–	1.0	ns
T_{amb} = -40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay 1An to 1Yn, 2An to 2Yn	see Figs 6 and 8	1.2	–	–	–	ns
			2.7	1.5	–	9.0	ns
			3.0 to 3.6	1.5	–	7.5	ns
t _{PZH} /t _{PZL}	3-state output enable time 1 $\overline{O\bar{E}}$ to 1Yn, 2 $\overline{O\bar{E}}$ to 2Yn	see Figs 7 and 8	1.2	–	–	–	ns
			2.7	1.5	–	11	ns
			3.0 to 3.6	1.0	–	9.5	ns
t _{PHZ} /t _{PLZ}	3-state output disable time 1 $\overline{O\bar{E}}$ to 1Yn, 2 $\overline{O\bar{E}}$ to 2Yn	see Figs 7 and 8	1.2	–	–	–	ns
			2.7	1.5	–	8.5	ns
			3.0 to 3.6	1.5	–	7.5	ns
t _{sk(0)}	skew	note 2		–	–	1.5	ns

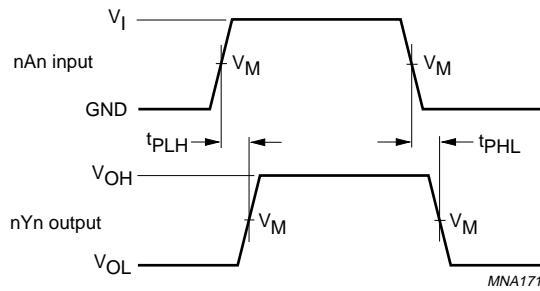
Notes

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

74LVC244A; 74LVCH244A

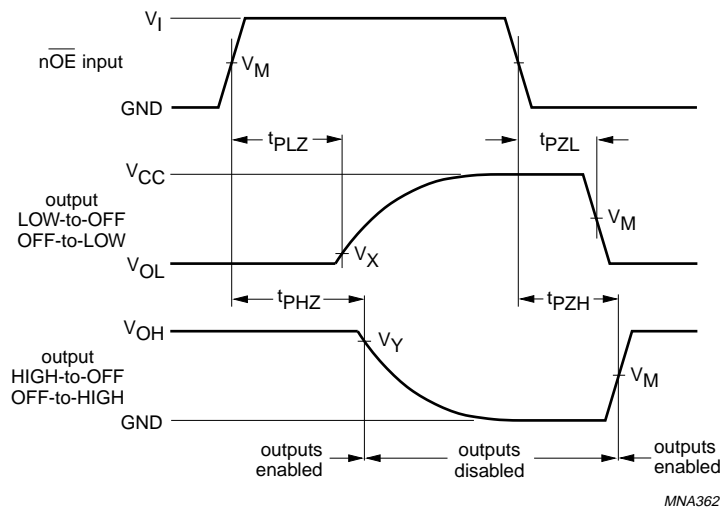
AC WAVEFORMS



$V_M = 1.5\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$.
 $V_M = 0.5V_{CC}$ at $V_{CC} < 2.7\text{ V}$.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 Input nA_n to output nY_n propagation delays.



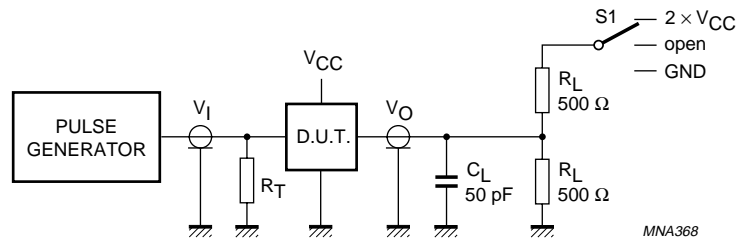
$V_M = 1.5\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$.
 $V_M = 0.5V_{CC}$ at $V_{CC} < 2.7\text{ V}$.
 $V_X = V_{OL} + 0.3\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$;
 $V_X = V_{OL} + 0.1V_{CC}$ at $V_{CC} < 2.7\text{ V}$.
 $V_Y = V_{OH} + 0.3\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$;
 $V_Y = V_{OH} + 0.1V_{CC}$ at $V_{CC} < 2.7\text{ V}$.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 3-state enable and disable times.

Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

74LVC244A; 74LVCH244A



SWITCH POSITION	
TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
<2.7 V	V_{CC}
2.7 to 3.6 V	2.7 V

Definitions for test circuits:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

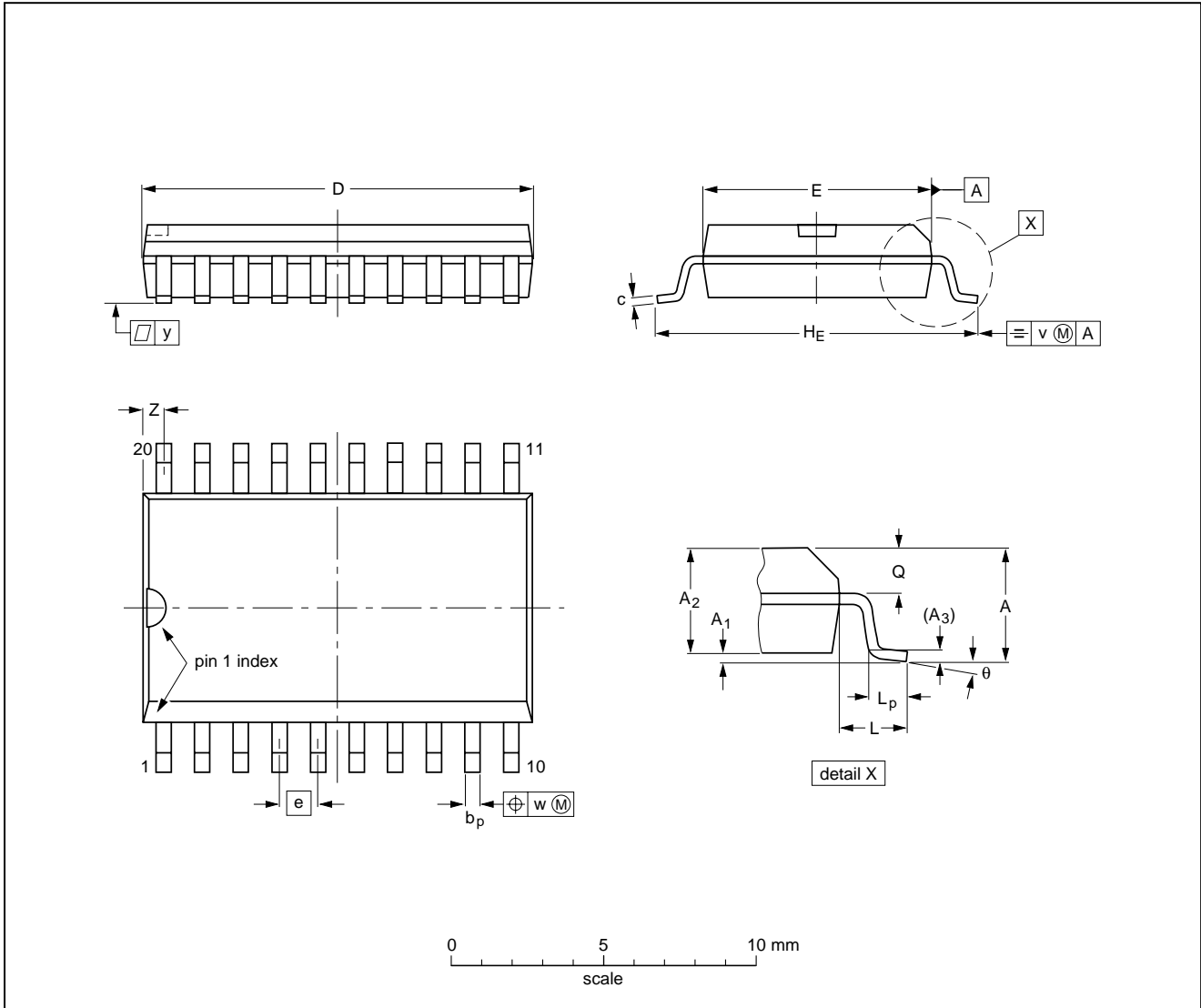
Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

74LVC244A; 74LVCH244A

PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

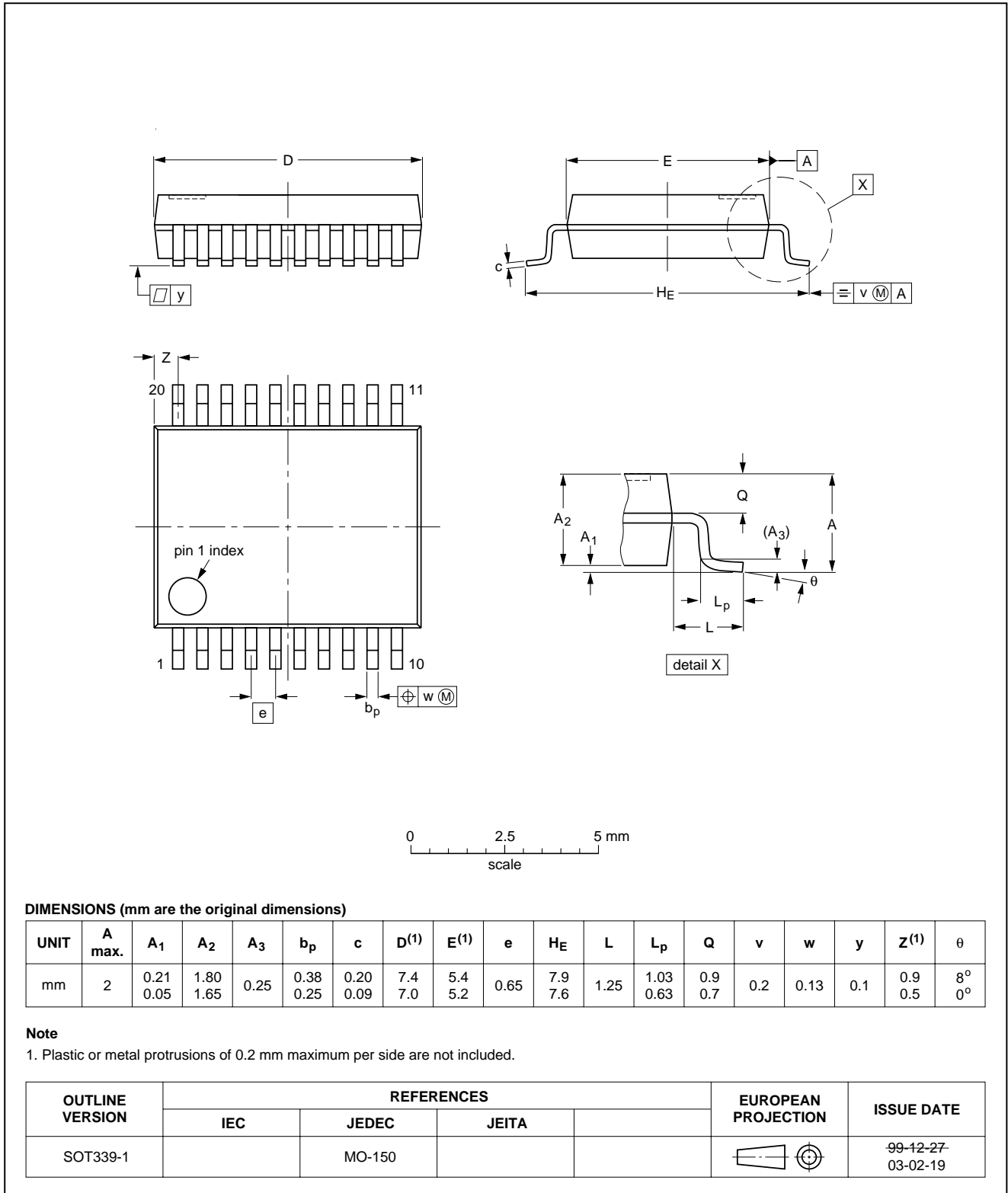
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

74LVC244A; 74LVCH244A

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

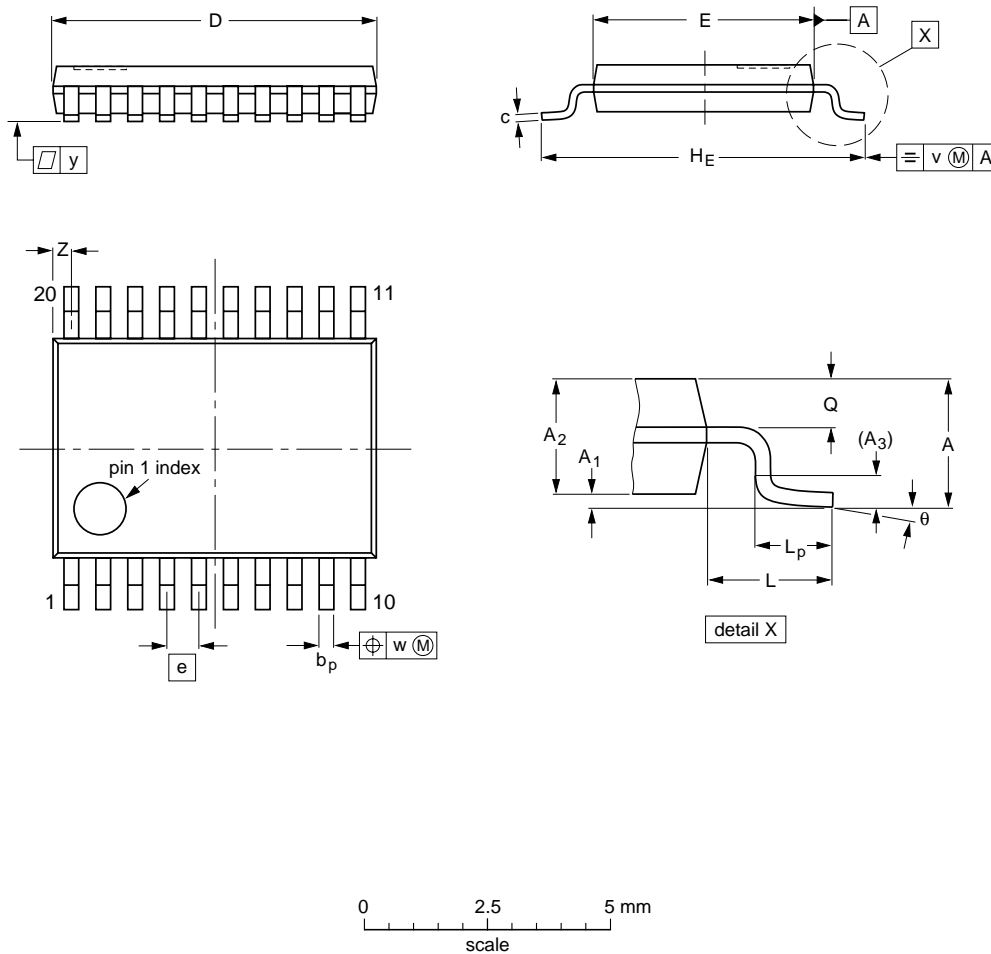


Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

74LVC244A; 74LVCH244A

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

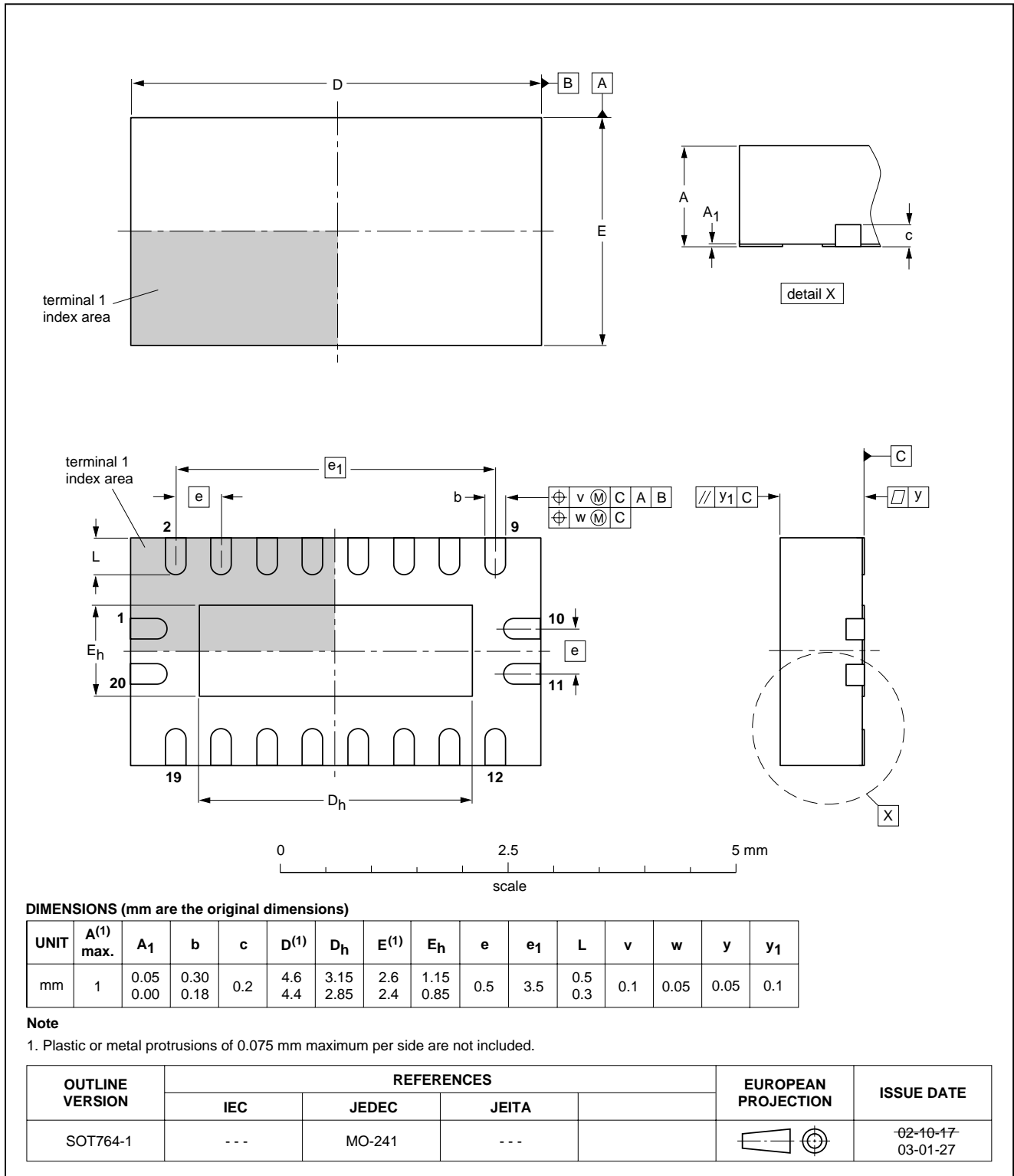
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	IEC	JEDEC	JEITA			
SOT360-1		MO-153				99-12-27 03-02-19

Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

74LVC244A; 74LVCH244A

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

74LVC244A; 74LVCH244A

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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