Freescale Semiconductor
Data Sheet: Technical Data

Document Number MPC5744P
Rev. 5, 08/2015

MPC5744P

MPC5744P Data Sheet

32-bit MCU suitable for ISO26262 ASIL-D chassis and safety applications

Features

- The MPC5744P microcontroller is based on the Power Architecture® developed by Freescale. It targets chassis and safety applications and other applications requiring a high Automotive Safety Integrity Level (ASIL). The MPC5744P is a SafeAssure solution.
- This document provides electrical specifications, pin assignments, and package diagram information for the MPC5744P series of microcontroller units (MCUs). For functional characteristics and the programming model, see the MPC5744P Reference Manual.
- Junction temperature: The upper limit is 150°C or 165°C depending on the device marking.

NXP reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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1 Introduction

1.1 Features

The following table summarizes the features of the MPC5744P.

Table 1. MPC5744P feature summary

Feature	Details
CPU	
Power Architecture	2 x e200z4 in delayed lock step
Architecture	Harvard
Execution speed	0 MHz to 200 MHz (+2% FM)
Embedded FPU	Yes
Core MPU	24 regions
Instruction Set PPC	No
Instruction Set VLE	Yes
Instruction cache	8 KB, EDC
Data cache	4 KB, EDC
Data local memory	64 KB, ECC
System MPU	Yes (16 regions)
Buses	
Core bus	AHB, 32-bit address, 64-bit data, e2e ECC
Internal periphery bus	32-bit address, 32-bit data
Crossbar	
Master x slave ports	4 x 5
Memory—see Table 2 for additional details	
Code/data flash memory	**2.5 MB**, ECC, RWW
Data flash memory	Supported with RWW
SRAM	**384 KB**, ECC
Overlay access to SRAM from Flash Memory Controller	Yes
Modules	
Interrupt controller	32 interrupt priority levels, 16 SW programmable interrupts
PIT	1 module with 4 channels
System Timer Module (STM)	1 module with 4 channels
Software Watchdog Timer (SWT)	Yes
eDMA	32 channels, in delayed lock step
FlexRay	1 module with 64 message buffer, dual channel
FlexCAN	3 modules with 64 message buffer
LINFlexD (UART and LIN with DMA support)	2 modules

Table continues on the next page...

Table 1. MPC5744P feature summary (continued)

Feature	Details
Clockout	Yes
Fault Control and Collection Unit (FCCU)	Yes
Cross Triggering Unit (CTU)	2 modules
eTimer	3 modules with 6 channels
FlexPWM	2 modules with 4 x (2+1) channels
Analog-to-digital converter (ADC)	4 modules with 12-bit ADC, each with 16 channels (25 external channels including shared channels plus internal channels)
Sine-wave generator (SGEN)	32 point
SPI	4 modules As many as 8 chip selects
CRC Unit	Yes
SENT	2 modules with 2 channels
Interprocessor serial link interface (SIPI)	Yes
Junction temperature sensor	Yes (replicated module)
Digital I/Os	≥ 16
Peripheral register protection	Yes
Ethernet	Yes
Error Injection Module (EIM)	Yes
Supply	
Device Power Supply	3.3 V with external ballast transistor 3.3 V with external 1.25 V low drop-out (LDO) regulator
ADC Analog Reference voltage	3.15 V to 5.5 V
Clocking	
Phase Lock Loop (PLL)	1 x PLL and 1 coupled FMPLL
Internal RC Oscillator	16 MHz
External Crystal Oscillator	8 MHz to 40 MHz
Low power modes	
HALT and STOP	Yes
Debug	
Nexus	Level 3+, MDO and Aurora interface
Package	
LQFP	144 pins, 0.5 mm pitch, 20 mm x 20 mm outline
MAPBGA	257 MAPBGA, 0.8 mm pitch, 14 mm x 14 mm outline
Temperature	
Temperature range (junction)	-40°C to +150°C, option for 165°C
Ambient temperature range (LQFP)	-40°C to +125°C, 135°C option (with 165°C junction option)
Ambient temperature range (BGA)	-40°C to +125°C, 135°C option (with 165°C junction option)

Table 2. Flash memory and SRAM sizes of MPC5744P, MPC5743P, MPC5742P, and MPC5741P

Part number	Flash memory	SRAM
MPC5744P	2.5 MB	384 KB
MPC5743P	2.0 MB	256 KB
MPC5742P	1.5 MB	192 KB
MPC5741P	1.0 MB	128 KB

1.2 Block Diagram

The following figure is a top-level diagram that shows the functional organization of the system.

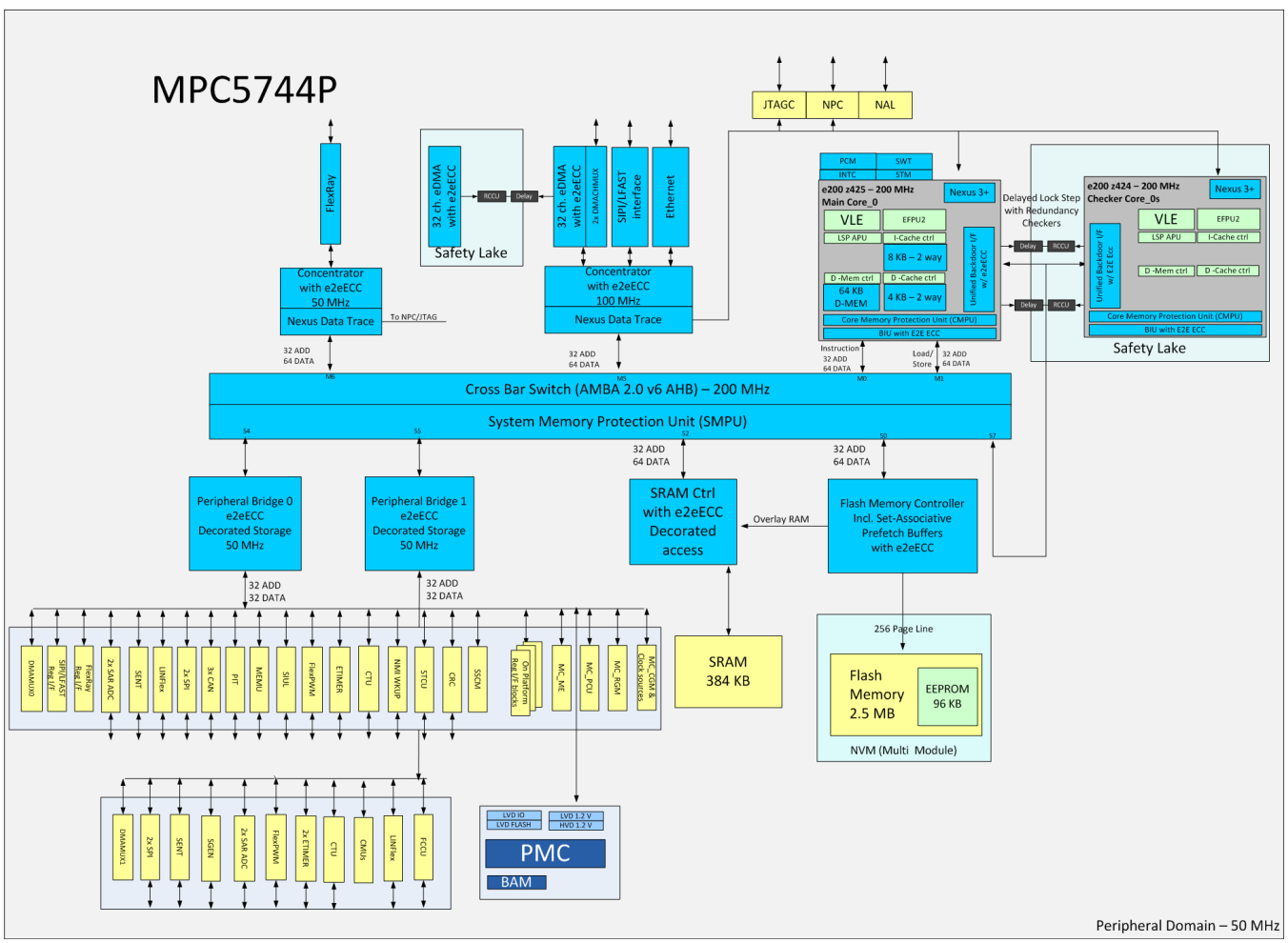


Figure 1. System Block Diagram

2 Pinouts

2.1 Package pinouts and ballmap

The following figures show the LQFP pinout and the BGA ballmap.

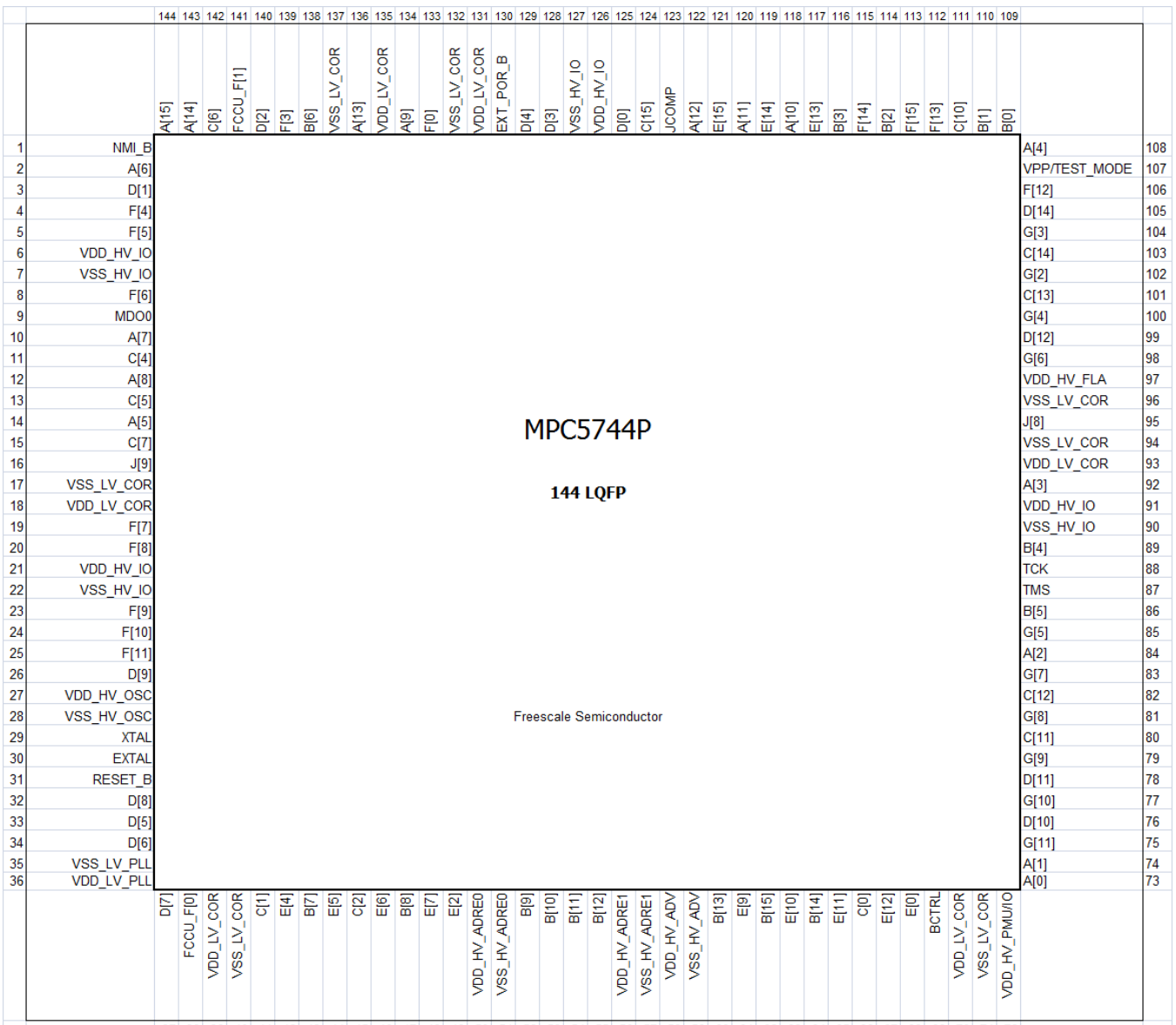
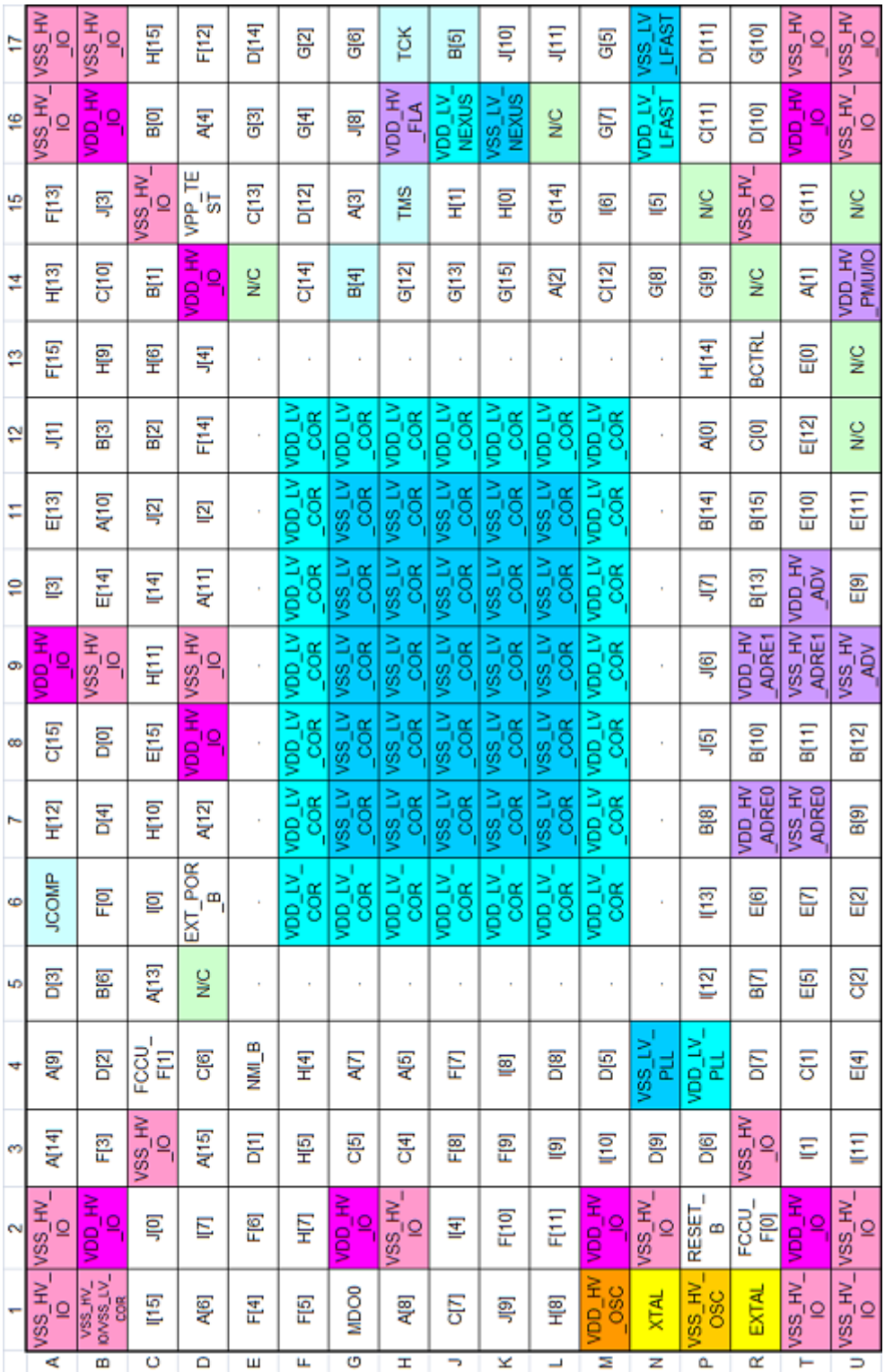


Figure 2. 144LQFP pinout



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS_HV_IO	VSS_HV_IO	A[14]	A[9]	D[3]	JCOMP	H[12]	C[15]	VDD_HV_IO	I[3]	E[13]	J[1]	F[15]	H[13]	F[13]	VSS_HV_IO	VSS_HV_IO
B	VSS_HV_IO/VSS_LV_COR	VDD_HV_IO	F[3]	D[2]	B[6]	F[0]	D[4]	D[0]	VSS_HV_IO	E[14]	A[10]	B[3]	H[9]	C[10]	J[3]	VDD_HV_IO	VSS_HV_IO
C	I[15]	J[0]	VSS_HV_IO	FCCU_F[1]	A[13]	I[0]	H[10]	E[15]	H[11]	I[14]	J[2]	B[2]	H[6]	B[1]	VSS_HV_IO	B[0]	H[15]
D	A[6]	I[7]	A[15]	C[6]	N/C	EXT_POR_B	A[12]	VDD_HV_IO	VSS_HV_IO	A[11]	I[2]	F[14]	J[4]	VDD_HV_IO	VPP_TEST	A[4]	F[12]
E	F[4]	F[6]	D[1]	NMI_B	.	.	.	.	.	.	.	.	.	N/C	C[13]	G[3]	D[14]
F	F[5]	H[7]	H[5]	H[4]	.	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	.	C[14]	D[12]	G[4]	G[2]
G	MDO0	VDD_HV_IO	C[5]	A[7]	.	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	.	B[4]	A[3]	J[8]	G[6]
H	A[8]	VSS_HV_IO	C[4]	A[5]	.	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	.	G[12]	TMS	VDD_HV_FLA	TCK
J	C[7]	I[4]	F[8]	F[7]	.	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	.	G[13]	H[1]	VDD_LV_NEXUS	B[5]
K	J[9]	F[10]	F[9]	I[8]	.	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	.	G[15]	H[0]	VSS_LV_NEXUS	J[10]
L	H[8]	F[11]	I[9]	D[8]	.	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	.	A[2]	G[14]	N/C	J[11]
M	VDD_HV_OSC	VDD_HV_IO	I[10]	D[5]	.	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	.	C[12]	I[6]	G[7]	G[5]
N	XTAL	VSS_HV_IO	D[9]	VSS_LV_PLL	.	.	.	.	.	.	.	.	.	G[8]	I[5]	VDD_LV_LFAST	VSS_LV_LFAST
P	VSS_HV_OSC	RESET_B	D[6]	VDD_LV_PLL	I[12]	I[13]	B[8]	J[5]	J[6]	J[7]	B[14]	A[0]	H[14]	G[9]	N/C	C[11]	D[11]
R	EXTAL	FCCU_F[0]	VSS_HV_IO	D[7]	B[7]	E[6]	VDD_HV_ADRE0	B[10]	VDD_HV_ADRE1	B[13]	B[15]	C[0]	BCTRL	N/C	VSS_HV_IO	D[10]	G[10]
T	VSS_HV_IO	VDD_HV_IO	I[1]	C[1]	E[5]	E[7]	VSS_HV_ADRE0	B[11]	VSS_HV_ADRE1	VDD_HV_ADV	E[10]	E[12]	E[0]	A[1]	G[11]	VDD_HV_IO	VSS_HV_IO
U	VSS_HV_IO	VSS_HV_IO	I[11]	E[4]	C[2]	E[2]	B[9]	B[12]	VSS_HV_ADV	E[9]	E[11]	N/C	N/C	VDD_HV_PMU/IO	N/C	VSS_HV_IO	VSS_HV_IO

Figure 3. 257MAPBGA ballmap

2.2 Pin/ball descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the device. Note that this section is under development.

2.2.1 Pin/ball startup and reset states

The following table provides startup state and reset state information for device pins/balls.

The startup state and subsequent states of the following pins/balls cannot be configured by the user:

- JCOMP
- TMS
- TCK
- XTAL/EXTAL
- FCCU_F[0] and FCCU_F[1]
- EXT_POR_B
- RESET_B

The user can configure the state after reset of the following pins/balls by programming the applicable MSCRs/IMCRs:

- GPIOs
- Analog inputs
- TDI
- TDO
- NMI_B
- FAB
- ABS[0]
- ABS[2]

Table 3. Pin/ball startup and reset states

Pin/ball	Startup state[1]	State during reset	State after reset	144LQFP	257MAPBGA
GPIOs	hi-z	hi-z	hi-z	Note[2]	Note[2]
Analog inputs[3]	hi-z	hi-z	hi-z	Note[2]	Note[2]
JCOMP (TRST)	hi-z	input, weak pull-down	input, weak pull-down	Note[4]	Note[4]
TDI	hi-z	input, weak pull-up	input, weak pull-up	Note[4]	Note[4]
TDO	hi-z	output, hi-z	output, hi-z	Note[4]	Note[4]
TMS[5]	hi-z	input, weak pull-up	input, weak pull-up	Note[4]	Note[4]

Table continues on the next page...

Table 3. Pin/ball startup and reset states (continued)

Pin/ball	Startup state[1]	State during reset	State after reset	144LQFP	257MAPBGA
TCK[5]	hi-z	input, weak pull-up	input, weak pull-up	Note[4]	Note[4]
XTAL/EXTAL	hi-z	hi-z	hi-z	Note[4]	Note[4]
FCCU_F[0][5]	hi-z	input, hi-z	output/input, hi-z	38	R2
FCCU_F[1][5]	hi-z	input, hi-z	output/input, hi-z	141	C4
EXT_POR_B	hi-z	input, weak pull-down	input, weak pull-down	Note[4]	Note[4]
RESET_B	hi-z	input, weak pull-down	input, weak pull-down	Note[4]	Note[4]
NMI_B	hi-z	input, weak pull-up	input,weak pull-up	Note[4]	Note[4]
FAB	hi-z	input, weak pull-down	input, weak pull-down	Note[4]	Note[4]
ABS[2]	hi-z	input, weak pull-down	input, weak pull-down	Note[4]	Note[4]
ABS[0]	hi-z	input, weak pull-down	input, weak pull-down	Note[4]	Note[4]

1. Startup state is exited when the core and high-voltage supplies reach minimum levels.
2. See Generic pins/balls.
3. Not all non-supply or reference pins on the device are explicitly defined in this table.
4. See System pins/balls.
5. This pin/ball is dedicated to and directly connected to a peripheral module pin.

2.2.2 Power supply and reference voltage pins/balls

Table 4. Power supply and reference voltage pins/balls

Supply			Package	
Symbol	**Type**	**Description**	**144LQFP**	**257MAPBGA**
$V_{DD\_LV\_COR}$	Power	Low voltage power Supply	18	F6
			39	F7
			70	F8
			93	F9
			131	F10
			135	F11
				F12
				G6
				G12
				H6
				H12
				J6
				J12
				K6
				K12
				L6
				L12
				M6
				M7
				M8
				M9
				M10
				M11
				M12

Table continues on the next page...

Table 4. Power supply and reference voltage pins/balls (continued)

Supply			Package	
Symbol	**Type**	**Description**	**144LQFP**	**257MAPBGA**
$V_{SS\_LV\_COR}$	Ground	Low voltage ground. PLL Ground is also connected to low voltage ground for core logic on 144LQFP (pin 35).	17	B1
			35	G7
			40	G8
			71	G9
			94	G10
			96	G11
			132	H7
			137	H8
				H9
				H10
				H11
				J7
				J8
				J9
				J10
				J11
				K7
				K8
				K9
				K10
				K11
				L7
				L8
				L9
				L10
				L11
$V_{DD\_LV\_PLL}$	Power	PLL low voltage Supply	36	P4
$V_{SS\_LV\_PLL}$	Ground	PLL low voltage Ground	35	N4

Table continues on the next page...

Table 4. Power supply and reference voltage pins/balls (continued)

Supply			Package	
Symbol	**Type**	**Description**	**144LQFP**	**257MAPBGA**
$V_{DD\_HV\_IO}$	Power	High voltage Power Supply for I/O	6	A9
			21	B2
			72	B16
			91	D8
			126	D14
				G2
				M2
				T2
				T16
				U14
$V_{SS\_HV\_IO}$	Ground	High voltage Ground Supply for I/O	7	A1
			22	A2
			90	A16
			127	A17
				B1
				B9
				B17
				C3
				C15
				D9
				H2
				N2
				R3
				R15
				T1
				T17
				U1
				U2
				U16
				U17
$V_{DD\_HV\_PMU}$ $V_{DD\_HV\_PMU\_AUX}$	Power	PMU high voltage Supply	72	U14
$V_{DD\_HV\_OSC}$	Power	Power Supply for the oscillator	27	M1
$V_{SS\_HV\_OSC}$	Ground	Ground Supply for the oscillator	28	P1
$V_{DD\_HV\_FLA}$	Power	Power Supply and decoupling pin for flash memory	97	H16
$V_{DD\_HV\_ADV}$	Power	High voltage Supply for ADC, TSENS, SGEN (3.3 V)	58	T10
$V_{SS\_HV\_ADV}$	Ground	High voltage Ground for ADC	59	U9

Table continues on the next page...

Table 4. Power supply and reference voltage pins/balls (continued)

Supply			Package	
Symbol	**Type**	**Description**	**144LQFP**	**257MAPBGA**
$V_{DD\_HV\_ADRE0}$	Supply	High voltage Supply for digital portion of ADC pads Voltage reference of ADC/TSENS High voltage Supply for ADC0 pads and shared pads for ADC0/1.	50	R7
$V_{SS\_HV\_ADRE0}$	Ground	High voltage Ground for digital portion of ADC pads Voltage reference Ground of ADC/TSENS High voltage Ground for ADC0 pads and shared pads for ADC0/1.	51	T7
$V_{DD\_HV\_ADRE1}$	Supply	High voltage Supply for digital portion of ADC pads Voltage reference of ADC/TSENS High voltage Supply for ADC1 pads, shared pads for ADC1/3, and shared pads for ADC2/3.	56	R9
$V_{SS\_HV\_ADRE1}$	Ground	High voltage Ground for digital portion of ADC pads Voltage reference Ground of ADC/TSENS High voltage Ground for ADC1 pads, shared pads for ADC1/3, and shared pads for ADC2/3.	57	T9
$V_{DD\_LV\_LFAST}$	Supply	LFAST PLL low voltage Supply	—	N16
$V_{SS\_LV\_LFAST}$	Ground	LFAST PLL low voltage Ground	—	N17
$V_{DD\_LV\_NEXUS}$	Supply	Aurora LVDS Supply	—	J16
$V_{SS\_LV\_NEXUS}$	Ground	Aurora LVDS Ground	—	K16

2.2.3 System pins/balls

The following table contains information about system pin functions for the devices.

Table 5. System pins/balls

Symbol	Type	Description	144LQFP	257MAPBGA
NMI_B	Input	Non-maskable Interrupt	1	E4
XTAL	Input	Crystal Oscillator/External Clock Input	29	N1
EXTAL	Input	Input of the oscillator amplifier circuit	30	R1
RESET_B	Input	Functional Reset	31	P2
EXT_POR_B	Input	External Power On Reset	130	D6
VPP_TEST[1]	Input	SoC Test Mode	107	D15
JCOMP	Input	JTAGC, JTAG Compliance Enable	123	A6
TCK	Input	JTAGC, Test Clock Input	88	H17
TMS	Input	JTAGC, Test Mode Select	87	H15
TDO	Output	JTAGC, Test Data Out	89	G14

Table continues on the next page...

Table 5. System pins/balls (continued)

Symbol	Type	Description	144LQFP	257MAPBGA
TDI	Input	JTAGC, Test Data Input	86	J17
MDO[0]	Output	NEXUS, Message data out pins; reflects the state of the internal power on reset signal until RESET is negated	9	G1
MDO[3:1]	Output	NEXUS, Message data out pins	4,5,8	E1, F1, E2
EVTO	Output	NEXUS, Event Out Pin	24	K2
EVTI	Input	NEXUS, Event In Pin	25	L2
MCKO	Output	NEXUS, Message clock out pin	19	J4
MSEO[1:0]	Output	NEXUS, Message Start/End out pin	20, 23	J3, K3
RDY_B	Output	NEXUS, Read/Write Transfer completed	—	J2
			16	K1
BCTRL	Output	Base control signal of external npn ballast	69	R13
J[11], J[10]	--	FSL Factory Test[2]	—	L17, K17

1. VPP_TEST must be connected to ground.
2. Do not connect on the board.

2.2.4 LVDS pins/balls

The following tables contain information on LVDS pin functions for the devices.

Table 6. SIPI LFAST LVDS pin descriptions

Functional block	Port pin	Signal	Signal description	Direction	257MAPBGA
SIPI LFAST[1, 2]	I[5]	SIPI_TXN	Interprocessor Bus LFAST, LVDS Transmit Negative Terminal	O	N15
	C[12][3]	SIPI_TXP	Interprocessor Bus LFAST, LVDS Transmit Positive Terminal	O	M14
	I[6]	SIPI_RXN	Interprocessor Bus LFAST, LVDS Receive Negative Terminal	I	M15
	G[7][3]	SIPI_RXP	Interprocessor Bus LFAST, LVDS Receive Positive Terminal	I	M16

1. DRCLK and TCK/DRCLK usage for SIPI LFAST are described in the reference manual's SIPI LFAST chapters.
2. For the MSCR SSS value of the port pin, see Table 8.
3. The 144LQFP package has G[7] and C[12] but no SIPI LFAST functionality.

CAUTION

SIPI LFAST pins are muxed with GPIOs. Do not use GPIO and SIPI LFAST functionality in parallel.

Table 7. Aurora LVDS pin descriptions

Functional block	Pad	Signal	Signal description	Direction	257MAPBGA[1]
Nexus Aurora High Speed Trace	G[12]	TX0P	Nexus Aurora High Speed Trace Lane 0, LVDS Positive Terminal	O	H14
	G[13]	TX0N	Nexus Aurora High Speed Trace Lane 0, LVDS Negative Terminal	O	J14
	G[14]	TX1P	Nexus Aurora High Speed Trace Lane 1, LVDS Positive Terminal	O	L15
	G[15]	TX1N	Nexus Aurora High Speed Trace Lane 1, LVDS Negative Terminal	O	K14
	H[0]	CLKP	Nexus Aurora High Speed Trace Clock, LVDS Positive Terminal	I	K15
	H[1]	CLKN	Nexus Aurora High Speed Trace Clock, LVDS Negative Terminal	I	J15

1. Nexus Aurora High Speed Trace is available only on the 257MAPBGA.

2.2.5 Generic pins/balls

The I/O signal descriptions for the device are in the following table. It contains the port definition, multiplexing, direction, pad type, and package pin/ball numbers for each I/O pin on the device.

MSCR registers are used for alternative (ALT) mode selection and programming of pad control options.

IMCR registers are used to configure input muxing by peripheral. See Peripheral input muxing for details.

Table 8. Pin muxing

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
A[0]	MSCR[0]	0000 (Default)[2]	GPIO[0]	SIUL2-GPIO[0]	General Purpose IO A[0]	I/O	73	P12
		0001	ETC0	eTimer_0	eTimer_0 Input/Output Data Channel 0	I/O		
		0010	SCK	DSPI2	DSPI 2 Serial Clock (output)	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[48]	0001	SCK	DSPI2	DSPI 2 Serial Clock (input)	I/O		
	IMCR[59]	0010	ETC0	eTimer_0	eTimer_0 Input Data Channel 0	I/O		
	IMCR[173]	0001	REQ0	SIUL2	SIUL2 External Interrupt 0	I		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
A[1]	MSCR[1]	0000 (Default)	GPIO[1]	SIUL2-GPIO[1]	General Purpose IO A[1]	I/O	74	T14
		0001	ETC1	eTimer_0	eTimer_0 Input/Output Data Channel 1	I/O		
		0010	SOUT	DSPI2	DSPI 2 Serial Data Out	O		
		0011-1111	—	Reserved	—	—		
	IMCR[60]	0010	ETC1	eTimer_0	eTimer_0 Input Data Channel 1	I/O		
	IMCR[174]	0001	REQ1	SIUL2	SIUL2 External Interrupt Source 1	I		
A[2]	MSCR[2]	0000 (Default)	GPIO[2]	SIUL2-GPIO[2]	General Purpose IO A[2]	I/O	84	L14
		0001	ETC2	eTimer_0	eTimer_0 Input/Output Data Channel 2	I/O		
		0010	—	Reserved	—	—		
		0011	A3	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[169]	0000 (Default)	ABS0	MC_RGM	RGM external boot mode 1	I		
	IMCR[47]	0010	SIN	DSPI2	DSPI 2 Serial Data Input	I		
	IMCR[61]	0010	ETC2	eTimer_0	eTimer_0 Input Data Channel 2	I/O		
	IMCR[97]	0001	A3	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 3	I/O		
	IMCR[175]	0001	REQ2	SIUL2	SIUL2 External Interrupt Source 2	I		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
A[3]	MSCR[3]	0000 (Default)	GPIO[3]	SIUL2-GPIO[3]	General Purpose IO A[3]	I/O	92	G15
		0001	ETC3	eTimer_0	eTimer_0 Input/Output Data Channel 3	I/O		
		0010	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I/O		
		0011	B3	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[171]	0000 (Default)	ABS2	MC_RGM	RGM external boot mode 2	I		
	IMCR[62]	0010	ETC3	eTimer_0	eTimer_0 Input Data Channel 3	I/O		
	IMCR[49]	0001	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I/O		
	IMCR[98]	0001	B3	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 3	I/O		
	IMCR[176]	0001	REQ3	SIUL2	SIUL2 External Interrupt Source 3	I		
A[4]	MSCR[4]	0000 (Default)	GPIO[4]	SIUL2-GPIO[4]	General Purpose IO A[4]	I/O	108	D16
		0001	ETC0	eTimer_1	eTimer_1 Input/Output Data Channel 0	I/O		
		0010	CS1	DSPI2	DSPI 2 Peripheral Chip Select 1	O		
		0011	ETC4	eTimer_0	eTimer_0 Input/Output Data Channel 4	I/O		
		0100	A2	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 2	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[112]	0001	A2	FlexPWM_1	FlexPWM_1 Channel A Input 2	I/O		
	IMCR[177]	0001	REQ4	SIUL2	SIUL2 External Interrupt Source 4	I		
	IMCR[172]	0000 (Default)	FAB	MC_RGM	RGM Force Alternate Boot Mode	I		
	IMCR[65]	0001	ETC0	eTimer_1	eTimer_1 Input Data Channel 0	I/O		
	IMCR[63]	0011	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
A[5]	MSCR[5]	0000 (Default)	GPIO[5]	SIUL2-GPIO[5]	General Purpose IO A[5]	I/O	14	H4
		0001	CS0	DSPI1	DSPI 1 Peripheral Chip Select 0	I/O		
		0010	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O		
		0011	CS7	DSPI0	DSPI 0 Peripheral Chip Select 7	O		
		0100-1111	—	Reserved	—	—		
	IMCR[70]	0001	ETC5	eTimer_1	eTimer_1 Input Data Channel 5	I/O		
	IMCR[178]	0001	REQ5	SIUL2	SIUL2 External Interrupt Source 5	I		
A[6]	MSCR[6]	0000 (Default)	GPIO[6]	SIUL2-GPIO[6]	General Purpose IO A[6]	I/O	2	D1
		0001	SCK	DSPI1	DSPI 1 Serial Clock (output)	I/O		
		0010	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[73]	0001	ETC2	eTimer_2	eTimer_2 Input Data Channel 2	I/O		
	IMCR[179]	0001	REQ6	SIUL2	SIUL2 External Interrupt Source 6	I		
A[7]	MSCR[7]	0000 (Default)	GPIO[7]	SIUL2-GPIO[7]	General Purpose IO A[7]	I/O	10	G4
		0001	SOUT	DSPI1	DSPI 1 Serial Data Out	O		
		0010	ETC3	eTimer_2	eTimer_2 Input/Output Data Channel 3	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[74]	0001	ETC3	eTimer_2	eTimer_2 Input Data Channel 3	I/O		
	IMCR[180]	0001	REQ7	SIUL2	SIUL2 External Interrupt Source 7	I		
A[8]	MSCR[8]	0000 (Default)	GPIO[8]	SIUL2-GPIO[8]	General Purpose IO A[8]	I/O	12	H1
		0001	—	Reserved	—	—		
		0010	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[44]	0001	SIN	DSPI1	DSPI 1 Serial Data Input	I		
	IMCR[75]	0001	ETC4	eTimer_2	eTimer_2 Input Data Channel 4	I/O		
	IMCR[181]	0001	REQ8	SIUL2	SIUL2 External Interrupt Source 8	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
A[9]	MSCR[9]	0000 (Default)	GPIO[9]	SIUL2-GPIO[9]	General Purpose IO A[9]	I/O	134	A4
		0001	CS1	DSPI2	DSPI 2 Peripheral Chip Select 1	O		
		0010	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O		
		0011	B3	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[76]	0001	ETC5	eTimer_2	eTimer_2 Input Data Channel 5	I/O		
	IMCR[98]	0010	B3	FlexPWM_0	FlexPWM_0 Channel B Input 3	I/O		
	IMCR[83]	0001	FAULT0	FlexPWM_0	FlexPWM_0 Fault Input 0	I		
	IMCR[206]	0011	SENT_RX[1]	SENT_0	SENT 0 Receiver channel 1	I		
A[10]	MSCR[10]	0000 (Default)	GPIO[10]	SIUL2-GPIO[10]	General Purpose IO A[10]	I/O	118	B11
		0001	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I/O		
		0010	B0	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 0	I/O		
		0011	X2	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 2	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[49]	0010	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I/O		
	IMCR[89]	0001	B0	FlexPWM_0	FlexPWM_0 Channel B Input 0	I/O		
	IMCR[96]	0001	X2	FlexPWM_0	FlexPWM_0 Auxiliary Input 2	I/O		
	IMCR[182]	0001	REQ9	SIUL2	SIUL2 External Interrupt Source 9	I		
	IMCR[214]	0011	SENT_RX[1]	SENT_1	SENT 1 Receiver channel 1	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
A[11]	MSCR[11]	0000 (Default)	GPIO[11]	SIUL2-GPIO[11]	General Purpose IO A[11]	I/O	120	D10
		0001	SCK	DSPI2	DSPI 2 Serial Clock (output)	I/O		
		0010	A0	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 0	I/O		
		0011	A2	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 2	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[48]	0010	SCK	DSPI2	DSPI 2 Serial Clock (input)	I/O		
	IMCR[88]	0001	A0	FlexPWM_0	FlexPWM_0 Channel A Input 0	I/O		
	IMCR[94]	0001	A2	FlexPWM_0	FlexPWM_0 Channel A Input 2	I/O		
	IMCR[183]	0001	REQ10	SIUL2	SIUL2 External Interrupt Source 10	I		
A[12]	MSCR[12]	0000 (Default)	GPIO[12]	SIUL2-GPIO[12]	General Purpose IO A[12]	I/O	122	D7
		0001	SOUT	DSPI2	DSPI 2 Serial Data Out	O		
		0010	A2	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 2	I/O		
		0011	B2	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 2	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[94]	0010	A2	FlexPWM_0	FlexPWM_0 Channel A Input 2	I/O		
	IMCR[95]	0001	B2	FlexPWM_0	FlexPWM_0 Channel B Input 2	I/O		
	IMCR[184]	0001	REQ11	SIUL2	SIUL2 External Interrupt Source 11	I		
A[13]	MSCR[13]	0000 (Default)	GPIO[13]	SIUL2-GPIO[13]	General Purpose IO A[13]	I/O	136	C5
		0001	—	Reserved	—	—		
		0010	B2	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 2	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[83]	0010	FAULT0	FlexPWM_0	FlexPWM_0 Fault Input 0	I		
	IMCR[95]	0010	B2	FlexPWM_0	FlexPWM_0 Channel B Input 2	I/O		
	IMCR[47]	0001	SIN	DSPI2	DSPI 2 Serial Data Input	I		
	IMCR[185]	0001	REQ12	SIUL2	SIUL2 External Interrupt Source 12	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
A[14]	MSCR[14]	0000 (Default)	GPIO[14]	SIUL2-GPIO[14]	General Purpose IO A[14]	I/O	143	A3
		0001	TXD	CAN1	CAN 1 Transmit Pin	O		
		0010	ETC4	eTimer_1	eTimer_1 Input/Output Data Channel 4	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[69]	0001	ETC4	eTimer_1	eTimer_1 Input Data Channel 4	I/O		
	IMCR[186]	0001	REQ13	SIUL2	SIUL2 External Interrupt Source 13	I		
A[15]	MSCR[15]	0000 (Default)	GPIO[15]	SIUL2-GPIO[15]	General Purpose IO A[15]	I/O	144	D3
		0001	—	Reserved	—	—		
		0010	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[32]	0001	RXD	CAN0	CAN 0 Receive Pin	I		
	IMCR[33]	0001	RXD	CAN1	CAN 1 Receive Pin	I		
	IMCR[70]	0010	ETC5	eTimer_1	eTimer_1 Input Data Channel 5	I/O		
	IMCR[187]	0001	REQ14	SIUL2	SIUL2 External Interrupt Source 14	I		
B[0]	MSCR[16]	0000 (Default)	GPIO[16]	SIUL2-GPIO[16]	General Purpose IO B[0]	I/O	109	C16
		0001	TXD	CAN0	CAN 0 Transmit Pin	O		
		0010	ETC2	eTimer_1	eTimer_1 Input/Output Data Channel 2	I/O		
		0011	DEBUG0	SSCM	SSCM Debug Output 0	O		
		0100-1111	—	Reserved	—	—		
	IMCR[67]	0001	ETC2	eTimer_1	eTimer_1 Input Data Channel 2	I/O		
	IMCR[188]	0001	REQ15	SIUL2	SIUL2 External Interrupt Source 15	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
B[1]	MSCR[17]	0000 (Default)	GPIO[17]	SIUL2-GPIO[17]	General Purpose IO B[1]	I/O	110	C14
		0001	—	Reserved	—	—		
		0010	ETC3	eTimer_1	eTimer_1 Input/Output Data Channel 3	I/O		
		0011	DEBUG1	SSCM	SSCM Debug Output 1	O		
		0100-1111	—	Reserved	—	—		
	IMCR[32]	0010	RXD	CAN0	CAN 0 Receive Pin	I		
	IMCR[33]	0010	RXD	CAN1	CAN 1 Receive Pin	I		
	IMCR[68]	0001	ETC3	eTimer_1	eTimer_1 Input Data Channel 3	I/O		
	IMCR[189]	0001	REQ16	SIUL2	SIUL2 External Interrupt Source 16	I		
B[2]	MSCR[18]	0000 (Default)	GPIO[18]	SIUL2-GPIO[18]	General Purpose IO B[2]	I/O	114	C12
		0001	TXD	LIN0	LINFlexD 0 Transmit Pin	O		
		0010	CS4	DSPI0	DSPI 0 Peripheral Chip Select 4	O		
		0011	DEBUG2	SSCM	SSCM Debug Output 2	O		
		0100-1111	—	Reserved	—	—		
	IMCR[190]	0001	REQ17	SIUL2	SIUL2 External Interrupt Source 17	I		
B[3]	MSCR[19]	0000 (Default)	GPIO[19]	SIUL2-GPIO[19]	General Purpose IO B[3]	I/O	116	B12
		0001	—	Reserved	—	—		
		0010	CS5	DSPI0	DSPI 0 Peripheral Chip Select 5	O		
		0011	DEBUG3	SSCM	SSCM Debug Output 3	O		
		0100-1111	—	Reserved	—	—		
	IMCR[165]	0001	RXD	LIN0	LIN 0 Receive Pin	I		
B[4]	MSCR[20]	0	GPIO[20]	SIUL2-GPIO[20]	General Purpose IO B[4]	I/O	89	G14
		0001 (Default)	TDO	NPC_HNDSHK	NPC_HNDSHK Test Data Out (TDO)	O		
		0010-1111	—	Reserved	—	—		
B[5]	MSCR[21]	0000 (Default)	GPIO[21]	SIUL2-GPIO[21]	JTAGC Test Data In (TDI)[3] General Purpose IO B[5]	I/O	86	J17
		0001	CS7	DSPI0	DSPI 0 Peripheral Chip Select 7	O		
		0010-1111	—	Reserved	—	—		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
B[6]	MSCR[22]	0000 (Default)	GPIO[22]	SIUL2-GPIO[22]	General Purpose IO B[6]	I/O	138	B5
		0001	CLK_OUT	MC_CGM	CGM Clock out for off-chip use and observation	O		
		0010	CS2	DSPI2	DSPI 2 Peripheral Chip Select 2	O		
		0011-1111	—	Reserved	—	—		
	IMCR[191]	0001	REQ18	SIUL2	SIUL2 External Interrupt Source 18	I		
B[7]	MSCR[23]	0000 (Default)	GPI[23][4] ADC0_AN[0]	SIUL2-GPI[23]	General Purpose Input B[7]	I	43	R5
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[165]	0010	RXD	LIN0	LIN 0 Receive Pin	I		
B[8]	MSCR[24]	0	GPI[24][4] ADC0_AN[1]	SIUL2-GPI[24]	General Purpose Input B[8]	I	47	P7
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[64]	0001	ETC5	eTimer_0	eTimer_0 Input Data Channel 5	I/O		
B[9]	MSCR[25]	0000 (Default)	GPI[25][4] ADC0_ADC1_AN[11]	SIUL2-GPI[25]	General Purpose Input B[9]	I	52	U7
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
B[10]	MSCR[26]	0000 (Default)	GPI[26][4] ADC0_ADC1_AN[12]	SIUL2-GPI[26]	General Purpose Input B[10]	I	53	R8
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
B[11]	MSCR[27]	0000 (Default)	GPI[27][4] ADC0_ADC1_AN[13]	SIUL2-GPI[27]	General Purpose Input B[11]	I	54	T8
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
B[12]	MSCR[28]	0000 (Default)	GPI[28][4] ADC0_ADC1_AN[14]	SIUL2-GPI[28]	General Purpose Input B[12]	I	55	U8
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
B[13]	MSCR[29]	0000 (Default)	GPI[29][4] ADC1_AN[0]	SIUL2-GPI[29]	General Purpose Input B[13]	I	60	R10
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[166]	0001	RXD	LIN1	LIN 1 Receive Pin	I		
B[14]	MSCR[30]	0000 (Default)	GPI[30][4] ADC1_AN[1]	SIUL2-GPI[30]	General Purpose Input B[14]	I	64	P11
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[63]	0001	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I/O		
	IMCR[192]	0001	REQ19	SIUL2	SIUL2 External Interrupt Source 19	I		
B[15]	MSCR[31]	0000 (Default)	GPI[31][4] ADC1_AN[2]	SIUL2-GPI[31]	General Purpose Input B[15]	I	62	R11
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[193]	0001	REQ20	SIUL2	SIUL2 External Interrupt Source 20	I		
C[0]	MSCR[32]	0000 (Default)	GPI[32][4] ADC1_AN[3]	SIUL2-GPI[32]	General Purpose Input C[0]	I	66	R12
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[1]	MSCR[33]	0000 (Default)	GPI[33][4] ADC0_AN[2]	SIUL2-GPI[33]	General Purpose Input C[1]	I	41	T4
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[2]	MSCR[34]	0000 (Default)	GPI[34][4] ADC0_AN[3]	SIUL2-GPI[34]	General Purpose Input C[2]	I	45	U5
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[4]	MSCR[36]	0000 (Default)	GPIO[36]	SIUL2-GPIO[36]	General Purpose IO C[4]	I/O	11	H3
		0001	CS0	DSPI0	DSPI 0 Peripheral Chip Select 0	I/O		
		0010	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 1	I/O		
		0011	DEBUG4	SSCM	SSCM Debug Output 4	O		
		0100-1111	—	Reserved	—	—		
	IMCR[93]	0001	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input 1	I/O		
	IMCR[195]	0001	REQ22	SIUL2	SIUL2 External Interrupt Source 22	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
C[5]	MSCR[37]	0000 (Default)	GPIO[37]	SIUL2-GPIO[37]	General Purpose IO C[5]	I/O	13	G3
		0001	SCK	DSPI0	DSPI 0 Serial Clock (output)	I/O		
		0010	—	Reserved	—	—		
		0011	DEBUG5	SSCM	SSCM Debug Output 5	O		
		0100-1111	—	Reserved	—	—		
	IMCR[86]	0001	FAULT3	FlexPWM_0	FlexPWM_0 Fault Input 3	I		
	IMCR[196]	0001	REQ23	SIUL2	SIUL2 External Interrupt Source 23	I		
C[6]	MSCR[38]	0000 (Default)	GPIO[38]	SIUL2-GPIO[38]	General Purpose IO C[6]	I/O	142	D4
		0001	SOUT	DSPI0	DSPI 0 Serial Data Out	O		
		0010	B1	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 1	I/O		
		0011	DEBUG6	SSCM	SSCM Debug Output 6	O		
		0100-1111	—	Reserved	—	—		
	IMCR[92]	0001	B1	FlexPWM_0	FlexPWM_0 Channel B Input 1	I		
	IMCR[197]	0001	REQ24	SIUL2	SIUL2 External Interrupt Source 24	I/O		
C[7]	MSCR[39]	0000 (Default)	GPIO[39]	SIUL2-GPIO[39]	General Purpose IO C[7]	I/O	15	J1
		0001	—	Reserved	—	—		
		0010	A1	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 1	I/O		
		0011	DEBUG7	SSCM	SSCM Debug Output 7	O		
		0100-1111	—	Reserved	—	—		
	IMCR[41]	0001	SIN	DSPI0	DSPI 0 Serial Data Input	I		
	IMCR[91]	0001	A1	FlexPWM_0	FlexPWM_0 Channel A Input 1	I/O		
C[10]	MSCR[42]	0000 (Default)	GPIO[42]	SIUL2-GPIO[42]	General Purpose IO C[10]	I/O	111	B14
		0001	CS2	DSPI2	DSPI 2 Peripheral Chip Select 2	O		
		0010	—	Reserved	—	—		
		0011	A3	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[84]	0001	FAULT1	FlexPWM_0	FlexPWM_0 Fault Input 1	I		
	IMCR[97]	0010	A3	FlexPWM_0	FlexPWM_0 Channel A Input 3	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
C[11]	MSCR[43]	0000 (Default)	GPIO[43]	SIUL2-GPIO[43]	General Purpose IO C[11]	I/O	80	P16
		0001	ETC4	eTimer_0	eTimer_0 Input/Output Data Channel 4	I/O		
		0010	CS2	DSPI2	DSPI 2 Peripheral Chip Select 2	O		
		0011	TX_ER	ENET_0	Ethernet transmit Data Error	O		
		0100	CS0	DSPI3	DSPI 3 Peripheral Chip Select 0	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[52]	0001	CS0	DSPI3	DSPI 3 Peripheral Chip Select 3	O		
	IMCR[63]	0100	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I/O		
C[12]	MSCR[44]	0000 (Default)	GPIO[44]	SIUL2-GPIO[44]	General Purpose IO C[12]	I/O	82	M14
		0001	ETC5	eTimer_0	eTimer_0 Input/Output Data Channel 5[5]	I/O		
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O		
		0011	—	LFAST	SIPI/LFAST PLL Phase 0 clock on positive terminal	O		
		0100	CS1	DSPI3	DSPI 3 Peripheral Chip Select 1	O		
		0101-1111	—	Reserved	—	—		
	IMCR[213]	0100	SENT_RX[0]	SENT1	SENT 1 Receiver Channel 0	I		
	IMCR[64]	0011	ETC5	eTimer_0	eTimer_0 Input Data Channel 5	I/O		
C[13]	MSCR[45]	0000 (Default)	GPIO[45]	SIUL2-GPIO[45]	General Purpose IO C[13]	I/O	101	E15
		0001	ETC1	eTimer_1	eTimer_1 Input/Output Data Channel 1	I/O		
		0010-0011	—	Reserved	—	—		
		0100	A0	FlexPWM_1	FlexPWM_1 Channel A Input 0	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[38]	0001	EXT_IN	CTU_0	CTU 0 External Trigger Input	I		
	IMCR[66]	0001	ETC1	eTimer_1	eTimer_1 Input Data Channel 1	I/O		
	IMCR[87]	0001	EXT_SYNC	FlexPWM_0	FlexPWM_0 External Trigger Input	I		
	IMCR[105]	0001	A0	FlexPWM_1	FlexPWM_1 Channel A Input 0	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
C[14]	MSCR[46]	0000 (Default)	GPIO[46]	SIUL2-GPIO[46]	General Purpose IO C[14]	I/O	103	F14
		0001	ETC2	eTimer_1	eTimer_1 Input/Output Data Channel 2	I/O		
		0010	EXT_TGR	CTU_0	CTU0 External Trigger Output	O		
		0011	CS7	DSPI1	DSPI 1 Peripheral Chip Select 7	O		
		0100	B0	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 0	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[67]	0010	ETC2	eTimer_1	eTimer_1 Input Data Channel 2	I/O		
	IMCR[106]	0001	B0	FlexPWM_1	FlexPWM_1 Channel B Input 0	I/O		
C[15]	MSCR[47]	0000 (Default)	GPIO[47]	SIUL2-GPIO[47]	General Purpose IO C[15]	I/O	124	A8
		0001	FR_A_TXEN	FLEXRAY	FlexRay Transmit Enable Channel A	O		
		0010	ETC0	eTimer_1	eTimer_1 Input/Output Data Channel 0	I/O		
		0011	A1	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 1	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[38]	0010	EXT_IN	CTU_0	CTU 0 External Trigger Input	I		
	IMCR[65]	0010	ETC0	eTimer_1	eTimer_1 Input Data Channel 0	I/O		
	IMCR[87]	0010	EXT_SYNC	FlexPWM_0	FlexPWM_0 External Sync Input	I		
	IMCR[91]	0010	A1	FlexPWM_0	FlexPWM_0 Channel A Input 1	I/O		
D[0]	MSCR[48]	0000 (Default)	GPIO[48]	SIUL2-GPIO[48]	General Purpose IO D[0]	I/O	125	B8
		0001	FR_A_TX	FLEXRAY	FlexRay Transmit Data Channel A	O		
		0010	ETC1	eTimer_1	eTimer_1 Input/Output Data Channel 1	I/O		
		0011	B1	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 1	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[66]	0010	ETC1	eTimer_1	eTimer_1 Input Data Channel 1	I/O		
	IMCR[92]	0010	B1	FlexPWM_0	FlexPWM_0 Channel B Input 1	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
D[1]	MSCR[49]	0000 (Default)	GPIO[49]	SIUL2-GPIO[49]	General Purpose IO D[1]	I/O	3	E3
		0001	—	Reserved	—	—		
		0010	ETC2	eTimer_1	eTimer_1 Input/Output Data Channel 2	I/O		
		0011	EXT_TGR	CTU_0	CTU 0 External Trigger Output	O		
		0100-1111	—	Reserved	—	—		
	IMCR[67]	0011	ETC2	eTimer_1	eTimer_1 Input Data Channel 2	I/O		
	IMCR[136]	0001	FR_A_RX	FLEXRAY	FlexRay Channel A Receive Pin	I		
D[2]	MSCR[50]	0000 (Default)	GPIO[50]	SIUL2-GPIO[50]	General Purpose IO D[2]	I/O	140	B4
		0001	—	Reserved	—	—		
		0010	ETC3	eTimer_1	eTimer_1 Input/Output Data Channel 3	I/O		
		0011	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[68]	0010	ETC3	eTimer_1	eTimer_1 Input Data Channel 3	I/O		
	IMCR[99]	0001	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input 3	I/O		
	IMCR[137]	0001	FR_B_RX	FLEXRAY	FlexRay Channel B Receive Pin	I		
D[3]	MSCR[51]	0000 (Default)	GPIO[51]	SIUL2-GPIO[51]	General Purpose IO D[3]	I/O	128	A5
		0001	FR_B_TX	FLEXRAY	FlexRay Transmit Data Channel B	O		
		0010	ETC4	eTimer_1	eTimer_1 Input/Output Data Channel 4	I/O		
		0011	A3	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[69]	0010	ETC4	eTimer_1	eTimer_1 Input Data Channel 4	I/O		
	IMCR[97]	0011	A3	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 3	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
D[4]	MSCR[52]	0000 (Default)	GPIO[52]	SIUL2-GPIO[52]	General Purpose IO D[4]	I/O	129	B7
		0001	FR_B_TXEN	FLEXRAY	FlexRay Transmit Enable Channel B	O		
		0010	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O		
		0011	B3	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[70]	0011	ETC5	eTimer_1	eTimer_1 Input Data Channel 5	I/O		
	IMCR[98]	0011	B3	FlexPWM_0	FlexPWM_0 Channel B Input 3	I/O		
D[5]	MSCR[53]	0000 (Default)	GPIO[53]	SIUL2-GPIO[53]	General Purpose IO D[5]	I/O	33	M4
		0001	CS3	DSPI0	DSPI 0 Peripheral Chip Select 3	O		
		0010	—	Reserved	—	—		
		0100	SOUT	DSPI3	DSPI 3 Serial Data Out	O		
		0101-1111	—	Reserved	—	—		
	IMCR[85]	0001	FAULT2	FlexPWM_0	FlexPWM_0 Fault Input 2	I		
	IMCR[205]	0001	SENT_RX[0]	SENT0	SENT 0 Receiver channel 0	I		
	IMCR[227]	0001	RX_D1	ENET_0	Ethernet MII/RMII receive data 1	I		
D[6]	MSCR[54]	0000 (Default)	GPIO[54]	SIUL2-GPIO[54]	General Purpose IO D[6]	I/O	34	P3
		0001	CS2	DSPI0	DSPI 0 Peripheral Chip Select 2	O		
		0010	—	Reserved	—	—		
		0011	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 3	I/O		
		0100	SCK	DSPI3	DSPI 3 Serial Clock (Output)	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[51]	0001	SCK	DSPI3	DSPI 3 Serial Clock (Output)	I/O		
	IMCR[84]	0010	FAULT1	FlexPWM_0	FlexPWM_0 Fault Input 1	I		
	IMCR[99]	0010	X3	FlexPWM_0	FlexPWM_0 Channel X Input 3	I/O		
	IMCR[226]	0001	RX_D0	ENET_0	Ethernet MII/RMII receive data 0	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
D[7]	MSCR[55]	0000 (Default)	GPIO[55][6] SGEN OUT[7]	SIUL2-GPIO[55]	General Purpose IO D[7]	I/O	37	R4
		0001	CS3	DSPI1	DSPI 1 Peripheral Chip Select 3	O		
		0010	—	Reserved	—	—		
		0011	CS4	DSPI0	DSPI 0 Peripheral Chip Select 4	O		
		0100-1111	—	Reserved	—	—		
	IMCR[50]	0010	SIN	DSPI3	DSPI 3 Serial Data Input	I		
	IMCR[213]	0001	SENT_RX[0]	SENT1	SENT 1 Receiver channel 0	I		
	IMCR[225]	0001	RX_DV	ENET_0	Ethernet Receive data valid	I		
D[8]	MSCR[56]	0000 (Default)	GPIO[56]	SIUL2-GPIO[56]	General Purpose IO D[8]	I/O	32	L4
		0001	CS2	DSPI1	DSPI 1 Peripheral Chip Select 2	O		
		0010	ETC4	eTimer_1	eTimer_1 Input/Output Data Channel 4	I/O		
		0011	CS5	DSPI0	DSPI 0 Peripheral Chip Select 5	O		
		0100-1111	—	Reserved	—	—		
	IMCR[69]	0011	ETC4	eTimer_1	eTimer_1 Input Data Channel 4	I/O		
	IMCR[86]	0010	FAULT3	FlexPWM_0	FlexPWM_0 Fault Input 3	I		
	IMCR[224]	0001	RX_CLK	ENET_0	Ethernet Receive clock	I		
D[9]	MSCR[57]	0000 (Default)	GPIO[57]	SIUL2-GPIO[57]	General Purpose IO D[9]	I/O	26	N3
		0001	X0	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 0	I/O		
		0010	TXD	LIN1	LINFlexD 1 Transmit Pin	O		
		0011-1111	—	Reserved	—	—		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
D[10]	MSCR[58]	0000 (Default)	GPIO[58]	SIUL2-GPIO[58]	General Purpose IO D[10]	I/O	76	R16
		0001	A0	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	TX_D2	ENET_0	Ethernet MII transmit data	O		
		0100	CS0	DSPI3	DSPI 3 Peripheral Chip Select 0	I/O		
		0110-1111	—	Reserved	—	—		
	IMCR[52]	0010	CS0	DSPI3	DSPI 3 Peripheral chip Select 0	I/O		
	IMCR[59]	0001	ETC0	eTimer_0	eTimer_0 Input Data Channel 0	I/O		
	IMCR[88]	0010	A0	FlexPWM_0	FlexPWM_0 Channel A Input 0	I/O		
D[11]	MSCR[59]	0000 (Default)	GPIO[59]	SIUL2-GPIO[59]	General Purpose IO D[11]	I/O	78	P17
		0001	B0	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	CS1	DSPI3	DSPI 3 Peripheral Chip Select 1	O		
		0100	SCK	DSPI3	DSPI 3 Serial Clock (Output)	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[51]	0010	SCK	DSPI3	DSPI 3 Serial Clock (Output)	I/O		
	IMCR[60]	0001	ETC1	eTimer_0	eTimer_0 Input Data Channel 1	I/O		
	IMCR[89]	0010	B0	FlexPWM_0	FlexPWM_0 Channel B Input 0	I/O		
D[12]	MSCR[60]	0000 (Default)	GPIO[60]	SIUL2-GPIO[60]	General Purpose IO D[12]	I/O	99	F15
		0001	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 1	I/O		
		0010	CS6	DSPI1	DSPI 1 Peripheral Chip Select 6	O		
		0011	CS2	DSPI3	DSPI 3 Peripheral Chip Select 2	O		
		0100	SOUT	DSPI3	DSPI 1 Serial Data Out	O		
		0101-1111	—	Reserved	—	—		
	IMCR[93]	0010	X1	FlexPWM_0	FlexPWM_0 Channel X Input 1	I/O		
	IMCR[166]	0010	RXD	LIN1	LIN 1 Receive Pin	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
D[14]	MSCR[62]	0000 (Default)	GPIO[62]	SIUL2-GPIO[62]	General Purpose IO D[14]	I/O	105	E17
		0001	B1	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 1	I/O		
		0010	—	Reserved	—	—		
		0011	CS3	DSPI3	DSPI 3 Peripheral Chip Select 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[50]	0011	SIN	DSPI3	DSPI 3 Serial Data Input	I		
	IMCR[62]	0001	ETC3	eTimer_0	eTimer_0 Input Data Channel 3	I/O		
	IMCR[92]	0011	B1	FlexPWM_0	FlexPWM_0 Channel B Input 1	I/O		
E[0]	MSCR[64]	0000 (Default)	GPI[64][4] ADC1_AN[5]/ ADC3_AN[4]	SIUL2-GPI[64]	General Purpose Input E[0]	I	68	T13
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[2]	MSCR[66]	0000 (Default)	GPI[66][4] ADC0_AN[5]	SIUL2-GPI[66]	General Purpose Input E[2]	I	49	U6
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[4]	MSCR[68]	0000 (Default)	GPI[68][4] ADC0_AN[7]	SIUL2-GPI[68]	General Purpose Input E[4]	I	42	U4
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[5]	MSCR[69]	0000 (Default)	GPI[69][4] ADC0_AN[8]	SIUL2-GPI[69]	General Purpose Input E[5]	I	44	T5
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[6]	MSCR[70]	0000 (Default)	GPI[70][4] ADC0_ADC2_AN[4]	SIUL2-GPI[70]	General Purpose Input E[6]	I	46	R6
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[7]	MSCR[71]	0000 (Default)	GPI[71][4] ADC0_AN[6]	SIUL2-GPI[71]	General Purpose Input E[7]	I	48	T6
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
E[9]	MSCR[73]	0000	GPI[73][4] ADC1_AN[7]/ ADC3_AN[6]	SIUL2-GPI[73]	General Purpose Input E[9]	I	61	U10
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[10]	MSCR[74]	0000 (Default)	GPI[74][4] ADC1_AN[8]/ ADC3_AN[7]	SIUL2-GPI[74]	General Purpose Input E[10]	I	63	T11
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[11]	MSCR[75]	0000 (Default)	GPI[75][4] ADC1_AN[4]/ ADC3_AN[3]	SIUL2-GPI[75]	General Purpose Input E[11]	I	65	U11
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[12]	MSCR[76]	0000 (Default)	GPI[76][4] ADC1_AN[6]/ ADC3_AN[5]	SIUL2-GPI[76]	General Purpose Input E[12]	I	67	T12
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[13]	MSCR[77]	0000 (Default)	GPIO[77]	SIUL2-GPIO[77]	General Purpose IO E[13]	I/O	117	A11
		0001	ETC5	eTimer_0	eTimer_0 Input/Output Data Channel 5	I/O		
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O		
		0011	CS4	DSPI1	DSPI 1 Peripheral Chip Select 4	O		
		0100	SCK	DSPI3	DSPI 3 Serial Clock (Output)	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[51]	0011	SCK	DSPI3	DSPI 3 Serial Clock (Output)	I/O		
	IMCR[198]	0001	REQ25	SIUL2	SIUL2 External Interrupt Source 25	I		
	IMCR[64]	0100	ETC5	eTimer_0	eTimer_0 Input Data Channel	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
E[14]	MSCR[78]	0000 (Default)	GPIO[78]	SIUL2-GPIO[78]	General Purpose IO E[14]	I/O	119	B10
		0001	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O		
		0010	SOUT	DSPI3	DSPI 3 Serial Data Out	O		
		0011	CS5	DSPI1	DSPI 1 Peripheral Chip Select 5	O		
		0100	B2	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 2	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[70]	0100	ETC5	eTimer_1	eTimer_1 Input Data Channel 5	I/O		
	IMCR[113]	0001	B2	FlexPWM_1	FlexPWM_1 Channel B Input 2	I/O		
	IMCR[199]	0001	REQ26	SIUL2	SIUL2 External Interrupt Source 26	I		
E[15]	MSCR[79]	0000 (Default)	GPIO[79]	SIUL2-GPIO[79]	General Purpose IO E[15]	I/O	121	C8
		0001	CS1	DSPI0	DSPI 0 Peripheral Chip Select 1	O		
		0010	—	Reserved	—	—		
		0011	TIMER1	ENET_0	Ethernet TIMER Outputs (Output Compare Events)	O		
		0100-1111	—	Reserved	—	—		
	IMCR[50]	0100	SIN	DSPI3	DSPI 3 Serial Data Input	I		
	IMCR[200]	0001	REQ27	SIUL2	SIUL2 External Interrupt Source 27	I		
F[0]	MSCR[80]	0000 (Default)	GPIO[80]	SIUL2-GPIO[80]	General Purpose IO F[0]	I/O	133	B6
		0001	A1	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 1	I/O		
		0010	CS3	DSPI3	DSPI 3 Peripheral Chip Select 3	I/O		
		0011	MDC	ENET_0	Ethernet MDIO clock output	O		
		0100-1111	—	Reserved	—	—		
	IMCR[61]	0001	ETC2	eTimer_0	eTimer_0 Input Data Channel 2	I/O		
	IMCR[91]	0011	A1	FlexPWM_0	FlexPWM_0 Channel A Input 1	I/O		
	IMCR[201]	0001	REQ28	SIUL2	SIUL2 External Interrupt Source 28	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
F[3]	MSCR[83]	0000 (Default)	GPIO[83]	SIUL2-GPIO[83]	General Purpose IO F[3]	I/O	139	B3
		0001	CS6	DSPI0	DSPI 0 Peripheral Chip Select 6	O		
		0010	—	Reserved	—	—		
		0011	CS2	DSPI3	DSPI 3 Peripheral Chip Select 2	O		
		0100	TIMER2	ENET_0	Ethernet TIMER Outputs 2 (Output Compare Events)	I/O		
		0101-1111	—	Reserved	—	—		
F[4]	MSCR[84]	0000 (Default)	GPIO[84]	SIUL2-GPIO[84]	General Purpose IO F[4]	I/O	4	E1
		0001	—	Reserved	—	I/O		
		0010	MDO[3]	NPC_WRAPPER	Nexus - Message Data Out Pin 3	O		
		0011	CS1	DSPI3	DSPI 3 Peripheral Chip Select 1	O		
		0100-1111	—	Reserved	—	—		
F[5]	MSCR[85]	0000 (Default)	GPIO[85]	SIUL2-GPIO[85]	General Purpose IO F[5]	I/O	5	F1
		0001	—	Reserved	—	I/O		
		0010	MDO[2]	NPC_WRAPPER	Nexus Message Data Out Pin 2	O		
		0011	CS0	DSPI3	DSPI 3 Peripheral Chip Select 0	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[52]	0011	CS0	DSPI3	DSPI 3 Peripheral Chip Select 0	I/O		
F[6]	MSCR[86]	0000 (Default)	GPIO[86]	SIUL2-GPIO[86]	General Purpose IO F[6]	I/O	8	E2
		0001	—	Reserved	—	I/O		
		0010	MDO[1]	NPC_WRAPPER	Nexus Message Data Out Pin 1	O		
		0011-1111	—	Reserved	—	—		
F[7]	MSCR[87]	0000 (Default)	GPIO[87]	SIUL2-GPIO[87]	General Purpose IO F[7]	I/O	19	J4
		0001	—	Reserved	—	I/O		
		0010	MCKO	NPC_WRAPPER	Nexus Message Clock Out for development tools	O		
		0011-1111	—	Reserved	—	—		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
F[8]	MSCR[88]	0000 (Default)	GPIO[88]	SIUL2-GPIO[88]	General Purpose IO F[8]	I/O	20	J3
		0001	—	Reserved	—	I/O		
		0010	MSEO_B[1]	NPC_WRAPPER	Nexus Message Start/End Out Pin 1	O		
		0011-1111	—	Reserved	—	—		
F[9]	MSCR[89]	0000 (Default)	GPIO[89]	SIUL2-GPIO[89]	General Purpose IO F[9]	I/O	23	K3
		0001	—	Reserved	—	I/O		
		0010	MSEO_B[0]	NPC_WRAPPER	Nexus Message Start/End Out Pin 0	O		
		0011-1111	—	Reserved	—	—		
F[10]	MSCR[90]	0000 (Default)	GPIO[90]	SIUL2-GPIO[90]	General Purpose IO F[10]	I/O	24	K2
		0001	—	Reserved	—	—		
		0010	EVTO_B	NPC_WRAPPER	Nexus Event Out Pin	O		
		0011-1111	—	Reserved	—	—		
F[11]	MSCR[91]	0000 (Default)	GPIO[91]	SIUL2-GPIO[91]	General Purpose IO F[11]	I/O	25	L2
		0001	—	Reserved	—	—		
		0010	EVTI_IN	NPC_WRAPPER	Nexus Event In Pin	I		
		0011-1111	—	Reserved	—	—		
F[12]	MSCR[92]	0000 (Default)	GPIO[92]	SIUL2-GPIO[92]	General Purpose IO F[12]	I/O	106	D17
		0001	ETC3	eTimer_1	eTimer_1 Input/Output Data Channel 3	I/O		
		0010-0011	—	Reserved	—	—		
		0100	A1	FlexPWM_1	FlexPWM_1 Channel A Input 1	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[68]	0011	ETC3	eTimer_1	eTimer_1 Input Data Channel 3	I/O		
	IMCR[109]	0001	A1	FlexPWM_1	FlexPWM_1 Channel A Input 1	I/O		
	IMCR[203]	0001	REQ30	SIUL2	SIUL2 External Interrupt Source 30	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
F[13]	MSCR[93]	0000 (Default)	GPIO[93]	SIUL2-GPIO[93]	General Purpose IO F[13]	I/O	112	A15
		0001	ETC4	eTimer_1	eTimer_1 Input/Output Data Channel 4	I/O		
		0010-0011	—	Reserved	—	—		
		0100	B1	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 1	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[69]	0100	ETC4	eTimer_1	eTimer_1 Input Data Channel 4	I/O		
	IMCR[110]	0001	B1	FlexPWM_1	FlexPWM_1 Channel B Input 1	I/O		
	IMCR[204]	0001	REQ31	SIUL2	SIUL2 External Interrupt Source 31	I		
F[14]	MSCR[94]	0000 (Default)	GPIO[94]	SIUL2-GPIO[94]	General Purpose IO F[14]	I/O	115	D12
		0001	TXD	LIN1	LINFlexD 1 Transmit Pin	O		
		0010	TXD	CAN2	CAN 2 Transmit Pin	O		
		0011-1111	—	Reserved	—	—		
F[15]	MSCR[95]	0000 (Default)	GPIO[95]	SIUL2-GPIO[95]	General Purpose IO F[15]	I/O	113	A13
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[166]	0011	RXD	LIN1	LIN1 RXD	I		
	IMCR[34]	0001	RXD	CAN2	CAN2 RXD	I		
G[2]	MSCR[98]	0000 (Default)	GPIO[98]	SIUL2-GPIO[98]	General Purpose IO G[2]	I/O	102	F17
		0001	X2	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 2	I/O		
		0010	CS1	DSPI1	DSPI 1 Peripheral Chip Select 1	O		
		0011-1111	—	Reserved	—	—		
	IMCR[96]	0010	X2	FlexPWM_0	FlexPWM_0 Auxiliary Input 2	I/O		
G[3]	MSCR[99]	0000 (Default)	GPIO[99]	SIUL2-GPIO[99]	General Purpose IO G[3]	I/O	104	E16
		0001	A2	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 2	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[63]	0010	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I/O		
	IMCR[94]	0011	A2	FlexPWM_0	FlexPWM_0 Channel A Input 2	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
G[4]	MSCR[100]	0000 (Default)	GPIO[100]	SIUL2-GPIO[100]	General Purpose IO G[4]	I/O	100	F16
		0001	B2	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 2	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[64]	0010	ETC5	eTimer_0	eTimer_0 Input Data Channel 5	I/O		
	IMCR[95]	0011	B2	FlexPWM_0	FlexPWM_0 Channel B Input 2	I/O		
G[5]	MSCR[101]	0000 (Default)	GPIO[101]	SIUL2-GPIO[101]	General Purpose IO G[5]	I/O	85	M17
		0001	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 3	I/O		
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O		
		0011	TX_EN	ENET_0	Ethernet Transmit Data Valid	O		
		0100-1111	—	Reserved	—	—		
	IMCR[99]	0011	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input 3	I/O		
G[6]	MSCR[102]	0000 (Default)	GPIO[102]	SIUL2-GPIO[102]	General Purpose IO G[6]	I/O	98	G17
		0001	A3	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 3	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[97]	0100	A3	FlexPWM_0	FlexPWM_0 Channel A Input 3	I/O		
G[7]	MSCR[103]	0000 (Default)	GPIO[103]	SIUL2-GPIO[103]	General Purpose IO G[7][8]	I/O	83	M16
		0001	B3	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 3	I/O		
		0010	—	Reserved	—	—		
		0011	—	LFAST	LVDS receive positive terminal	I		
		0100-1111	—	Reserved	—	—		
	IMCR[98]	0100	B3	FlexPWM_0	FlexPWM_0 Channel B Input 3	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
G[8]	MSCR[104]	0000 (Default)	GPIO[104]	SIUL2-GPIO[104]	General Purpose IO G[8]	I/O	81	N14
		0001	FR_DBG[0]	FLEXRAY	FlexRay Debug Strobe Signal 0	O		
		0010	CS1	DSPI0	DSPI 0 Peripheral Chip Select 1	O		
		0011	RMII_CLK	ENET_0	Ethernet RMII Clock (used in MII to RMII Gaskets)	O		
		0100-1111	—	Reserved	—	—		
	IMCR[83]	0011	FAULT0	FlexPWM_0	FlexPWM_0 Fault Input 0	I		
	IMCR[194]	0001	REQ21	SIUL2	SIUL2 External Interrupt Source 21	I		
	IMCR[205]	0011	SENT_RX[0]	SENT_0	SENT 0 Receiver channel 0	I		
	IMCR[233]	0001	TX_CLK	ENET_0	Ethernet Transmit Clock	I		
G[9]	MSCR[105]	0000 (Default)	GPIO[105]	SIUL2-GPIO[105]	General Purpose IO G[9]	I/O	79	P14
		0001	FR_DBG[1]	FLEXRAY	FlexRay Debug Strobe Signal 1	O		
		0010	CS1	DSPI1	DSPI 1 Peripheral Chip Select 1	O		
		0011	TX_D0	ENET_0	Ethernet MII/RMII transmit data 0	O		
		0100-1111	—	Reserved	—	—		
	IMCR[84]	0011	FAULT1	FlexPWM_0	FlexPWM_0 Fault Input 1	I		
	IMCR[202]	0001	REQ29	SIUL2	SIUL2 External Interrupt Source 29	I		
	IMCR[213]	0011	SENT_RX[0]	SENT_1	SENT 1 Receiver channel 0	I		
G[10]	MSCR[106]	0000 (Default)	GPIO[106]	SIUL2-GPIO[106]	General Purpose IO G[10]	I/O	77	R17
		0001	FR_DBG[2]	FLEXRAY	FlexRay Debug Strobe Signal 2	O		
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O		
		0011	TX_D1	ENET_0	Ethernet MII/RMII transmit data 1	O		
		0100-1111	—	Reserved	—	—		
	IMCR[85]	0010	FAULT2	FlexPWM_0	FlexPWM_0 Fault Input 2	I		
	IMCR[206]	0100	SENT_RX[1]	SENT_0	SENT 0 Receiver channel 1	I		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
G[11]	MSCR[107]	0000 (Default)	GPIO[107]	SIUL2-GPIO[107]	General Purpose IO G[11]	I/O	75	T15
		0001	FR_DBG[3]	FLEXRAY	FlexRay Debug Strobe Signal 3	O		
		0010	—	Reserved	—	—		
		0011	TX_D3	ENET_0	Ethernet MII/RMII transmit data 3	O		
		0100-1111	—	Reserved	—	—		
	IMCR[86]	0011	FAULT3	FlexPWM_0	FlexPWM_0 Fault Input 3	I		
	IMCR[214]	0100	SENT_RX[1]	SENT_1	SENT 1 Receiver channel 1	I		
H[4]	MSCR[116]	0000 (Default)	GPIO[116]	SIUL2-GPIO[116]	General Purpose IO H[4]	I/O		F4
		0001	X0	FlexPWM_1	FlexPWM_1 Auxiliary Input/ Output 0	I/O		
		0010	ETC0	eTimer_2	eTimer_2 Input/Output Data Channel 0	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[71]	0001	ETC0	eTimer_2	eTimer_2 Input Data Channel 0	I/O		
	IMCR[231]	0001	CRS	ENET_0	Ethernet MII Carrier Sense	I		
H[5]	MSCR[117]	0000 (Default)	GPIO[117]	SIUL2-GPIO[117]	General Purpose IO H[5]	I/O		F3
		0001	A0	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	CS4	DSPI0	DSPI 0 Peripheral Chip Select 4	O		
		0100-1111	—	Reserved	—	—		
	IMCR[105]	0010	A0	FlexPWM_1	FlexPWM_1 Channel A Input 0	I/O		
	IMCR[230]	0001	COL	ENET_0	Ethernet MII Collision	I		
H[6]	MSCR[118]	0000 (Default)	GPIO[118]	SIUL2-GPIO[118]	General Purpose IO H[6]	I/O		C13
		0001	B0	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	CS5	DSPI0	DSPI 0 Peripheral Chip Select 5	O		
		0100-1111	—	Reserved	—	—		
	IMCR[106]	0010	B0	FlexPWM_1	FlexPWM_1 Channel B Input 0	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
H[7]	MSCR[119]	0000 (Default)	GPIO[119]	SIUL2-GPIO[119]	General Purpose IO H[7]	I/O		F2
		0001	X1	FlexPWM_1	FlexPWM_1 Auxiliary Input/ Output 1	I/O		
		0010	ETC1	eTimer_2	eTimer_2 Input/Output Data Channel 1	I/O		
		0011	MDIO	ENET_0	Ethernet MDIO input/output data	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[72]	0001	ETC1	eTimer_2	eTimer_2 Input Data Channel 1	I/O		
H[8]	MSCR[120]	0000 (Default)	GPIO[120]	SIUL2-GPIO[120]	General Purpose IO H[8]	I/O		L1
		0001	A1	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 1	I/O		
		0010	—	Reserved	—	—		
		0011	CS6	DSPI0	DSPI 0 Peripheral Chip Select 6	O		
		0100-1111	—	Reserved	—	—		
	IMCR[109]	0010	A1	FlexPWM_1	FlexPWM_1 Channel A Input 1	I/O		
	IMCR[228]	0001	RX_D2	ENET_0	Ethernet MII Receive Data 2	I		
H[9]	MSCR[121]	0000 (Default)	GPIO[121]	SIUL2-GPIO[121]	General Purpose IO H[9]	I/O		B13
		0001	B1	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 1	I/O		
		0010	—	Reserved	—	—		
		0011	CS7	DSPI0	DSPI 0 Peripheral Chip Select 7	O		
		0100-1111	—	Reserved	—	—		
	IMCR[110]	0010	B1	FlexPWM_1	FlexPWM_1 Channel B Input 1	I/O		
H[10]	MSCR[122]	0000 (Default)	GPIO[122]	SIUL2-GPIO[122]	General Purpose IO H[10]	I/O		C7
		0001	X2	FlexPWM_1	FlexPWM_1 Auxiliary Input/ Output 2	I/O		
		0010	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[73]	0010	ETC2	eTimer_2	eTimer_2 Input Data Channel 2	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
H[11]	MSCR[123]	0000 (Default)	GPIO[123]	SIUL2-GPIO[123]	General Purpose IO H[11]	I/O		C9
		0001	A2	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 2	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[112]	0010	A2	FlexPWM_1	FlexPWM_1 Channel A Input 2	I/O		
H[12]	MSCR[124]	0000 (Default)	GPIO[124]	SIUL2-GPIO[124]	General Purpose IO H[12]	I/O		A7
		0001	B2	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 2	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[113]	0010	B2	FlexPWM_1	FlexPWM_1 Channel B Input 2	I/O		
H[13]	MSCR[125]	0000 (Default)	GPIO[125]	SIUL2-GPIO[125]	General Purpose IO H[13]	I/O		A14
		0001	X3	FlexPWM_1	FlexPWM_1 Auxiliary Input/ Output 3	I/O		
		0010	ETC3	eTimer_2	eTimer_2 Input/Output Data Channel 3	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[74]	0010	ETC3	eTimer_2	eTimer_2 Input Data Channel 3	I/O		
H[14]	MSCR[126]	0000 (Default)	GPIO[126]	SIUL2-GPIO[126]	General Purpose IO H[14]	I/O		P13
		0001	A3	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 3	I/O		
		0010	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[75]	0010	ETC4	eTimer_2	eTimer_2 Input Data Channel 4	I/O		
H[15]	MSCR[127]	0000 (Default)	GPIO[127]	SIUL2-GPIO[127]	General Purpose IO H[15]	I/O		C17
		0001	B3	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 3	I/O		
		0010	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[76]	0010	ETC5	eTimer_2	eTimer_2 Input Data Channel 5	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
I[0]	MSCR[128]	0000 (Default)	GPIO[128]	SIUL2-GPIO[128]	General Purpose IO I[0]	I/O		C6
		0001	ETC0	eTimer_2	eTimer_2 Input/Output Data Channel 0	I/O		
		0010	CS4	DSPI0	DSPI 0 Peripheral Chip Select 4	O		
		0011-1111	—	Reserved	—	—		
	IMCR[71]	0010	ETC0	eTimer_2	eTimer_2 Input Data Channel 0	I/O		
	IMCR[100]	0001	FAULT0	FlexPWM_1	FlexPWM_1 Fault Input 0	I		
I[1]	MSCR[129]	0000 (Default)	GPIO[129]	SIUL2-GPIO[129]	General Purpose IO I[1]	I/O		T3
		0001	ETC1	eTimer_2	eTimer_2 Input/Output Data Channel 1	I/O		
		0010	CS5	DSPI0	DSPI 0 Peripheral Chip Select 5	O		
		0011-1111	—	Reserved	—	—		
	IMCR[72]	0010	ETC1	eTimer_2	eTimer_2 Input Data Channel 1	I/O		
	IMCR[101]	0001	FAULT1	FlexPWM_1	FlexPWM_1 Fault Input 1	I		
	IMCR[232]	0001	RX_ER	ENET_0	Ethernet Receive Data Error	I		
I[2]	MSCR[130]	0000 (Default)	GPIO[130]	SIUL2-GPIO[130]	General Purpose IO I[2]	I/O		D11
		0001	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O		
		0010	CS6	DSPI0	DSPI 0 Peripheral Chip Select 6	O		
		0011-1111	—	Reserved	—	—		
	IMCR[73]	0011	ETC2	eTimer_2	eTimer_2 Input Data Channel 2	I/O		
	IMCR[102]	0001	FAULT2	FlexPWM_1	FlexPWM_1 Fault Input 2	I		
I[3]	MSCR[131]	0000 (Default)	GPIO[131]	SIUL2-GPIO[131]	General Purpose IO I[3]	I/O		A10
		0001	ETC3	eTimer_2	eTimer_2 Input/Output Data Channel 3	I/O		
		0010	CS7	DSPI0	DSPI 0 Peripheral Chip Select 7	O		
		0011	EXT_TGR	CTU_0	CTU0 External Trigger Output	O		
		0100	TIMER0	ENET_0	Ethernet TIMER Outputs 0 (Output Compare Events)	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[74]	0011	ETC3	eTimer_2	eTimer_2 Input Data Channel 3	I/O		
	IMCR[103]	0001	FAULT3	FlexPWM_1	FlexPWM_1 Fault Input 3	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
RDY_ B/I[4]	MSCR[132]	0000 (Default)	GPIO[132]	SIUL2-GPIO[132]	General Purpose IO I[4]	I/O		J2
		0001	—	Reserved	—	—		
		0010	NEX_RDY_B	NPC_WRAPPER	Nexus data ready for transfer (RDY_B)	O		
		0011-1111	—	Reserved	—	—		
I[5]	MSCR[133]	0000 (Default)	GPIO[133]	SIUL2-GPIO[133]	General Purpose IO I[5][9]	I/O		N15
		0001	TXD	CAN2	CAN 2 Transmit Pin	O		
		0010	—	Reserved	—	—		
		0011	—	LFAST	SIPI/LFAST PLL Phase 0 clock on negative terminal	O		
		0100-1111	—	Reserved	—	—		
I[6]	MSCR[134]	0000 (Default)	GPIO[134]	SIUL2-GPIO[134]	General Purpose IO I[6][10]	I/O		M15
		0001	—	Reserved	—	—		
		0010	—	Reserved	—	—		
		0011	—	LFAST	LVDS receive negative terminal	I		
		0100-1111	—	Reserved	—	—		
	IMCR[34]	0010	RXD	CAN2	CAN 2 Receive Pin	I		
I[7]	MSCR[135]	0000 (Default)	GPIO[135]	SIUL2-GPIO[135]	General Purpose IO I[7]	I/O		D2
		0001	LFAST_REF_CLK	MC_CGM	SIPI LFAST reference clock	—		
		0010-1111	—	Reserved	—	—		
	IMCR[205]	0010	SENT_RX[0]	SENT0	SENT 0 Receiver channel 0	I		
I[8]	MSCR[136]	0000 (Default)	GPIO[136]	SIUL2-GPIO[136]	General Purpose IO I[8]	I/O		K4
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[213]	0010	SENT_RX[0]	SENT1	SENT 1 Receiver channel 0	I		
I[9]	MSCR[137]	0000 (Default)	GPIO[137]	SIUL2-GPIO[137]	General Purpose IO I[9]	I/O		L3
		0001	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[75]	0011	ETC4	eTimer_2	eTimer_2 Input Data Channel 4	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
I[10]	MSCR[138]	0000 (Default)	GPIO[138]	SIUL2-GPIO[138]	General Purpose IO I[10]	I/O		M3
		0001	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[76]	0011	ETC5	eTimer_2	eTimer_2 Input Data Channel 5	I/O		
I[11]	MSCR[139]	0000 (Default)	GPIO[139]	SIUL2-GPIO[139]	General Purpose IO I[11]	I/O		U3
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[206]	0001	SENT_RX[1]	SENT0	SENT 0 Receiver channel 1	I		
I[12]	MSCR[140]	0000 (Default)	GPIO[140]	SIUL2-GPIO[140]	General Purpose IO I[12]	I/O		P5
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[214]	0001	SENT_RX[1]	SENT1	SENT 1 Receiver channel 1	I		
I[13]	MSCR[141]	0000	GPIO[141]	SIUL2-GPIO[141]	General Purpose IO I[13]	I/O		P6
		0001	EXT_TGR	CTU_1	CTU1 External Trigger Output	I/O		
		0010-1111	—	Reserved	—	—		
I[14]	MSCR[142]	0000 (Default)	GPIO[142]	SIUL2-GPIO[142]	General Purpose IO I[14]	I/O		C10
		0001	CS0	DSPI3	DSPI 3 Peripheral Chip Select 0	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[52]	0100	CS0	DSPI3	DSPI 3 Peripheral Chip Select 0	I/O		
I[15]	MSCR[143]	0000 (Default)	GPIO[143]	SIUL2-GPIO[143]	General Purpose IO I[15]	I/O		C1
		0001	SCK	DSPI3	DSPI 3 Serial Clock (output)	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[51]	0100	SCK	DSPI3	DSPI 3 Peripheral Serial Clock (Output)	I/O		
J[0]	MSCR[144]	0000 (Default)	GPIO[144]	SIUL2-GPIO[144]	General Purpose IO J[0]	I/O		C2
		0001	SOUT	DSPI3	DSPI 3 Serial Data Out	O		
		0010-1111	—	Reserved	—	—		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
J[1]	MSCR[145]	0000 (Default)	GPIO[145]	SIUL2-GPIO[145]	General Purpose IO J[1]	I/O		A12
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[50]	0001	SIN	DSPI3	DSPI 3 Serial Data Input	I		
J[2]	MSCR[146]	0000 (Default)	GPIO[146]	SIUL2-GPIO[146]	General Purpose IO J[2]	I/O		C11
		0001	CS1	DSPI3	DSPI 3 Peripheral Chip Select 1	O		
		0010-1111	—	Reserved	—	—		
J[3]	MSCR[147]	0000 (Default)	GPIO[147]	SIUL2-GPIO[147]	General Purpose IO J[3]	I/O		B15
		0001	CS2	DSPI3	DSPI 3 Peripheral Chip Select 2	O		
		0010-1111	—	Reserved	—	—		
J[4]	MSCR[148]	0000 (Default)	GPIO[148]	SIUL2-GPIO[148]	General Purpose IO J[4]	I/O		D13
		0001	CS3	DSPI3	DSPI 3 Peripheral Chip Select 3	O		
		0010-1111	—	Reserved	—	—		
	IMCR[39]	0001	EXT_IN	CTU_1	CTU 1 External Trigger Input	I		
J[5]	MSCR[149]	0000 (Default)	GPI[149][4] ADC2_ADC3_AN[0]	SIUL2-GPI[149]	General Purpose Input J[5]	I		P8
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[206]	0010	SENT_RX[1]	SENT0	SENT 0 Receiver channel 1	I		
J[6]	MSCR[150]	0000 (Default)	GPI[150][4] ADC2_ADC3_AN[1]	SIUL2-GPI[150]	General Purpose Input J[6]	I		P9
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[214]	0010	SENT_RX[1]	SENT1	SENT 1 Receiver channel 1	I		
J[7]	MSCR[151]	0000 (Default)	GPI[151][4] ADC2_ADC3_AN[2]	SIUL2-GPI[151]	General Purpose Input J[7]	I		P10
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
J[8]	MSCR[152]	0000 (Default)	GPIO[152]	SIUL2-GPIO[152]	General Purpose IO J[8]	I/O	95	G16
		0001	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O		
		0010	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[34]	0011	RXD	CAN2	CAN 2 Receive Pin	I		
	IMCR[73]	0100	ETC2	eTimer_2	eTimer_2 Input Data Channel 2	I/O		
	IMCR[75]	0100	ETC4	eTimer_2	eTimer_2 Input Data Channel 4	I/O		
J[9]	MSCR[153]	0000 (Default)	GPIO[153]	SIUL2-GPIO[153]	General Purpose IO J[9]	I/O	16	K1
		0001	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O		
		0010	NEX_RDY_B	NPC	Nexus data ready for transfer (RDY_B)	O		
		0011-1111	—	Reserved	—	—		
	IMCR[39]	0010	EXT_IN	CTU_1	CTU_1 External Trigger Input	I		
	IMCR[76]	0100	ETC5	eTimer_2	eTimer_2 Input Data Channel 5	I/O		
	IMCR[229]	0001	RX_D3	ENET_0	Ethernet MII Receive Data 3	I		
NMI_B	MSCR[154]	0000 (Default)	NMI_B	Core	Non-Maskable Interrupt	I	1	E4

1. Selecting an alternative function with a "Reserved" source function causes the pin to enter a null state (input buffer and output buffer enables are both 0).
2. **(Default) = ALT mode configuration after reset.**
3. Changing the B[5] configuration during debug might affect the availability of TDI.
4. ADC analog input: Program corresponding MSCR APC bit and enable ADC to switch on the analog input path.
5. Shared with SIPI LFAST transmit pad SIPI_TXP. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.
6. To operate D[7] as GPIO, disable the Sine Wave Generator (SGEN) and the peripheral bus clock of the SGEN: Program the MC_ME_PCTL239 register to select an MC_ME_RUN_PCn (or MC_ME_LP_PCn) configuration where the field for the desired mode is 0.
7. SGEN output if SGEN is enabled.
8. Shared with SIPI LFAST receive pad SIPI_RXP. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.
9. Shared with SIPI LFAST receive pad SIPI_TXN. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.
10. Shared with SIPI LFAST receive pad SIPI_RXN. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.

The following table list ports that are not implemented. The corresponding control and data registers are not implemented.

Table 9. Ports - Not Implemented

Port Name	Port Index
C	3,8,9
D	13,15
E	1,3,8
F	1,2
G	0,1,[12:15]
H	[0:3]
J	[10:15]

Any attempt to access unimplemented MSCRs generates a bus error. The read value from unimplemented ports must be masked in case of parallel port accesses.

2.2.6 Peripheral input muxing

The following table describes the peripheral muxing capabilities of the device.

Table 10. Peripheral muxing

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
FlexCAN_0	RXD	IMCR[32]	0000 (Default)[1]	—	Disable
			0001	I/O-Pad	A[15]
			0010	I/O-Pad	B[1]
			0011-1111	—	Reserved[2]
FlexCAN_1	RXD	IMCR[33]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[15]
			0010	I/O-Pad	B[1]
			0011-1111	—	Reserved
FlexCAN_2	RXD	IMCR[34]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[15]
			0010	I/O-Pad	I[6]
			0011	I/O-Pad	J[8]
			0100-1111	—	Reserved
CTU_0	EXT_IN	IMCR[38]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[13]
			0010	I/O-Pad	C[15]
			0011-1111	—	Reserved

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
CTU_1	EXT_IN	IMCR[39]	0000 (Default)	—	Disable
			0001	I/O-Pad	J[4]
			0010	I/O-Pad	J[9]
			0011-1111	—	Reserved
DSPI_0	SIN	IMCR[41]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[7]
			0010-1111	—	Reserved
DSPI_1	SIN	IMCR[44]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[8]
			0010-1111	—	Reserved
DSPI_2	SIN	IMCR[47]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[13]
			0010	I/O-Pad	A[2]
			0011-1111	—	Reserved
DSPI_2	SCK	IMCR[48]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[0]
			0010	I/O-Pad	A[11]
			0011-1111	—	Reserved
DSPI_2	SC0	IMCR[49]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[3]
			0010	I/O-Pad	A[10]
			0011-1111	—	Reserved
DSPI_3	SIN	IMCR[50]	0000 (Default)	—	Disable
			0001	I/O-Pad	J[1]
			0010	I/O-Pad	D[7]
			0011	I/O-Pad	D[14]
			0100	I/O-Pad	E[15]
			0101-1111	—	Reserved
DSPI_3	SCK	IMCR[51]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[6]
			0010	I/O-Pad	D[11]
			0011	I/O-Pad	E[13]
			0100	I/O-Pad	I[15]
			0101-1111	—	Reserved

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
DSPI_3	CS0	IMCR[52]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[11]
			0010	I/O-Pad	D[10]
			0011	I/O-Pad	F[5]
			0100	I/O-Pad	I[14]
			0101-1111	—	Reserved
eTimer_0	ETC0	IMCR[59]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[10]
			0010	I/O-Pad	A[0]
			0011-1111	—	Reserved
eTimer_0	ETC1	IMCR[60]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[11]
			0010	I/O-Pad	A[1]
			0011-1111	—	Reserved
eTimer_0	ETC2	IMCR[61]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[0]
			0010	I/O-Pad	A[2]
			0011-1111	—	Reserved
eTimer_0	ETC3	IMCR[62]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[14]
			0010	I/O-Pad	A[3]
			0011-1111	—	Reserved
eTimer_0	ETC4	IMCR[63]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[14]
			0010	I/O-Pad	G[3]
			0011	I/O-Pad	A[4]
			0100	I/O-Pad	C[11]
			0101-1111	—	Reserved
eTimer_0	ETC5	IMCR[64]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[8]
			0010	I/O-Pad	G[4]
			0011	I/O-Pad	C[12]
			0100	I/O-Pad	E[13]
			0101-1111	—	Reserved
eTimer_1	ETC0	IMCR[65]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[4]
			0010	I/O-Pad	C[15]
			0011-1111	—	Reserved

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
eTimer_1	ETC1	IMCR[66]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[13]
			0010	I/O-Pad	D[0]
			0011-1111	—	Reserved
eTimer_1	ETC2	IMCR[67]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[0]
			0010	I/O-Pad	C[14]
			0011	I/O-Pad	D[1]
			0100-1111	—	Reserved
eTimer_1	ETC3	IMCR[68]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[1]
			0010	I/O-Pad	D[2]
			0011	I/O-Pad	F[12]
			0100-1111	—	Reserved
eTimer_1	ETC4	IMCR[69]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[14]
			0010	I/O-Pad	D[3]
			0011	I/O-Pad	D[8]
			0100	I/O-Pad	F[13]
			0101-1111	—	Reserved
eTimer_1	ETC5	IMCR[70]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[5]
			0010	I/O-Pad	A[15]
			0011	I/O-Pad	D[4]
			0100	I/O-Pad	E[14]
			0101-1111	—	Reserved
eTimer_2	ETC0	IMCR[71]	0000 (Default)	—	Disable
			0001	I/O-Pad	H[4]
			0010	I/O-Pad	I[0]
			0011-1111	—	Reserved
eTimer_2	ETC1	IMCR[72]	0000 (Default)	—	Disable
			0001	I/O-Pad	H[7]
			0010	I/O-Pad	I[1]
			0011-1111	—	Reserved

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Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
eTimer_2	ETC2	IMCR[73]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[6]
			0010	I/O-Pad	H[10]
			0011	I/O-Pad	I[2]
			0100	I/O-Pad	J[8]
			0101-1111	—	Reserved
eTimer_2	ETC3	IMCR[74]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[7]
			0010	I/O-Pad	H[13]
			0011	I/O-Pad	I[3]
			0100-1111	—	Reserved
eTimer_2	ETC4	IMCR[75]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[8]
			0010	I/O-Pad	H[14]
			0011	I/O-Pad	I[9]
			0100	I/O-Pad	J[8]
			0101-1111	—	Reserved
eTimer_2	ETC5	IMCR[76]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[9]
			0010	I/O-Pad	H[15]
			0011	I/O-Pad	I[10]
			0100	I/O-Pad	J[9]
			0101-1111	—	Reserved
FlexPWM_0	FAULT0	IMCR[83]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[9]
			0010	I/O-Pad	A[13]
			0011	I/O-Pad	G[8]
			0100-1111	—	Reserved
FlexPWM_0	FAULT1	IMCR[84]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[10]
			0010	I/O-Pad	D[6]
			0011	I/O-Pad	G[9]
			0100-1111	—	Reserved
FlexPWM_0	FAULT2	IMCR[85]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[5]
			0010	I/O-Pad	G[10]
			0011-1111	—	Reserved

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
FlexPWM_0	FAULT3	IMCR[86]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[5]
			0010	I/O-Pad	D[8]
			0011	I/O-Pad	G[11]
			0100-1111	—	Reserved
FlexPWM_0	EXT_SYNC	IMCR[87]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[13]
			0010	I/O-Pad	C[15]
			0011-1111	—	Reserved
FlexPWM_0	A0	IMCR[88]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[11]
			0010	I/O-Pad	D[10]
			0011-1111	—	Reserved
FlexPWM_0	B0	IMCR[89]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[10]
			0010	I/O-Pad	D[11]
			0011-1111	—	Reserved
FlexPWM_0	A1	IMCR[91]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[7]
			0010	I/O-Pad	C[15]
			0011	I/O-Pad	F[0]
			0100-1111	—	Reserved
FlexPWM_0	B1	IMCR[92]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[6]
			0010	I/O-Pad	D[0]
			0011	I/O-Pad	D[14]
			0100-1111	—	Reserved
FlexPWM_0	X1	IMCR[93]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[4]
			0010	I/O-Pad	D[12]
			0011-1111	—	Reserved
FlexPWM_0	A2	IMCR[94]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[11]
			0010	I/O-Pad	A[12]
			0011	I/O-Pad	G[3]
			0100-1111	—	Reserved

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
FlexPWM_0	B2	IMCR[95]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[12]
			0010	I/O-Pad	A[13]
			0011	I/O-Pad	G[4]
			0100-1111	—	Reserved
FlexPWM_0	X2	IMCR[96]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[10]
			0010	I/O-Pad	G[2]
			0011-1111	—	Reserved
FlexPWM_0	A3	IMCR[97]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[2]
			0010	I/O-Pad	C[10]
			0011	I/O-Pad	D[3]
			0100	I/O-Pad	G[6]
			0101-1111	—	Reserved
FlexPWM_0	B3	IMCR[98]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[3]
			0010	I/O-Pad	A[9]
			0011	I/O-Pad	D[4]
			0100	I/O-Pad	G[7]
			0101-1111	—	Reserved
FlexPWM_0	X3	IMCR[99]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[2]
			0010	I/O-Pad	D[6]
			0011	I/O-Pad	G[5]
			0100-1111	—	Reserved
FlexPWM_1	FAULT0	IMCR[100]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[0]
			0010-1111	—	Reserved
FlexPWM_1	FAULT1	IMCR[101]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[1]
			0010-1111	—	Reserved
FlexPWM_1	FAULT2	IMCR[102]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[2]
			0010-1111	—	Reserved
FlexPWM_1	FAULT3	IMCR[103]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[3]
			0010-1111	—	Reserved

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
FlexPWM_1	A0	IMCR[105]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[13]
			0010	I/O-Pad	H[5]
			0011-1111	—	Reserved
FlexPWM_1	B0	IMCR[106]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[14]
			0010	I/O-Pad	H[6]
			0011-1111	—	Reserved
FlexPWM_1	A1	IMCR[109]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[12]
			0010	I/O-Pad	H[8]
			0011-1111	—	Reserved
FlexPWM_1	B1	IMCR[110]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[13]
			0010	I/O-Pad	H[9]
			0011-1111	—	Reserved
FlexPWM_1	A2	IMCR[112]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[4]
			0010	I/O-Pad	H[11]
			0011-1111	—	Reserved
FlexPWM_1	B2	IMCR[113]	0000	—	Disable
			0001	I/O-Pad	E[14]
			0010	I/O-Pad	H[12]
			0011-1111	—	Reserved
FlexRay	FR_A_RX	IMCR[136]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[1]
			0010-1111	—	Reserved
FlexRay	FR_B_RX	IMCR[137]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[2]
			0010-1111	—	Reserved
LIN_0	RXD	IMCR[165]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[3]
			0010	I/O-Pad	B[7]
			0011-1111	—	Reserved
LIN_1	RXD	IMCR[166]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[13]
			0010	I/O-Pad	D[12]
			0011	I/O-Pad	F[15]
			0100-1111	—	Reserved

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
MC_RGM	ABS0	IMCR[169]	0000 (Default)	I/O-Pad	A[2]
			0001	—	Disable
			0010-1111	—	Reserved
MC_RGM	ABS2	IMCR[171]	0000 (Default)	I/O-Pad	A[3]
			0001	—	Disable
			0010-1111	—	Reserved
MC_RGM	FAB	IMCR[172]	0000 (Default)	I/O-Pad	A[4]
			0001	—	Disable
			0010-1111	—	Reserved
SIUL	REQ0	IMCR[173]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[0]
			0010-1111	—	Reserved
SIUL	REQ1	IMCR[174]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[1]
			0010-1111	—	Reserved
SIUL	REQ2	IMCR[175]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[2]
			0010-1111	—	Reserved
SIUL	REQ3	IMCR[176]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[3]
			0010-1111	—	Reserved
SIUL	REQ4	IMCR[177]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[4]
			0010-1111	—	Reserved
SIUL	REQ5	IMCR[178]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[5]
			0010-1111	—	Reserved
SIUL	REQ6	IMCR[179]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[6]
			0010-1111	—	Reserved
SIUL	REQ7	IMCR[180]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[7]
			0010-1111	—	Reserved
SIUL	REQ8	IMCR[181]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[8]
			0010-1111	—	Reserved
SIUL	REQ9	IMCR[182]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[10]
			0010-1111	—	Reserved

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
SIUL	REQ10	IMCR[183]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[11]
			0010-1111	—	Reserved
SIUL	REQ11	IMCR[184]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[12]
			0010-1111	—	Reserved
SIUL	REQ12	IMCR[185]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[13]
			0010-1111	—	Reserved
SIUL	REQ13	IMCR[186]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[14]
			0010-1111	—	Reserved
SIUL	REQ14	IMCR[187]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[15]
			0010-1111	—	Reserved
SIUL	REQ15	IMCR[188]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[0]
			0010-1111	—	Reserved
SIUL	REQ16	IMCR[189]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[1]
			0010-1111	—	Reserved
SIUL	REQ17	IMCR[190]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[2]
			0010-1111	—	Reserved
SIUL	REQ18	IMCR[191]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[6]
			0010-1111	—	Reserved
SIUL	REQ19	IMCR[192]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[14]
			0010-1111	—	Reserved
SIUL	REQ20	IMCR[193]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[15]
			0010-1111	—	Reserved
SIUL	REQ21	IMCR[194]	0000 (Default)	—	Disable
			0001	I/O-Pad	G[8]
			0010-1111	—	Reserved
SIUL	REQ22	IMCR[195]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[4]
			0010-1111	—	Reserved

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
SIUL	REQ23	IMCR[196]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[5]
			0010-1111	—	Reserved
SIUL	REQ24	IMCR[197]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[6]
			0010-1111	—	Reserved
SIUL	REQ25	IMCR[198]	0000 (Default)	—	Disable
			0001	I/O-Pad	E[13]
			0010-1111	—	Reserved
SIUL	REQ26	IMCR[199]	0000 (Default)	—	Disable
			0001	I/O-Pad	E[14]
			0010-1111	—	Reserved
SIUL	REQ27	IMCR[200]	0000 (Default)	—	Disable
			0001	I/O-Pad	E[15]
			0010-1111	—	Reserved
SIUL	REQ28	IMCR[201]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[0]
			0010-1111	—	Reserved
SIUL	REQ29	IMCR[202]	0000 (Default)	—	Disable
			0001	I/O-Pad	G[9]
			0010-1111	—	Reserved
SIUL	REQ30	IMCR[203]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[12]
			0010-1111	—	Reserved
SIUL	REQ31	IMCR[204]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[13]
			0010-1111	—	Reserved
SENT_0	SENT_RX[0]	IMCR[205]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[5]
			0010	I/O-Pad	I[7]
			0011	I/O-Pad	G[8]
			0100-1111	—	Reserved
SENT_0	SENT_RX[1]	IMCR[206]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[11]
			0010	I/O-Pad	J[5]
			0011	I/O-Pad	A[9]
			0100	I/O-Pad	G[10]
			0101-1111	—	Reserved

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Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
SENT_1	SENT_RX[0]	IMCR[213]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[7]
			0010	I/O-Pad	I[8]
			0011	I/O-Pad	G[9]
			0100	I/O-Pad	C[12]
			0101-1111	—	Reserved
SENT_1	SENT_RX[1]	IMCR[214]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[12]
			0010	I/O-Pad	J[6]
			0011	I/O-Pad	A[10]
			0100	I/O-Pad	G[11]
			0101-1111	—	Reserved
ENET_0	RX_CLK	IMCR[224]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[8]
			0010-1111	—	Reserved
ENET_0	RX_DV	IMCR[225]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[7]
			0010-1111	—	Reserved
ENET_0	RX_D0	IMCR[226]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[6]
			0010-1111	—	Reserved
ENET_0	RX_D1	IMCR[227]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[5]
			0010-1111	—	Reserved
ENET_0	RX_D2	IMCR[228]	0000 (Default)	—	Disable
			0001	I/O-Pad	H[8]
			0010-1111	—	Reserved
ENET_0	RX_D3	IMCR[229]	0000 (Default)	—	Disable
			0001	I/O-Pad	J[9]
			0010-1111	—	Reserved
ENET_0	COL	IMCR[230]	0000 (Default)	—	Disable
			0001	I/O-Pad	H[5]
			0010-1111	—	Reserved
ENET_0	CRS	IMCR[231]	0000 (Default)	—	Disable
			0001	I/O-Pad	H[4]
			0010-1111	—	Reserved
ENET_0	RX_ER	IMCR[232]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[1]
			0010-1111	—	Reserved

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
ENET_0	TX_CLK	IMCR[233]	0000 (Default)	—	Disable
			0001	I/O-Pad	G[8]
			0010-1111	—	Reserved

1. (Default) = configuration after reset
2. Selecting an alternate function with a 'Reserved' source function causes the pin to enter a null state (Input buffer and Output buffer enables both at 0).

Table 11. Peripheral muxing example

SSS field value in IMCR[214]	Result
0001	I/O-Pad I[12] is connected to SENT_1 Receive input SENT_RX[1]
0010	I/O-Pad J[6] is connected to SENT_1 Receive input SENT_RX[1]

See Table 9 concerning the availability of port pins on the packages.

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

This device is designed to operate at 200 MHz.

3.2 165°C junction temperature option

For orderable parts whose device marking shows they support this extended temperature option:

- Operation at 150°C < T_J < 165°C is allowed for a maximum cumulative time of 200 hours over the device lifetime.
- Production parameters at 165°C reflect testing over an ambient temperature range of –40°C to 150°C with appropriate guardbanding to guarantee operation at 165°C.

3.3 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed.

CAUTION

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 12. Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD_LV}	1.25 V core supply voltage[1, 2, 3]	—	–0.3	1.5	V
$V_{DD\_LV\_PLL}$	1.25 V PLL supply voltage[1, 2, 3]	—	–0.3	1.5	V
$V_{DD\_LV\_LFAST}$	1.25 V LFAST PLL supply voltage[1, 2, 3]	—	–0.3	1.5	V
$V_{DD\_LV\_NEXUS}$	1.25 V Aurora LVDS supply voltage[1, 2, 3]	—	–0.3	1.5	V
$V_{DD\_HV\_PMU}$	3.3 V voltage regulator supply voltage	—	–0.3	4.0[4, 5]	V
$V_{DD\_HV\_IO}$	3.3 V input/output supply voltage	—	–0.3	3.63[4, 5]	V
$V_{SS\_HV\_IO}$	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD\_HV\_FLA}$	3.3 V flash supply voltage	—	–0.3	3.63[4, 5]	V
$V_{SS\_HV\_FLA}$	Flash memory ground	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	3.3 V crystal oscillator amplifier supply voltage	—	–0.3	4.0[4, 5]	V
$V_{SS\_HV\_OSC}$	3.3 V crystal oscillator amplifier ground	—	–0.1	0.1	V
$V_{DD\_HV\_ADRE0}$[6] $V_{DD\_HV\_ADRE1}$	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	–0.3	6	V
$V_{SS\_HV\_ADRE0}$ $V_{SS\_HV\_ADRE1}$	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADV}$	3.3 V ADC supply voltage	—	–0.3	4.0[4, 5]	V
$V_{SS\_HV\_ADV}$	3.3 V ADC supply ground	—	–0.1	0.1	V
TV_{DD}	Supply ramp rate	—	0.9 V/s	0.06 V/µs	
V_{INA}	Voltage on analog pin with respect to ground ($V_{SS\_HV\_IO}$)	—	–0.3	6	V
V_{IN}	Voltage on any digital pin with respect to ground ($V_{SS\_HV\_IO}$)	Relative to $V_{DD\_HV\_IO}$	–0.3	$V_{DD\_HV\_IO}$ + 0.3[7]	V
I_{INJ}	Maximum DC injection current per pin, 5 V pads	Note [8]	–5	5	mA
I_{INJPAD}	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{STG}	Storage temperature	—	–55	165	°C

1. 1.45 V to 1.5 V allowed for 60 seconds cumulative time at maximum T_J=165°C; remaining time as defined in note 2 and note 3.
2. 1.375 V to 1.45 V allowed for 10 hours cumulative time at maximum T_J=165°C; remaining time as defined in note 3.
3. 1.32 V to 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum T_J=165°C.
4. 5.3 V for 10 hours cumulative over lifetime of device; 3.3 V +10% for time remaining.
5. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
6. $V_{DD\_HV\_ADRE0}$ and $V_{DD\_HV\_ADRE1}$ cannot be operated at different voltages and must be supplied by the same voltage source.
7. Only when $V_{DD\_HV\_IO}$ < 3.63 V.
8. The following conditions apply:
   - Absolute maximum supply: $V_{DD\_HV\_IO}$ = 6.0 V (60 seconds lifetime, no restrictions—part can switch)
   - Absolute maximum supply: $V_{DD\_HV\_IO}$ = 6.0 V (10 hours, device in reset—no switching)
   - Absolute maximum supply: $V_{DD\_HV\_IO}$ = 5.5 V (always)
   - Absolute maximum I/O pin voltage = 7.0 V (60 seconds lifetime)
   - Absolute maximum I/O pin voltage = 6.5 V (always while respecting 5 mA maximum injection)

3.4 Recommended operating conditions

NOTE

Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and DC electrical specifications for I/Os might not be guaranteed.

Table 13. Recommended operating conditions ($V_{DD\_HV\_xx}$ = 3.3 V)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD\_HV\_PMU}$[1]	3.3 V voltage regulator supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_IO}$[2]	3.3 V input/output supply voltage	—	3.15	3.6	V
$V_{SS\_HV\_IO}$	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FLA}$[3]	3.3 V flash supply voltage	—	3.15	3.6	V
$V_{SS\_HV\_FLA}$	Flash memory ground	—	0	0	V
$V_{DD\_HV\_OSC}$[4]	3.3 V crystal oscillator amplifier supply voltage	—	3.15	3.6	V
$V_{SS\_HV\_OSC}$	3.3 V crystal oscillator amplifier ground	—	0	0	V
$V_{DD\_HV\_ADRE0}$[5] $V_{DD\_HV\_ADRE1}$	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	$T_J \le 150°C$	3.15 to 5.5		V
$V_{DD\_HV\_ADRE0}$[5] $V_{DD\_HV\_ADRE1}$	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	150°C < T_J < 165°C (only for corresponding marked parts)	3.15 to 5.25		V
$V_{SS\_HV\_ADRE0}$[5] $V_{SS\_HV\_ADRE1}$	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	0	0	V
$V_{DD\_HV\_ADV}$[6]	3.3 V ADC supply voltage	—	3.15	3.6	V
$V_{SS\_HV\_ADV}$	3.3 V ADC supply ground	—	0	0	V
$V_{DD\_LV\_COR}$[7]	Core supply, 1.25 V +/-5%	—	1.19	1.32	V
$V_{DD\_LV\_CORx}$	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$	Internal reference voltage	—	0	0	V

Table continues on the next page...

Table 13. Recommended operating conditions ($V_{DD\_HV\_xx}$ = 3.3 V) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD\_LV\_PLL}$	Internal PLL supply voltage	—	1.19	1.32	V
$V_{SS\_LV\_PLL}$	Internal PLL reference voltage	—	0	0	V
$V_{DD\_LV\_NEXUS}$	Aurora LVDS supply voltage	—	1.19	1.32	V
$V_{SS\_LV\_NEXUS}$	Aurora LVDS supply ground	—	0	0	V
$V_{DD\_LV\_LFAST}$	LFAST PLL supply voltage	—	1.19	1.32	V
$V_{SS\_LV\_LFAST}$	LFAST PLL supply ground	—	0	0	V
I_{IC}	DC injection current per pin[8, 9, 10]	Digital pins	–3.0	3.0	mA
		Analog pins	–3.0	3.0	
		Shared analog pins	–3.6	3.6	
T_A	Ambient temperature under bias	f_{CPU}≤ 200MHz	–40	135[11]	°C
T_J	Junction temperature under bias	—	–40	165[12, 13]	°C

1. The chip functions down to the point where LVD_PMC resets the chip. When the voltage drops below LVD_PMC, the chip resets.
2. The chip functions down to the point where LVD_IO resets the chip. When the voltage drops below LVD_IO, the chip resets.
3. The chip functions down to the point where LVD_FLASH resets the chip. When the voltage drops below LVD_FLASH, the chip resets.
4. The chip functions down to the point where LVD_OSC resets the chip. When the voltage drops below LVD_OSC, the chip resets.
5. $V_{DD\_HV\_ADRE0}$ and $V_{DD\_HV\_ADRE1}$ cannot be operated at different voltages and need to be supplied by the same voltage source.
6. The chip functions down to the point where LVD_ADC resets the chip. When the voltage drops below LVD_ADC, the chip resets.
7. The chip functions down to the point where LVD_CORE or up to the point where HVD_CORE resets the chip by default.
8. I/O and analog input specifications are valid only if the injection current on adjacent pins is within these limits. See the absolute maximum ratings table for maximum input current for reliability requirements.
9. Full device lifetime without performance degradation.
10. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current will be injected through the clamp diode to the supply rail. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
11. For a maximum T_J of 150°C, the corresponding maximum T_A is 125°C.
12. Some orderable parts have a maximum T_J value of 150°C. See the device marking for the applicable temperature range.
13. For devices supporting the 165°C junction temperature option: Operation at 150°C < T_J < 165°C is allowed for a maximum cumulative time of 200 hours over the device lifetime.

3.5 Thermal characteristics

Table 14. Thermal characteristics for 144LQFP and 257MAPBGA packages

Symbol	Parameter	Conditions	144LQFP	257MAPBGA	Unit
$R_{\theta JA}$	Thermal resistance, junction-to-ambient natural convection[1, 2]	Single layer board - 1s[3]	39	45	°C/W
		Four layer board - 2s2p[4]	31	25	
$R_{\theta JMA}$	Thermal resistance, junction-to-ambient forced convection at 200 ft/min[1]	Single layer board - 1s[3]	31	36	°C/W
		Four layer board - 2s2p[4]	25	21	
$R_{\theta JB}$	Thermal resistance junction-to-board[5]	—	18	13	°C/W

Table continues on the next page...

Table 14. Thermal characteristics for 144LQFP and 257MAPBGA packages (continued)

Symbol	Parameter	Conditions	144LQFP	257MAPBGA	Unit
$R_{\theta JC}$	Thermal resistance junction-to-case[6]	—	8	8	°C/W
Ψ_{JT}	Junction-to-package-top natural convection[7]	—	2	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. Board temperature is measured on the top surface of the board near the package.
6. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
7. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.5.1.1 References

Semiconductor Equipment and Materials International; 3081 Zanker Road; San Jose, CA 95134 USA; (408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the Web at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.

3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.6 Electromagnetic compatibility (EMC)

Tests were carried out in accordance with the International Electrotechnical Commission specifications:

- IEC 61967: Integrated Circuits, Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz
- IEC 61967-2: Measurement of radiated emissions – TEM-cell and wideband TEM-cell method

Parameter	Test #	Conditions[1]		Classification level[2]	Unit
		Comm. modules[3]	GPIO		
V_{EME}	1	On	Off, input pull-up	L	dBµV
	2	On	Off, input pull-up	L	dBµV
	3	On	Off, input pull-up	L	dBµV
	4	On	Off, input pull-up	—[4]	dBµV
	5	On	Off, input pull-up	L	dBµV
	6	On	PG1[5] input, pull-up	L	dBµV
	7	Off	PG1[5] output high, half drive	L	dBµV
	8	Off	PG1[5] output high, full drive	L	dBµV
	9	Off	PG1[5] output low, half drive	L	dBµV
	10	Off	PG1[5] output low, full drive	L	dBµV
	11	Off	All I/O tri-stated	I	dBµV
	12	Off	PG2[6] toggle @ 5 kHz, half drive, SR off	L	dBµV
	13	Off	PG2[6] toggle @ 5 kHz, half drive, SR on	L	dBµV
	14	Off	PG2[6] toggle @ 5 kHz, full drive, SR off	L	dBµV
	15	Off	PG2[6] toggle @ 5 kHz, full drive, SR on	I	dBµV

1. All tests ran with core and bus frequency at 200 MHz. Test #2 had "weak" FM modulation and Test #3 had "strong" FM modulation.
2. I = Class 1 (36 dBµV), L = Class 2 (24 dBµV), N = Class 3 (12 dBµV)
3. LINFlex0/1 running at 19.2 kbd, SPI0 running at 2.5 MHz, SPI1 running at 7.5 MHz, SPI2 running at 4.5 MHz, CAN0/1 running at 500 kbd
4. Test #4 values were slightly above class I level.
5. PG1 = port group 1: pins F[3:15]
6. PG2 = port group 2: pins A[2:4], C[11:14], D14, F12, G6, J8

Each of the tests ran once across each of the following frequency bands.

Frequency band	RBW (kHz)	VBW (kHz)	Sweep time (ms/MHz)	Pre-amplifier	Detector
150 kHz to 30 MHz	9	30	5	ON (–20 dB)	Peak-Average
30 MHz to 1000 MHz	120	300			

3.7 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements.

Table 15. ESD ratings

No.	Symbol	Parameter	Conditions[1]	Class	Max value	Unit
1	$V_{ESD(HBM)}$	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

3.8 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- High power regulator (external NPN to support core current)
- Low voltage detector (LVD_IO) for 3.3 V supply to IO ($V_{DD\_HV\_IO}$)
- Low voltage detector (LVD_PMC) for 3.3 V supply ($V_{DD\_HV\_PMU}$)
- Low voltage detector (LVD_FLASH) for 3.3 V flash memory supply ($V_{DD\_HV\_FLA}$)
- Low voltage detector (LVD_ADC) for 3.3 V ADC supply ($V_{DD\_HV\_ADV}$)
- Low voltage detector (LVD_OSC) for 3.3 V OSC supply ($V_{DD\_HV\_OSC}$)
- Low voltage detector (LVD_CORE) for 1.25 V digital core supply (V_{DD_LV})

- Low voltage detector (LVD_CORE_BK) for the self-test of LVD_CORE
- High voltage detector (HVD_CORE) for 1.25 V digital core supply (V_{DD_LV})
- High voltage detector (HVD_CORE_BK) for the self-test of HVD_CORE
- Power on Reset (POR)

The following bipolar transistor is supported:

- ON Semiconductor™ NJD2873 (requires a heat sink to operate up to 165 °C): See Table 16.

Table 16. Recommended operating characteristics: NJD2873

Symbol	Parameter	Value	Unit
h_{FE}	DC current gain (Beta)	60-550	—
P_D	Absolute minimum power dissipation	1.60	W
I_{CMaxDC}	Minimum peak collector current	2.0	A
VCE_{SAT}	Collector to emitter saturation voltage	300	mV
V_{BE}	Base to emitter voltage	0.95	V
V_c	Minimum voltage at transistor collector	2.5	V

Table 17. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{ld}	External decoupling / stability capacitor	Min value granted with respect to tolerance, voltage, temperature, and aging variations	4	—	—	µF
—	Combined ESR of external capacitor	—	0.03	—	0.15	Ω
t_{SU}	Start-up time after main supply stabilization	C_{ld} = 4 µF	—	—	2.5	ms
L_{bw}	Bonding inductance	—	—	—	13	nH
R_{bw}	Bonding wire and pad resistance	—	—	—	0.5	Ω
R_{sd}	Series resistance of on-chip power grid	—	—	—	0.1	Ω
C_{pd}	Parallel decoupling capacitor	Per pin; must use at least 6 capacitors, but total of all capacitors must be no more than 300 nF	47	—	—	nF
—	Power supply rejection (C_{ld} = 4 µF)	@DC no load @200 kHz no load @DC 400 mA @200 kHz 400 mA	—	—	–23 –23 –23 –23	dB

Table continues on the next page...

Table 17. Voltage regulator electrical specifications (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
—	Load current transient	Iload from 20% to 80% C_{ld} = 4 µF	—	—	1.0	µs
—	Supply ramp rate VDD12_CORE	—	0.01 V/ ms	—	0.125 V/ µs	
—	Supply ramp rate VDD33_REG	—	0.9 V/s	—	0.06 V/ µs	
—	POR VDD12_CORE	—	0.98	1.02	1.08	V
—	POR VDD33_REG	—	2.4	2.59	2.76	V
—	LVD_CORE, LVD_CORE_BK	calibrated (trimmed)	1.12	1.15	1.18	V
—	HVD_CORE, HVD_CORE_BK	calibrated (trimmed)	1.32	1.36	1.40	V
—	LVD_PMC	calibrated (trimmed)	2.93	3.02	3.13	V
—	LVD_IO	calibrated (trimmed)	2.93	3.02	3.13	V
—	LVD_FLASH	calibrated (trimmed)	2.93	3.02	3.13	V
—	LVD_ADC	calibrated (trimmed)	2.93	3.02	3.13	V
—	LVD_OSC	calibrated (trimmed)	2.93	3.02	3.13	V
—	Hysteresis LVD_CORE	—	—	10	—	mV
—	Hysteresis HVD_CORE	—	—	—	—	mV
—	Hysteresis LVD_PMC, LVD_IO, LVD_FLASH, LVD_ADC, LVD_OSC	—	—	20	—	mV
—	LVD/HVD trimming	16 steps	—	5	—	mV
T_J	Junction Temperature	—	–40	—	165	°C

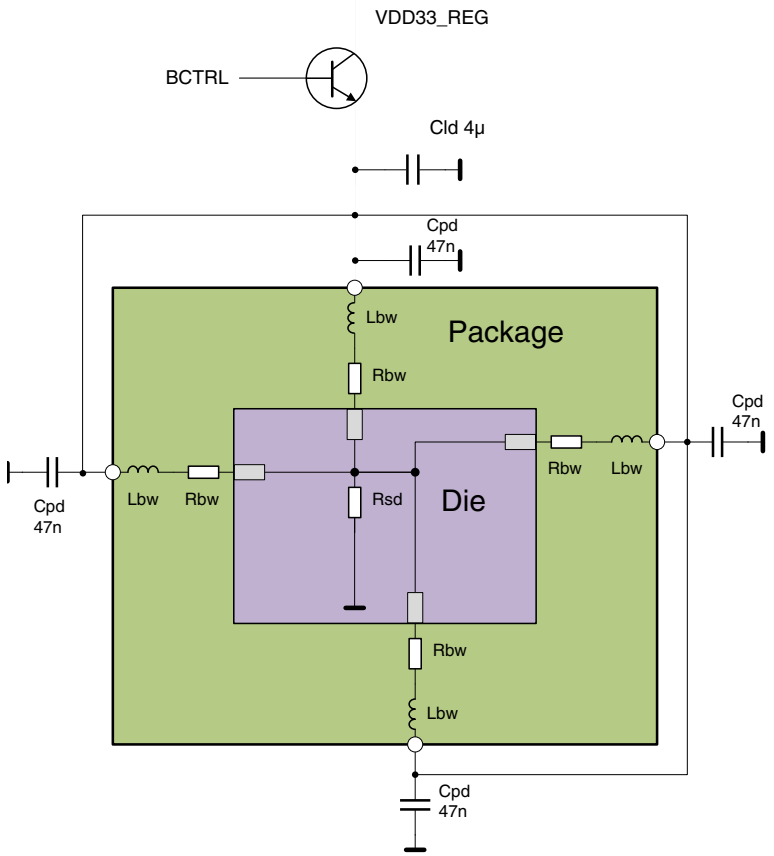


Figure 4. Core supply decoupling and parasitics

3.9 DC electrical characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 18 provides output driver characteristics FlexRay I/Os (SYM).
- Table 19 provides output driver characteristics for LFAST I/Os.

NOTE

See the FlexRay section for parameters dedicated to this interface.

Table 18. FlexRay (SYM) configuration output buffer electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
R_{OH_Y}	PMOS output impedance SYM configuration	Push Pull, I_{OH} = 2 mA, $V_{OH} = V_{DD\_HV\_IO}$–(0.28...0.52V)	35	50	65	Ω
R_{OL_Y}	PMOS output impedance SYM configuration	Push Pull, I_{OL} = 2 mA, V_{OL} = 0.28...0.52 V	35	50	65	Ω

Table continues on the next page...

Table 18. FlexRay (SYM) configuration output buffer electrical characteristics (continued)

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
F_{max_Y}	Output frequency SYM configuration	C_L = 20 pF, $V_{DD\_HV\_IO}$=3.3 V –5%, +10%	—	—	50	MHz
T_{tr_Y}	Transition time output pin SYM configuration	C_L = 20 pF, $V_{DD\_HV\_IO}$=3.3 V –5%, +10%	1	—	6	ns
$\lvert T_{skew\_Y} \rvert$	Difference between rise and fall time	—	0	—	1	ns

1. $V_{DD\_HV\_IO}$ = 3.3 V (–5%, +10%), T_J = –40 to 165 °C, unless otherwise specified.

NOTE

See the LFAST section for parameters dedicated to this interface.

Table 19. LFAST output buffer electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
$\lvert \Delta_{VO\_L} \rvert$	Absolute value for differential output voltage swing (terminated)	—	100	200	285	mV
V_{ICOM_L}	Common mode voltage	—	1.08	1.2	1.32	V
T_{tr_L}	Transition time output pin LVDS configuration	—	0.2	—	1.5	ns

1. $V_{DD\_HV\_IO}$ = 3.3 V (–5%, +10%), T_J = –40 to 165 °C, unless otherwise specified.

NOTE

Fast IOs must be specified only as fast (and not as high current). See Table 20.

Table 20. DC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{DD_LV}[1]	LV (core) Supply Voltage	—	1.19	—	1.32	V
$V_{DD\_HV\_IO}$[1]	I/O Supply Voltage	—	3.15	—	3.6	V
V_{IH}	CMOS Input Buffer High Voltage (with hysteresis disabled)	—	0.55 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{IL}	CMOS Input Buffer Low Voltage (with hysteresis disabled)	—	Vss - 0.3	—	0.40 * $V_{DD\_HV\_IO}$	V
V_{HYS}	CMOS Input Buffer Hysteresis	—	0.1 * $V_{DD\_HV\_IO}$	—	—	V
$Pull\_I_{OH}$	Weak Pullup Current[2]	—	10	—	80	µA
$Pull\_I_{OL}$	Weak Pulldown Current[3]	—	10	—	80	µA

Table continues on the next page...

Table 20. DC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{INACT_D}	Digital Pad Input Leakage Current (weak pull inactive)[4]	—	-2.5	—	2.5	µA
V_{OH}	Output High Voltage[5]	—	0.8 * $V_{DD\_HV\_IO}$	—	—	V
V_{OL}	Output Low Voltage[6]	—	—	—	0.2 * $V_{DD\_HV\_IO}$	V
I_{OH_F}	Full drive I_{OH} (SIUL2_MSCRn's SRC[1:0] field is 11b)	—	10	—	180	mA
I_{OL_F}	Full drive I_{OL} (SIUL2_MSCRn's SRC[1:0] field is 11b)	—	21	—	230	mA
I_{OH_H}	Half drive I_{OH} (SIUL2_MSCRn's SRC[1:0] field is 10b)	—	9	—	90	mA
I_{OL_H}	Half drive I_{OL} (SIUL2_MSCRn's SRC[1:0] field is 10b)	—	10.5	—	115	mA

1. Max power supply ramp rate is 100 V / ms
2. Measured when pad = 0 V
3. Measured when pad = $V_{DD\_HV\_IO}$
4. The specified values apply to all pads except D[7] (SGEN output pad). For D[7], leakage current specifications are -15µA Min and 15µA Max.
5. Measured when pad is sourcing 2 mA
6. Measured when pad is sinking 2 mA

3.10 Supply current characteristics

Current consumption data is given in the following table.

Table 21. Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
I_{DD_LV} + $I_{DD\_LV\_PLL}$[2]	Operating current	T_A = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	350	400	mA
		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	440	570	
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	470	610	
$I_{DD\_LV\_BIST}$ + $I_{DD\_LV\_PLL}$	Operating current	Normal startup self-test T_A = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	340	—	mA
		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	410	—	
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	430	—	

Table continues on the next page...

Table 21. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_LV\_STOP}$	Operating current in V_{DD} STOP mode	T_A = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	25	35	mA
		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	90	230	
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	120	310	
$I_{DD\_LV\_HALT}$	Operating current in V_{DD} HALT mode	T_A = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	25	40	mA
		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	110	300	
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	140	400	
$I_{DD\_LV\_LFAST}$	Operating current	T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	6.6	mA
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	6.8	
$I_{DD\_LV\_NEXUS}$	Operating current	T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	12.1	mA
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	12.5	
$I_{DD\_HV\_ADV}$[3]	Operating current	T_J = 150 °C 4 ADCs operating at 80 MHz $V_{DD\_HV\_ADV}$ = 3.6 V	—	3.4	4.2	mA
		T_J = 165 °C 4 ADCs operating at 80 MHz $V_{DD\_HV\_ADV}$ = 3.6 V	—	3.5	4.5	
$I_{DD\_HV\_ADRE}$[4]	Operating current	T_J = 150 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 3.6 V	—	0.20	0.28	mA
		T_J = 150 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 5.5 V	—	0.32	0.50	
		T_J = 165 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 3.6 V	—	0.24	0.40	
		T_J = 165 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 5.5 V	—	0.40	0.70	

Table continues on the next page...

Table 21. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_HV\_OSC}$	Operating current	T_J = 150 °C 3.3 V supplies Frequency: 200MHz	—	—	1.6	mA
		T_J = 165 °C 3.3 V supplies Frequency: 200MHz	—	—	1.8	
$I_{DD\_HV\_FLA}$	Operating current	T_J = 150 °C 3.3 V supplies Frequency: 200MHz	—	—	5.5	mA
		T_J = 165 °C 3.3 V supplies Frequency: 200MHz	—	—	7.0	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Enabled modules: ADC0/1, FlexPWM0, eTimer0, two SPIs, two FlexCANs, FlexRay, one LINFlexD, DMA. At maximum frequency. I/O supply current excluded.
3. Internal structures hold the input voltage less than $V_{DD\_HV\_ADV}$ + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
4. This value is the total current for two ADCs.

3.11 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 22. Temperature sensor electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
—	Temperature monitoring range	—	–40	—	165	°C
T_{SENS}	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	Accuracy for linear temperature sensor	T_J = –40 to 150 °C	–3	—	+3	°C
		T_J = 150 to 165 °C	–5	—	+5	
—	Accuracy for temperature-threshold digital flags	T_J = –40 to 150 °C	–5	—	+5	°C
—	Temperature variation for each customer-adjustable trim step	T_J = –40 to 150 °C	0.4	0.7	1.0	°C
—	Operating current	T_J = –40 to 165 °C	—	—	675	µA

3.12 Main oscillator electrical characteristics

This device provides a driver for the oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing EMI and power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between the crystal and the MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter, is also available in cases of parasitic capacitances that cannot be reduced or of using a crystal with high equivalent series resistance. This mode requires special care regarding the serial resistance used to avoid the crystal overdrive.

Two other provided modes are External (EXT Wave) and disable (OFF mode). For EXT Wave, the drive is disabled and an external clock source within the CMOS level based in the analog oscillator supply can be used. When OFF, the EXTAL is pulled down by a 240-kohm resistor and the feedback resistor remains active, connecting XTAL through EXTAL by a 1M resistor.

The following figure describes a simple model of the internal oscillator driver and provides an example of connections for an oscillator.

NOTE

When selecting C1 and C2 in your oscillator circuit, contact the crystal manufacturer for their recommended values. Capacitor loading of the oscillator must be fully characterized at the system level to ensure proper operation.

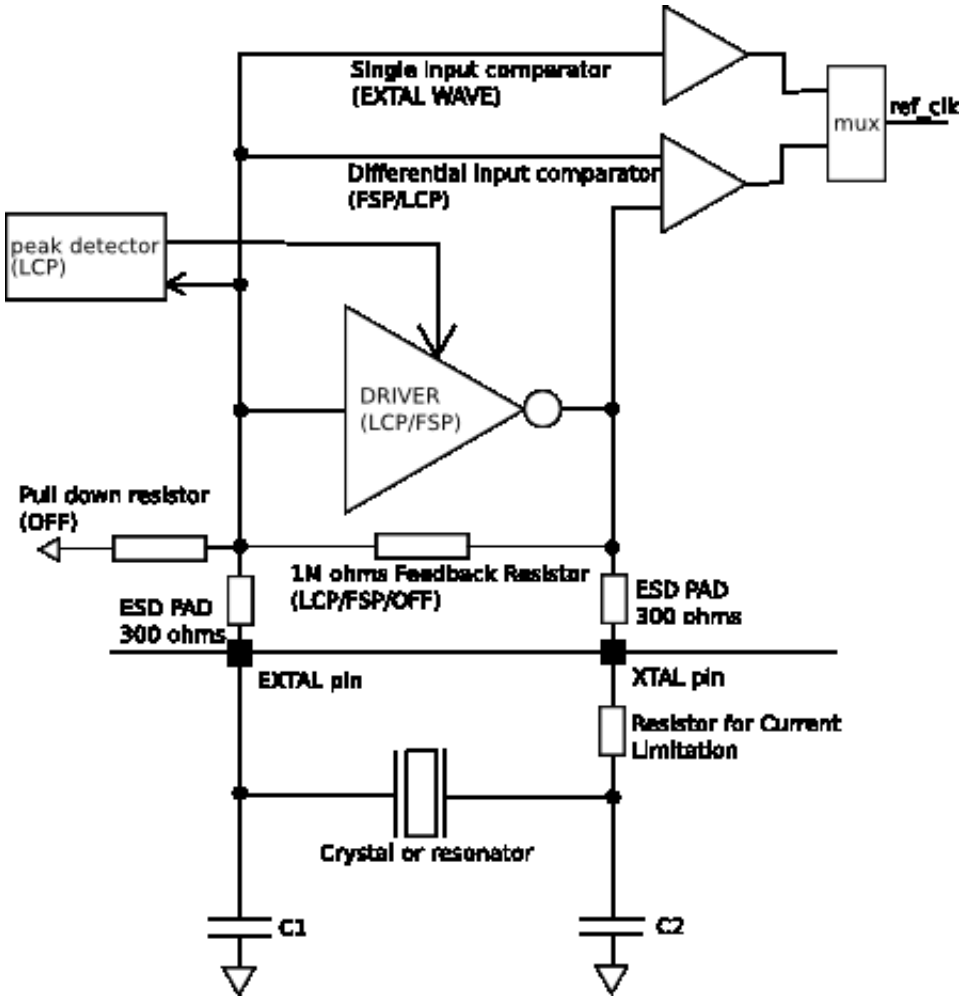


Figure 5. Oscillator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions[1]	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP	—	4[2]	—	40	MHz
$g_{mXOSCHS}$	Driver transconductance	LCP	$V_{DD\_HV\_OSC}$ = 3.3V	—	20	—	mA/V
		FSP	–5%, +10%	—	30	—	
V_{XOSCHS}	Oscillation amplitude	LCP[3]	f_{OSC} = 4, 8, 16 MHz	1.1	1.3	2.6	V
			f_{OSC} = 40 MHz	1.2	1.5	1.7	V
$T_{XOSCHSSU}$	Oscillator startup time	FSP/LCP[3]	f_{OSC} = 4 MHz	1.75	2.5	2.9	ms
			f_{OSC} = 8, 16, 40 MHz	0.25	0.5	1.1	ms

Table continues on the next page...

Table 23. Main oscillator electrical characteristics (continued)

Symbol	Parameter	Mode	Conditions[1]	Min	Typ	Max	Unit
V_{IH}	Input high level CMOS Schmitt Trigger	EXT Wave	Oscillator bypass mode	—	1.48	—	V
V_{IL}	Input low level CMOS Schmitt Trigger	EXT Wave	Oscillator bypass mode	—	1.85	—	V
V_{HYS}	Input low level CMOS Schmitt hysteresis	EXT Wave	Oscillator bypass mode	—	0.37	—	V

1. $V_{DD\_HV\_OSC}$ = 3.3 V –5%, +10%, T_J = 27 °C, unless otherwise specified
2. When using XOSC as the source for PLL0IN, the minimum frequency requirement of the PLL must be fulfilled as stated in the PLL0 electrical characteristics.
3. Values are very dependent on crystal or resonator used and parasitic capacitance observed in the board.

3.13 PLLDIG electrical characteristics

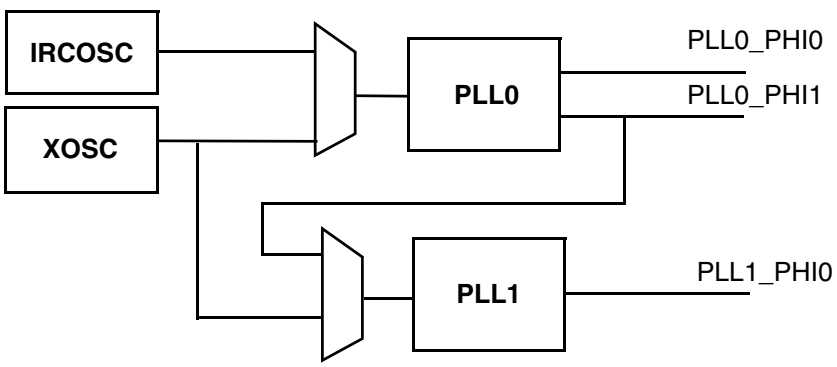


Figure 6. PLL integration

Table 24. PLL0 electrical characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{PLL0IN}	PLL0 input clock[2]	—	8	—	40	MHz
Δ_{PLL0IN}	PLL0 input clock duty cycle[2]	—	40	—	60	%
$f_{PLL0VCO}$	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI0}$	PLL0 output clock PHI0	—	4.76	—	200	MHz
$f_{PLL0PHI1}$	PLL0 output clock PHI1	—	20	—	156	MHz
$t_{PLL0LOCK}$	PLL0 lock time	—	—	—	100	µs
$\lvert\Delta_{PLL0PHISPJ}\rvert$	PLL0_PHI single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI}$ = 400 MHz, 6-sigma	—	—	200	ps
$\lvert\Delta_{PLL0PHI1SPJ}\rvert$	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma	—	—	300[3]	ps

Table continues on the next page...

Table 24. PLL0 electrical characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$\Delta_{PLL0LTJ}$	PLL0 output long term jitter[3] f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	±250	ps
		16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
		long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	PLL0 consumption	FINE LOCK state	—	—	5	mA

1. V_{DD_LV} =1.25 V ± 5%, T_J = -40 to 165 °C unless otherwise specified.
2. PLL0IN clock retrieved directly from either IRCOSC or external XOSC clock. Input characteristics are granted when using IRCOSC or when external oscillator is used in functional mode.
3. VDD_LV noise due to application in the range V_{DD_LV} = 1.25 V±5%, with frequency below PLL bandwidth (40 kHz) will be filtered.

Table 25. FMPLL1 electrical characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{PLL1IN}	PLL1 input clock[2]	—	38	—	78	MHz
Δ_{PLL1IN}	PLL0 input clock duty cycle[2]	—	35	—	65	%
$f_{PLL1VCO}$	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI0}$	PLL1 output clock PHI0	—	4.76	—	200	MHz
$t_{PLL1LOCK}$	PLL1 lock time	—	—	—	100	µs
$f_{PLL1MOD}$	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
		Down spread	0.5	—	4	%
I_{PLL1}	PLL1 consumption	FINE LOCK state	—	—	6	mA

1. V_{DD_LV} = 1.25 V ± 5%, T_J = -40 to 165 °C unless otherwise specified.
2. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock. Input characteristics are granted when using internal PLL0 or when external oscillator is used in functional mode.

3.14 16 MHz Internal RC Oscillator (IRCOSC) electrical specifications

NOTE

Unless stated otherwise, specifications in Table 26 assume the following: $V_{DD\_HV\_PMU}$=3.15V to 3.6V, V_{SS}=0V, V_{DD_LV}=1.18V to 1.32V, V_{SS}=0V, T_J=–40 to 165°C.

Table 26. Internal RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{Target}	IRCOSC target frequency	—	—	16	—	MHz

Table continues on the next page...

Table 26. Internal RC Oscillator electrical specifications (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{Untrimmed}$	IRCOSC frequency (untrimmed)	—	9.6	—	24	MHz
δF_{var_noT}[1]	IRC frequency variation without temperature compensation	T_J < 150 °C	–8	—	8	%
		T_J < 165 °C	–10	—	10	
$T_{startup}$	Startup time without temperature compensation	—	—	—	5	µs
I_{VDD3}	Current consumption on 3.3 V power supply	After $T_{startup}$	—	—	55	µA
I_{VDD12}	Current consumption on 1.2 V power supply	After $T_{startup}$	—	—	270	µA

1. The typical user trim step size (dfTRIM) is +48kHz for frequencies trimmed above nominal and -40kHz for frequencies trimmed below nominal based on characterization results.

3.15 ADC electrical characteristics

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

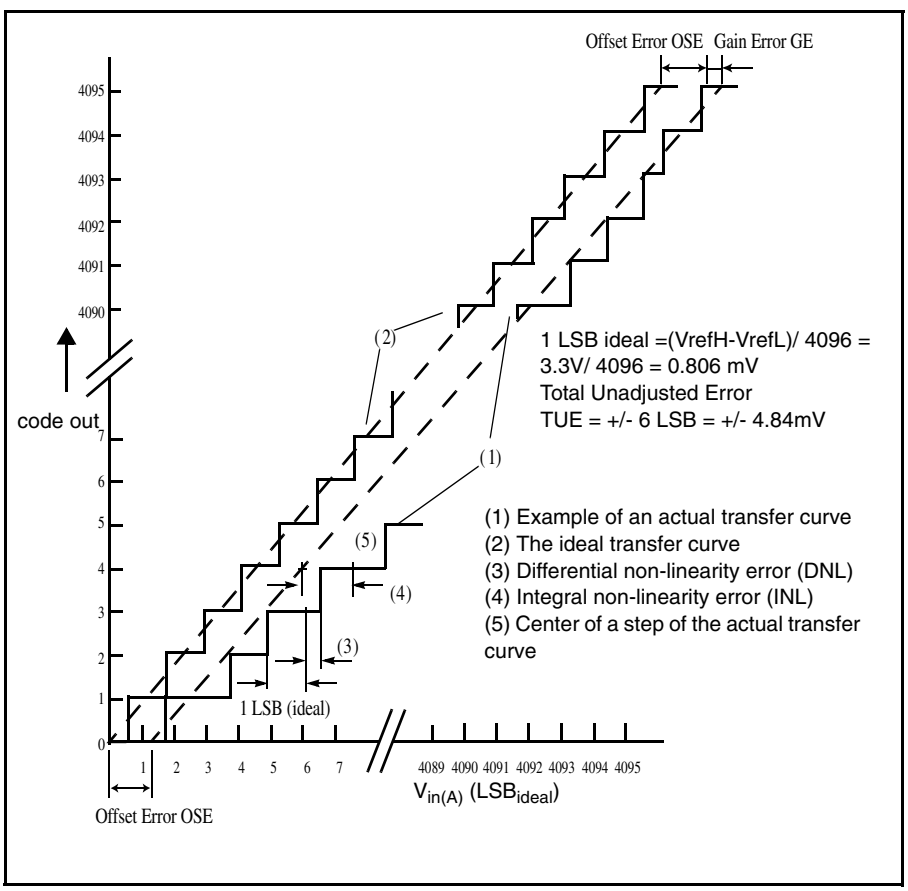


Figure 7. ADC characteristics and error definitions

3.15.1 Input equivalent circuit and ADC conversion characteristics

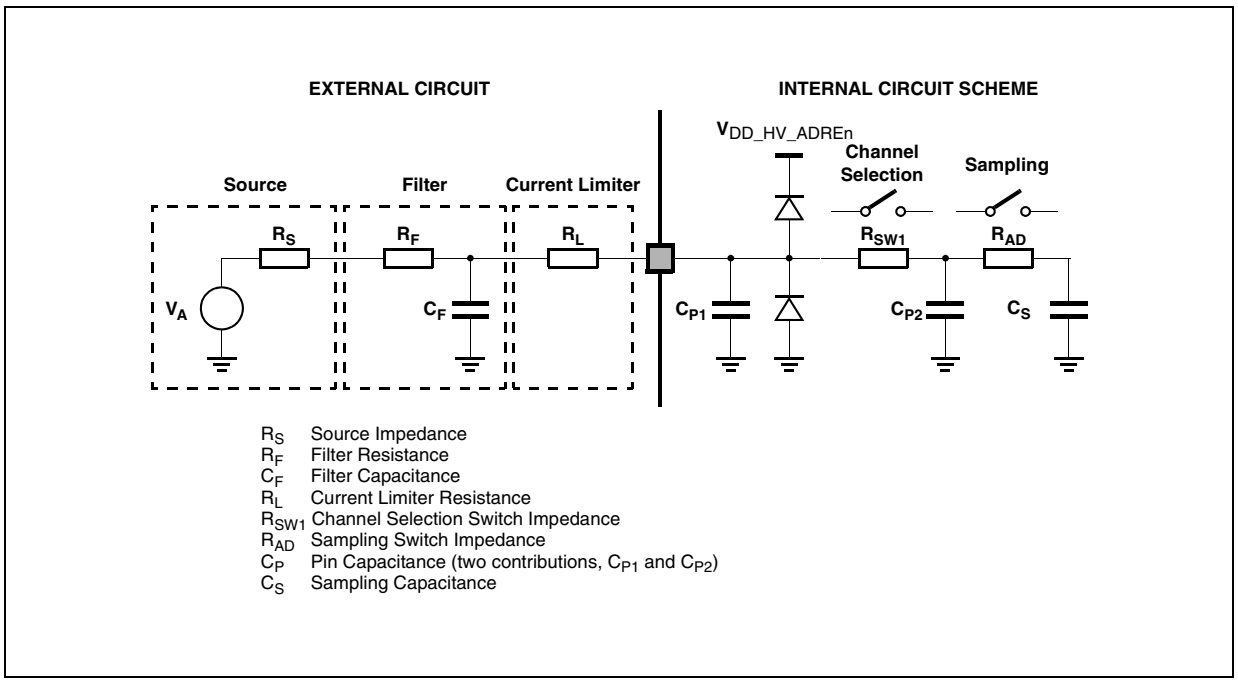


Figure 8. Input equivalent circuit

NOTE

Unless noted otherwise, the specifications in Table 27 assume the use of 13-bit resolution: In ADC_CALBISTREG, set OPMODE to 110b.

Table 27. ADC conversion characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.)	—	20	—	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz, 12-bit resolution	250	—	—	ns
		80 MHz, 13-bit resolution	250	—	—	
t_{conv}	Conversion time[4]	80 MHz, 12-bit resolution	650	—	—	ns
		80 MHz, 13-bit resolution	700	—	—	
C_S[5]	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[5]	ADC input pin capacitance 1	—	—	—	5[6]	pF
C_{P2}[5]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[5]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω

Table continues on the next page...

Table 27. ADC conversion characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
R_{AD}[5]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–4	—	4	LSB
GNE	Gain error	—	–4	—	4	LSB
Input (single ADC channel)	Max leakage	150 °C	—	—	250	nA
	Max positive/negative injection	—	–3	—	3	mA
Input (double ADC channel)	Max leakage	150 °C	—	—	300	nA
	Max positive/negative injection	$\lvert V_{REF\_AD0} - V_{REF\_AD1} \rvert$ < 150mV	–3.6	—	3.6	mA
SNR[7]	Signal-to-noise ratio	V_{REF} = 3.3 V, Fin < 125kHz	67	—	—	dB
SNR[7]	Signal-to-noise ratio	V_{REF} = 5.0 V, Fin < 125kHz	69	—	—	dB
THD	Total harmonic distortion	Fin ≤ 125 kHz	65	70	—	dB
ENOB	Effective number of bits	Fin < 125 kHz	10.5	—	—	bits
SINAD	Signal-to-noise and distortion	See ENOB	(6.02 * ENOB) + 1.76			dB
$TUE_{IS1WINJ}$	Total unadjusted error for IS1WINJ (single ADC channels)	Without current injection	–6	—	6	LSB
$TUE_{IS1WINJ}$	Total unadjusted error for IS1WINJ (single ADC channels)	Current injection: ±3 mA for each channel, max 3 channels	–8	—	8	LSB

1. $V_{DD\_HV\_IO}$ = 3.3 V -5%,+10%, T_J = –40 to +165 °C, unless otherwise specified, and analog input voltage from V_{AGND} to V_{AREF}
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See Figure 8.
6. For the 144-pin package.
7. Test conditions have an influence on the achieved performance. Please contact FSL personnel to share the conditions for these results.

NOTE

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel.

3.16 Flash memory specifications

3.16.1 Maximum junction temperature 150°C

3.16.1.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 28 shows the estimated Program/Erase times.

Table 28. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgn}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgn}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

3.16.1.2 Flash memory Array Integrity and Margin Read specifications

Table 29. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependant on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

3.16.1.3 Flash memory module life specifications

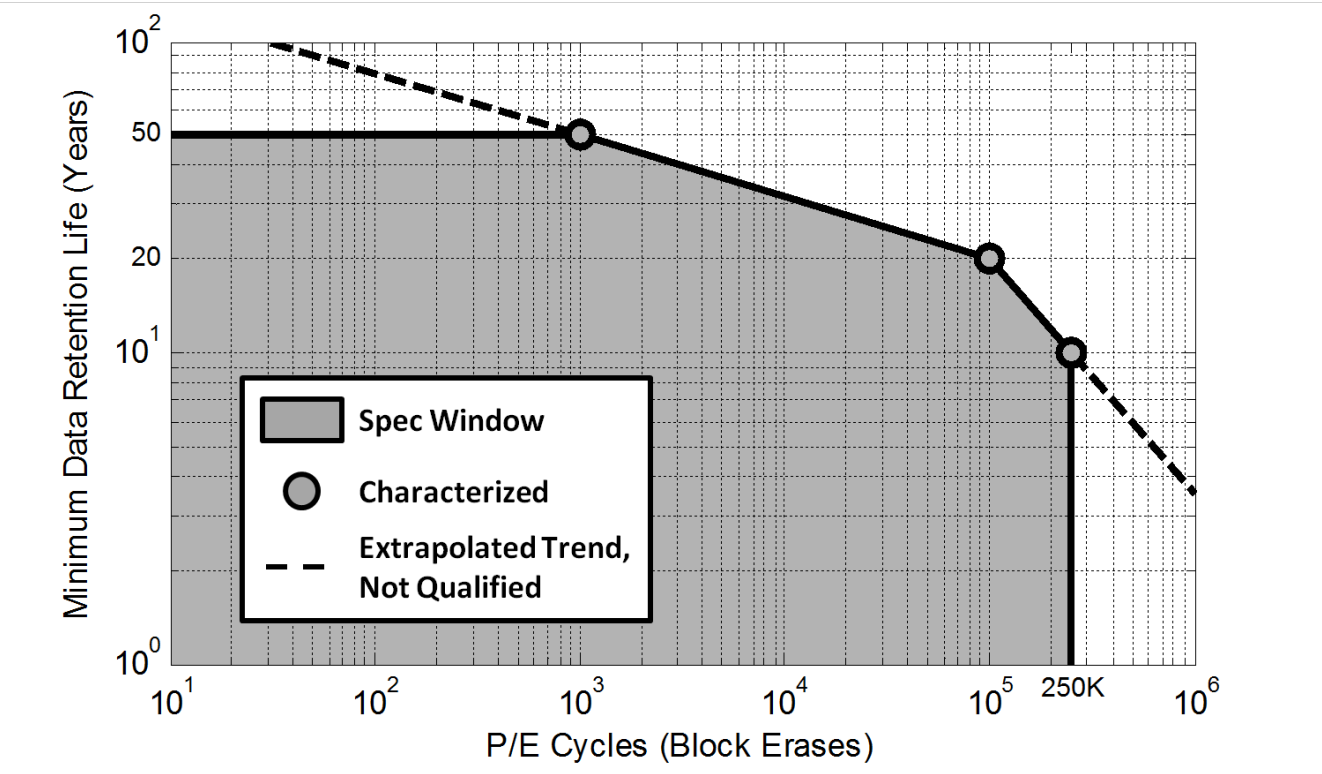
Table 30. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

3.16.1.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



3.16.1.5 Flash memory AC timing specifications

Table 31. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	7 plus four system clock periods	9.1 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns

Table continues on the next page...

Table 31. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

3.16.2 Maximum junction temperature 165°C

3.16.2.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 32 shows the estimated Program/Erase times.

Table 32. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Units
			Initial Max	Initial Max Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C≤ T_A ≤ 30°C[4]	–40°C≤ T_J ≤ 150°C[4]	–40°C≤ T_J ≤ 165 °C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	65	650		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	145	650		µs
t_{qppgn}	Quad-page (1024 bits) program time	268	800	1,200	540	2,700		µs
t_{16kers}	16 KB Block erase time	168	290	320	500	9,000		ms
t_{16kpgn}	16 KB Block program time	34	45	50	70	1,400		ms
t_{32kers}	32 KB Block erase time	217	360	390	610	9,000		ms
t_{32kpgm}	32 KB Block program time	69	100	110	140	2,800		ms
t_{64kers}	64 KB Block erase time	315	490	590	820	9,000		ms
t_{64kpgm}	64 KB Block program time	138	180	210	280	5,500		ms
$t_{256kers}$	256 KB Code erase time[7]	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Code program time[7]	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: –40°C ≤ T_J ≤ 165°C; full spec voltage. 16 KB, 32 KB and 64 KB blocks are allowed to be programmed or erased up to T_J = 165°C with restrictions.
7. 256 KB blocks may be programmed or erased at T_J = 150°C maximum. Times listed on this row are T_J = 150°C times.

3.16.2.2 Flash memory Array Integrity and Margin Read specifications

Table 33. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16KB block.	—	—	512 x Tperiod x Nread	—

Table continues on the next page...

Table 33. Flash memory Array Integrity and Margin Read specifications (continued)

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependant on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

3.16.2.3 Flash memory module life specifications

Table 34. Flash memory module life specifications

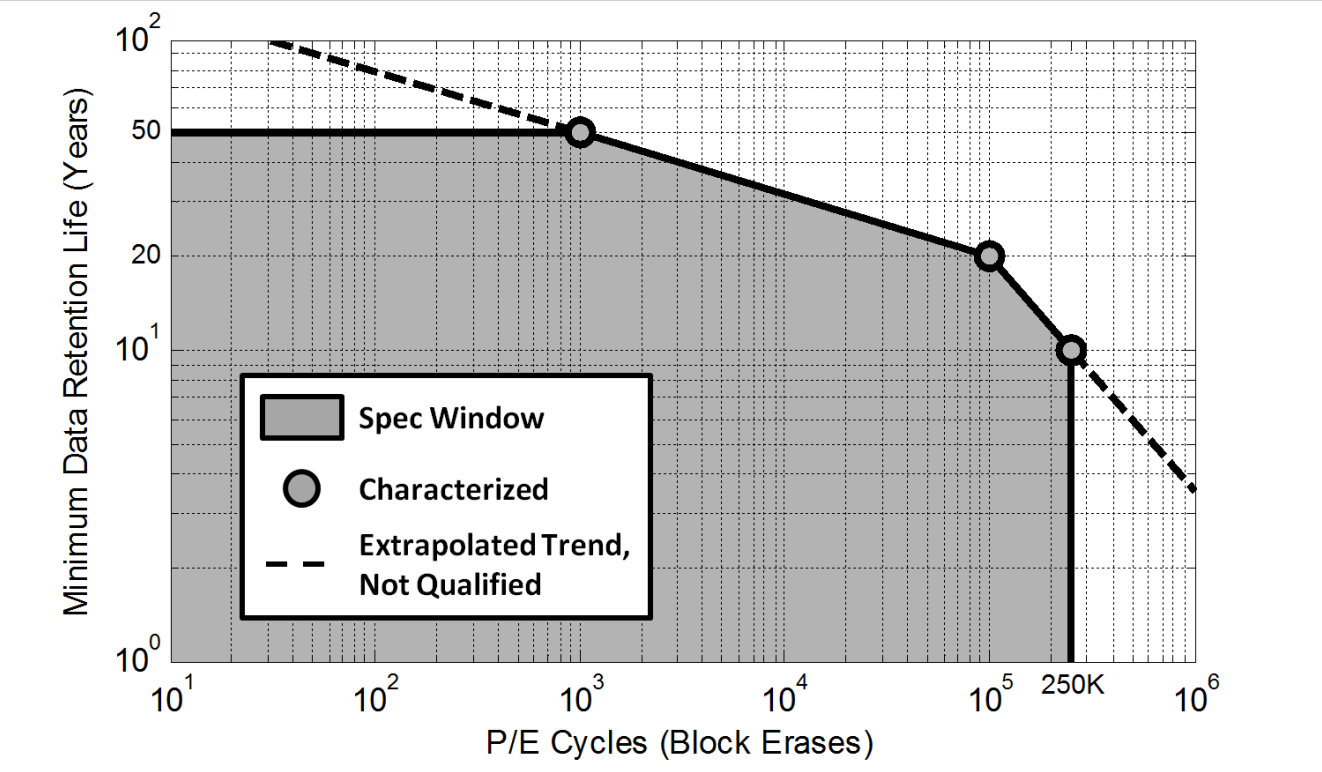
Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	-	250,000	-	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	-	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	-	Years
		Blocks with 100,000 P/E cycles.	20	-	Years
		Blocks with 250,000 P/E cycles.	10	-	Years

1. Program and erase supported across standard temperature specs. Up to 10,000 program and erase cycles may be done between 150 °C and 165 °C out of the total specified number of cycles.
2. Program and erase supported across standard temperature specs.

3.16.2.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.

Maximum junction temperature 165°C



3.16.2.5 Flash memory AC timing specifications

Table 35. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	7 plus four system clock periods	9.1 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs

Table continues on the next page...

Table 35. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UTO-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UTO-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

3.16.3 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1[RWSC] and PFCR1[APC] fields at various operating frequencies, based on specified intrinsic flash memory access times of the C55FMC array at 150°C.

NOTE

If the user does not follow these recommended settings, the user must run the flash memory's array integrity (AI) check with breakpoints disabled: Set the Array Integrity Break Point Enable bit in the C55FMC's UTest 0 register (C55FMC_UT0[AIBPE]) to 0.

Table 36. Flash memory read wait-state and address-pipeline control combinations

Operating frequency (f_{CPU} = SYS_CLK)		RWSC	APC	Flash read latency on mini-cache miss (# of f_{CPU} clock periods)	Flash read latency on mini-cache hit (# of f_{CPU} clock periods)
–40°C to 150°C	Max 165°C option				
0 MHz < f_{CPU} ≤ 33 MHz	0 MHz < f_{CPU} ≤ 30 MHz	0	0	3	1
33 MHz < f_{CPU} ≤ 100 MHz	30 MHz < f_{CPU} ≤ 90 MHz	2	1	5	1

Table continues on the next page...

Table 36. Flash memory read wait-state and address-pipeline control combinations (continued)

Operating frequency (f_{CPU} = SYS_CLK)		RWSC	APC	Flash read latency on mini-cache miss (# of f_{CPU} clock periods)	Flash read latency on mini-cache hit (# of f_{CPU} clock periods)
–40°C to 150°C	Max 165°C option				
100 MHz < f_{CPU} ≤ 133 MHz	90 MHz < f_{CPU} ≤ 120 MHz	3	1	6	1
133 MHz < f_{CPU} ≤ 167 MHz	120 MHz < f_{CPU} ≤ 150 MHz	4	1	7	1
167 MHz < f_{CPU} ≤ 200 MHz	150 MHz < f_{CPU} ≤ 180 MHz	5	2	8	1

3.17 SGEN electrical characteristics

Table 37. SGEN electrical characteristics

Symbol	Parameter	Min	Max	Unit
	Input clock	12	20	MHz
SINAD	Signal-to-noise ratio plus distortion	50	—	dB
FREQ	Frequency range of the sine wave	1	50	kHz
FRP	Frequency precision of the sine wave (peak to peak variation)	–5	5	%
APP	Sine wave amplitude (peak to peak)	0.426	2.063	V
Load	Load capacitance	25	100	pF
Current	Output current	—	100	µA
T_J	Junction temperature	–40	165	°C

3.18 RESET sequence duration

This following table shows the duration of different reset sequences. See the chip's Reference Manual for details about the reset sequences.

Table 38. RESET sequences

Symbol	Parameter	Conditions	T_{Reset}			Unit
			Min	Typ	Max[1]	
T_{DRB}	'Destructive' reset sequence, BIST enabled	Self test clock in STCU is the PLL generated clock. Self test configuration as per DCF record programming. For four LBIST partitions in design, two LBIST partitions are run in parallel.	—	—	18.0	ms
T_{DR}	'Destructive' reset sequence, BIST disabled	—	—	440	480	µs

Table continues on the next page...

Table 38. RESET sequences (continued)

Symbol	Parameter	Conditions	T_{Reset}			Unit
			Min	Typ	Max[1]	
T_{ERLB}	External reset sequence—long, BIST enabled	Self test clock in STCU is the PLL generated clock. Self test configuration as per DCF record programming. For four LBIST partitions in design, two LBIST partitions are run in parallel.	—	—	17.5	ms
T_{ERL}	External reset sequence—long, BIST disabled	—	—	120	150	µs
T_{FRL}	Functional reset sequence—long	—	—	165	180	µs
T_{FRS}	Functional reset sequence—short	—	—	10.0	12.0	µs

1. The maximum value applies only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

3.19 AC specifications

AC Parameters are specified over the full operating junction temperature range of -40°C to +165°C and for the full operating range of the V_{DD_IO} supply defined in DC electrical characteristics.

Table 39. Functional Pad AC Specifications

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn's SRC[1:0] field
	Min	Max	Min	Max		MSB,LSB
I/O (output)	2.5/2.5	7.5/7.5	0.9/0.9	3/3	50	11
	—	—	—	12/12	200	
	—	8/8	—	3.5/3.5	25	10
	—	11.5/11.5	—	6.5/6.5	50	
	—	—	—	30/30	200	
	—	45/45	—	25/25	50	01[2]
	—	65/65	—	30/30	200	
	—	75/75	—	40/40	50	00[2]
	—	110/110	—	50/50	200	
I/O (input)	—	1.5/1.5	—	0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

3.19.1 Reset pad (EXT_POR, RESET) electrical characteristics

The device implements a dedicated bidirectional RESET pin.

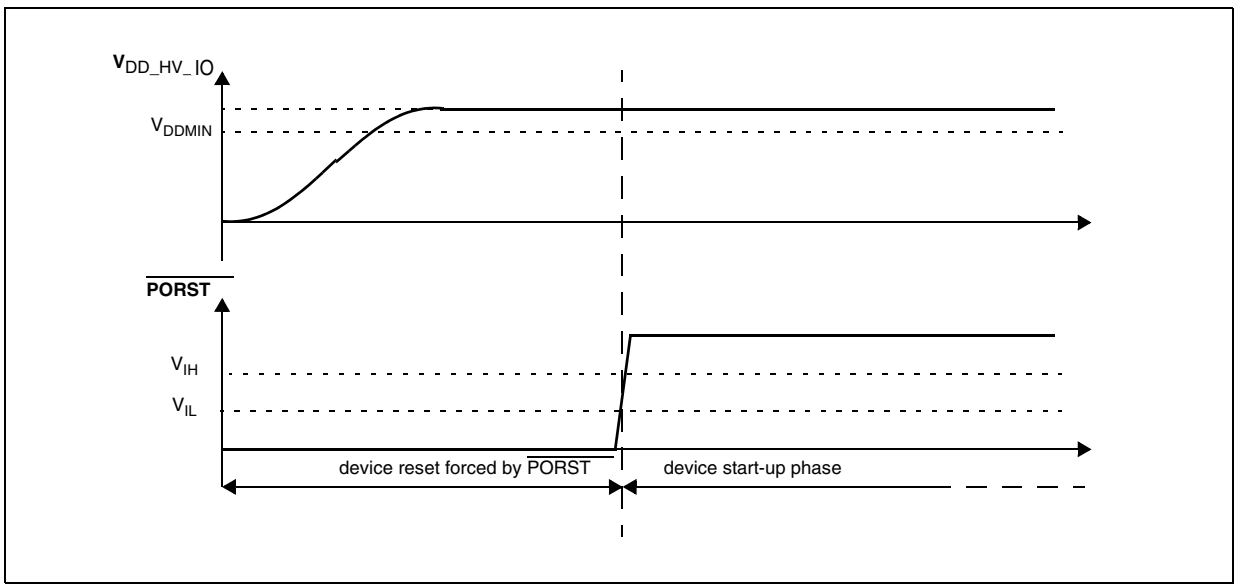


Figure 9. Start-up reset requirements

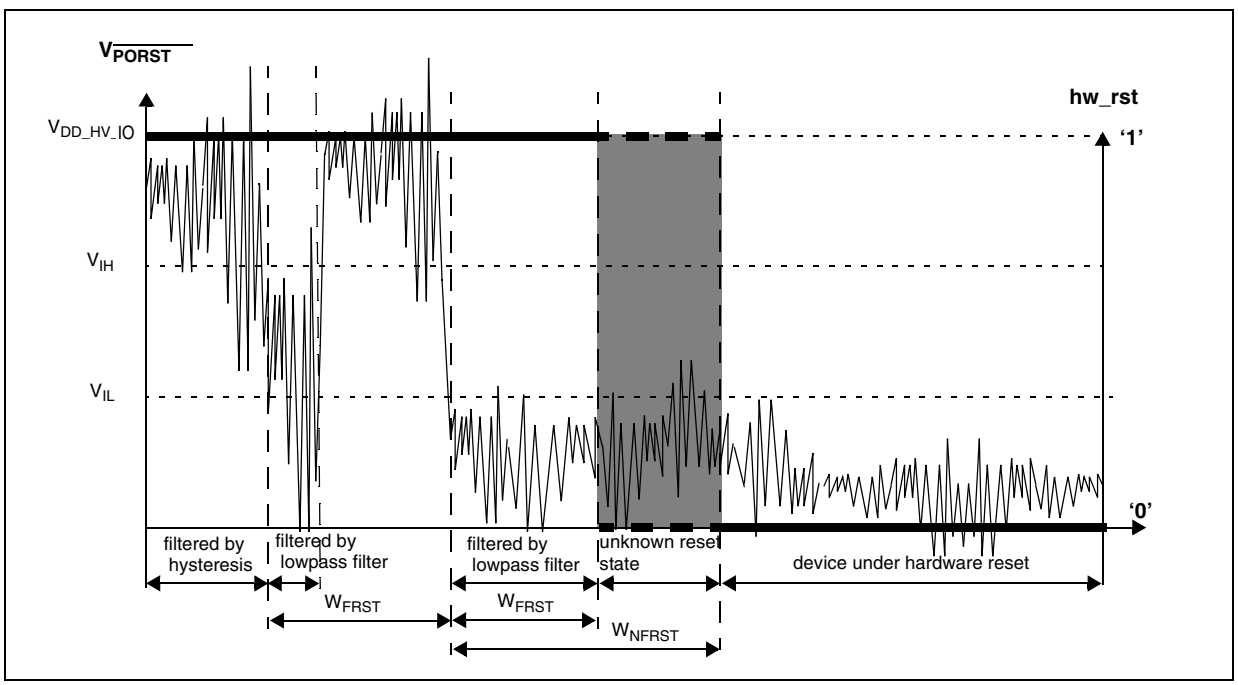


Figure 10. Noise filtering on reset signal

Table 40. Reset ($\overline{\text{RESET}}$) electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
V_{IH}	Input high level TTL (Schmitt Trigger)	—	2.0	—	$V_{DD\_HV\_IO}$ + 0.4	V
V_{IL}	Input low level TTL (Schmitt Trigger)	—	–0.4	—	0.8	V
V_{HYS}	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV
I_{OL_R}	Strong pull-down current	Device under power-on reset $V_{DD\_HV\_A}$=1.0 V V_{OL} = 0.35*$V_{DD\_HV\_IO}$	0.2	—	—	mA
		Device under power-on reset $V_{DD\_HV\_IO}$=3.0 V V_{OL} = 0.35*$V_{DD\_HV\_IO}$	15	—	—	mA
W_{FRST}	($\overline{\text{RESET}}$)-input filtered pulse	—	—	—	500	ns
W_{NFRST}	($\overline{\text{RESET}}$)-input not filtered pulse	—	2	—	—	µs
$\lvert I_{WPD} \rvert$	Weak pull-down current absolute value	RESET pin V_{IN} = V_{DD}	30	—	80	µA

1. $V_{DD\_HV\_IO}$ = 3.3 V -5%,+10%, T_J = –40 to 165 °C, unless otherwise specified

Table 41. Reset ($\overline{\text{EXT\_POR}}$) electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
W_{FPORST}	PORST input filtered pulse	—	—	—	500	ns
$W_{NFPORST}$	PORST input not filtered pulse	—	2000	—	—	ns
W_{IH}	Input high level	—	2	—	$V_{DD\_HV\_IO}$ +0.4	V
W_{IL}	Input low level	—	-0.4	—	0.8	V

3.19.2 WKUP/NMI timing

Table 42. WKUP/NMI glitch filter

Symbol	Parameter	Min	Typ	Max	Unit
W_{FNMI}	NMI pulse width that is rejected	—	—	20	ns
W_{NFNMI}	NMI pulse width that is passed	400	—	—	ns

3.19.3 Debug/JTAG/Nexus/Aurora timing

3.19.3.1 JTAG interface timing

Table 43. JTAG pin AC electrical characteristics [1]

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}	TCK Cycle Time[2]	36	—	ns
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO Data Valid	—	15[3]	ns
7	t_{TDOI}	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO High Impedance	—	15	ns
9	t_{JCMPPW}	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600[4]	ns
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

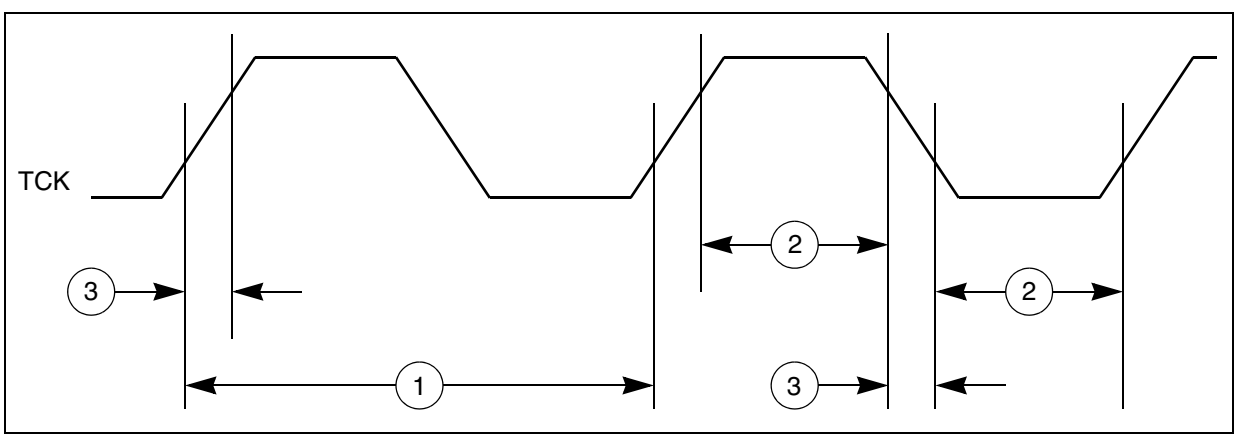


Figure 11. JTAG test clock input timing

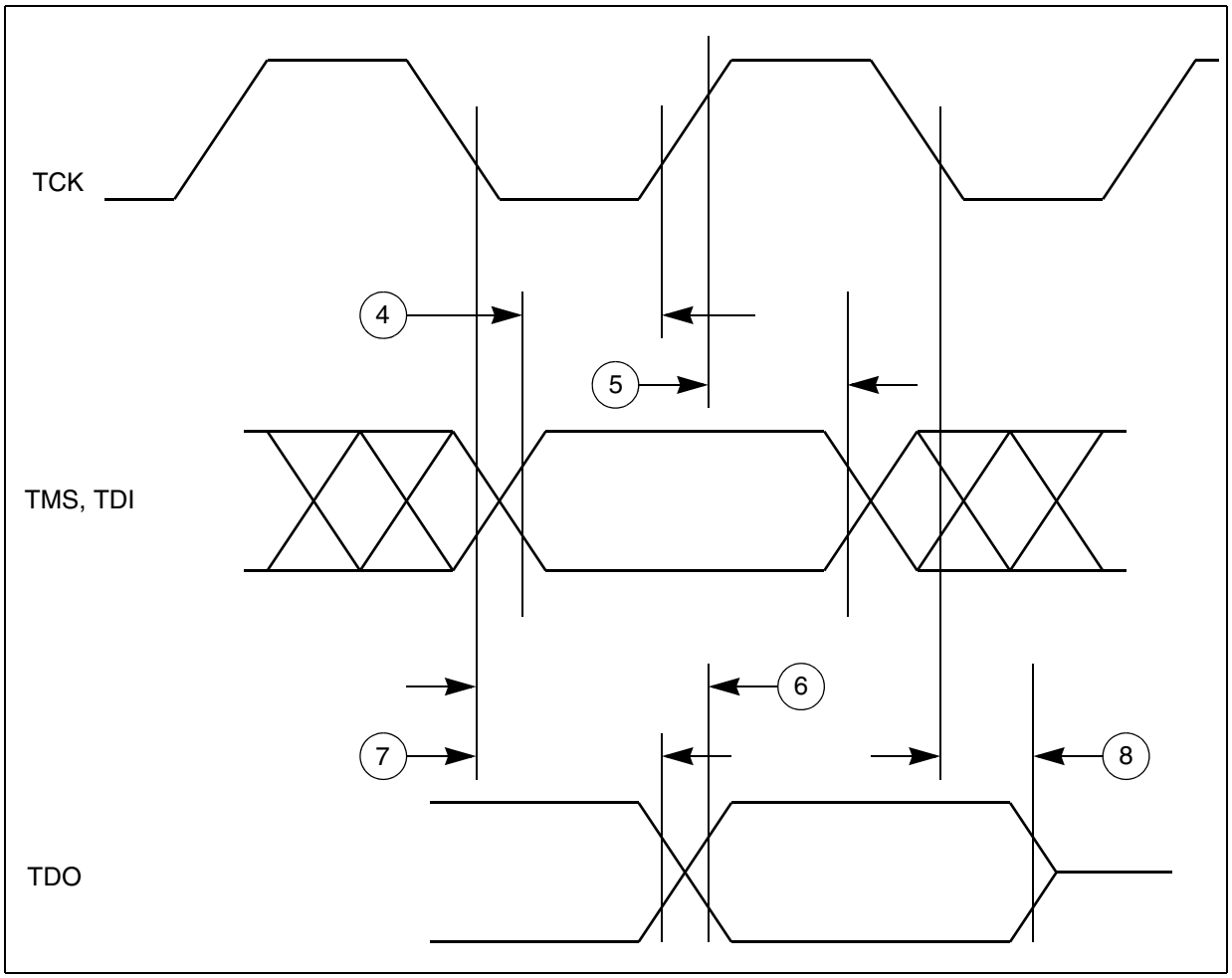


Figure 12. JTAG test access port timing

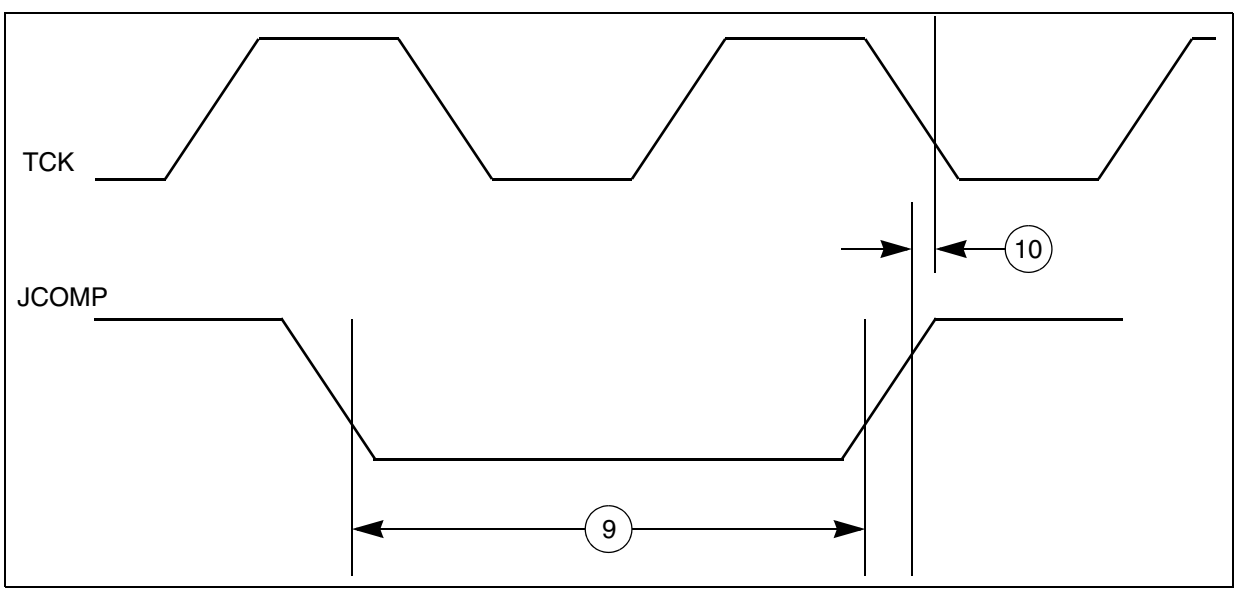


Figure 13. JTAG JCOMP timing

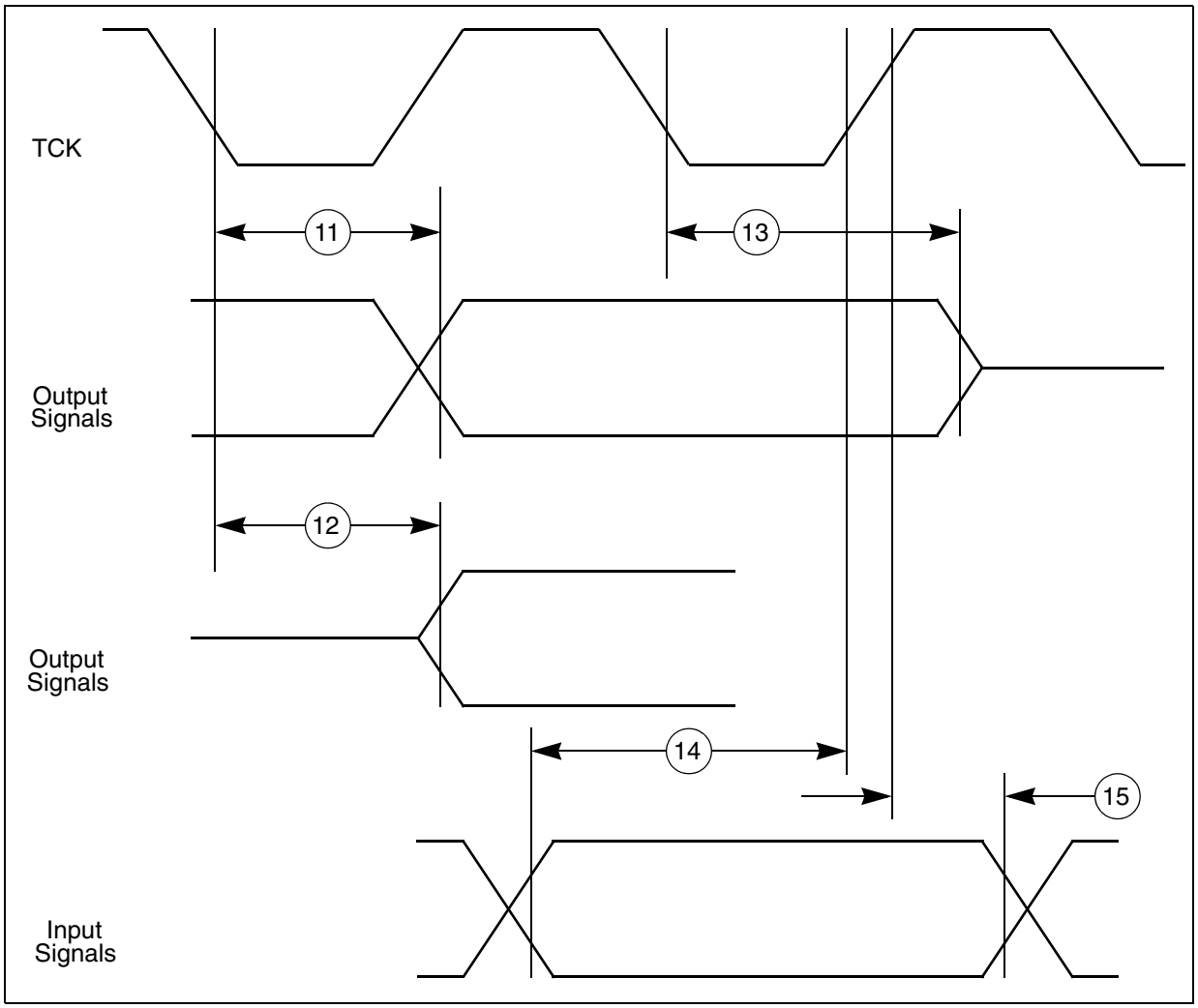


Figure 14. JTAG boundary scan timing

3.19.3.2 Nexus timing

Table 44. Nexus debug port timing [1]

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	MCKO Low to MDO, $\overline{MSEO}$, $\overline{EVTO}$ Data Valid[2]	—	–0.1	0.25	t_{MCYC}
4	t_{EVTIPW}	$\overline{EVTI}$ Pulse Width	—	4	—	t_{TCYC}
5	t_{EVTOPW}	$\overline{EVTO}$ Pulse Width	—	1	—	t_{MCYC}
6	t_{TCYC}	TCK Cycle Time[3]	—	62.5	—	ns
7	t_{TDC}	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	TDI, TMS Data Setup Time	—	8	—	ns
9	t_{NTDIH}, t_{NTMSH}	TDI, TMS Data Hold Time	—	5	—	ns
10	t_{JOV}	TCK Low to TDO/RDY Data Valid	—	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

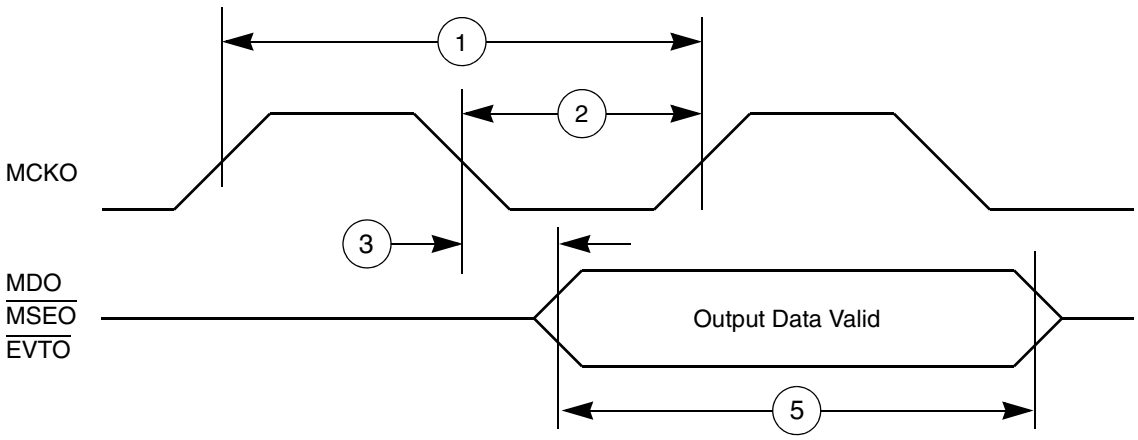


Figure 15. Nexus output timing

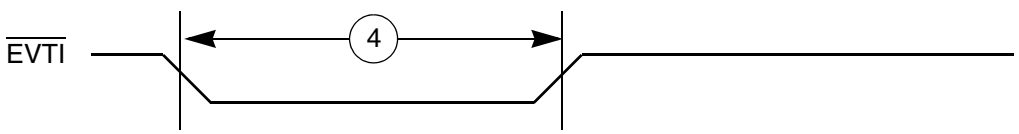


Figure 16. Nexus EVTI Input Pulse Width

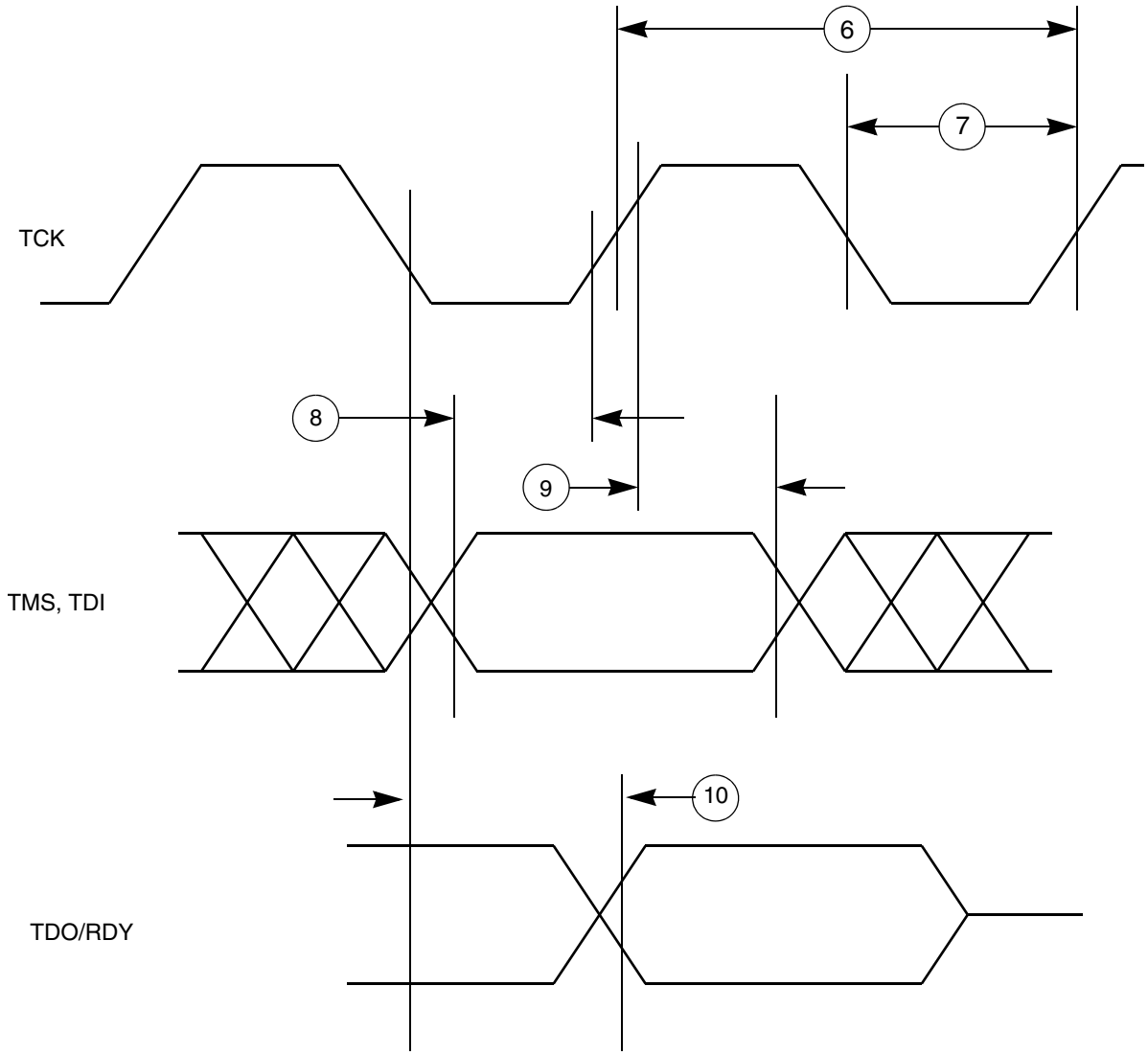


Figure 17. Nexus TDI, TMS, TDO timing

3.19.3.3 Aurora LVDS driver electrical characteristics

Table 45. Aurora LVDS driver electrical characteristics

Symbol	Parameter[1]	Value			Unit
		Min	Typ	Max	
Data Rate					
DATARATE	Data rate	—	1250	Typ+0.1%	Mbps
STARTUP					
T_{STRT_BIAS}	Bias startup time[2]	—	—	5	µs
T_{STRT_TX}	Transmitter startup time[3]	—	—	5	µs
T_{STRT_RX}	Receiver startup time[4]	—	—	4	µs

1. Conditions for these values are $V_{DD\_HV\_IO}$ = 3.3 V (–5%, +10%), T_J = –40 to 150 °C
2. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.

3. Startup time is defined as the time taken by LVDS transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.
4. Startup time is defined as the time taken by LVDS receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

3.19.3.4 Nexus Aurora debug port timing

Table 46. Nexus Aurora debug port timing

#	Symbol	Characteristic	Min	Max	Unit
1	t_{REFCLK}	Reference clock frequency	625	1250	MHz
2	t_{RCDC}	Reference Clock Duty Cycle	45	55	%
3	J_{RC}	Reference Clock jitter	—	40	ps
4	$t_{STABILITY}$	Reference Clock Stability	50	—	PPM
5	BER	Bit Error Rate	—	10^{-12}	—
6	J_D	Transmit lane Deterministic Jitter	—	0.17	OUI
7	J_T	Transmit lane Total Jitter	—	0.35	OUI
8	S_O	Differential output skew	—	20	ps
9	S_{MO}	Lane to lane output skew	—	1000	ps
10	UI	Aurora lane Unit Interval	800	1600	ps

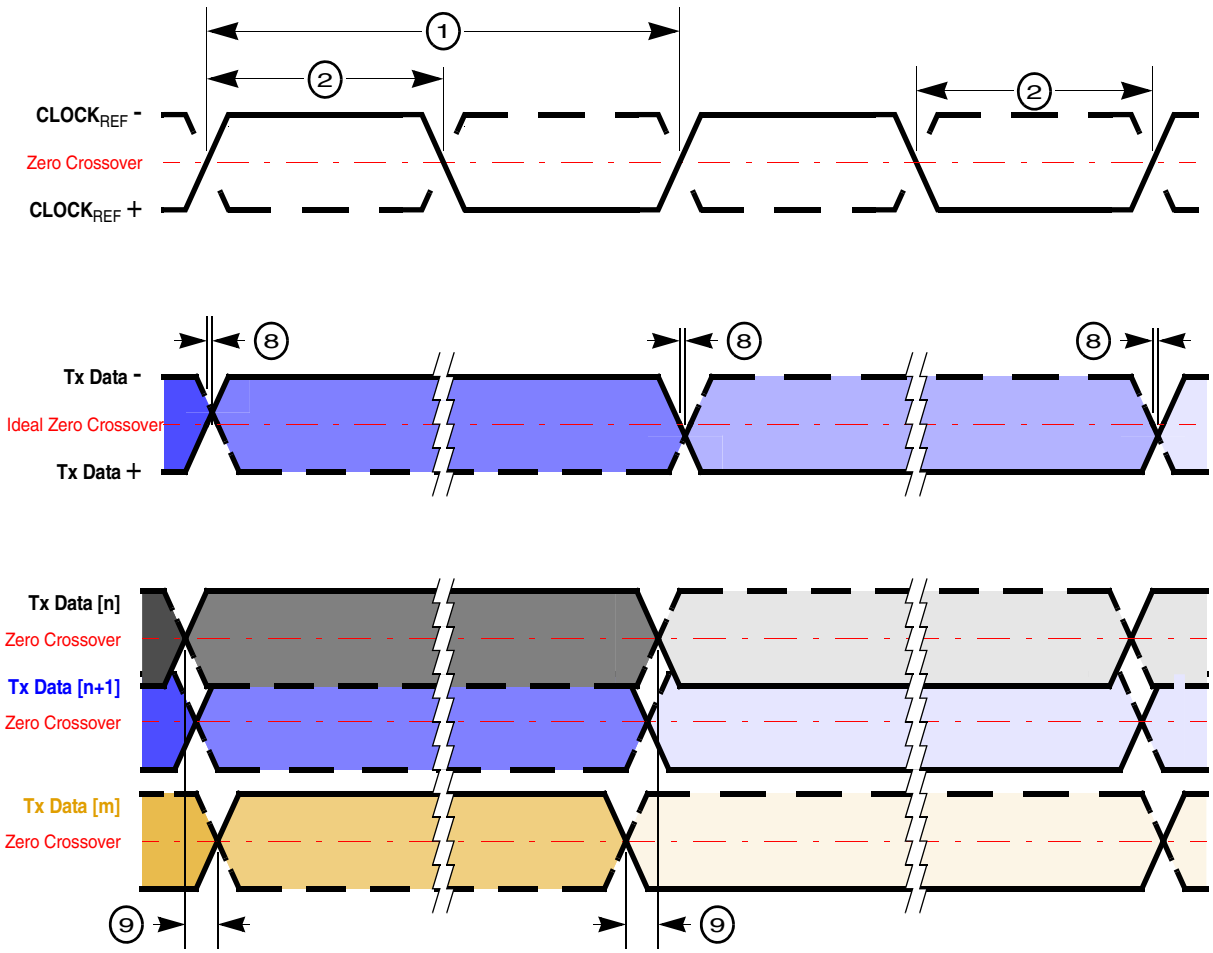


Figure 18. Nexus Aurora timings

Rise/fall timing for the Nexus Aurora debug port reference clock must conform to the area between the minimum and maximum value ranges shown in the following receiver "eye" diagram.

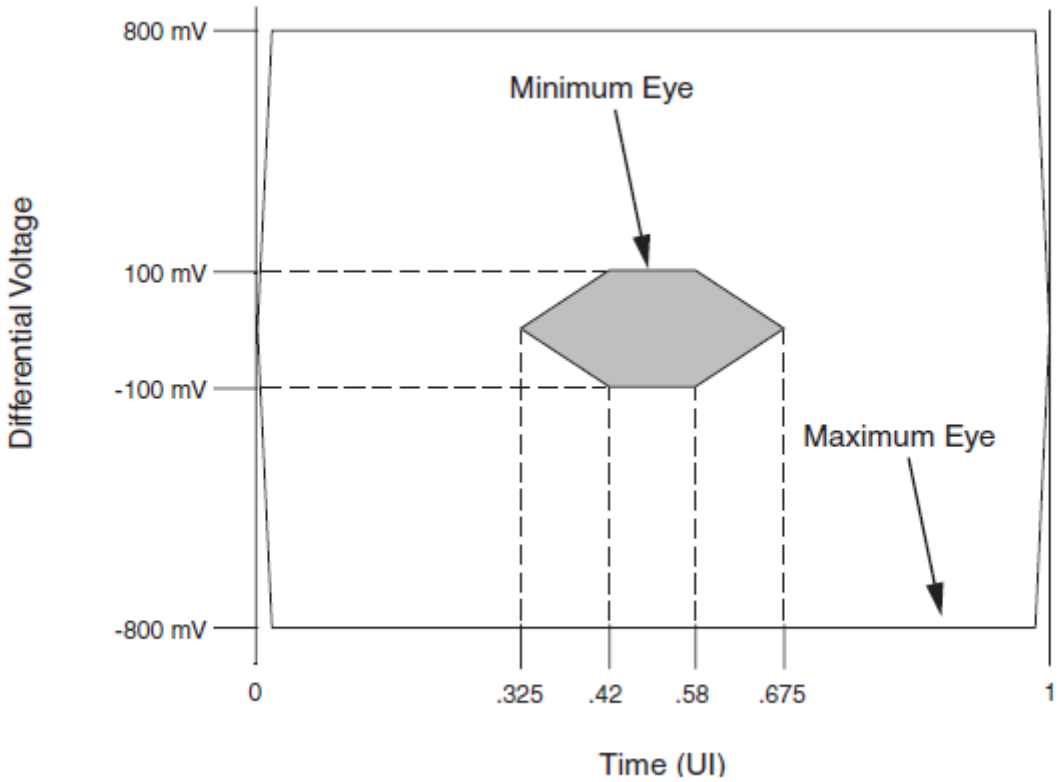


Figure 19. Nexus Aurora receiver "eye" diagram

3.19.4 External interrupt timing (IRQ pin)

Table 47. External interrupt timing

#	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	IRQ edge to edge time[1]	—	6	—	t_{CYC}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both

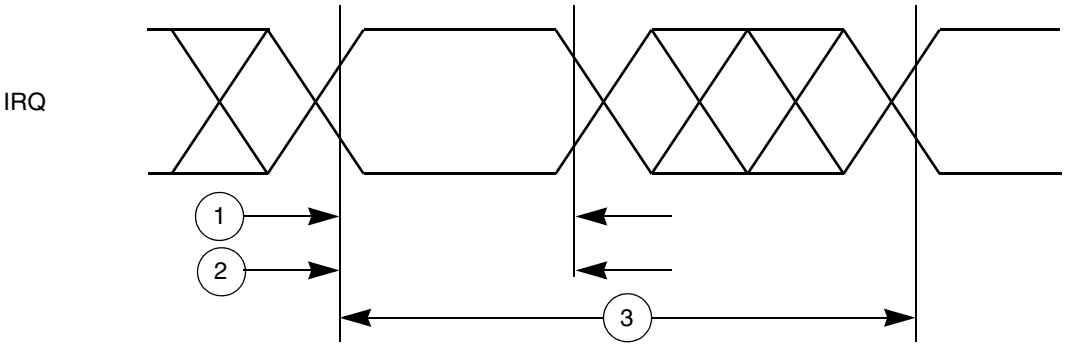


Figure 20. External interrupt timing

3.19.5 SPI timing

Table 48. SPI timing

#	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	SPI cycle time	Master (MTFE = 0)	40	—	ns
			Slave (MTFE = 0)	40	—	
			Slave Receive Only Mode[1]	16	—	
2	t_{CSC}	PCS to SCK delay	—	16	—	ns
3	t_{ASC}	After SCK delay	—	16	—	ns
4	t_{SDC}	SCK duty cycle	—	$t_{SCK}/2 - 4$	$t_{SCK}/2 + 4$	ns
5	t_A	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	ns
6	t_{DIS}	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	25	ns
7	t_{PCSC}	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	Data setup time for inputs	Master (MTFE = 0)	16	—	ns
			Slave	2	—	
			Master (MTFE = 1, CPHA = 0)	$16 - (P^2 \times t_{SYS}, ^3)$	—	
			Master (MTFE = 1, CPHA = 1)	16	—	
10	t_{HI}	Data hold time for inputs	Master (MTFE = 0)	–3	—	ns
			Slave	4	—	
			Master (MTFE = 1, CPHA = 0)	$-3 + (P^2 \times t_{SYS}, ^3)$	—	
			Master (MTFE = 1, CPHA = 1)	–3	—	
11	t_{SUO}	Data valid (after SCK edge) time for outputs	Master (MTFE = 0)	—	4	ns
			Slave	—	17	
			Master (MTFE = 1, CPHA = 0)	—	$4 + t_{SYS}^3$	
			Master (MTFE = 1, CPHA = 1)	—	4	

Table continues on the next page...

Table 48. SPI timing (continued)

#	Symbol	Parameter	Conditions	Min	Max	Unit
12	t_{HO}	Data hold time for outputs	Master (MTFE = 0)	–4	—	ns
			Slave	3.6	—	
			Master (MTFE = 1, CPHA = 0)	–4	—	
			Master (MTFE = 1, CPHA = 1)	–4	—	

1. Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the SPI can receive data on SIN, but no valid data is transmitted on SOUT.
2. P is the number of clock cycles added to delay the SPI input sample point and is software programmable.
3. t_{SYS} is the period of the DSPI_CLKn clock, the input clock to the SPI module. Maximum frequency is 50 MHz (min t_{SYS} = 20 ns).

NOTE

For numbers shown in the following figures, see Table 48.

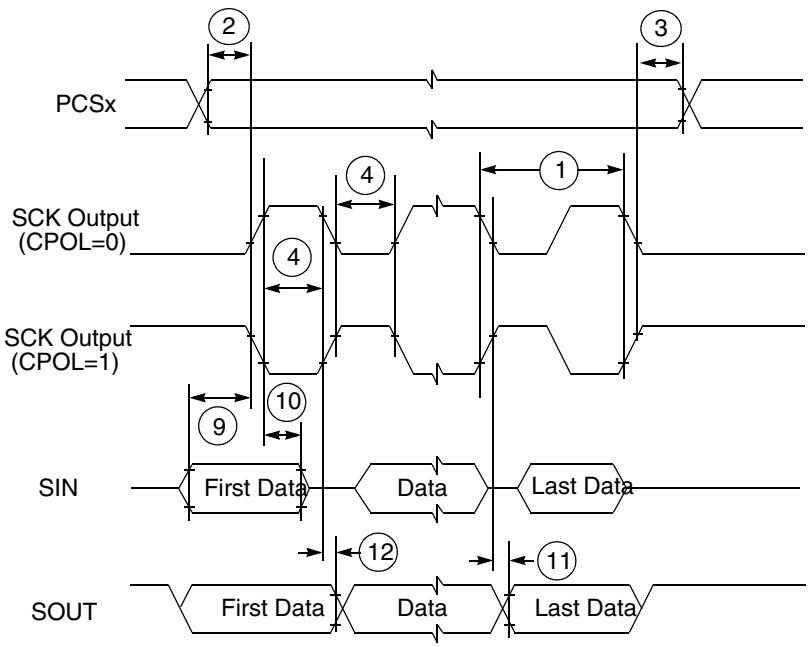


Figure 21. DSPI classic SPI timing — master, CPHA = 0

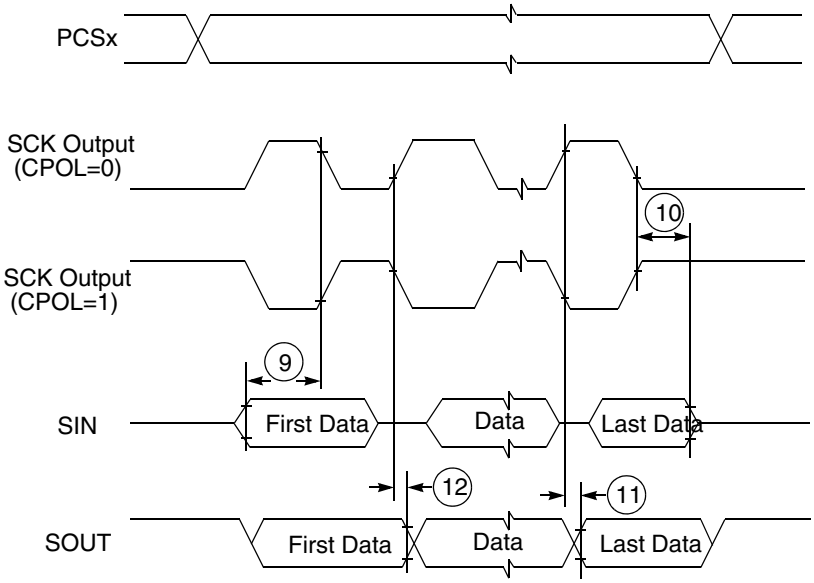


Figure 22. DSPI classic SPI timing — master, CPHA = 1

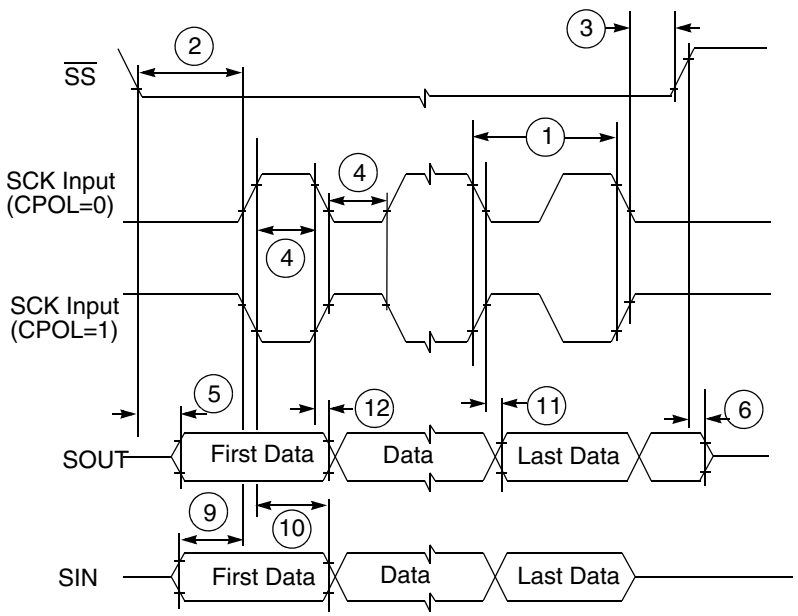


Figure 23. DSPI classic SPI timing — slave, CPHA = 0

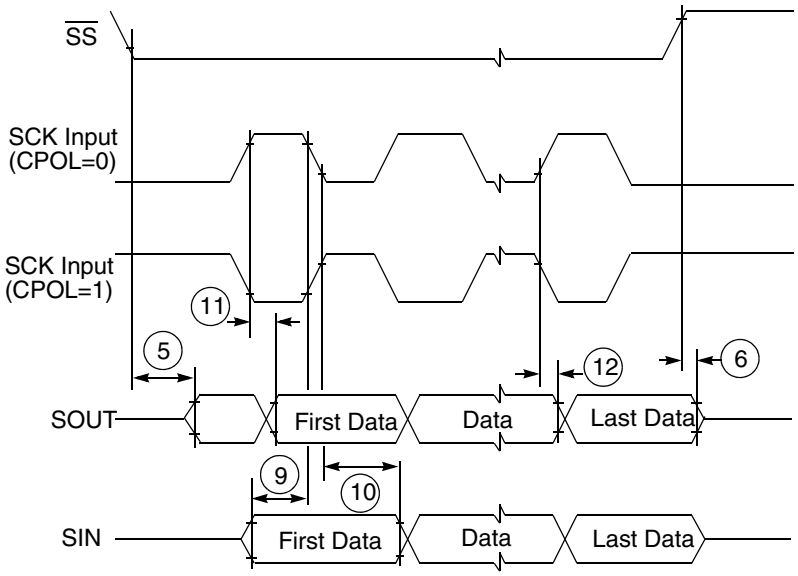


Figure 24. DSPI classic SPI timing — slave, CPHA = 1

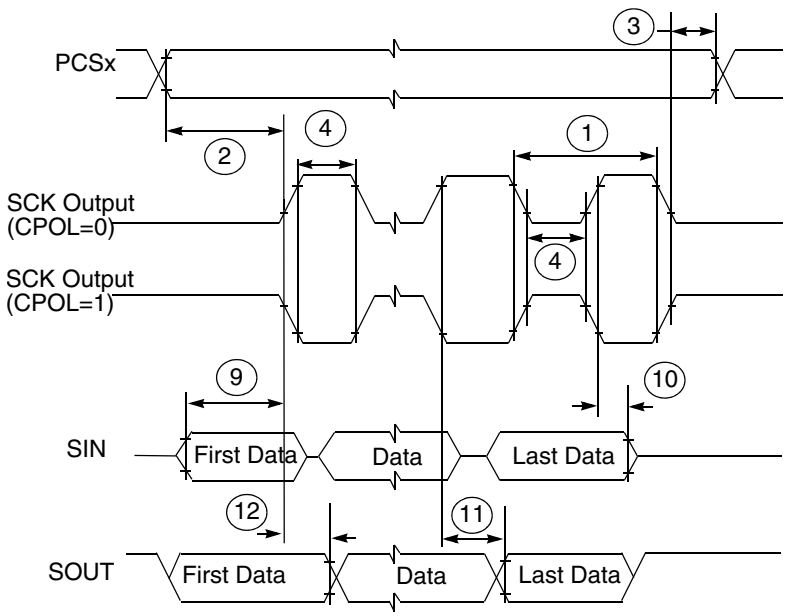


Figure 25. DSPI modified transfer format timing — master, CPHA = 0

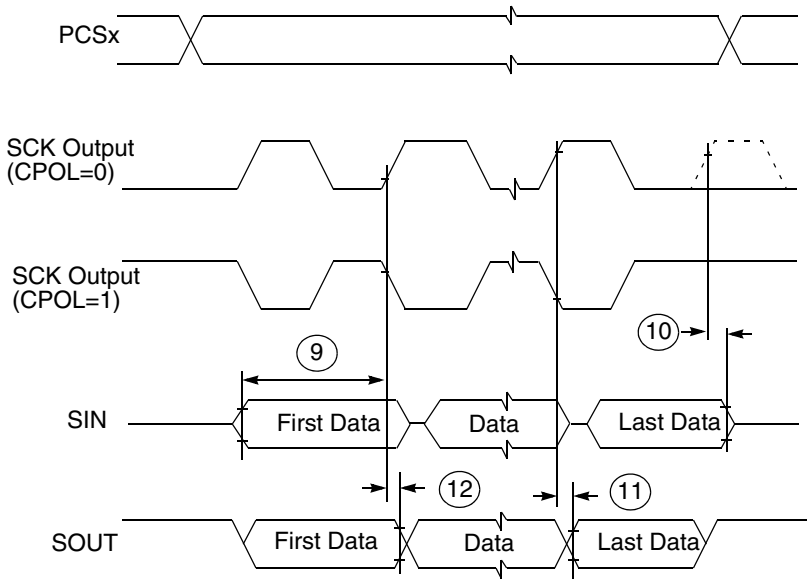


Figure 26. DSPI modified transfer format timing — master, CPHA = 1

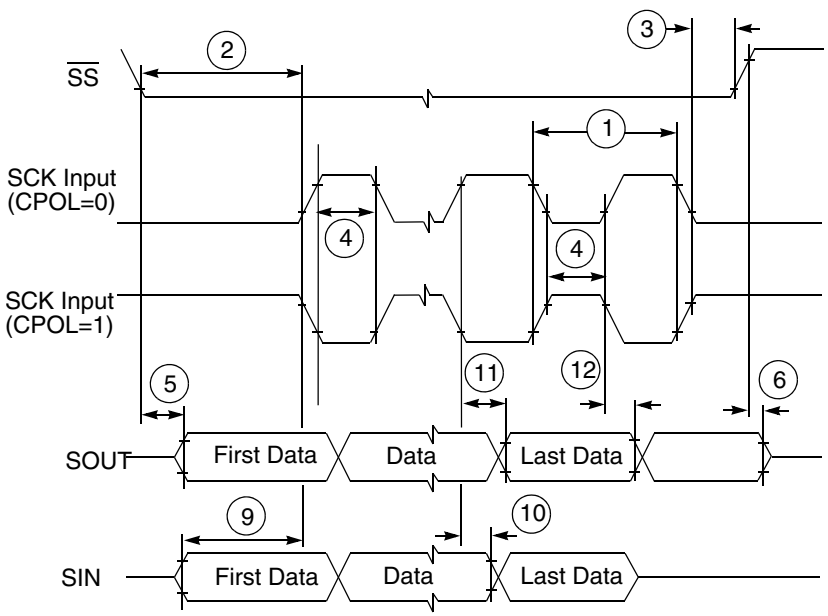


Figure 27. DSPI modified transfer format timing – slave, CPHA = 0

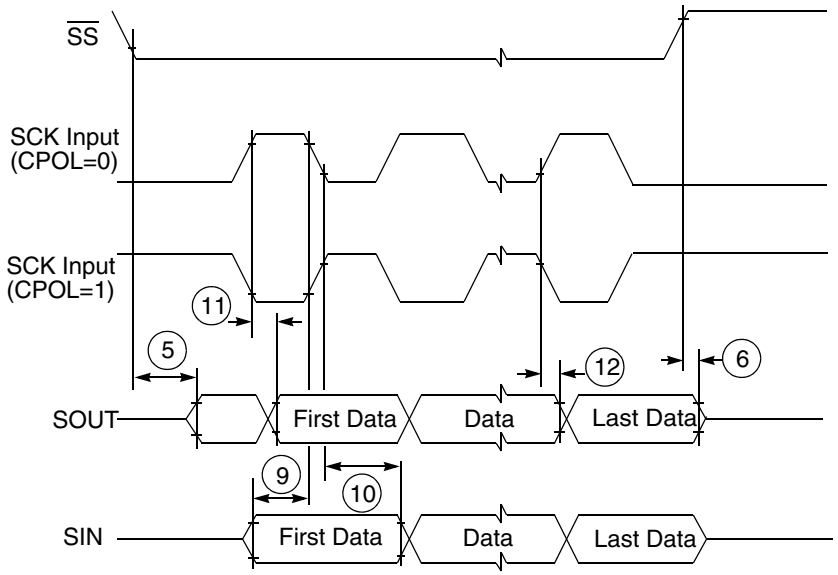


Figure 28. DSPI modified transfer format timing — slave, CPHA = 1

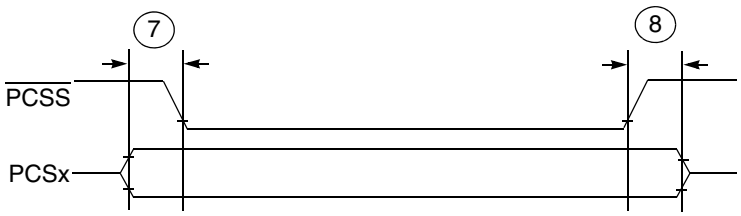


Figure 29. DSPI PCS strobe (PCSS) timing

3.19.6 LFAST

3.19.6.1 LFAST interface timing diagrams

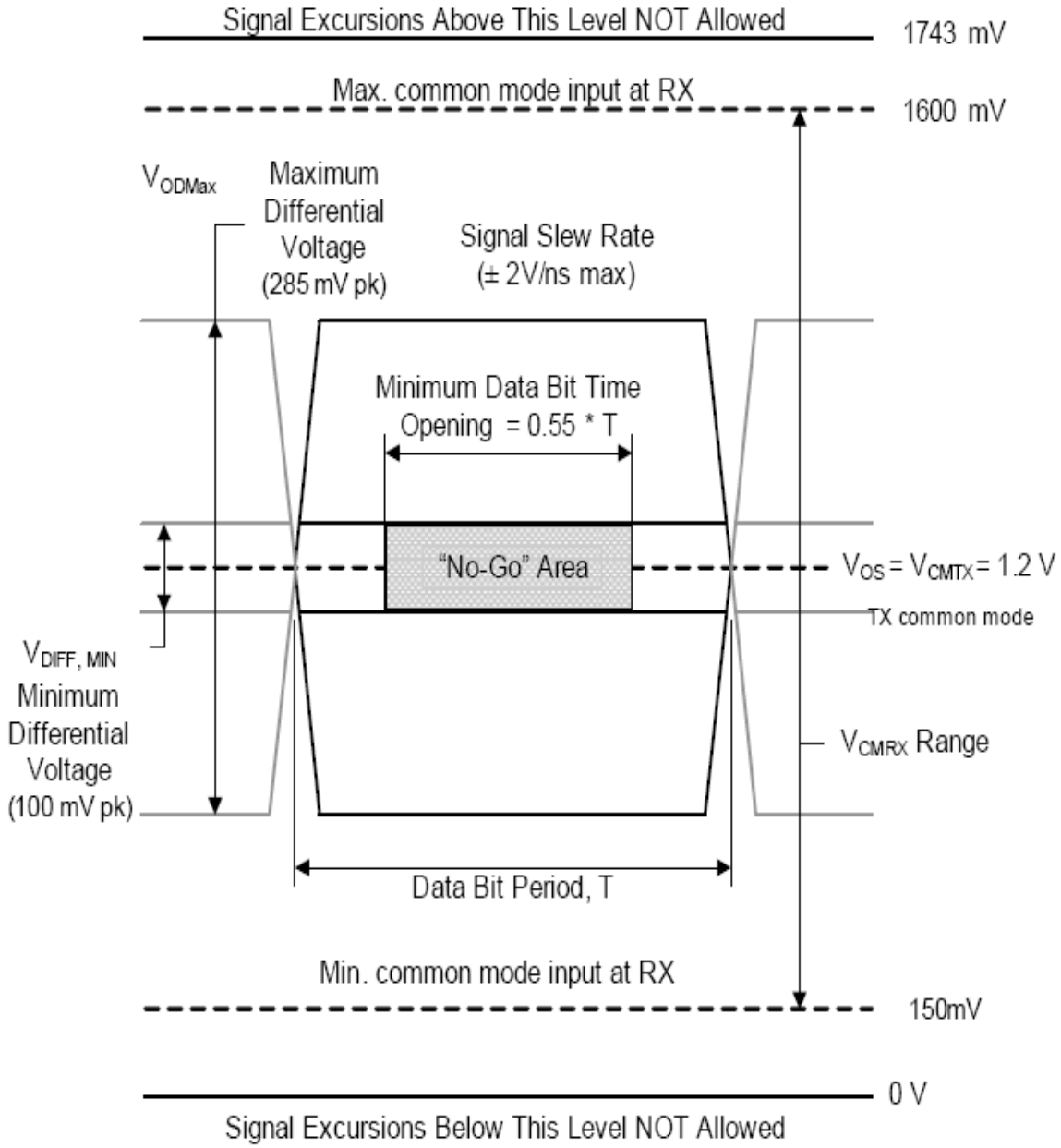


Figure 30. LFAST timing definition

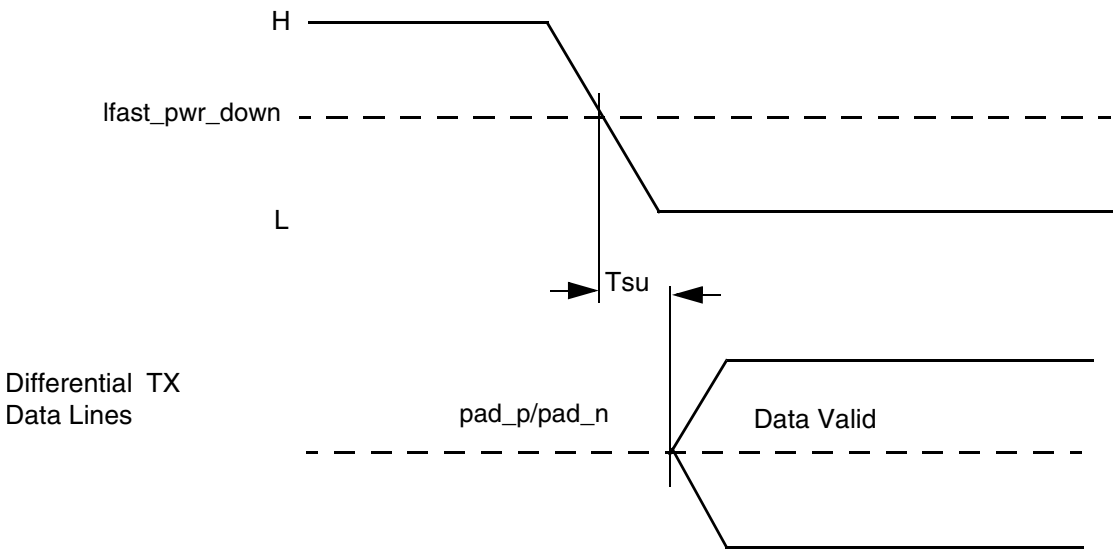


Figure 31. Power-down exit time

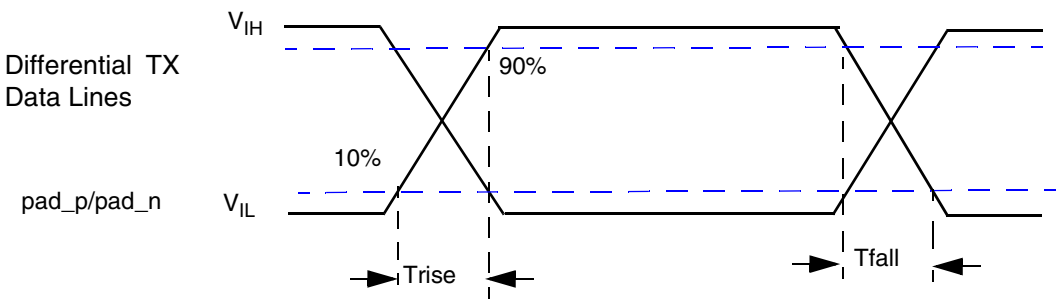


Figure 32. Rise/fall time

3.19.6.2 LFAST interface electrical characteristics

Table 49. LFAST electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
$V_{DD\_HV\_IO}$	Operating supply conditions		3.15	—	3.6	V
Data Rate						
DATARATE	Data rate	—	—	312/320	Typ+0.1%	Mbps
STARTUP						
T_{STRT_BIAS}	Bias startup time[2]	—	—	0.5	3	µs
T_{PD2NM_TX}	Transmitter startup time (power down to normal mode)[3]	—	—	0.2	2	µs
T_{SM2NM_TX}	Transmitter startup time (sleep mode to normal mode)[4]	—	—	0.2	0.5	µs
T_{PD2NM_RX}	Receiver startup time[5] (Power down to Normal mode)	—	—	20	40	ns
T_{PD2SM_RX}	Receiver startup time[4] (Power down to Sleep mode)	—	—	20	50	ns

Table continues on the next page...

Table 49. LFAST electrical characteristics (continued)

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
TRANSMITTER						
V_{OS_DRF}	Common mode voltage	—	1.18	—	1.32	V
$\lvert\Delta V_{OD\_DRF}\rvert$	Differential output voltage swing (terminated)	—	±100	±200	± 285	mV
T_{TR_DRF}	Rise/Fall time (10% - 90% of swing)	—	0.26	—	1.5	ns
R_{OUT_DRF}	Terminating resistance	—	67	—	198	Ω
C_{OUT_DRF}	Capacitance[6]	—	—	—	5	pF
RECEIVER						
V_{ICOM_DRF}	Common mode voltage	—	0.15[7]	—	1.6[8]	V
$\lvert ID_{VI\_DRF}\rvert$	Differential input voltage	—	100	—	—	mV
V_{HYS_DRF}	Input hysteresis	—	25	—	—	mV
R_{IN_DRF}	Terminating resistance	—	80	115	150	Ω
C_{IN_DRF}	Capacitance[9]	—	—	3.5	6	pF
L_{IN_DRF}	Parasitic Inductance[10]	—	—	5	10	nH

1. $V_{DD\_VH\_IO}$ = 3.3 V -5%,+10%, T_J = –40 to 165 °C, unless otherwise specified
2. Startup time is defined as the time taken by LFAST current reference block for settling bias current after its pwr_down (power down) has been deasserted. LFAST functionality is guaranteed only after the startup time.
3. Startup time is defined as the time taken by LFAST transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
4. Startup time is defined as the time taken by LFAST transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
5. Startup time is defined as the time taken by LFAST receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
6. Total lumped capacitance including silicon, package pin and bond wire. Application board simulation is needed to verify LFAST template compliancy.
7. Absolute min = 0.15 V – (285 mV / 2) = 0 V
8. Absolute max = 1.6 V + (285 mV / 2) = 1.743 V
9. Total capacitance including silicon, package pin and bond wire
10. Total inductance including silicon, package pin and bond wire

Table 50. LFAST electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Nominal	Max	
F_{RF_REF}	SysClk Frequency	—	10	—	26	MHz
ERR_{REF}	SysClk Frequency Error	—	-1	—	1	%
DC_{REF}	SysClk Duty Cycle	—	45	—	55	%
C_{LOAD}	Output Buffer Load Capacitance	—	—	—	10	pF
R_{LOAD}	Output Buffer Load Resistance	—	10	—	—	kΩ

Table continues on the next page...

Table 50. LFAST electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Nominal	Max	
PN	Integrated Phase Noise (single side band)	20 MHz	—	—	-58	dBc
		10 MHz	—	—	-64	dBc
F_{VCO}	PLL VCO Frequency	—	—	320	—	MHz
T_{LOCK}	PLL Phase Lock	—	—	—	40	µs
ΔPER	PLL Long Term Jitter (peak to peak)	—	—	—	600	ps

1. The specifications in this table apply to both the interprocessor bus and debug LFAST interfaces.

3.19.7 FlexRay

3.19.7.1 FlexRay timing parameters

This section provides the FlexRay interface timing characteristics for the input and output signals. These numbers are recommended per the FlexRay Electrical Physical Layer Specification, Version 3.0.1, and subject to change per the final timing analysis of the device.

3.19.7.2 TxEN

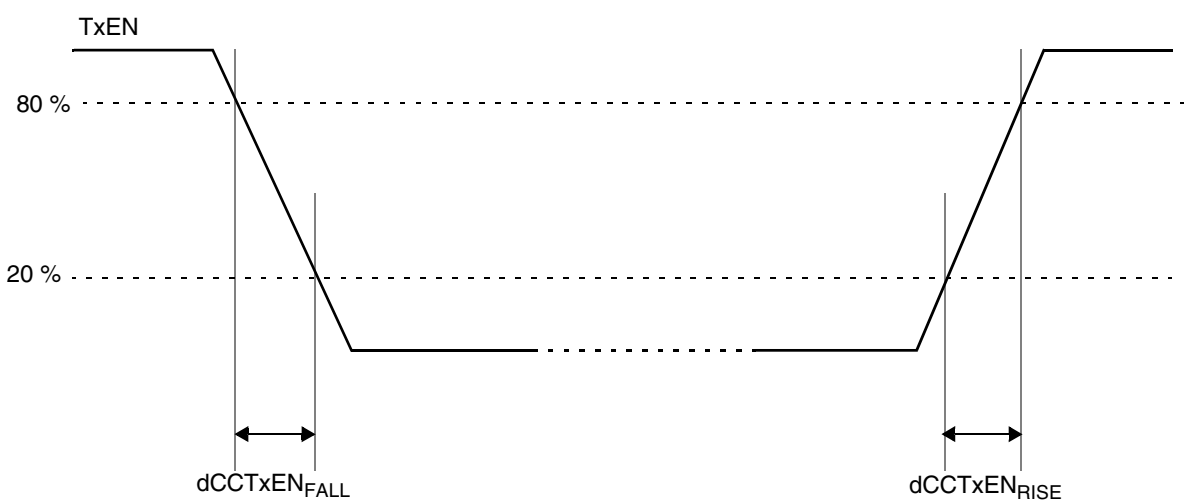


Figure 33. FlexRay TxEN signal

Table 51. TxEN output characteristics[1]

Name	Description	Min	Max	Unit
$dCCTxEN_{RISE25}$	Rise time of TxEN signal at CC	—	9	ns
$dCCTxEN_{FALL25}$	Fall time of TxEN signal at CC	—	9	ns
$dCCTxEN_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxEN_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IO}$ = 3.3 V -5%, +10%, T_J = –40 °C / 165 °C, TxEN pin load maximum 25 pF

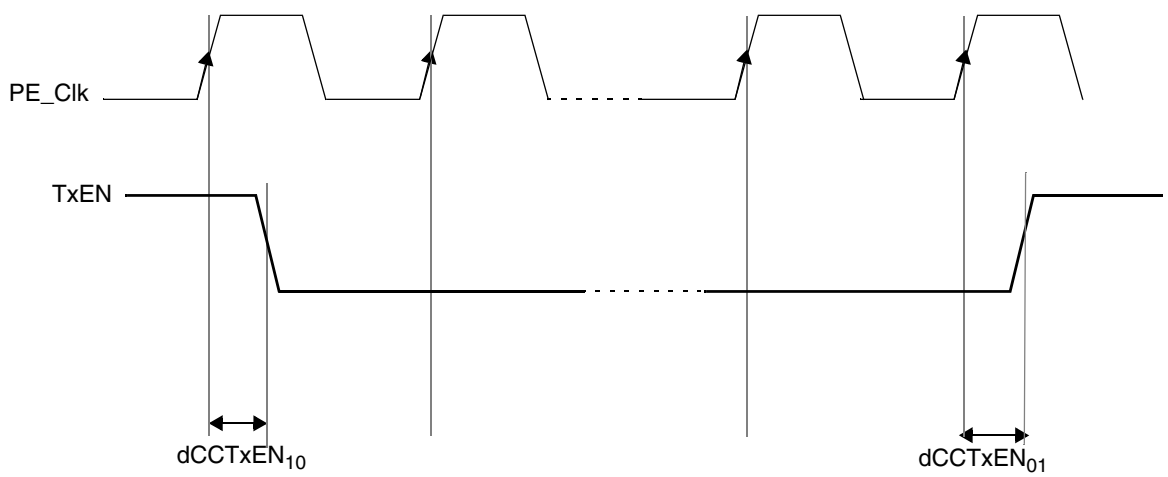


Figure 34. FlexRay TxEN signal propagation delays

3.19.7.3 TxD

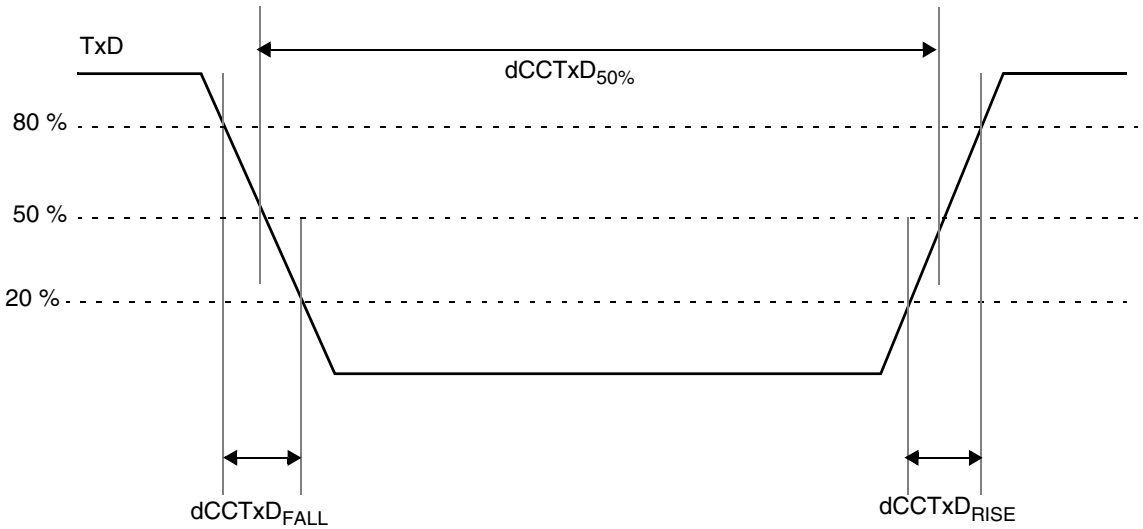
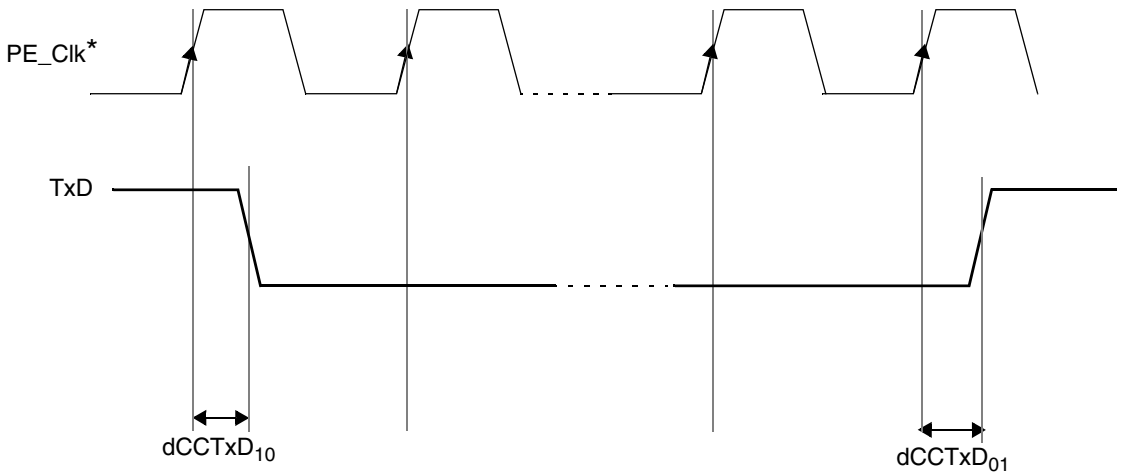


Figure 35. FlexRay TxD signal

Table 52. TxD output characteristics

Name	Description[1]	Min	Max	Unit
$dCCT_{xAsym}$	Asymmetry of sending CC @ 25 pF load (=$dCCTxD_{50\%}$ - 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	Sum of Rise and Fall time of TxD signal at the output	—	9	ns
$dCCTxD_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IO}$ = 3.3 V -5%, +10%, T_J = –40 °C / 165 °C, TxD pin load maximum 25 pF



*FlexRay Protocol Engine Clock

Figure 36. FlexRay TxD signal propagation delays

3.19.7.4 RxD

Table 53. RxD input characteristic

Name	Description[1]	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns

1. All parameters specified for $V_{DD\_HV\_IO}$ = 3.3 V -5%, +10%, T_J = –40 / 165 °C

3.19.7.5 Receiver asymmetry

Table 54. Receiver asymmetry

Name	Description	Min	Max	Unit
$dCCRxAsymAccept_{15}$	Acceptance of asymmetry at receiving CC with 15 pF load (*)	–31.5	+44.0	ns
$dCCRxAsymAccept_{25}$	Acceptance of asymmetry at receiving CC with 25 pF load (*)	–30.5	+43.0	ns

3.19.8 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

3.19.8.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 55. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

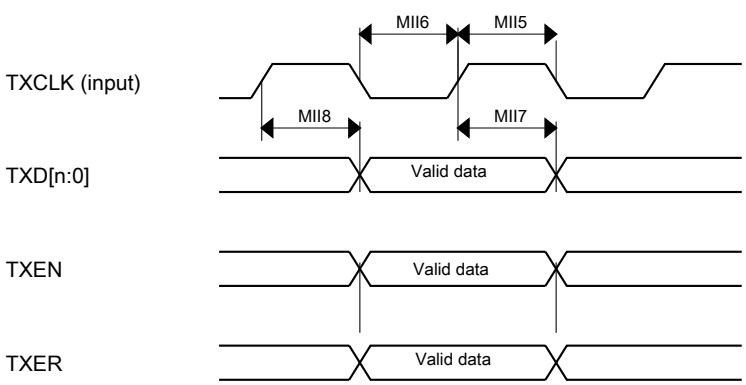


Figure 37. RMII/MII transmit signal timing diagram

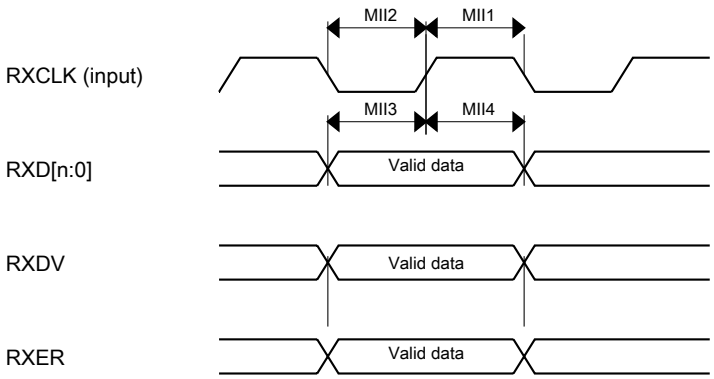


Figure 38. RMII/MII receive signal timing diagram

3.19.8.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 56. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

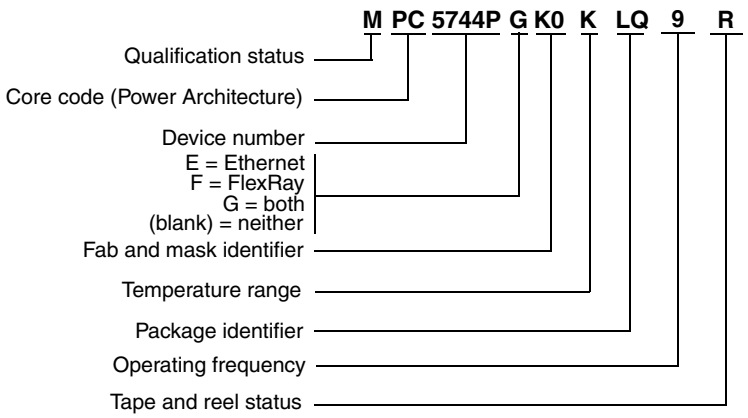
4 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
144-pin LQFP	98ASS23177W
257-ball MAPBGA	98ASA00081D

5 Ordering information



Temperature range	Package identifier	Operating frequency	Qualification status	Tape and reel status
M = –40°C to +125°C K = –40°C to +135°C for extended temp (+165°C T_J)	LQ = 144 LQFP MM = 257 MAPBGA	9 = 200 MHz 8 = 180 MHz 5 = 150 MHz	P = Pre-qualification M = Fully spec. qualified, general market flow S = Fully spec. qualified, automotive flow	R = Tape and reel (blank) = Trays

Note: Not all options are available on all devices.

Table 57. Orderable part number examples

Part number[1]	Flash/SRAM	Package	Other features
SPC5744PFK1MLQ9	2.5 MB/384 KB	144 LQFP (Pb free)	-40 to +125 °C
SPC5744PGK1MMM9	2.5 MB/384 KB	257 MAPBGA (Pb free)	Ethernet interface LFAST interface Nexus Aurora -40 to +125 °C
SPC5743PFK1MLQ9	2 MB/256 KB	144 LQFP (Pb free)	-40 to +125 °C
SPC5743PGK1MMM9	2 MB/256 KB	257 MAPBGA (Pb free)	Ethernet interface LFAST interface Nexus Aurora -40 to +125 °C
SPC5742PFK1MLQ9	1.5 MB/192 KB	144 LQFP (Pb free)	-40 to +125 °C
SPC5742PGK1MMM9	1.5 MB/192 KB	257 MAPBGA (Pb free)	Ethernet interface LFAST interface Nexus Aurora -40 to +125 °C
SPC5741PFK1MLQ9	1 MB/128 KB	144 LQFP (Pb free)	-40 to +125 °C
SPC5741PGK1MMM9	1 MB/128 KB	257 MAPBGA (Pb free)	Ethernet interface LFAST interface Nexus Aurora -40 to +125 °C

1. All packaged devices are PPC, rather than MPC or SPC, until product qualifications are complete. Not all configurations are available in the PPC parts.

6 Document revision history

The following table summarizes revisions to this document since the previous release.

Table 58. Revision history

Revision	Date	Description of changes

5	08/2015	Recommended operating conditions
		• In Table 13 existing row for $V_{DD\_LV\_COR}$, added a footnote "The chip functions down to the point where LVD_CORE or up to the point where HVD_CORE resets the chip by default."
		
		RESET sequence duration
		• In Table 38 existing row for T_{DRB}, typical value removed and max value changed from 14 to 18 ms.
		• In Table 38 existing row for T_{ERLB}, typical value removed and max value changed from 13.5 to 17.5 ms.
		
		ADC electrical characteristics
		• Added a note: "The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel".
		
		16 MHz Internal RC Oscillator (IRCOSC) electrical specifications
		• In Table 26 existing row δF_{var_noT} added a footnote: "The typical user trim step size (dfTRIM) .....on characterization results."
		
		Reset pad (EXT_POR, RESET) electrical characteristics
		• Updated Figure 9 and Figure 10
		• Updated Table 40 and seperated EXT_POR electrical specifications into new Table 41
		• Added Table 41 for EXT_POR electrical specifications.
		
		DC electrical characteristics
		• In Table 20 updated LV (core) Supply Voltage to 1.19 volts
		
		Voltage regulator electrical characteristics
		• In Table 17 existing row "supply ramp rate" max value is changed from 1 V/ms to 0.125 V/µs.
		
		LVDS pins/balls
		• Deleted "Debug LFAST" from foot note 1 in Table 6
		
		Generic pins/balls
		• In Table 8
		  • Signal description of port pin I[5] is changed from "LFAST PLL Phase 0 clock on negative terminal" to "SIPI/LFAST PLL Phase 0 clock on negative terminal".
		  • Signal description of port pin C[12] is changed from "LFAST PLL Phase 0 clock on positive terminal" to "SIPI/LFAST PLL Phase 0 clock on positive terminal".

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Document Number MPC5744P
Revision 5, 08/2015