MC9S08PB16 Reference Manual

Supports: MC9S08PB16VTJ MC9S08PB16MTJ MC9S08PB16VTG
MC9S08PB16MTG MC9S08PB8VTJ MC9S08PB8MTJ
MC9S08PB8VTG MC9S08PB8MTG

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Chapter 1
About This Document

1.1 Overview

1.1.1 Purpose

This document describes the features, architecture, and programming model of the NXP microcontrollers.

1.1.2 Audience

A reference manual is primarily for system architects and software application developers who are using or considering using an NXP product in a system.

1.2 Conventions

1.2.1 Numbering systems

The following suffixes identify different numbering systems:

This suffix	Identifies a
b	Binary number. For example, the binary equivalent of the number 5 is written 101b. In some cases, binary numbers are shown with the prefix *0b*.
d	Decimal number. Decimal numbers are followed by this suffix only when the possibility of confusion exists. In general, decimal numbers are shown without a suffix.
h	Hexadecimal number. For example, the hexadecimal equivalent of the number 60 is written 3Ch. In some cases, hexadecimal numbers are shown with the prefix *0x*.

1.2.2 Typographic notation

The following typographic notation is used throughout this document:

Example	Description
placeholder, x	Items in italics are placeholders for information that you provide. Italicized text is also used for the titles of publications and for emphasis. Plain lowercase letters are also used as placeholders for single letters and numbers.
`code`	Fixed-width type indicates text that must be typed exactly as shown. It is used for instruction mnemonics, directives, symbols, subcommands, parameters, and operators. Fixed-width type is also used for example code. Instruction mnemonics and directives in text and tables are shown in all caps; for example, BSR.
SR[SCM]	A mnemonic in brackets represents a named field in a register. This example refers to the Scaling Mode (SCM) field in the Status Register (SR).
REVNO[6:4], XAD[7:0]	Numbers in brackets and separated by a colon represent either: • A subset of a register's named field For example, REVNO[6:4] refers to bits 6–4 that are part of the COREREV field that occupies bits 6–0 of the REVNO register. • A continuous range of individual signals of a bus For example, XAD[7:0] refers to signals 7–0 of the XAD bus.

1.2.3 Special terms

The following terms have special meanings:

Term	Meaning
asserted	Refers to the state of a signal as follows: • An active-high signal is asserted when high (1). • An active-low signal is asserted when low (0).
deasserted	Refers to the state of a signal as follows: • An active-high signal is deasserted when low (0). • An active-low signal is deasserted when high (1). In some cases, deasserted signals are described as *negated*.
reserved	Refers to a memory space, register, or field that is either reserved for future use or for which, when written to, the module or chip behavior is unpredictable.

Chapter 2
Introduction

2.1 Introduction

The MC9S08PB16 devices are highly-integrated, low-power and low pin count 8-bit microcontrollers based on the S08L core platform.

The features are as follows:

- Maximum CPU frequency of 20 MHz which is used as bus frequency
- Scalable memory options, up to 16 KB Flash and 1 KB RAM
- Operating voltage ranges from 2.7 V to 5.5 V with full functional Flash program/erase/read operations
- Multiple package options of 20-pin and 16-pin
- Ambient operating temperature ranges from -40 °C to 105 °C for V part and -40 °C to 125 °C for M part

2.2 Module functional categories

The modules on this device are grouped into functional categories. Information found here describes the modules assigned to each category in more detail.

Table 2-1. Module functional categories

Module category	Description
HCS08 core	• 8-bit MCU core, 20 MHz CPU frequency.
System	• System integration module • Power management and mode controllers • Multiple power modes available based on run, wait, stop, and power-down modes • Interrupt priority controller (IPC)
Memories	• Up to 16 KB flash memory for PB16 and up to 8 KB flash memory for PB8 • Up to 1 KB SRAM
Clocks	• Internal clock source • 31.25 to 39.0625 kHz IRC

Table continues on the next page...

Table 2-1. Module functional categories (continued)

Module category	Description
	• 20 kHz oscillator with functional in all power modes • Frequency-locked loop • Oscillator (OSC), loop-controlled pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 4MHz to 20 MHz • DC to 20 MHz
Security	• Windowed COP watchdog • One cyclic redundancy check (CRC) • One fault detect and shutdown (FDS) module
Analog	• One 12-bit analog-to-digital converters (ADC) • Two high speed comparators (CMP) with internal 6-bit digital-to-analog converter (DAC) • One operational amplifier (OPAMP)
Timers	• Up to two 16-bit FTM modules • Two 8-bit modulo timer (MTIM) modules • One pulse width timers (PWT) • One real timer clock (RTC)
Communications	• One inter-integrated circuit (I^2C) module • One serial communications interface (SCI)
Human-Machine Interfaces (HMI)	• Port control (PORT) • One keyboard interrupt (KBI)

2.2.1 S08L core modules

The following core modules are available on this device.

Table 2-2. Core modules

Module	Description
HCS08 V6 CPU	The HCS08 CPU is fully source- and object-code-compatible with the M68HC08 CPU. Several instructions and enhanced addressing modes were added to improve C compiler efficiency and to support a new background debug system which replaces the monitor mode of earlier M68HC08 microcontrollers.
Debug module	The DBG module implements an on-chip ICE (in-circuit emulation) system and allows non-intrusive debug of application software by providing an on-chip trace buffer with flexible triggering capability. The trigger can also provide extended breakpoint capacity. The on-chip ICE system is optimized for the HCS08 8-bit architecture and supports 64 KB of memory space.

2.2.2 System modules

The following system modules are available on this device.

Table 2-3. System modules

Module	Description
System Control module (SYS)	The SYS includes integration logic and several module configuration settings.
Power management controller (PMC)	The PMC provides the user with multiple power options. Multiple modes are supported that allow the user to optimize power consumption for the level of functionality needed. Includes power-on-reset (POR) and integrated low voltage detect (LVD) with reset (brownout) capability and selectable LVD trip points.
Development support	Development supports single-wire background debug mode (BDM), which uses the on-chip background debug controller (BDC) module, and the independent on-chip realtime in-circuit emulation (ICE) system, which uses the on-chip debug (DBG) module.
Debug module (DBG)	The DBG module implements an on-chip ICE (in-circuit emulation) system and allows non-intrusive debug of application software by providing an on-chip trace buffer with flexible triggering capability.

2.2.3 Memories and memory interfaces

The following memories and memory interfaces are available on this device.

Table 2-4. Memories and memory interfaces

Module	Description
Flash memory	Program flash memory — up to 16 KB or 8 KB of the non-volatile flash memory that can execute program code.
SRAM	Up to 1 KB random-access memory (RAM).

2.2.4 Clocks

The following clock modules are available on this device.

Table 2-5. Clock modules

Module	Description
Internal Clock Source (ICS)	ICS module containing an internal reference clock (ICSIRCLK) and a frequency locked loop (FLL).
Oscillator (OSC)	The OSC module, in conjunction with an external crystal or resonator, generates a clock for the MCU that can be used as reference clock or bus clock.
Low-Power Oscillator (LPO)	The PMC module contains a 1 kHz low-power oscillator which acts as a standalone low-frequency clock source in all modes.

2.2.5 Security and integrity modules

The following security and integrity modules are available on this device:

Table 2-6. Security and integrity modules

Module	Description
Windowed COP watchdog (WCOP)	The COP watchdog is used to force a system reset when the application software fails to execute as expected.
Cyclic Redundancy Check (CRC)	The cyclic redundancy check (CRC) module generates 16/32-bit CRC code for error detection.
Fault Detect and Shutdown (FDS)	The FDS module provides a mechanism to immediately place port pins in a pre-defined state when a fault condition occurs.

2.2.6 Analog modules

The following analog modules are available on this device:

Table 2-7. Analog modules

Module	Description
Analog-to-digital converters (ADC)	12-bit successive-approximation ADC module.
Comparator (CMP)	Two comparators that compare two analog input voltages across the full range of the supply voltage and can trigger an ADC acquisition, FTM update, or CPU interrupt.
6-bit digital-to-analog converters (DAC)	64-tap resistor ladder network which provides a selectable voltage reference for comparator.
Operational Amplifier (OPAMP)	• x 20 default gain • 0-100mV input range • single-ended • gain adjustable with external resistor (only feasible for differential input)

2.2.7 Timer modules

The following timer modules are available on this device:

Table 2-8. Timer modules

Module	Description
FlexTimer Module (FTM)	• Selectable FTM source clock, programmable prescaler • 16-bit counter supporting free-running, and counting is up or up-down • Input capture, output compare, and edge-aligned and center-aligned PWM modes

Table continues on the next page...

Table 2-8. Timer modules (continued)

Module	Description
	• Operation of FTM channels as pairs with equal outputs or independent channels with independent outputs • Programmable interrupt on input capture, reference compare, overflowed counter
Pulse Width Timer (PWT)	• Automatic measurement of pulse width with 16-bit resolution • Separate positive and negative pulse width measurements • Programmable triggering edge for starting measurement • Programmable measuring time between successive alternating edges, rising edges or falling edges • Programmable pre-scaler from clock input as 16-bit counter time base • Two selectable clock sources • Four selectable pulse inputs • Programmable interrupt generation upon pulse width value updated and counter overflow
8-bit modulo timer (MTIM)	• 8-bit up-counter • Four software selectable clock sources for input to prescaler • Nine selectable clock prescale values • Modulo compare matched can be an output
Real Time Clock (RTC)	The RTC is consisting of one 16-bit counter, one 16-bit comparator, several binary-based and decimal-based prescaler dividers, two clock sources, and one programmable periodic interrupt.

2.2.8 Communication interfaces

The following communication interfaces are available on this device:

Table 2-9. Communication modules

Module	Description
Inter-integrated circuit (I2C)	Allows communication between a number of devices. Also supports the System Management Bus (SMBus) Specification, version 2.
Serial communications interface (SCI)	SCI is used to connect to the RS232 serial input/output port of a personal computer or workstation and communicate with other embedded controllers.

2.2.9 Human-machine interfaces

The following human-machine interfaces (HMI) are available on this device:

Table 2-10. HMI modules

Module	Description
Port Control (PORT)	Some general purpose input or output pins are capable of interrupt request generation.

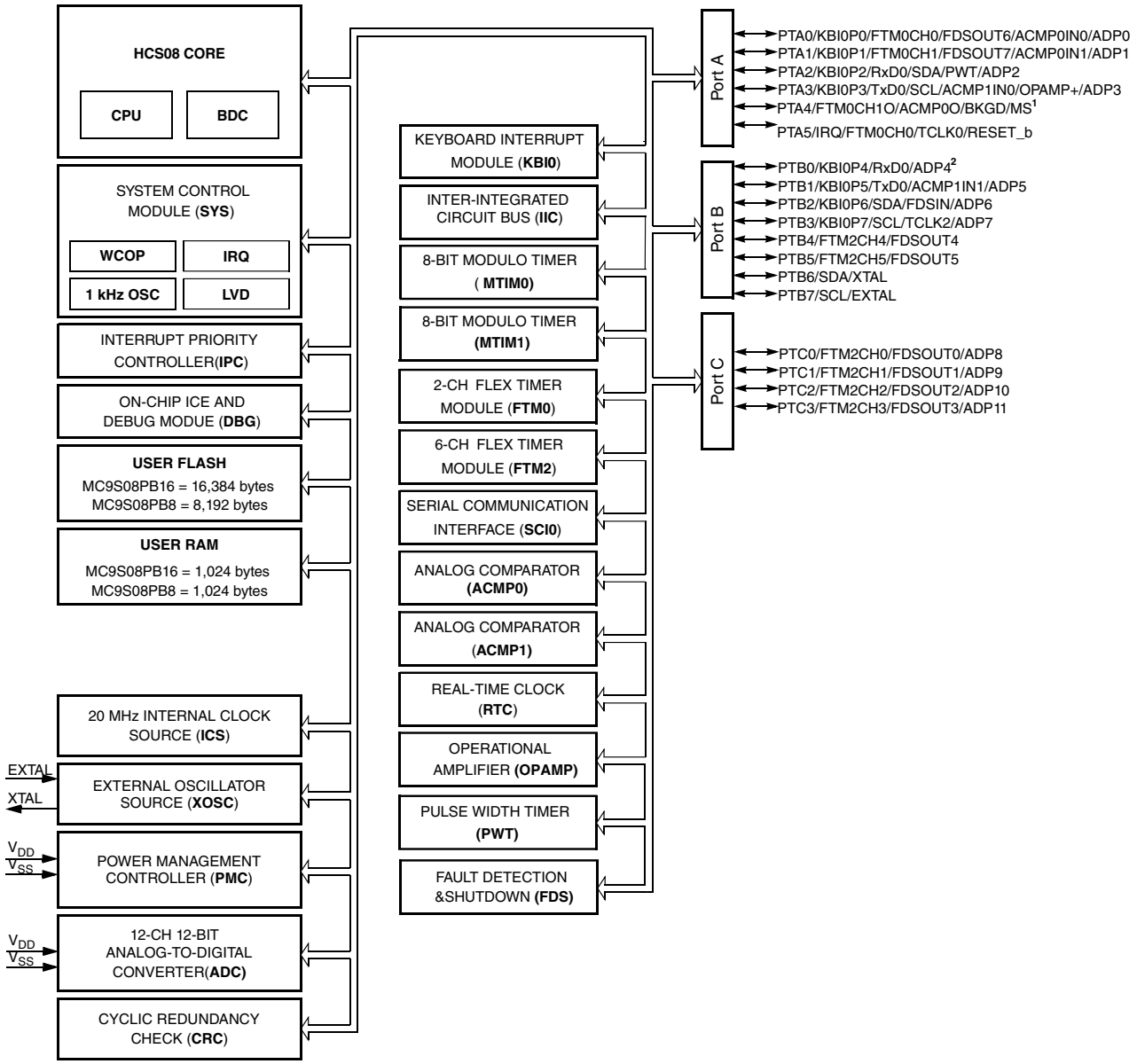
Table continues on the next page...

Table 2-10. HMI modules (continued)

Module	Description
Keyboard Interrupts (KBI)	• Up to eight keyboard interrupt pins with individual pin enable bits • Each keyboard interrupt pin is programmable • One software-enabled keyboard interrupt • Exit from low-power modes

2.3 MCU block diagram

The block diagram below shows the structure of the MCUs.



1. PTA4/FTM0CH1O/ACMP0O/BKGD/MS is an output-only pin when used as port pin.
2. PTB0 operates as true-open drain when working as output.

Figure 2-1. MCU block diagram

2.4 Orderable part numbers

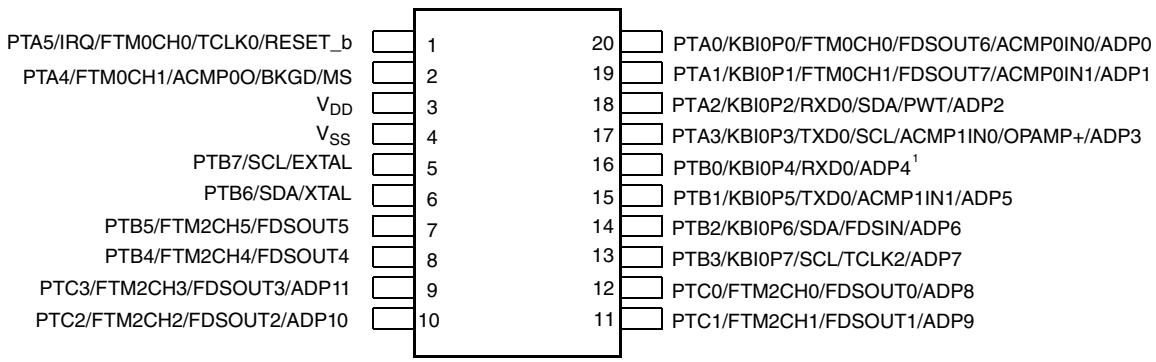
The following table summarizes the part numbers of the devices covered by this document.

Table 2-11. Orderable part numbers summary

Feature	MC9S08PB16		MC9S08PB8	
Part Number	VTJ	VTG	VTJ	VTG
	MTJ	MTG	MTJ	MTG
Max. frequency (MHz)	20	20	20	20
Flash memory (KB)	16	16	8	8
RAM (KB)	1	1	1	1
12-bit ADC	12ch	8ch	12ch	8ch
ACMP	2	2	2	2
OPAMP	1	1	1	1
16-bit FlexTimer	6ch+2ch	2ch+2ch	6ch+2ch	2ch+2ch
8-bit Modulo timer	2	2	2	2
RTC	Yes	Yes	Yes	Yes
PWT	1	1	1	1
I2C	1	1	1	1
SCI (LIN Capable)	1	1	1	1
WCOP	Yes	Yes	Yes	Yes
CRC	Yes	Yes	Yes	Yes
FDS	Yes	Yes	Yes	Yes
FDS pins	8	4	8	4
KBI pins	8	8	8	8
GPIO	18	14	18	14
Package	20-TSSOP	16-TSSOP	20-TSSOP	16-TSSOP

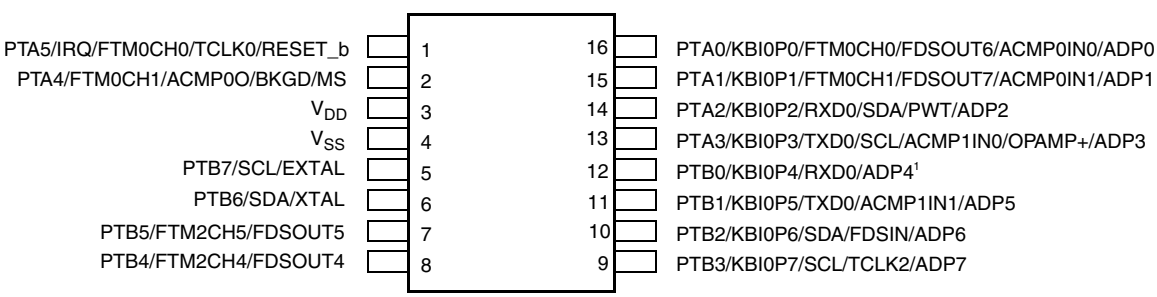
Chapter 3
Pins and connections

3.1 Device pin assignment



1. True open drain pin

Figure 3-1. 20-pin TSSOP package



1. True open drain pin

Figure 3-2. 16-pin TSSOP package

3.2 Pin functions

3.2.1 Power (V_{DD}, V_{SS})

V_{DD} and V_{SS} are the primary power supply pins for the MCU. This voltage source supplies power to all I/O buffer circuitry and to an internal voltage regulator. The internal voltage regulator provides a regulated lower-voltage source to the CPU and to the MCU's other internal circuitry.

Typically, application systems have two separate capacitors across the power pins. In this case, there should be a bulk electrolytic capacitor, such as a 10 µF tantalum capacitor, that provides bulk charge storage for the overall system and a 0.1 µF ceramic bypass capacitor located as near to the paired V_{DD} and V_{SS} power pins as practical to suppress high-frequency noise.

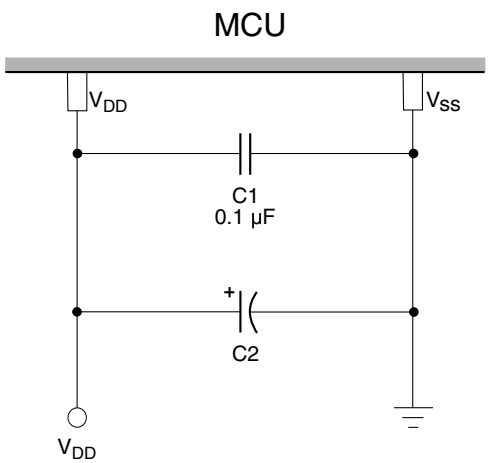


Figure 3-3. Power supply bypassing

3.2.2 Analog power supply and reference pins (V_{DDA}/V_{REFH} and V_{SSA}/V_{REFL})

V_{DDA} and V_{SSA} are the power supply pins for the analog-to-digital converter (ADC). Connect the V_{DDA} pin to the same voltage potential as V_{DD}, and the V_{SSA} pin to the same voltage potential as V_{SS}.

De-coupling of these pins should be as per the digital supply. A 0.1 µF ceramic bypass capacitor should be located as near to the MCU power pins as practical to suppress high-frequency noise.

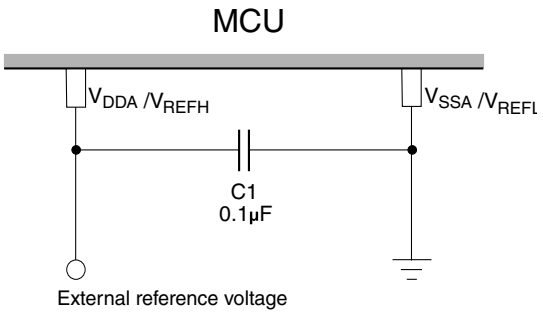


Figure 3-4. Analog power supply bypassing

V_{REFH} is the high reference supply for the ADC, and is internally connected to V_{DDA}. V_{REFL} is the low reference supply for the ADC, and is internally connected to V_{SSA}.

3.2.3 Oscillator (XTAL, EXTAL)

The XTAL and EXTAL pins are used to provide the connections for the on-chip oscillator. The oscillator (XOSC) in this MCU is a Pierce oscillator that can accommodate a crystal or ceramic resonator. Optionally, an external clock source can be connected to the EXTAL input pin. The oscillator can be configured to run in stop3 mode.

Refer to the following figure, R_S (when used) and R_F must be low-inductance resistors such as carbon composition resistors. Wire-wound resistors, and some metal film resistors, have too much inductance. C1 and C2 normally must be high-quality ceramic capacitors that are specifically designed for high-frequency applications.

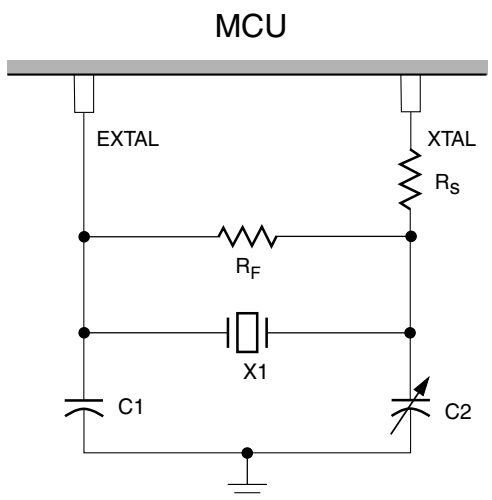


Figure 3-5. Typical crystal or resonator circuit

R_F is used to provide a bias path to keep the EXTAL input in its linear range during crystal startup; its value is not generally critical. Typical systems use 1 M to 10 M. Higher values are sensitive to humidity and lower values reduce gain and (in extreme cases) could prevent startup.

C1 and C2 are typically in the 5 pF to 25 pF range and are chosen to match the requirements of a specific crystal or resonator. Take into account printed circuit board (PCB) capacitance and MCU pin capacitance when selecting C1 and C2. The crystal manufacturer typically specifies a load capacitance, which is the series combination of C1 and C2 (which are usually the same size). As a first-order approximation, use 10 pF as an estimate of combined pin and PCB capacitance for each oscillator pin (EXTAL and XTAL).

3.2.4 External reset pin ($\overline{\text{RESET}}$)

A low on the $\overline{\text{RESET}}$ pin forces the MCU to a known startup state. $\overline{\text{RESET}}$ is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. This pin contains an internal pullup resistor.

RESET shares an I/O pin with PTA5. The $\overline{\text{RESET}}$ pin function is enabled by default after POR reset, because internal power-on reset and low-voltage reset circuitry typically make external reset circuitry unnecessary. This pin is normally connected to the standard 6-pin background debug connector so that a development system can directly reset the MCU system. If $\overline{\text{RESET}}$ function of PTA5/IRQ/FTM0CH0/TCLK0/$\overline{\text{RESET}}$ pin is enabled, a manual external reset can be added by supplying a simple switch to ground (pull reset pin low to force a reset). When the $\overline{\text{RESET}}$ pin function is enabled, an internal pullup resistor is connected to this pin and a reset signal can feed into MCU with an input hysteresis. POR reset brings $\overline{\text{RESET}}$ pin into its default configuration, reset other than POR has no effect on the $\overline{\text{RESET}}$ pin function configuration.

When PTA5/IRQ/FTM0CH0/TCLK0/$\overline{\text{RESET}}$ is enabled as IRQ pin, it is the input source for the IRQ interrupt and is also the input for the BIH and BIL instructions. IRQ is asynchronous external interrupt pins.

In EMC-sensitive applications, an external RC filter is recommended on the reset pin. See the following figure for example.

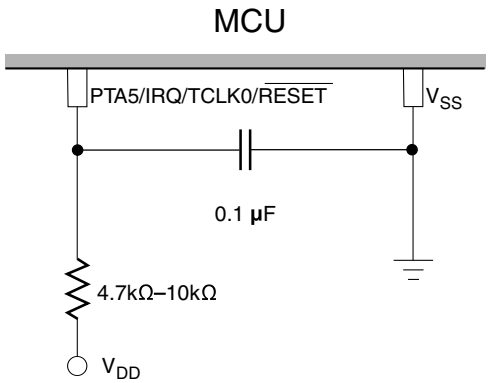


Figure 3-6. PTA5/IRQ/FTM0CH0/TCLK0/$\overline{\text{RESET}}$ external RC filter

3.2.5 Background/mode select (BKGD/MS)

During a power-on-reset (POR) or background debug force reset, the PTA4/FTM0CH1O/ACMP0O/BKGD/MS pin functions as a mode select pin. Immediately after internal reset rises the pin functions as the background pin and can be used for background debug communication. While the pin functions as a background/mode selection pin, it includes an internal pullup device and a standard output driver.

The background debug communication function is enabled when SOPT1[BKGDPE] bit is set. SOPT1[BKGDPE] is set following any reset of the MCU and must be cleared to use the PTA4/FTM0CH1O/ACMP0O/BKGD/MS pin's alternative pin functions.

If this pin is floating, the MCU will enter normal operating mode at the rising edge of reset. If a debug system is connected to the 6-pin standard background debug header, it can hold BKGD/MS low during the POR or immediately after issuing a background debug force reset, which will force the MCU into active background mode.

The BKGD pin is used primarily for background debug controller (BDC) communications using a custom protocol that uses 16 clock cycles of the target MCU's BDC clock per bit time. The target MCU's BDC clock can run as fast as the bus clock, so there should never be any significant capacitance connected to the BKGD/MS pin that interferes with background serial communications. When the pin performs output only PTA4, it can drive only capacitance-limited MOSFET. Driving a bipolar transistor directly by PTA4 is prohibited because this can cause mode entry fault and BKGD errors.

Although the BKGD pin is a pseudo open-drain pin, the background debug communication protocol provides brief, actively driven, high speedup pulses to ensure fast rise time. Small capacitances from cables and the absolute value of the internal pullup device play almost no role in determining rise and fall time on the BKGD pin.

3.2.6 Port A input/output (I/O) pins (PTA5-PTA0)

PTA5–PTA0 are general-purpose, bidirectional I/O port pins. These port pins also have selectable pullup devices when configured for input mode except PTA4. The pullup devices are selectable on an individual port bit basis. The pulling devices are disengaged when configured for output mode except when PTA2 and PTA3 are used as SDA and SCL function.

PTA4 is output only when used as port pin. The pulling device is disabled at this condition.

3.2.7 Port B input/output (I/O) pins (PTB7–PTB0)

PTB7–PTB0 are general-purpose, bidirectional I/O port pins. These port pins also have selectable pullup devices when configured for input mode, the pullup devices are selectable on an individual port bit basis. The pulling devices are disengaged when configured for output mode.

3.2.8 Port C input/output (I/O) pins (PTC–PTC0)

PTC3–PTC0 are general-purpose, bidirectional I/O port pins. These port pins also have selectable pullup devices when configured for input mode, and the pullup devices are selectable on an individual port bit basis. The pulling devices are disengaged when configured for output mode.

3.3 Peripheral pinouts

These MCUs support up to 18 general-purpose I/O pins, which are shared with on-chip peripheral functions (FTM, ACMP, ADC, SCI, KBI, etc.).These 18 general-purpose I/O pins include one output-only pin (PTA4).

When a port pin is configured as general-purpose input, or when a peripheral uses the port pin as an input, the software can enable a pullup device.

For information about controlling these pins as general-purpose I/O pins, see the Port Control. For information about how and when on-chip peripheral systems use these pins, see the appropriate module chapter.

Immediately after reset, all pins are configured as high-impedance general-purpose IO with internal pullup devices disabled.

Table 3-1. Pin availability by package pin-count

Pin number		Lowest Priority <-- --> Highest					
20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4	Alt 5
1	1	PTA5	IRQ	FTM0CH0	TCLK0	-	RESET
2	2	PTA4	-	FTM0CH1	ACMP0O	BKGD	MS
3	3	-	-	-	-	-	VDD
4	4	-	-	-	-	-	VSS
5	5	PTB7	-	-	SCL	-	EXTAL
6	6	PTB6	-	-	SDA	-	XTAL
7	7	PTB5	-	FTM2CH5	-	FDSOUT5	-
8	8	PTB4	-	FTM2CH4	-	FDSOUT4	-
9	-	PTC3	-	FTM2CH3	-	FDSOUT3	ADP11
10	-	PTC2	-	FTM2CH2	-	FDSOUT2	ADP10
11	-	PTC1	-	FTM2CH1	-	FDSOUT1	ADP9
12	-	PTC0	-	FTM2CH0	-	FDSOUT0	ADP8
13	9	PTB3	KBI0P7	SCL	TCLK2	-	ADP7
14	10	PTB2	KBI0P6	SDA	-	FDSIN	ADP6
15	11	PTB1	KBI0P5	TXD0	-	-	ACMP1IN1/ ADP5
16	12	PTB0 [1]	KBI0P4	RXD0	-	-	ADP4
17	13	PTA3	KBI0P3	TXD0	SCL	-	ACMP1IN0/ OPAMP+/ ADP3
18	14	PTA2	KBI0P2	RXD0	SDA	PWT	ADP2
19	15	PTA1	KBI0P1	FTM0CH1	-	FDSOUT7	ACMP0IN1/ ADP1
20	16	PTA0	KBI0P0	FTM0CH0	-	FDSOUT6	ACMP0IN0/ ADP0

1. This is a true open-drain pin when operating as output.

NOTE

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

Chapter 4
Power management

4.1 Introduction

The operating modes of the device are described in this chapter. Entry into each mode, exit from each mode, and functionality while in each of the modes are described.

4.2 Features

These MCUs feature the following power modes:

- Run mode
- Wait mode
  - CPU shuts down to conserve power
  - Bus clocks are running
  - Full voltage regulation is maintained
- Stop3 modes
  - System clocks stopped; voltage regulator in standby
  - all internal circuits powered for fast recovery

4.2.1 Run mode

This is the normal operating mode. In this mode, the CPU executes code from internal memory with execution beginning at the address fetched from memory at 0xFFFE: 0xFFFF after reset. The power supply is fully regulating and all peripherals can be active in run mode.

4.2.2 Wait mode

Wait mode is entered by executing a WAIT instruction. Upon execution of the WAIT instruction, the CPU enters a low-power state in which it is not clocked. The I bit in CCR is cleared when the CPU enters the wait mode, enabling interrupts. When an interrupt request occurs, the CPU exits the wait mode and resumes processing, beginning with the stacking operations leading to the interrupt service routine.

While the MCU is in wait mode, there are some restrictions on which background debug commands can be used. Only the BACKGROUND command and memory-access-with-status commands are available when the MCU is in wait mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the MCU is in either stop or wait mode. The BACKGROUND command can be used to wake the MCU from wait mode and enter active background mode.

4.2.3 Stop3 mode

To enter stop3, the user must execute a STOP instruction with stop mode enabled (SOPT1[STOPE] = 1). Upon entering the stop3 mode, all of the clocks in the MCU are halted by default, but OSC clock and internal reference clock can be turned on by setting the ICS control registers. The ICS enters its standby state, as does the voltage regulator and the ADC. The states of all of the internal registers and logic, as well as the RAM content, are maintained. The I/O pin states are not latched at the pin. Instead they are maintained by virtue of the states of the internal logic driving the pins being maintained.

Exit from stop3 is done by asserting reset or through an interrupt. The interrupt include the asynchronous interrupt from the IRQ or KBI pins, the SCI receive interrupt, the ADC, ACMP, I^2C or LVI interrupt and the real-time interrupt.

If stop3 is exited by means of the $\overline{\text{RESET}}$ pin, then the MCU will be reset and operation will resume after taking the reset vector. Exit by means of an asynchronous interrupt or the real-time interrupt will result in the MCU taking the appropriate interrupt vector.

The LPO (≈1 kHz) for the real-time counter clock allows a wakeup from stop3 mode with no external components. When RTC_SC2[RTCPS] is clear, the real-time counter clock function is disabled.

4.2.4 Active BDM enabled in stop3 mode

Entry into the active background mode from run mode is enabled if the BDC_SCR[ENBDM] bit is set. This register is described in the development support. If BDC_SCR[ENBDM] is set when the CPU executes a STOP instruction, the system clocks to the background debug logic remain active when the MCU enters stop mode, so background debug communication is still possible. In addition, the voltage regulator does not enter its low-power standby state but maintains full internal regulation.

Most background commands are not available in stop mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the MCU is in either stop or wait mode. The BACKGROUND command can be used to wake the MCU from stop and enter active background mode if the BDC_SCR[ENBDM] bit is set. After entering background debug mode, all background commands are available.

4.2.5 LVD enabled in stop mode

The LVD system is capable of generating either an interrupt or a reset when the supply voltage drops below the LVD voltage. If the LVD is enabled in stop (LVDE and LVDSE bits in SPMSC1 both set) at the time the CPU executes a STOP instruction, then the voltage regulator remains active during stop3 mode.

4.2.6 Power modes behaviors

Executing the WAIT or STOP command puts the MCU in a low power consumption mode for standby situations. The system integration module (SIM) holds the CPU in a non-clocked state. The operation of each of these modes is described in the following subsections. Both STOP and WAIT clear the interrupt mask (I) in the condition code register, allowing interrupt to occur. The following table shows the low power mode behaviors.

Table 4-1. Low power mode behavior

Mode	Run	Wait	Stop3
PMC	Full regulation	Full regulation	Loose regulation
ICS	On	On	Optional on
OSC	On	On	Optional on
LPO	On	On	On
CPU	On	Standby	Standby
FLASH	On	On	Standby

Table continues on the next page...

Table 4-1. Low power mode behavior (continued)

Mode	Run	Wait	Stop3
RAM	On	Standby	Standby
ADC	On	On	Optional on
ACMP	On	On	Optional on
I/O	On	On	States held
SCI	On	On	Standby
I^2C	On	On	Standby
MTIM	On	On	Standby
OPAMP	On	On	Optional on
FDS	On	On	Standby
FTM	On	On	Standby
PWT	On	On	Standby
WDOG	On	On	Optional on
KBI	On	On	Optional on
DBG	On	On	Standby
IPC	On	On	Standby
CRC	On	On	Standby
RTC	On	On	Optional on
LVD	On	On	Optional on

4.3 Low voltage detect (LVD) system

This device includes a system to protect against low voltage conditions in order to protect memory contents and control MCU system states during supply voltage variations. This system consists of a power-on reset (POR) circuit and an LVD circuit with a user selectable trip voltage, either high (V_{LVDH}) or low (V_{LVDL}). The LVD circuit is enabled when SPMSC1[LVDE] is set and the trip voltage is selected by SPMSC2[LVDV]. The LVD is disabled upon entering the stop modes unless the SPMSC1[LVDSE] bit is set or active BDM enabled (BDCSCR[ENBDM]=1). If SPMSC1[LVDSE] and SPMSC1[LVDE] are both set, the current consumption in stop3 with the LVD enabled will be greater.

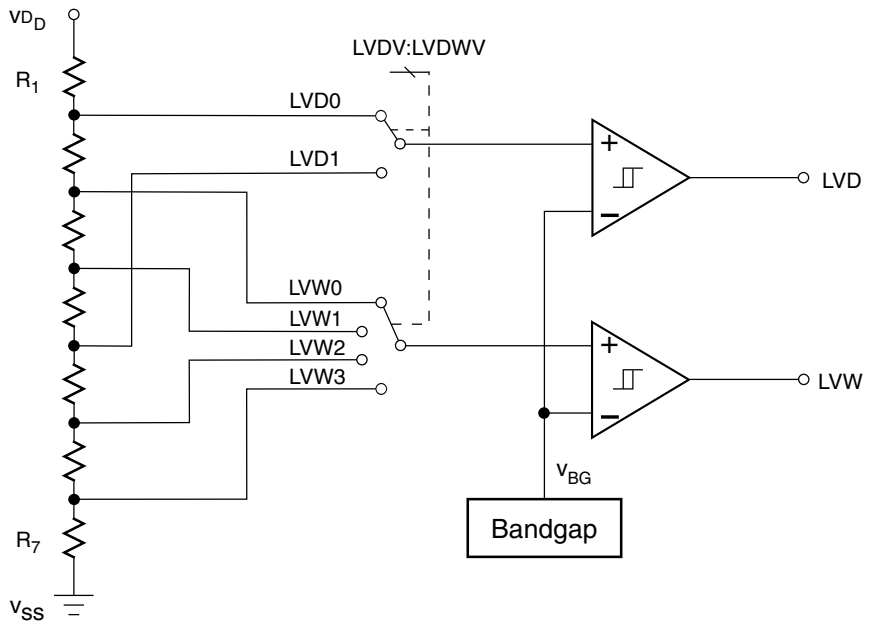


Figure 4-1. Low voltage detect (LVD) block diagram

4.3.1 Power-on reset (POR) operation

When power is initially applied to the MCU, or when the supply voltage drops below the V_{POR} level, the POR circuit will cause a reset condition. As the supply voltage rises, the LVD circuit will hold the chip in reset until the supply has risen above the V_{LVDL} level. Both the SRS[POR] and SRS[LVD] are set following a POR.

4.3.2 LVD reset operation

The LVD can be configured to generate a reset upon detection of a low voltage condition by setting SPMSC1[LVDRE] to 1. After an LVD reset has occurred, the LVD system will hold the MCU in reset until the supply voltage has risen above the level determined by LVDV. The SRS[LVD] bit is set following either an LVD reset or POR.

4.3.3 Low-voltage warning (LVW)

The LVD system has a low voltage warning flag to indicate that the supply voltage is approaching the LVD voltage. When a low voltage condition is detected and the LVD circuit is configured for interrupt operation (SPMSC1[LVDE] set, SPMSC1[LVWIE] set), SPMSC1[LVWF] will be set and LVW interrupt will occur. There are four user-selectable trip voltages for the LVW upon each LVDV configuration. The trip voltage is selected by SPMSC2[LVWV].

4.4 Power management control bits and registers

PMC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3040	System Power Management Status and Control 1 Register (PMC_SPMSC1)	8	R/W	1Ch	4.4.1/52
3041	System Power Management Status and Control 2 Register (PMC_SPMSC2)	8	R/W	00h	4.4.2/54

4.4.1 System Power Management Status and Control 1 Register (PMC_SPMSC1)

This high page register contains status and control bits to support the low-voltage detection function, and to enable the bandgap voltage reference for use by the ADC module. This register should be written during the user's reset initialization program to set the desired controls, even if the desired settings are the same as the reset settings.

Address: 3040h base + 0h offset = 3040h

Bit	7	6	5	4	3	2	1	0
Read	LVWF	0	LVWIE	LVDRE	LVDSE	LVDE	BGBDS	BGBE
Write		LVWACK						
Reset	0	0	0	1	1	1	0	0

PMC_SPMSC1 field descriptions

Field	Description
7 LVWF	Low-Voltage Warning Flag The LVWF bit indicates the low-voltage warning status. **NOTE:** LVWF will be set in the case when V_{Supply} transitions below the trip point or after reset and V_{Supply} is already below V_{LVW}. LVWF bit may be 1 after power on reset, therefore, to use LVW interrupt function, before enabling LVWIE, LVWF must be cleared by writing LVWACK first. 0 Low-voltage warning is not present. 1 Low-voltage warning is present or was present.
6 LVWACK	Low-Voltage Warning Acknowledge If LVWF = 1, a low-voltage condition has occurred. To acknowledge this low-voltage warning, write 1 to LVWACK, which automatically clears LVWF to 0 if the low-voltage warning is no longer present.
5 LVWIE	Low-Voltage Warning Interrupt Enable

Table continues on the next page...

PMC_SPMSC1 field descriptions (continued)

Field	Description
	This bit enables hardware interrupt requests for LVWF. 0 Hardware interrupt disabled (use polling). 1 Request a hardware interrupt when LVWF = 1.
4 LVDRE	Low-Voltage Detect Reset Enable This write-once bit enables LVD events to generate a hardware reset (provided LVDE = 1). **NOTE:** This bit can be written only one time after reset. Additional writes are ignored. 0 LVD events do not generate hardware resets. 1 Force an MCU reset when an enabled low-voltage detect event occurs.
3 LVDSE	Low-Voltage Detect Stop Enable Provided LVDE = 1, this read/write bit determines whether the low-voltage detect function operates when the MCU is in stop mode. 0 Low-voltage detect disabled during stop mode. 1 Low-voltage detect enabled during stop mode.
2 LVDE	Low-Voltage Detect Enable This write-once bit enables low-voltage detect logic and qualifies the operation of other bits in this register. **NOTE:** This bit can be written only one time after reset. Additional writes are ignored. 0 LVD logic disabled. 1 LVD logic enabled.
1 BGBDS	Bandgap Buffer Drive Select This bit is used to select the high drive mode of the bandgap buffer. 0 Bandgap buffer enabled in low drive mode if BGBE = 1. 1 Bandgap buffer enabled in high drive mode if BGBE = 1.
0 BGBE	Bandgap Buffer Enable This bit enables an internal buffer for the bandgap voltage reference for use by the ADC module on one of its internal channels. 0 Bandgap buffer disabled. 1 Bandgap buffer enabled.

4.4.2 System Power Management Status and Control 2 Register (PMC_SPMSC2)

This register is used to report the status of the low-voltage warning function, and to configure the stop mode behavior of the MCU. This register should be written during the user's reset initialization program to set the desired controls, even if the desired settings are the same as the reset settings.

Address: 3040h base + 1h offset = 3041h

Bit	7	6	5	4	3	2	1	0
Read	0	LVDV	LVWV		0			
Write								
Reset	0	0	0	0	0	0	0	0

PMC_SPMSC2 field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 LVDV	Low-Voltage Detect Voltage Select This write-once bit selects the low-voltage detect (LVD) trip point setting. See data sheet for details. 0 Low trip point selected ($V_{LVD} = V_{LVDL}$). 1 High trip point selected ($V_{LVD} = V_{LVDH}$).
5–4 LVWV	Low-Voltage Warning Voltage Select This bit selects the low-voltage warning (LVW) trip point voltage. See data sheet for details. 00 Low trip point selected ($V_{LVW} = V_{LVW1}$). 01 Middle 1 trip point selected ($V_{LVW} = V_{LVW2}$). 10 Middle 2 trip point selected ($V_{LVW} = V_{LVW3}$). 11 High trip point selected ($V_{LVW} = V_{LVW4}$).
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Chapter 5
Memory map

5.1 Memory map

In this device, the most frequently used registers are placed in the direct page, memory 0x0000 to 0x003F. Also a portion of RAM is placed in the direct page to take advantage of the direct addressing mode of the CPU. All other register locations in the extended page are the same in terms of instruction cycle times.The placement of the other peripheral modules is not critical because CPU instructions for all other extended memory have the same timing requirements.

As shown below, on-chip memory in this device consists of RAM and flash program memory for nonvolatile data storage, plus I/O and control/status registers. The registers are divided into three groups: direct-page registers, high-page registers and nonvolatile registers.

- User flash memory (flash)
  - MC9S08PB16: 16,384 bytes; 32 pages of 512 bytes each
  - MC9S08PB8: 8,192 bytes; 16 pages of 512 bytes each
- Random-access memory (RAM)
  - MC9S08PB16: 1,024 bytes
  - MC9S08PB8: 1,024 bytes
- Direct-page registers (0x0000 through 0x003F)
- High-page registers (0x3000 through 0x30FF)

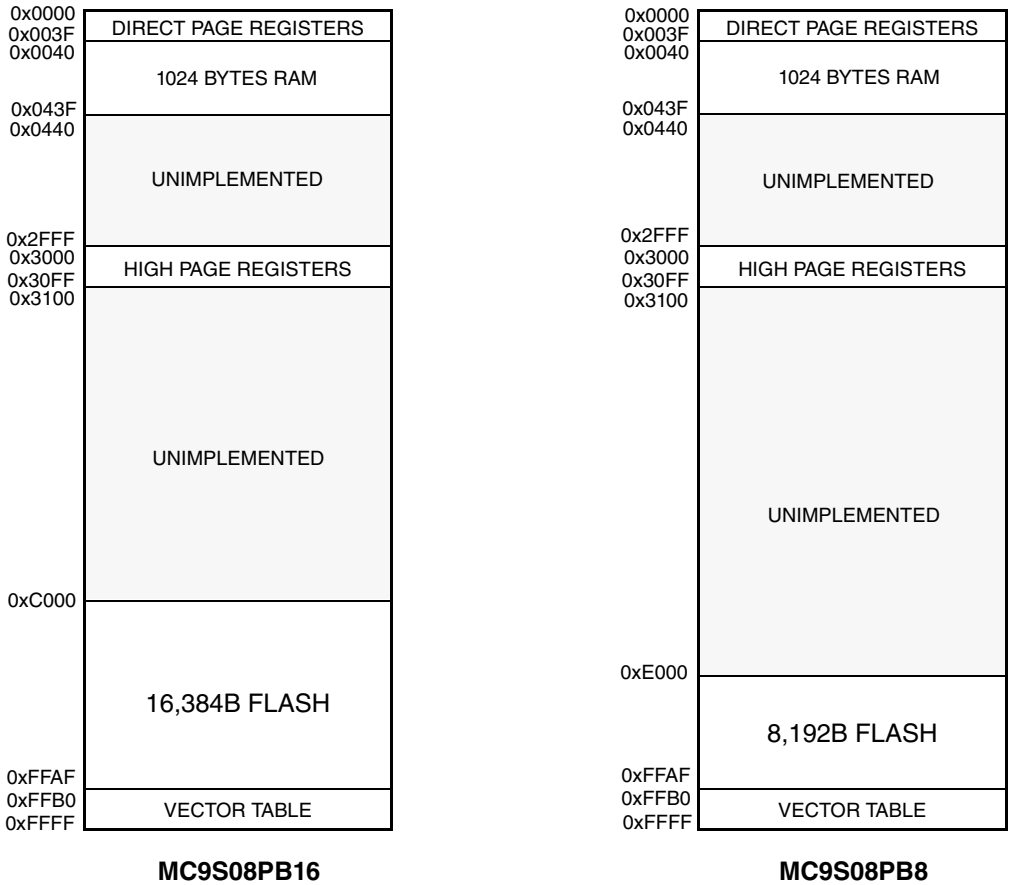


Figure 5-1. Memory map

5.2 Peripheral register addresses

The register definitions vary in different memory sizes. The register addresses of unused peripherals are reserved. The following table shows the register availability of the devices.

Table 5-1. Peripheral register addresses

Address	Size (Byte)	Peripheral
0x0000-0x0002	3	Port data
0x0010-0x0017	8	ADC
0x0018-0x001B	4	MTIM0
0x001C-0x001F	4	MTIM1
0x0020-0x002A	11	FTM0
0x002C-0x002F	4	ACMP0
0x003B-0x003B	1	IRQ
0x003C-0x003C	1	KBI0

Table continues on the next page...

Table 5-1. Peripheral register addresses (continued)

Address	Size (Byte)	Peripheral
0x003E-0x003F	2	IPC
0x3000-0x300B	12	SYS
0x300C-0x300F	4	SCG
0x3010-0x301F	16	DBG
0x3020-0x302C	13	NVM
0x3030-0x3037	8	PWT
0x3038-0x303C	5	ICS
0x303E-0x303E	1	OSC
0x3040-0x3041	2	PMC
0x304A-0x304B	2	SYS (ILLA)
0x3050-0x305A	11	IPC
0x305C-0x305F	4	ACMP1
0x3060-0x3068	9	CRC
0x306A-0x306F	6	RTC
0x3070-0x307B	12	I^2C
0x307C-0x307D	2	KBI0
0x3080-0x3087	8	SCI0
0x30AC-0x30AD	2	ADC
0x30B0-0x30B2	3	Port output enable
0x30B8-0x30BA	3	Port input enable
0x30C0-0x30D6	23	FTM2
0x30DD-0x30E2	6	FDS
0x30EC-0x30EF	4	Port filter
0x30F0-0x30F2	3	Port pullup
0x30F8-0x30FF	8	SYS (UUID)

Several reserved flash memory locations, shown in the following table, are used for storing values used by several registers. These registers include an 8-byte backdoor key, NV_BACKKEY, which can be used to gain access to secure memory resources. During reset events, the contents of NVPROT and NVOPT in the reserved flash memory are transferred into corresponding FPROT and FOPT registers in the high-page registers area to control security and block protection options

Table 5-2. Reserved flash memory addresses

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0xFF6E	NV_FTRIM	—	—	—	—	—	—	—	FTRIM
0xFF6F	NV_ICSTRM	TRIM							
0xFF70	NV_BACKKEY0	BACKKEY0							
0xFF71	NV_BACKKEY1	BACKKEY1							

Table continues on the next page...

Table 5-2. Reserved flash memory addresses (continued)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0xFF72	NV_BACKKEY2	BACKKEY2							
0xFF73	NV_BACKKEY3	BACKKEY3							
0xFF74	NV_BACKKEY4	BACKKEY4							
0xFF75	NV_BACKKEY5	BACKKEY5							
0xFF76	NV_BACKKEY6	BACKKEY6							
0xFF77	NV_BACKKEY7	BACKKEY7							
0xFF78	Reserved	—	—	—	—	—	—	—	—
0xFF79	Reserved	—	—	—	—	—	—	—	—
0xFF7A	Reserved	—	—	—	—	—	—	—	—
0xFF7B	Reserved	—	—	—	—	—	—	—	—
0xFF7C	NV_FPROT	FPOPEN	—	FPHDIS	FPH		—	—	—
0xFF7D	Reserved	—	—	—	—	—	—	—	—
0xFF7E	NV_FOPT	NV							
0xFF7F	NV_FSEC	KEYEN		1	1	1	1	SEC	

The 8-byte comparison key can be used to temporarily disengage memory security provided the key enable field, NV_FSEC[KEYEN], is 10b. This key mechanism can be accessed only through user code running in secure memory. A security key cannot be entered directly through background debug commands. This security key can be disabled completely by programming the NV_FSEC[KEYEN] bit to 0b. If the security key is disabled, the only way to disengage security is by mass erasing the flash if needed, normally through the background debug interface and verifying that flash is blank. To avoid returning to secure mode after the next reset, program the security bits, NV_FSEC[SEC], to the unsecured state (10b).

5.3 Random-access memory (RAM)

This section describes the 1024 bytes of RAM (random-access memory).

These devices include static RAM. The locations in RAM below 0x0100 can be accessed using the more efficient direct addressing mode. Any single bit in this area can be accessed with the bit manipulation instructions (BCLR, BSET, BRCLR, and BRSET).

The RAM retains data when the MCU is in low-power wait, or stop3 mode. At power-on, the contents of RAM are uninitialized. RAM data is unaffected by any reset provided that the supply voltage does not drop below the minimum value for RAM retention.

For compatibility with older M68HC05 MCUs, the HCS08 resets the stack pointer to 0x00FF. In this series, re-initialize the stack pointer to the top of the RAM so that the direct-page RAM can be used for frequently accessed RAM variables and bit-addressable program variables. Include the following 2-instruction sequence in your reset initialization routine (where RamLast is equated to the highest address of the RAM in the equate file).

```
LDHX     #RamLast+1    ;point one past RAM
TXS                    ;SP<-(H:X-1)
```

When security is enabled, the RAM is considered a secure memory resource and is not accessible through BDM or code executing from non-secure memory.

5.4 Flash memory

This device includes flash memory. The flash memory is ideal for single-supply applications that allow for field reprogramming without requiring external high voltage sources for program or erase operations. The flash module includes a memory controller that executes commands to modify flash memory contents. The user interface to the memory controller consists of the indexed flash common command object (FCCOB) register, which is written to with the command, global address, data, and any required command parameters. The memory controller must complete the execution of a command before the FCCOB register is written to with a new command.

CAUTION

A flash byte or longword must be in the erased state before being programmed. Cumulative programming of bits within a flash byte or longword is not allowed.

The flash memory is read as two bytes per read. Read access time is one bus cycle for two bytes. For flash memory, an erased bit reads 1 and a programmed bit reads 0.

Chapter 6
Interrupt

6.1 Interrupts

Interrupts save the current CPU status and registers, execute an interrupt service routine (ISR), and then restore the CPU status so that processing resumes where it left off before the interrupt. Other than the software interrupt (SWI), which is a program instruction, interrupts are caused by hardware events such as an edge on the IRQ pin or a timer-overflow event. The debug module can also generate an SWI under certain circumstances.

If an event occurs in an enabled interrupt source, an associated read-only status flag will be set. The CPU will not respond unless only the local interrupt enable is a logic 1. The I bit in the CCR is 0 to allow interrupts. The global interrupt mask (I bit) in the CCR is initially set after reset that masks (prevents) all maskable interrupt sources. The user program initializes the stack pointer and performs other system setups before clearing the I bit to allow the CPU to respond to interrupts.

When the CPU receives a qualified interrupt request, it completes the current instruction before responding to the interrupt. The interrupt sequence obeys the same cycle-by-cycle sequence as the SWI instruction and consists of:

- Saving the CPU registers on the stack.
- Setting the I bit in the CCR to mask further interrupts.
- Fetching the interrupt vector for the highest-priority interrupt that is currently pending.
- Filling the instruction queue with the first three bytes of program information starting from the address fetched from the interrupt vector locations.

While the CPU is responding to the interrupt, the I bit is automatically set to prevent another interrupt from interrupting the ISR itself, which is called nesting of interrupts. Normally, the I bit is restored to 0 when the CCR is restored from the value stacked on

entry to the ISR. In rare cases, the I bit may be cleared inside an ISR, after clearing the status flag that generated the interrupt, so that other interrupts can be serviced without waiting for the first service routine to finish. This practice is recommended only for the most experienced programmers because it can lead to subtle program errors that are difficult to debug.

The interrupt service routine ends with a return-from-interrupt (RTI) instruction that restores the CCR, A, X, and PC registers to their pre-interrupt values by reading the previously saved information off the stack.

Note

For compatibility with the M68HC08, the H register is not automatically saved and restored. Push H onto the stack at the start of the interrupt service routine (ISR) and restore it immediately before the RTI that is used to return from the ISR.

When two or more interrupts are pending when the I bit is cleared, the highest priority source is serviced first.

6.1.1 Interrupt stack frame

The following figure shows the contents and organization of a stack frame. Before the interrupt, the stack pointer (SP) points at the next available byte location on the stack. The current values of CPU registers are stored on the stack, starting with the low-order byte of the program counter (PC) and ending with the CCR. After stacking, the SP points at the next available location on the stack, which is the address that is one less than the address where the CCR was saved. The PC value that is stacked is the address of the instruction in the main program that would have executed next if the interrupt had not occurred.

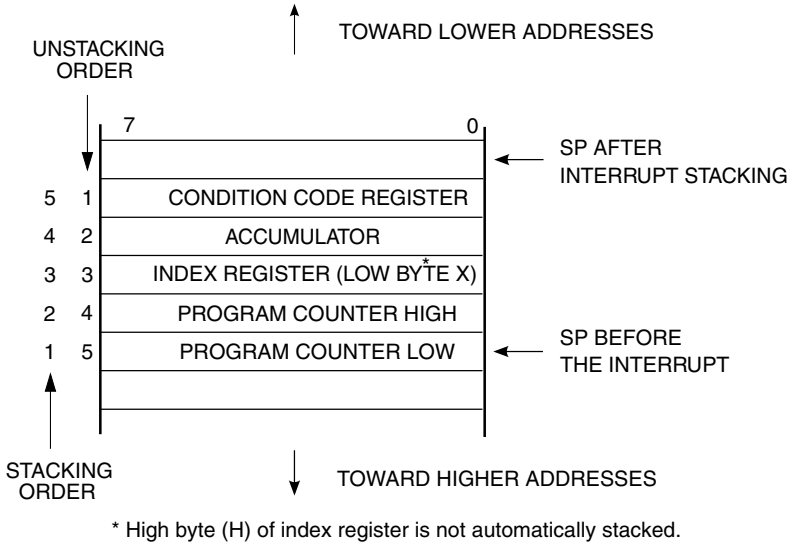


Figure 6-1. Interrupt stack frame

When an RTI instruction executes, these values are recovered from the stack in reverse order. As part of the RTI sequence, the CPU fills the instruction pipeline by reading three bytes of program information, starting from the PC address recovered from the stack.

The status flag causing the interrupt must be acknowledged (cleared) before returning from the ISR. Typically, the flag must be cleared at the beginning of the ISR because if another interrupt is generated by this source it will be registered so that it can be serviced after completion of the current ISR.

6.1.2 Interrupt vectors, sources, and local masks

The following table provides a summary of all interrupt sources. High-priority sources are located toward the bottom of the table. The high-order byte of the address for the interrupt service routine is located at the first address in the vector address column, and the low-order byte of the address for the interrupt service routine is located at the next higher address.

When an interrupt condition occurs, an associated flag bit is set. If the associated local interrupt enable is 1, an interrupt request is sent to the CPU. If the global interrupt mask (I bit in the CCR) is 0, the CPU finishes the current instruction, stacks the PCL, PCH, X, A, and CCR CPU registers, sets the I bit, and then fetches the interrupt vector for the highest priority pending interrupt. Processing then continues in the interrupt service routine.

Table 6-1. Reset and interrupt vectors

Vector number	Address (High/ Low)	Vector	Vector Name	Source	Local Enable
39	0xFFB0:FFB1	NVM	Vnvm	CCIF	CCIE
38	0xFFB2:FFB3	—	—	—	—
37	0xFFB4:FFB5	KBI0	Vkbi0	KBF	KBIE
36	0xFFB6:FFB7	—	—	—	—
35	0xFFB8:FFB9	RTC	Vrtc	RTIF	RTIE
34	0xFFBA:FFBB	IIC	Viic	IICIF	IICIE
33	0xFFBC:FFBD	—	—	—	—
32	0xFEFE:FFBF	—	—	—	—
31	0xFFC0:FFC1	—	—	—	—
30	0xFFC2:FFC3	—	—	—	—
29	0xFFC4:FFC5	—	—	—	—
28	0xFFC4:FFC7	—	—	—	—
27	0xFFC4:FFC9	—	—	—	—
26	0xFFCA:FFCB	—	—	—	—
25	0xFFCC:FFCD	SCI0 transmit	Vsci0txd	TRDE	TIE
				TC	TCIE
24	0xFFCE:FFCF	SCI0 receive	Vsci0rxd	IDLE	ILIE
				RDRF	RIE
				LBKDIF	LBKDIE
				RXEDGIF	RXEDGIE
23	0xFFD0:FFD1	SCI0 error	Vsci0err	OR	ORIE
				NF	NEIE
				FE	FEIE
				PF	PEIE
22	0xFFD2:FFD3	ADC	Vadc	COCO	AIEN
21	0xFFD4:FFD5	ACMP0	Vacmp0	ACF	ACIE
20	0xFFD6:FFD7	MTIM1	Vmtim1	TOF	TOIE
19	0xFFD8:FFD9	MTIM0	Vmtim0	TOF	TOIE
18	0xFFDA:FFDB	FTM0 Overflow	Vftm0ovf	TOF	TOIE
17	0xFFDC:FFDD	FTM0 Channel 1	Vftm0ch1	CH1F	CH1IE
16	0xFFDE:FFDF	FTM0 Channel 0	Vftm0ch0	CH0F	CH0IE
15	0xFFE0:FFE1	ACMP1	Vacmp1	ACF	ACIE
14	0xFFE2:FFE3	PWT overflow	Vpwtovf	PWTOV	POVIE
13	0xFFE4:FFE5	PWT data ready	Vpwtrdy	PWTRDY	PRDYIE
12	0xFFE6:FFE7	FTM2 Overflow	Vftm2ovf	TOF	TOIE
11	0xFFE8:FFE9	FTM2 Channel 5	Vftm2ch5	CH5F	CH5IE
10	0xFFEA:FFEB	FTM2 Channel 4	Vftm2ch4	CH4F	CH4IE
9	0xFFEC:FFED	FTM2 Channel 3	Vftm2ch3	CH3F	CH3IE
8	0xFFEE:FFEF	FTM2 Channel 2	Vftm2ch2	CH2F	CH2IE

Table continues on the next page...

Table 6-1. Reset and interrupt vectors (continued)

Vector number	Address (High/ Low)	Vector	Vector Name	Source	Local Enable
7	0xFFF0:FFF1	FTM2 Channel 1	Vftm2ch1	CH1F	CH1IE
6	0xFFF2:FFF3	FTM2 Channel 0	Vftm2ch0	CH0F	CH0IE
5	0xFFF4:FFF5	FDS	Vfds	FDF	FDIE
4	0xFFF6:FFF7	Clock Lost	Vclk	LOLS	LOLIE
3	0xFFF8:FFF9	Low Voltage Warning	Vlvw	LVWF	LVWIE
2	0xFFFA:FFFB	IRQ	Virq	IRQF	IRQIE
1	0xFFFC:FFFD	SWI	Vswi	SWI Instruction	—
0	0xFFFE:FFFF	Reset	Vreset	WCOP	COPT
				LVD	LVDRE
				RESET pin	RSTPE
				Illegal opcode	—
				Illegal address	—
				POR	—
				ICS	CME
				BDFR	—
				FILA	—

6.1.3 Hardware nested interrupt

This device has interrupt priority controller (IPC) module to provide up to four-level nested interrupt capability. IPC includes the following features:

- Four-level programmable interrupt priority for each interrupt source.
- Support for prioritized preemptive interrupt service routines
  - Low-priority interrupt requests are blocked when high-priority interrupt service routines are being serviced.
  - Higher or equal priority level interrupt requests can preempt lower priority interrupts being serviced.
- Automatic update of interrupt priority mask with being serviced interrupt source priority level when the interrupt vector is being fetched.

- Interrupt priority mask can be modified during main flow or interrupt service execution.
- Previous interrupt mask level is automatically stored when interrupt vector is fetched (four levels of previous values accommodated)

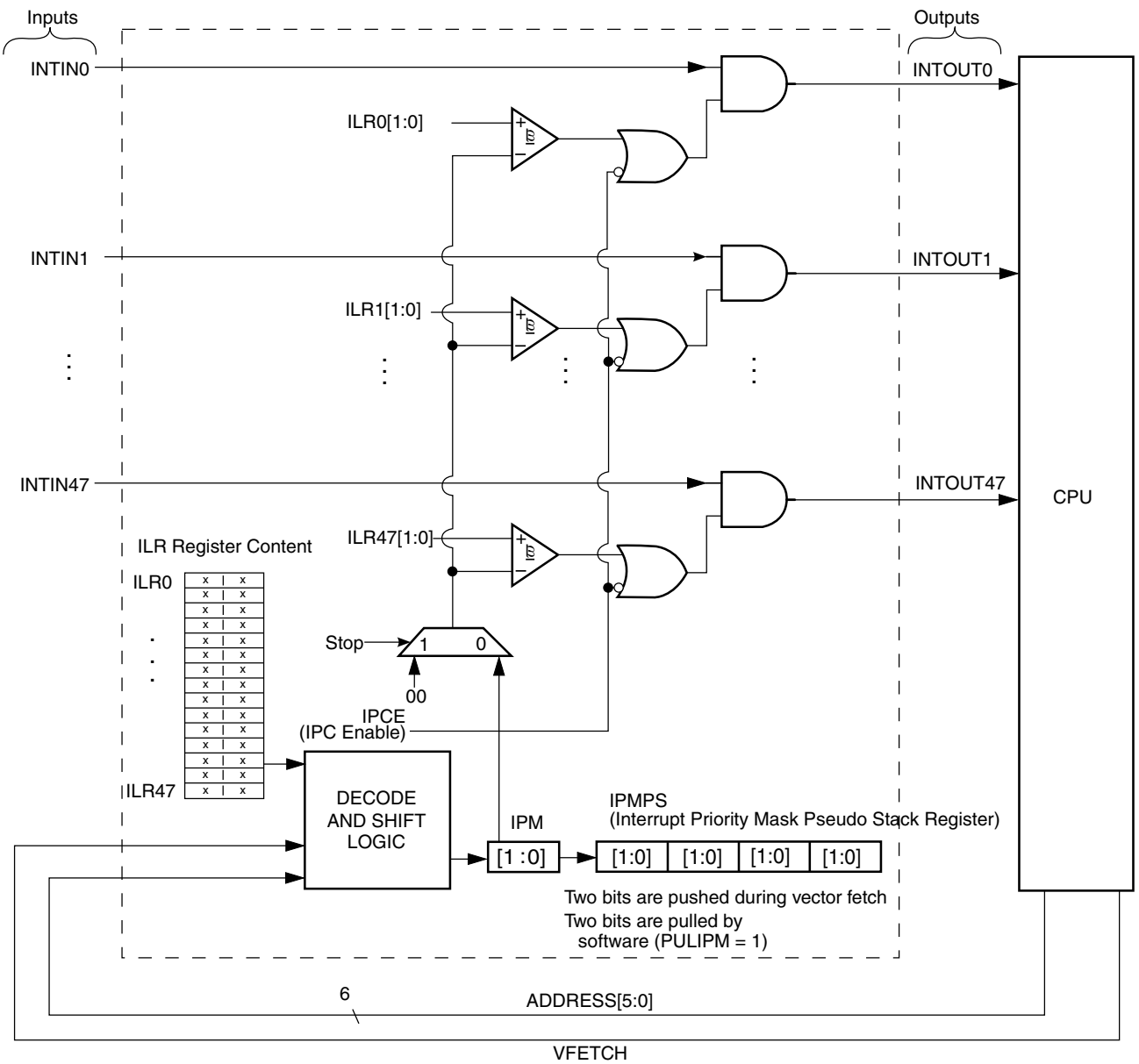


Figure 6-2. Interrupt priority controller block diagram

The IPC works with the existing HCS08 interrupt mechanism to allow nested interrupts with programmable priority levels. This module also allows implementation of preemptive interrupt according to the programmed interrupt priority with minimal software overhead. The IPC consists of three major functional blocks:

- The interrupt priority level registers
- The interrupt priority level comparator set
- The interrupt mask register update and restore mechanism

6.1.3.1 Interrupt priority level register

This set of registers is associated with the interrupt sources to the HCS08 CPU. Each interrupt priority level is a 2-bit value such that a user can program the interrupt priority level of each source to priority 0, 1, 2, or 3. Level 3 has the highest priority while level 0 has the lowest. Software can read or write to these registers at any time. The interrupt priority level comparator set, interrupt mask register update, and restore mechanism use this information.

6.1.3.2 Interrupt priority level comparator set

When the module is enabled, an active interrupt request forces a comparison between the corresponding ILR and the 2-bit interrupt mask IPM[1:0]. In stop3 mode, the IPM[1:0] is substituted by value 00b. If the ILR value is greater than or equal to the value of the interrupt priority mask (IPM bits in IPCSC), the corresponding interrupt out (INTOUT) signal will be asserted and signals an interrupt request to the HCS08 CPU.

When the module is disabled, the interrupt request signal from the source is directly passed to the CPU.

The interrupt priority level programmed in the interrupt priority register will not affect the inherent interrupt priority arbitration as defined by the HCS08 CPU because the IPC is an external module. Therefore, if two (or more) interrupts are present in the HCS08 CPU at the same time, the inherent priority in HCS08 CPU will perform arbitration by the inherent interrupt priority.

6.1.3.3 Interrupt priority mask update and restore mechanism

The interrupt priority mask (IPM) is two bits located in the least significant end of IPCSC register. These two bits control which interrupt is allowed to be presented to the HCS08 CPU. During vector fetch, the interrupt priority mask is updated automatically with the value of the ILR corresponding to that interrupt source. The original value of the IPM will be saved onto IPMPS for restoration after the interrupt service routine completes execution. When the interrupt service routine completes execution, the user restore the

original value of IPM by writing 1 to the IPCSC[PULIPM] bit. In both cases, the IPMPS is a shift register functioning as a pseudo stack register for storing the IPM. When the IPM is updated, the original value is shifted into IPMPS. The IPMPS can store four levels of IPM. If the last position of IPMPS is written, the PSF flag indicates that the IPMPS is full. If all the values in the IPMPS were read, the PSE flag indicates that the IPMPS is empty.

6.1.3.4 Integration and application of the IPC

All interrupt inputs that comes from peripheral modules are synchronous signals. None of the asynchronous signals of the interrupts are routed to IPC. The asynchronous signals of the interrupts are routed directly to SIM module to wake system clocks in stop3 mode.

Additional care must be exercised when IRQ is reprioritized by IPC. CPU instructions BIL and BIH need input from IRQ pin. If IRQ interrupt is masked, BIL and BIH still work but the IRQ interrupt will not occur.

- The interrupt priority controller must be enabled to function. While inside an interrupt service routine, some work has to be done to enable other higher priority interrupts. The following is a pseudo code example written in assembly language:

```
INT_SER :
        BCLR        INTFLAG,INTFLAG_R ; clear flag that generate interrupt
        .                             ; do the most critical part
        .                             ; which it cannot be interrupted
        .
        .
        .
        CLI                           ; global interrupt enable and nested interrupt
enabled
        .                             ; continue the less critical
        .
        .
        .
        BSET        PULIPM, PULIPM_R  ; restore the old IPM value before leaving
        RTI                           ; then you can return
```

- A minimum overhead of six bus clock cycles is added inside an interrupt services routine to enable preemptive interrupts.
- As an interrupt of the same priority level is allowed to pass through IPC to HCS08 CPU, the flag generating the interrupt must be cleared before doing CLI to enable preemptive interrupts.

- The IPM is automatically updated to the level the interrupt is servicing and the original level is kept in IPMPS. Watch out for the full (PSF) bit if nesting for more than four levels is expected.
- Before leaving the interrupt service routine, the previous levels must be restored manually by setting PULIPM bit. Watch out for the full (PSF) bit and empty (PSE) bit.

6.2 IRQ

The IRQ (external interrupt) module provides a maskable interrupt input.

6.2.1 Features

Features of the IRQ module include:

- A Dedicated External Interrupt Pin IRQ
- IRQ Interrupt Control Bits
- Programmable Edge-only or Edge and Level Interrupt Sensitivity
- Automatic Interrupt Acknowledge
- Internal pullup device

A low level applied to the external interrupt request (IRQ) pin can latch a CPU interrupt request. The following figure shows the structure of the IRQ module:

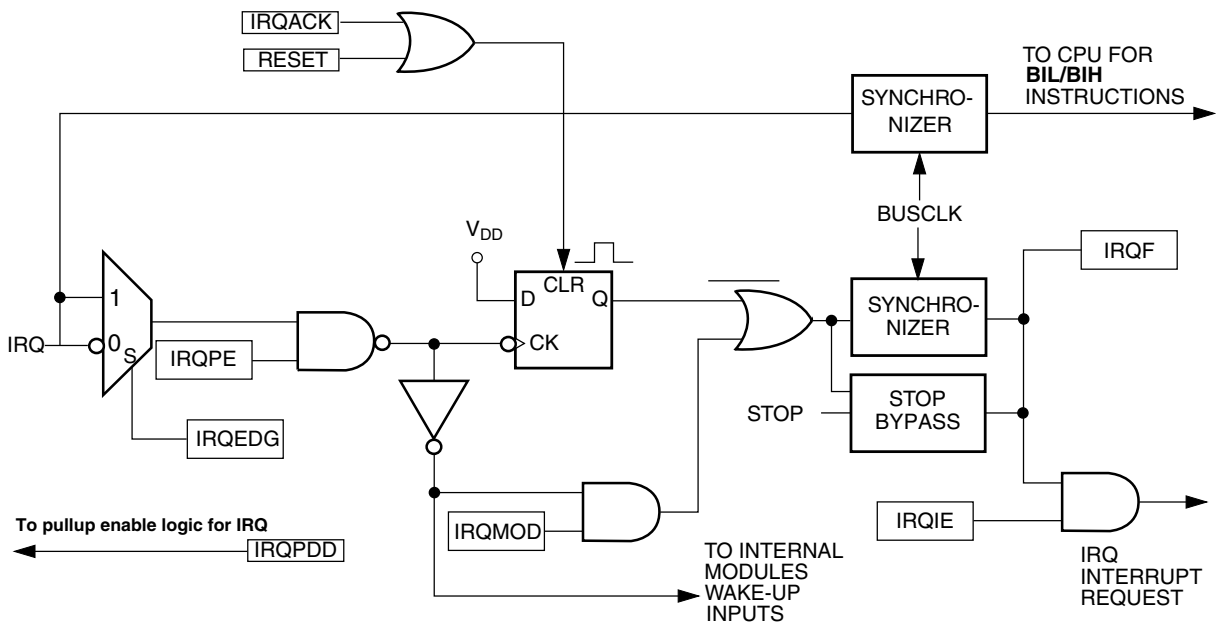


Figure 6-3. IRQ module block diagram

External interrupts are managed by the IRQSC status and control register. When the IRQ function is enabled, synchronous logic monitors the pin for edge-only or edge-and-level events. When the MCU is in stop mode and system clocks are shut down, a separate asynchronous path is used so that the IRQ, if enabled, can wake the MCU.

6.2.1.1 Pin configuration options

The IRQ pin enable control bit (IRQSC[IRQPE]) must be 1 for the IRQ pin to act as the IRQ input. The user can choose the polarity of edges or levels detected (IRQEDG), whether the pin detects edges-only or edges and levels (IRQMOD), or whether an event causes an interrupt or only sets the IRQF flag, which can be polled by software.

When enabled, the IRQ pin defaults to use an internal pullup device (IRQSC[IRQPDD] = 0). If the user uses an external pullup or pulldown, the IRQSC[IRQPDD] can be written to a 1 to turn off the internal device.

BIH and BIL instructions may be used to detect the level on the IRQ pin when it is configured to act as the IRQ input.

Note

This pin does not contain a clamp diode to V_{DD} and must not be driven above V_{DD}. The voltage measured on the internally pullup IRQ pin may be as low as V_{DD} – 0.7 V. The internal gates connected to this pin are pulled all the way to V_{DD}.

When enabling the IRQ pin for use, the IRQF will be set, and must be cleared prior to enabling the interrupt. When configuring the pin for falling edge and level sensitivity in a 3 V system, it is necessary to wait at least cycles between clearing the flag and enabling the interrupt.

6.2.1.2 Edge and level sensitivity

The IRQSC[IRQMOD] control bit reconfigures the detection logic so that it can detect edge events and pin levels. In this detection mode, the IRQF status flag is set when an edge is detected, if the IRQ pin changes from the de-asserted to the asserted level, but the flag is continuously set and cannot be cleared as long as the IRQ pin remains at the asserted level.

6.3 Interrupt pin request register

IRQ memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3B	Interrupt Pin Request Status and Control Register (IRQ_SC)	8	R/W	00h	6.3.1/71

6.3.1 Interrupt Pin Request Status and Control Register (IRQ_SC)

This direct page register includes status and control bits, which are used to configure the IRQ function, report status, and acknowledge IRQ events.

Address: 3Bh base + 0h offset = 3Bh

Bit	7	6	5	4	3	2	1	0
Read	0	IRQPDD	IRQEDG	IRQPE	IRQF	0	IRQIE	IRQMOD
Write						IRQACK		
Reset	0	0	0	0	0	0	0	0

IRQ_SC field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 IRQPDD	Interrupt Request (IRQ) Pull Device Disable

Table continues on the next page...

IRQ_SC field descriptions (continued)

Field	Description
	This read/write control bit is used to disable the internal pullup device when the IRQ pin is enabled (IRQPE = 1) allowing for an external device to be used. 0 IRQ pull device enabled if IRQPE = 1. 1 IRQ pull device disabled if IRQPE = 1.
5 IRQEDG	Interrupt Request (IRQ) Edge Select This read/write control bit is used to select the polarity of edges or levels on the IRQ pin that cause IRQF to be set. The IRQMOD control bit determines whether the IRQ pin is sensitive to both edges and levels or only edges. When the IRQ pin is enabled as the IRQ input and is configured to detect rising edges, the optional pullup resistor is disabled. 0 IRQ is falling edge or falling edge/low-level sensitive. 1 IRQ is rising edge or rising edge/high-level sensitive.
4 IRQPE	IRQ Pin Enable This read/write control bit enables the IRQ pin function. When this bit is set the IRQ pin can be used as an interrupt request. 0 IRQ pin function is disabled. 1 IRQ pin function is enabled.
3 IRQF	IRQ Flag This read-only status bit indicates when an interrupt request event has occurred. 0 No IRQ request. 1 IRQ event detected.
2 IRQACK	IRQ Acknowledge This write-only bit is used to acknowledge interrupt request events (write 1 to clear IRQF). Writing 0 has no meaning or effect. Reads always return 0. If edge-and-level detection is selected (IRQMOD = 1), IRQF cannot be cleared while the IRQ pin remains at its asserted level.
1 IRQIE	IRQ Interrupt Enable This read/write control bit determines whether IRQ events generate an interrupt request. 0 Interrupt request when IRQF set is disabled (use polling). 1 Interrupt requested whenever IRQF = 1.
0 IRQMOD	IRQ Detection Mode This read/write control bit selects either edge-only detection or edge-and-level detection. 0 IRQ event on falling/rising edges only. 1 IRQ event on falling/rising edges and low/high levels.

6.4 Interrupt priority control register

IPC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3E	IPC Status and Control Register (IPC_SC)	8	R/W	20h	6.4.1/73
3F	Interrupt Priority Mask Pseudo Stack Register (IPC_IPMPS)	8	R	00h	6.4.2/74
3050	Interrupt Level Setting Registers n (IPC_ILRS0)	8	R/W	00h	6.4.3/75
3051	Interrupt Level Setting Registers n (IPC_ILRS1)	8	R/W	00h	6.4.3/75
3052	Interrupt Level Setting Registers n (IPC_ILRS2)	8	R/W	00h	6.4.3/75
3053	Interrupt Level Setting Registers n (IPC_ILRS3)	8	R/W	00h	6.4.3/75
3054	Interrupt Level Setting Registers n (IPC_ILRS4)	8	R/W	00h	6.4.3/75
3055	Interrupt Level Setting Registers n (IPC_ILRS5)	8	R/W	00h	6.4.3/75
3056	Interrupt Level Setting Registers n (IPC_ILRS6)	8	R/W	00h	6.4.3/75
3057	Interrupt Level Setting Registers n (IPC_ILRS7)	8	R/W	00h	6.4.3/75
3058	Interrupt Level Setting Registers n (IPC_ILRS8)	8	R/W	00h	6.4.3/75
3059	Interrupt Level Setting Registers n (IPC_ILRS9)	8	R/W	00h	6.4.3/75

6.4.1 IPC Status and Control Register (IPC_SC)

This register contains status and control bits for the IPC.

Address: 3Eh base + 0h offset = 3Eh

Bit	7	6	5	4	3	2	1	0
Read	IPCE	0	PSE	PSF	0	0	IPM	
Write					PULIPM			
Reset	0	0	1	0	0	0	0	0

IPC_SC field descriptions

Field	Description
7 IPCE	Interrupt Priority Controller Enable This bit enables/disables the interrupt priority controller module. 0 Disables IPCE. Interrupt generated from the interrupt source is passed directly to CPU without processing (bypass mode). The IPMPS register is not updated when the module is disabled. 1 Enables IPCE and interrupt generated from the interrupt source is processed by IPC before passing to CPU.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

IPC_SC field descriptions (continued)

Field	Description
5 PSE	Pseudo Stack Empty This bit indicates that the pseudo stack has no valid information. This bit is automatically updated after each IPMPS register push or pull operation.
4 PSF	Pseudo Stack Full This bit indicates that the pseudo stack register IPMPS register is full. It is automatically updated after each IPMPS register push or pull operation. If additional interrupt is nested after this bit is set, the earliest interrupt mask value(IPM0[1:0]) stacked in IPMPS will be lost. 0 IPMPS register is not full. 1 IPMPS register is full.
3 PULIPM	Pull IPM from IPMPS This bit pulls stacked IPM value from IPMPS register to IPM bits of IPCSC. Zeros are shifted into bit positions 1 and 0 of IPMPS. 0 No operation. 1 Writing 1 to this bit causes a 2-bit value from the interrupt priority mask pseudo stack register to be pulled to the IPM bits of IPCSC to restore the previous IPM value.
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
IPM	Interrupt Priority Mask This field sets the mask for the interrupt priority control. If the interrupt priority controller is enabled, the interrupt source with an interrupt level (ILRxx) value that is greater than or equal to the value of IPM will be presented to the CPU. Writes to this field are allowed, but doing this will not push information to the IPMPS register. Writing IPM with PULIPM setting when IPCE is already set, the IPM will restore the value pulled from the IPMPS register, not the value written to the IPM register.

6.4.2 Interrupt Priority Mask Pseudo Stack Register (IPC_IPMPS)

This register is used to store the previous interrupt priority mask level temporarily when the currently active interrupt is executed.

Address: 3Eh base + 1h offset = 3Fh

Bit	7	6	5	4	3	2	1	0
Read	IPM3		IPM2		IPM1		IPM0	
Write								
Reset	0	0	0	0	0	0	0	0

IPC_IPMPS field descriptions

Field	Description
7–6 IPM3	Interrupt Priority Mask pseudo stack position 3 This field is the pseudo stack register for IPM3. The most recent information is stored in IPM3.

Table continues on the next page...

IPC_IPMPS field descriptions (continued)

Field	Description
5–4 IPM2	Interrupt Priority Mask pseudo stack position 2 This field is the pseudo stack register for IPM2. The most recent information is stored in IPM2.
3–2 IPM1	Interrupt Priority Mask pseudo stack position 1 This field is the pseudo stack register for IPM1. The most recent information is stored in IPM1.
IPM0	Interrupt Priority Mask pseudo stack position 0 This field is the pseudo stack register for IPM0. The most recent information is stored in IPM0.

6.4.3 Interrupt Level Setting Registers n (IPC_ILRS*n*)

This set of registers (ILRS0-ILRS9) contains the user specified interrupt level for each interrupt source, and indicates the number of the register (ILRSn is ILRS0 through ILRS9).

Address: 3Eh base + 3012h offset + (1d × i), where i=0d to 9d

Bit	7	6	5	4	3	2	1	0
Read Write	ILRn3		ILRn2		ILRn1		ILRn0	
Reset	0	0	0	0	0	0	0	0

IPC_ILRS*n* field descriptions

Field	Description
7–6 ILRn3	Interrupt Level Register for Source n*4+3 This field sets the interrupt level for interrupt source n*4+3.
5–4 ILRn2	Interrupt Level Register for Source n*4+2 This field sets the interrupt level for interrupt source n*4+2.
3–2 ILRn1	Interrupt Level Register for Source n*4+1 This field sets the interrupt level for interrupt source n*4+1.
ILRn0	Interrupt Level Register for Source n*4+0 This field sets the interrupt level for interrupt source n*4+0.

Chapter 7
System control

7.1 System device identification (SDID)

This device is hard coded to the value 0x0046 in SDID registers.

7.2 Universally unique identification (UUID)

This device contains up to 64-bit UUID to identify each device in this family. The intent of UUID is to enable distributed systems to uniquely identify information without significant central coordination.

7.3 Reset and system initialization

Resetting the MCU provides a way to start processing from a set of known initial conditions. During reset, most control and status registers are forced to initial values and the program counter is loaded from the reset vector (0xFFFE:0xFFFF). On-chip peripheral modules are disabled and I/O pins are initially configured as general-purpose high-impedance inputs with disabled pullup devices. The CCR[I] bit is set to block maskable interrupts so that the user program has a chance to initialize the stack pointer (SP) and system control settings. SP is forced to 0x00FF at reset.

This device has the following sources for reset:

- Power-on reset (POR)
- Low-voltage detect (LVD)
- Watchdog (WDOG) timer
- Illegal opcode detect (ILOP)

- Background debug forced reset
- External reset pin (RESET)
- Internal clock source module reset (CLK)
- Flash Illegal Access (FILA)

Each of these sources, with the exception of the background debug forced reset, has an associated bit in the system reset status (SRS) register.

7.4 System options

7.4.1 BKGD pin enable

After POR, PTA4/FTM0CH1/ACMP0O/BKGD/MS/ pin functions as BKGD output. The SYS_SOPT1[BKGDPE] bit must be set to enable the background debug mode pin enable function. When this bit is clear, this pin can function as PTA4, FTM0CH1 or ACMP0 output.

7.4.2 $\overline{\text{RESET}}$ pin enable

After POR reset, PTA5/IRQ/FTM0CH0/TCLK0/RESET_b functions as RESET_b. The SYS_SOPT1[RSTPE] bit must be set to enable the reset functions. When this bit is clear, this pin can function as PTA5, IRQ, FTM0CH0, or TCLK0.

7.4.3 SCI0 pin reassignment

After reset, SCI0 module pinouts of RxD and TxD are mapped on PTB0 and PTB1, respectively. SYS_SOPT1[SCI0PS] bit enables to reassign SCI0 pinouts on PTA2 and PTA3.

7.4.4 I2C pins reassignments

After POR reset, I2C module pinouts of SDA and SCL are mapped on PTA2 and PTA3. SYS_SOPT1[IICPS] bit enables to reassign the I2C pinout pair on PTB6 and PTB7, or PTB2 and PTB3 respectively. All the I2C pins support pseudo open drain. When they act as IIC pins, the remote I2C level is limited to no more than MCU V_{DD}.

7.4.5 FTM0 channels pin reassignment

After reset, FTM0 channels pinouts of FTM0CH0 and FTM0CH1 are mapped on PTA0 and PTA1, respectively. SOPT3[FTM0PS] bit enables to reassign FTM0 channels pinouts on PTA5 and PTA4 (output only).

7.5 System interconnection

This device contains a set of system-level logics for module-to-module interconnection for flexible configuration. These interconnections provide the hardware trigger function between modules with least software configuration, which is ideal for infrared communication, serial communication baudrate detection, low-end motor control, metering clock calibration, and other general-purpose applications.

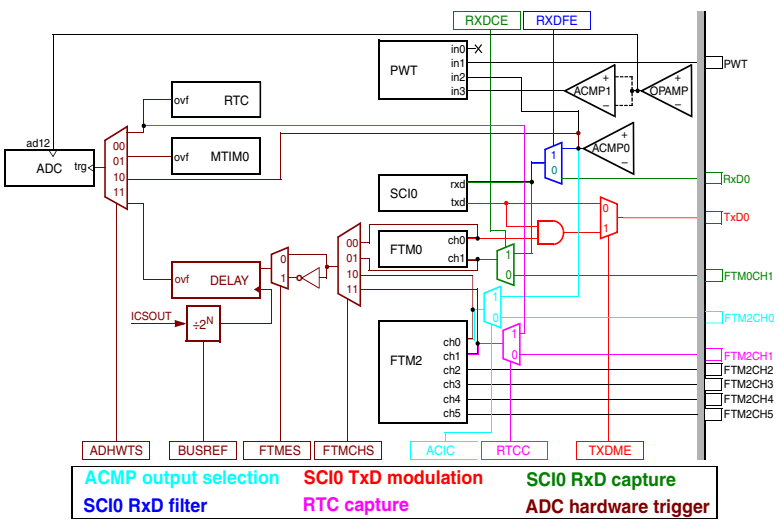


Figure 7-1. System interconnection diagram

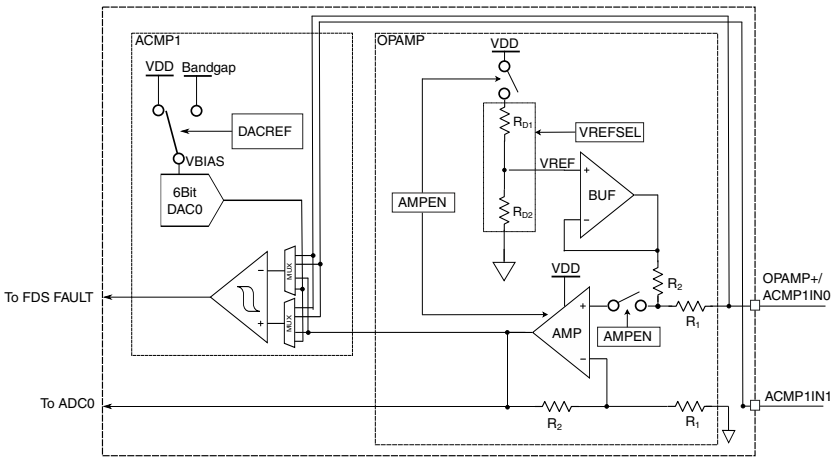


Figure 7-2. OPAMP and ACMP1 interconnection

7.5.1 ACMP output selection

When set, the SYS_SOPT2[ACIC] bit enables the output of ACMP0 to connect to the FTM2CH0, the FTM2CH0 pin is released to other shared functions regardless of the configuration of FTM2 pin reassignment.

7.5.2 SCI0 TxD modulation

SCI0 TXD can be modulated by FTM0 channel 0 output. When SYS_SOPT2[TXDME] bit is set, the TXD output is passed to an AND gate with FTM0 channel 0 output before mapping on TXD0 pinout. When this bit is clear, the TXD is directly mapped on the pinout. To enable IR modulation function, both FTM0CH0 and SCI must be active. The FTM0 counter modulo register specifies the period of the PWM, and the FTM0 channel 0 value register specifies the duty cycle of the PWM. Then, when TXDME bit is enabled, each data transmitted via TXD0 from SCI0 is modulated by the FTM0 channel 0 output, and the FTM0CH0 pin is released to other shared functions regardless of the configuration of FTM0 pin reassignment.

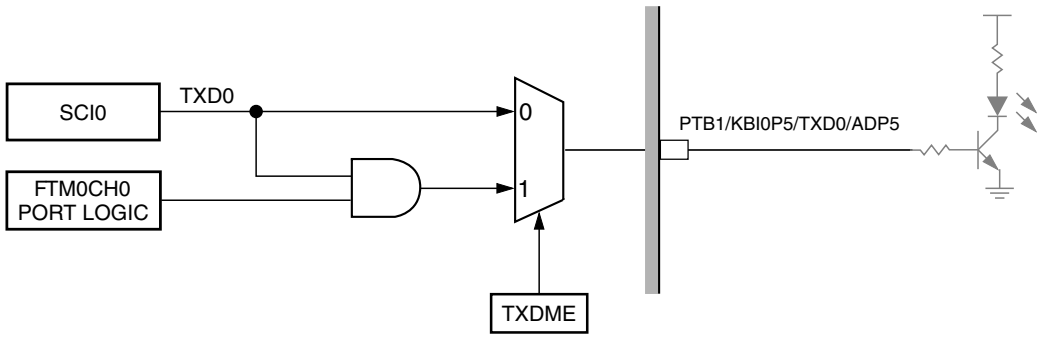


Figure 7-3. IR modulation diagram

7.5.3 SCI0 RxD capture

RxD0 pin is selectable connected to SCI0 module directly or tagged to FTM0 channel 1. When SYS_SOPT2[RXDCE] bit is set, the RxD0 pin is connected to both SCI0 and FTM0 channel 1, and the FTM0CH1 pin is released to other shared functions regardless of the configuration of FTM0 pin reassignment. When this bit is clear, the RxD0 pin is connected to SCI0 only.

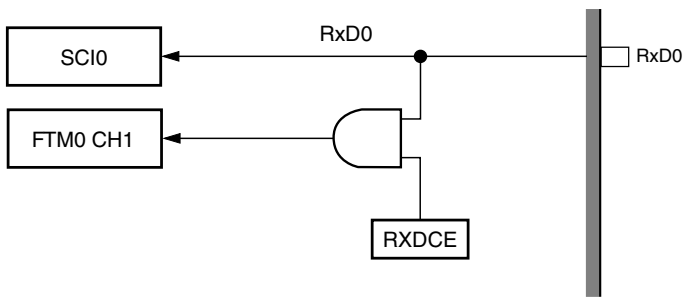


Figure 7-4. RxD0 capture function diagram

7.5.4 SCI0 RxD filter

When SYS_SOPT2[RXDFE] bit is clear, the RxD0 pin is connected to SCI0 module directly. When this bit is set, the ACMP0 output is connected to the receive channel of SCI0. To enable RxD filter function, both SCI0 and ACMP0 must be active. If this function is active, the SCI0 external RxD0 pin is released to other shared functions regardless of the configuration of SCI0 pin reassignment. When SCI0 RxD capture function is active, the ACMP0 output is injected to FTM0CH1 as well.

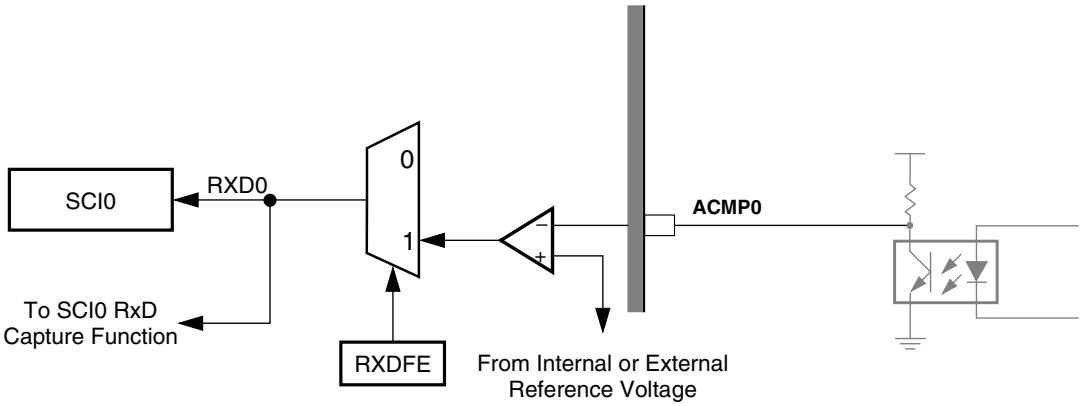


Figure 7-5. IR demodulation diagram

7.5.5 RTC capture

RTC overflow may be captured by FTM2 channel 1 by setting SYS_SOPT2[RTCC] bit. When this bit is set, the RTC overflow is connected to FTM2 channel 1 for capture, the FTM2CH1 pin is released to other shared functions.

7.5.6 ADC hardware trigger

ADC module may initiate a conversion via a hardware trigger. RTC, MTIM0 overflow, ACMP0 output, FTM output with 8-bit programmable delay can be enabled as the hardware trigger for the ADC module by setting the SYS_SOPT2[ADHWTS] bits. The following table shows the ADC hardware trigger setting.

Table 7-1. ADC hardware trigger setting

ADHWT	ADC hardware trigger
0:0	RTC overflow
0:1	MTIM0 overflow
1:0	ACMP0 output
1:1	FTM0 channel 0/1 or FTM2 channel 0/1 output with 8-bit programmable delay and selectable edge

When ADC hardware trigger selects the output of FTM output, an 8-bit delay block will be enabled. This logic delays any trigger from FTM output with an 8-bit counter whose value is specified by SYS_SOPT4[DELAY] bit. The reference clock to this module is the output of ICSOUT with selectable pre-divider specified by SYS_SOPT3[BUSREF]. The FTM output trigger's effective edge (rising edge or falling edge) can be selected by SYS_SOPT2[FTMES] bit.

When FTM runs in output compare mode or PWM mode, the channels output can be selected as ADC hardware trigger, and the selected channel pin is released to other shared functions. When FTM runs in input capture mode, no trigger is generated from FTM channels.

NOTE

Do not set the FTM channel in input capture mode when this channel is selected as the ADC hardware trigger source, because of the input pin is not controlled by FTM modules.

7.5.7 OPAMP and ACMP1 interconnection

The output of single end input OPAMP is connected to ACMP1 or ADC0 input. The output of ACMP1 is connected to Fault Detection and Shutdown (FDS) module.

7.6 FTM software controlled output

The FTM software controlled output feature is added to control the FTM0 and FTM2 channel output value by software. The SYS_SOPT7[FTMxCHyOC] field enables or disables FTMx channel y software output function, and SYS_SOPT8[FTMxCHyOCV] register controls the desired output value.

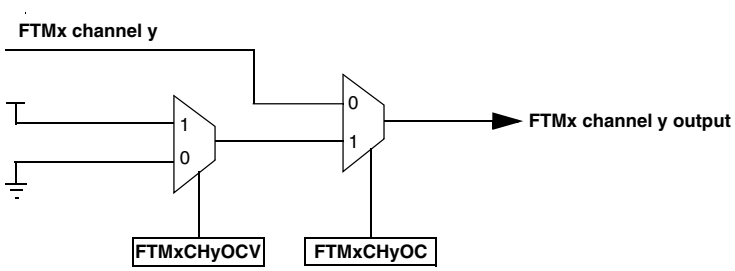


Figure 7-6. FTM software controlled output

7.7 System Control Registers

SYS memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3000	System Reset Status Register (SYS_SRS)	8	R	82h	7.7.1/84

Table continues on the next page...

SYS memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3001	System Background Debug Force Reset Register (SYS_SBDFR)	8	W (always reads 0)	00h	7.7.2/86
3002	System Device Identification Register: High (SYS_SDIDH)	8	R	00h	7.7.3/87
3003	System Device Identification Register: Low (SYS_SDIDL)	8	R	46h	7.7.4/87
3004	System Options Register 1 (SYS_SOPT1)	8	R/W	0Ch	7.7.5/88
3005	System Options Register 2 (SYS_SOPT2)	8	R/W	00h	7.7.6/89
3006	System Options Register 3 (SYS_SOPT3)	8	R/W	00h	7.7.7/90
3007	System Options Register 4 (SYS_SOPT4)	8	R/W	00h	7.7.8/91
3008	System Options Register 5 (SYS_SOPT5)	8	R/W	C0h	7.7.9/92
3009	System Options Register 6 (SYS_SOPT6)	8	R/W	04h	7.7.10/93
300A	System Options Register 7 (SYS_SOPT7)	8	R/W	00h	7.7.11/94
300B	System Options Register 8 (SYS_SOPT8)	8	R/W	00h	7.7.12/95
300C	System Clock Gating Control 1 Register (SYS_SCGC1)	8	R/W	AFh	7.7.13/96
300D	System Clock Gating Control 2 Register (SYS_SCGC2)	8	R/W	FCh	7.7.14/97
300E	System Clock Gating Control 3 Register (SYS_SCGC3)	8	R/W	12h	7.7.15/99
300F	System Clock Gating Control 4 Register (SYS_SCGC4)	8	R/W	E9h	7.7.16/99
304A	Illegal Address Register: High (SYS_ILLAH)	8	R	Undefined	7.7.17/101
304B	Illegal Address Register: Low (SYS_ILLAL)	8	R	Undefined	7.7.18/101
30F8	Universally Unique Identifier Register 1 (SYS_UUID1)	8	R	Undefined	7.7.19/102
30F9	Universally Unique Identifier Register 2 (SYS_UUID2)	8	R	Undefined	7.7.20/102
30FA	Universally Unique Identifier Register 3 (SYS_UUID3)	8	R	Undefined	7.7.21/103
30FB	Universally Unique Identifier Register 4 (SYS_UUID4)	8	R	Undefined	7.7.22/103
30FC	Universally Unique Identifier Register 5 (SYS_UUID5)	8	R	Undefined	7.7.23/104
30FD	Universally Unique Identifier Register 6 (SYS_UUID6)	8	R	Undefined	7.7.24/104
30FE	Universally Unique Identifier Register 7 (SYS_UUID7)	8	R	Undefined	7.7.25/105
30FF	Universally Unique Identifier Register 8 (SYS_UUID8)	8	R	Undefined	7.7.26/105

7.7.1 System Reset Status Register (SYS_SRS)

This register includes read-only status flags to indicate the source of the most recent reset. When a debug host forces reset by writing 1 to the SYS_SBDFR[BDFR] bit, none of the status bits in SRS will be set. The reset state of these bits depends on what caused the MCU to reset.

NOTE

For PIN, WDOG, and ILOP, any of these reset sources that are active at the time of reset (not including POR or LVR) will

cause the corresponding bit(s) to be set; bits corresponding to sources that are not active at the time of reset will be cleared.

NOTE

The RESET values in the figure are values for power on reset; for other resets, the values depend on the trigger causes.

Address: 3000h base + 0h offset = 3000h

Bit	7	6	5	4	3	2	1	0
Read	POR	PIN	WCOP	ILOP	ILAD	LOC	LVD	FILA
Write								
Reset	1	0	0	0	0	0	1	0

SYS_SRS field descriptions

Field	Description
7 POR	Power-On Reset Reset was caused by the power-on detection logic. When the internal supply voltage was ramping up at the time, the low-voltage reset (LVR) status bit is also set to indicate that the reset occurred while the internal supply was below the LVR threshold. **NOTE:** This bit POR to 1, LVR to uncertain value and reset to 0 at any other conditions. 0 Reset not caused by POR. 1 POR caused reset.
6 PIN	External Reset Pin Reset was caused by an active low level on the external reset pin. 0 Reset not caused by external reset pin. 1 Reset came from external reset pin.
5 WCOP	Windowed COP (WCOP) Reset was caused by the WCOP timer timing out. This reset source may be blocked by SYS_SOPT5[COPT] =00. 0 Reset not caused by WCOP timeout. 1 Reset caused by WCOP timeout.
4 ILOP	Illegal Opcode Reset was caused by an attempt to execute an unimplemented or illegal opcode. The STOP instruction is considered illegal if stop is disabled by STOPE = 0 in the SOPT register. The BGND instruction is considered illegal if active background mode is disabled by ENBDM = 0 in the BDCSC register. 0 Reset not caused by an illegal opcode. 1 Reset caused by an illegal opcode.
3 ILAD	Illegal Address Reset was caused by an attempt to access a illegal address. The illegal address is captured in illegal address register (ILLAH:ILLAL).

Table continues on the next page...

SYS_SRS field descriptions (continued)

Field	Description
	0 Reset not caused by an illegal address. 1 Reset caused by an illegal address.
2 LOC	Internal Clock Source Module Reset Reset was caused by an ICS module reset. 0 Reset not caused by ICS module. 1 Reset caused by ICS module.
1 LVD	Low Voltage Detect If the LVDRE bit is set in run mode or both LVDRE and LVDSE bits are set in stop mode, and the supply drops below the LVD trip voltage, an LVD reset will occur. This bit is also set by POR. **NOTE:** This bit reset to 1 on POR and LVR and reset to 0 on other reset. 0 Reset not caused by LVD trip or POR. 1 Reset caused by LVD trip or POR.
0 FILA	Flash Illegal Access Reset was caused by an flash illegal access. 0 Reset not caused by an flash illegal access. 1 Reset caused by an flash illegal access.

7.7.2 System Background Debug Force Reset Register (SYS_SBDFR)

This register contains a single write-only control bit. A serial background command such as WRITE_BYTE must be used to write to SYS_SBDFR. Attempts to write this register from a user program are ignored. Reads always return 0x00.

NOTE

This register is the same as the BDC_SBDFR.

Address: 3000h base + 1h offset = 3001h

Bit	7	6	5	4	3	2	1	0
Read	0							0
Write								BDFR
Reset	0	0	0	0	0	0	0	0

SYS_SBDFR field descriptions

Field	Description
7–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 BDFR	Background Debug Force Reset

Table continues on the next page...

SYS_SBDFR field descriptions (continued)

Field	Description
	A serial background command such as WRITE_BYTE may be used to allow an external debug host to force a target system reset. Writing logic 1 to this bit forces an MCU reset. This bit cannot be written from a user program. **NOTE:** BDFR is writable only through serial background debug commands, not from user programs.

7.7.3 System Device Identification Register: High (SYS_SDIDH)

This read-only register, together with SYS_SDIDL, is included so that host development systems can identify the HCS08 derivative and revision number. This allows the development software to recognize where specific memory blocks, registers, and control bits are located in a target MCU.

Address: 3000h base + 2h offset = 3002h

Bit	7	6	5	4	3	2	1	0
Read	Reserved				ID			
Write								
Reset	0	0	0	0	0	0	0	0

SYS_SDIDH field descriptions

Field	Description
7–4 Reserved	This field is reserved.
ID	Part Identification Number These bits, together with the SYS_SDIDL, indicate part identification number. Each derivative in the HCS08 family has a unique identification number. This device is hard coded to the value 0x46.

7.7.4 System Device Identification Register: Low (SYS_SDIDL)

This read-only register, together with SYS_SDIDH, is included so host development systems can identify the HCS08 derivative and revision number. This allows the development software to recognize where specific memory blocks, registers, and control bits are located in a target MCU.

Address: 3000h base + 3h offset = 3003h

Bit	7	6	5	4	3	2	1	0
Read	ID							
Write								
Reset	0	1	0	0	0	1	1	0

SYS_SDIDL field descriptions

Field	Description
ID	Part Identification Number These bits, together with the SYS_SDIDH, indicate part identification number. Each derivative in the HCS08 family has a unique identification number. This device is hard coded to the value 0x46.

7.7.5 System Options Register 1 (SYS_SOPT1)

Address: 3000h base + 4h offset = 3004h

Bit	7	6	5	4	3	2	1	0
Read	SCI0PS	IICPS		0	BKGDPE	RSTPE	FWAKE	STOPE
Write								
Reset	0	0	0	0	1	1	0	0

SYS_SOPT1 field descriptions

Field	Description
7 SCI0PS	SCI0 Pin Select This write-once bit selects the SCI0 pinouts. 0 SCI0 RxD and TxD are mapped on PTB0 and PTB1. 1 SCI0 RxD and TxD are mapped on PTA2 and PTA3.
6–5 IICPS	IIC Port Pin Select This write-once bit selects the IIC port pins. 00 IIC SCL and SDA are mapped on PTA3 and PTA2, respectively. 01 IIC SCL and SDA are mapped on PTB7 and PTB6, respectively. 10 IIC SCL and SDA are mapped on PTB3 and PTB2, respectively. 11 Reserved.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 BKGDPE	Background Debug Mode Pin Enable This write-once bit when set enables the PTA4/FTM0CH1O/ACMP0O/BKGD/MS pin to function as BKGD/MS. When clear, the pin functions as output only PTA4. This pin defaults to the BKGD/MS function following any MCU reset. 0 PTA4/FTM0CH1O/ACMP0O/BKGD/MS as PTA4, FTM0CH1O or ACMPOO function. 1 PTA4/FTM0CH1O/ACMP0O/BKGD/MS as BKGD function.
2 RSTPE	RESET Pin Enable This write-once bit can be written after any reset. When RSTPE is set, the PTA5/IRQ/FTM0CH0/TCLK0/RESET_b pin functions as RESET. When clear, the pin functions as one of its alternative functions. This pin defaults to RESET following an MCU POR. Other resets will not affect this bit. When RSTPE is set, an internal pullup device on RESET is enabled.

Table continues on the next page...

SYS_SOPT1 field descriptions (continued)

Field	Description
	0 PTA5/IRQ/FTM0CH0/TCLK0/RESET_b pin functions as PTA5, IRQ, FTM0CH0 or TCLK0. 1 PTA5/IRQ/FTM0CH0/TCLK0/RESET_b pin functions as RESET.
1 FWAKE	Fast Wakeup Enable This write once bit can set CPU wakeup without any interrupt subroutine serviced. This action saved more than 11 cycles(whole interrupt subroutine time). After wake up CPU continue the address before wait or stop. **NOTE:** When FWAKE is set, user should avoid generating interrupt 0-8 bus clock cycles after issuing the stop instruction, or the MCU may stuck at stop3 mode and cannot wake up by interrupts. 0 CPU wakes up as normal. 1 CPU wakes up without any interrupt subroutine serviced.
0 STOPE	Stop Mode Enable This write-once bit defaults to 0 after reset, which disables stop mode. If stop mode is disabled and a user program attempts to execute a STOP instruction, an illegal opcode reset occurs. 0 Stop mode disabled. 1 Stop mode enabled.

7.7.6 System Options Register 2 (SYS_SOPT2)

This register may be read/write at any time. SYS_SOPT2 should be written during the user's reset initialization program to set the desired controls even if the desired settings are the same as the reset settings.

Address: 3000h base + 5h offset = 3005h

Bit	7	6	5	4	3	2	1	0
Read Write	TXDME	FTMES	RXDFE	RXDCE	ACIC	RTCC	ADHWTS	
Reset	0	0	0	0	0	0	0	0

SYS_SOPT2 field descriptions

Field	Description
7 TXDME	SCI0 TxD Modulation Select This bit enables the SCI0 TxD output modulated by FTM0 channel 0. 0 TxD0 output is connected to pinout directly. 1 TxD0 output is modulated by FTM0 channel 0 before mapped to pinout.
6 FTMES	FTM Edge Select This bit selects the effective FTM output edge to trigger ADC. 0 Rising edge. 1 Falling edge.

Table continues on the next page...

SYS_SOPT2 field descriptions (continued)

Field	Description
5 RXDFE	SCI0 RxD Filter Select This bit enables the SCI0 RxD input filtered by ACMP0. When this function is enabled, any signal tagged with ACMP0 inputs can be regarded SCI0. 0 RXD0 input signal is connected to SCI0 module directly. 1 RXD0 input signal is filtered by ACMP0, then injected to SCI0.
4 RXDCE	SCI0 RxD Capture Select This bit enables the SCI0 RxD is captured by FTM0 channel 1. 0 RXD0 input signal is connected to SCI0 module only. 1 RXD0 input signal is connected to SCI0 module and FTM0 channel 1.
3 ACIC	Analog Comparator to Input Capture Enable This bit connects the output of ACMP0 to FTM2 input channel 0. 0 ACMP0 output not connected to FTM2 input channel 0. 1 ACMP0 output connected to FTM2 input channel 0.
2 RTCC	Real-Time Counter Capture This bit allows the Real-time Counter (RTC) overflow to be captured by FTM2 channel 1. 0 RTC overflow is not connected to FTM2 input channel 1. 1 RTC overflow is connected to FTM2 input channel 1.
ADHWTS	ADC Hardware Trigger Source These bits select the ADC hardware trigger source. All trigger sources start ADC conversion on rising edge. 00 RTC overflow as the ADC hardware trigger. 01 MTIM0 overflow as the ADC hardware trigger. 10 ACMP0 output as the ADC hardware trigger. 11 FTM0 channel 0/1 or FTM2 channel 0/1 output with 8-bit programmable delay and selectable edge.

7.7.7 System Options Register 3 (SYS_SOPT3)

This register may be read and written at any time.

Address: 3000h base + 6h offset = 3006h

Bit	7	6	5	4	3	2	1	0
Read	0	FTM0PS	FTMCHS		0	BUSREF		
Write								
Reset	0	0	0	0	0	0	0	0

SYS_SOPT3 field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 FTM0PS	FTM0 Pin Select This bit selects the FTM0 Pinouts. 0 FTM0CH0 and FTM0CH1 are mapped on PTA0 and PTA1. 1 FTM0CH0 and FTM0CH1 are mapped on PTA5 and PTA4.
5–4 FTMCHS	FTM Channel Select These bits select one channel from those of FTM0 and FTM2 to be used as the ADC hardware trigger source. 00 FTM0 channel 0 is selected for the ADC hardware trigger. 01 FTM0 channel 1 is selected for the ADC hardware trigger. 10 FTM2 channel 0 is selected for the ADC hardware trigger. 11 FTM2 channel 1 is selected for the ADC hardware trigger.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
BUSREF	BUS Output select This bit enables bus clock output for delay block via an optional prescalar. 000 Bus. 001 Bus divided by 2. 010 Bus divided by 4. 011 Bus divided by 8. 100 Bus divided by 16. 101 Bus divided by 32. 110 Bus divided by 64. 111 Bus divided by 128.

7.7.8 System Options Register 4 (SYS_SOPT4)

Address: 3000h base + 7h offset = 3007h

Bit	7	6	5	4	3	2	1	0
Read Write	DELAY							
Reset	0	0	0	0	0	0	0	0

SYS_SOPT4 field descriptions

Field	Description
DELAY	FTM Trigger Delay These bits specify the delay from FTM0 channel 0/1 or FTM2 channel 0/1 output to ADC hardware trigger upon the setting of ADHWTS. The 8-bit modulo value allows the delay from 0 to 255 upon the BUSREF

SYS_SOPT4 field descriptions (continued)

Field	Description
	clock settings. This is a one-shot counter that starts ticking when the trigger arrives and stop ticking when the counter value reaches the modulo value that is defined.

7.7.9 System Options Register 5 (SYS_SOPT5)

Address: 3000h base + 8h offset = 3008h

Bit	7	6	5	4	3	2	1	0
Read	COPT		COPCLKS		COPW	0		
Write								
Reset	1	1	0	0	0	0	0	0

SYS_SOPT5 field descriptions

Field	Description
7–6 COPT	COP Timeout These write-once bits selects the timeout period of the WCOP. COPT along with SOPT5[COPCLKS] defines the WCOP timeout period as described in windowed computer operating properly (WCOP) watchdog.

COPCLKS	COPT	WCOP Timeout Period
N/A	00	WCOP is disabled
00/10	01	2^5 cycles
00/10	10	2^8 cycles
00/10	11	2^{10} cycles
01/11	01	2^{13} cycles
01/11	10	2^{16} cycles
01/11	11	2^{18} cycles

5–4 COPCLKS	WCOP Clock Source Select These write-once bits selects the WCOP clock source. 00 WCOP logic runs from internal LPO clock (LPOCLK). 01 WCOP logic runs from system bus clock (BUSCLK). 10 WCOP logic runs from internal RC oscillator clock (IRCLK). 11 WCOP logic runs from external clock (EXTCLK).
3 COPW	WCOP Window Mode Enable This write-once bit specifies whether the WCOP operates in Normal or Window mode. In Window mode, the 0x55-0xAA write sequence to the SRS register must occur within the last 25% of the selected period; any write to the SRS register during the first 75% of the selected period resets the microcontroller. 0 Normal mode. 1 Window mode.

Table continues on the next page...

SYS_SOPT5 field descriptions (continued)

Field	Description
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

7.7.10 System Options Register 6 (SYS_SOPT6)

This register may be read and written at any time.

Address: 3000h base + 9h offset = 3009h

Bit	7	6	5	4	3	2	1	0
Read	ESFC	0				VREFSEL		AMPEN
Write								
Reset	0	0	0	0	0	1	0	0

SYS_SOPT6 field descriptions

Field	Description
7 ESFC	Enable Stalling Flash Controller Enables stalling flash controller when flash is busy. Enables stalling flash controller when flash is busy. When software needs to access the flash memory while a flash memory resource is being manipulated by a flash command, software can enable a stall mechanism to avoid a read collision. The stall mechanism allows software to execute code from the same block on which flash operations are being performed. However, software must ensure the sector the flash operations are being performed on is not the same sector from which the code is executing. ESFC enables the stall mechanism. This bit must be set only just before the flash operation is executed and must be cleared when the operation completes. 0 Disable stalling flash controller when flash is busy. 1 Enable stalling flash controller when flash is busy.
6–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2–1 VREFSEL	OPAMP Reference Select This bit selects the operational amplifier (OPAMP) module reference level. 00 OPAMP reference is 1/8 analog power. 01 OPAMP reference is 1/4 analog power. 10 OPAMP reference is 1/2 analog power. 11 Reserved.
0 AMPEN	OPAMP Module Enable This bit enables or disables the operational amplifier (OPAMP) module. 0 Disable OPAMP. 1 Enable OPAMP.

7.7.11 System Options Register 7 (SYS_SOPT7)

Address: 3000h base + Ah offset = 300Ah

Bit	7	6	5	4	3	2	1	0
Read Write	FTM2CH5OC	FTM2CH4OC	FTM2CH3OC	FTM2CH2OC	FTM2CH1OC	FTM2CH0OC	FTM0CH1OC	FTM0CH0OC
Reset	0	0	0	0	0	0	0	0

SYS_SOPT7 field descriptions

Field	Description
7 FTM2CH5OC	FTM2 channel 5 Output Control This bit enables the software output control function for FTM2 channel 5 output. 0 Software output control function for FTM2 channel 5 is disabled. 1 Software output control function for FTM2 channel 5 is enabled.
6 FTM2CH4OC	FTM2 channel 4 Output Control This bit enables the software output control function for FTM2 channel 4 output. 0 Software output control function for FTM2 channel 4 is disabled. 1 Software output control function for FTM2 channel 4 is enabled.
5 FTM2CH3OC	FTM2 channel 3 Output Control This bit enables the software output control function for FTM2 channel 3 output. 0 Software output control function for FTM2 channel 3 is disabled. 1 Software output control function for FTM2 channel 3 is enabled.
4 FTM2CH2OC	FTM2 channel 2 Output Control This bit enables the software output control function for FTM2 channel 2 output. 0 Software output control function for FTM2 channel 2 is disabled. 1 Software output control function for FTM2 channel 2 is enabled.
3 FTM2CH1OC	FTM2 channel 1 Output Control This bit enables the software output control function for FTM2 channel 1 output. 0 Software output control function for FTM2 channel 1 is disabled. 1 Software output control function for FTM2 channel 1 is enabled.
2 FTM2CH0OC	FTM2 channel 0 Output Control This bit enables the software output control function for FTM2 channel 0 output. 0 Software output control function for FTM2 channel 0 is disabled. 1 Software output control function for FTM2 channel 0 is enabled.
1 FTM0CH1OC	FTM0 channel 1 Output Control This bit enables the software output control function for FTM0 channel 1 output.

Table continues on the next page...

SYS_SOPT7 field descriptions (continued)

Field	Description
	0 Software output control function for FTM0 channel 1 is disabled. 1 Software output control function for FTM0 channel 1 is enabled.
0 FTM0CH0OC	FTM0 channel 0 Output Control This bit enables the software output control function for FTM0 channel 0 output. 0 Software output control function for FTM0 channel 0 is disabled. 1 Software output control function for FTM0 channel 0 is enabled.

7.7.12 System Options Register 8 (SYS_SOPT8)

Address: 3000h base + Bh offset = 300Bh

Bit	7	6	5	4
Read Write	FTM2CH5OCV	FTM2CH4OCV	FTM2CH3OCV	FTM2CH2OCV
Reset	0	0	0	0

Bit	3	2	1	0
Read Write	FTM2CH1OCV	FTM2CH0OCV	FTM0CH1OCV	FTM0CH0OCV
Reset	0	0	0	0

SYS_SOPT8 field descriptions

Field	Description
7 FTM2CH5OCV	FTM2 channel 5 Output Control Value This bit selects the software output control value for FTM2 channel 5 output. 0 Software output control value for FTM2 channel 5 is 0. 1 Software output control value for FTM2 channel 5 is 1.
6 FTM2CH4OCV	FTM2 channel 4 Output Control Value This bit selects the software output control value for FTM2 channel 4 output. 0 Software output control value for FTM2 channel 4 is 0. 1 Software output control value for FTM2 channel 4 is 1.
5 FTM2CH3OCV	FTM2 channel 3 Output Control Value This bit selects the software output control value for FTM2 channel 3 output. 0 Software output control value for FTM2 channel 3 is 0. 1 Software output control value for FTM2 channel 3 is 1.
4 FTM2CH2OCV	FTM2 channel 2 Output Control Value This bit selects the software output control value for FTM2 channel 2 output. 0 Software output control value for FTM2 channel 2 is 0. 1 Software output control value for FTM2 channel 2 is 1.

Table continues on the next page...

SYS_SOPT8 field descriptions (continued)

Field	Description
3 FTM2CH1OCV	FTM2 channel 1 Output Control Value This bit selects the software output control value for FTM2 channel 1 output. 0 Software output control value for FTM2 channel 1 is 0. 1 Software output control value for FTM2 channel 1 is 1.
2 FTM2CH0OCV	FTM2 channel 0 Output Control Value This bit selects the software output control value for FTM2 channel 0 output. 0 Software output control value for FTM2 channel 0 is 0. 1 Software output control value for FTM2 channel 0 is 1.
1 FTM0CH1OCV	FTM0 channel 1 Output Control Value This bit selects the software output control value for FTM0 channel 1 output. 0 Software output control value for FTM0 channel 1 is 0. 1 Software output control value for FTM0 channel 1 is 1.
0 FTM0CH0OCV	FTM0 channel 0 Output Control Value This bit selects the software output control value for FTM0 channel 0 output. 0 Software output control value for FTM0 channel 0 is 0. 1 Software output control value for FTM0 channel 0 is 1.

7.7.13 System Clock Gating Control 1 Register (SYS_SCGC1)

This high page register contains control bits to enable or disable the bus clock to the FTMs, PWT, MTIM2, and RTC modules. Gating off the clocks to unused peripherals is used to reduce the MCU's run and wait currents.

NOTE

User software must disable the peripheral before disabling the clocks to the peripheral. When clocks are re-enabled to a peripheral, the peripheral registers need to be re-initialized by user software.

Address: 3000h base + Ch offset = 300Ch

Bit	7	6	5	4	3	2	1	0
Read	FTM2	0	FTM0	0	PWT	MTIM1	MTIM0	RTC
Write								
Reset	1	0	1	0	1	1	1	1

SYS_SCGC1 field descriptions

Field	Description
7 FTM2	FTM2 Clock Gate Control This bit controls the clock gate to the FTM2 module. 0 Bus clock to the FTM2 module is disabled. 1 Bus clock to the FTM2 module is enabled.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 FTM0	FTM0 Clock Gate Control This bit controls the clock gate to the FTM0 module. 0 Bus clock to the FTM0 module is disabled. 1 Bus clock to the FTM0 module is enabled.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 PWT	PWT Clock Gate Control This bit controls the clock gate to the PWT module. 0 Bus clock to the PWT module is disabled. 1 Bus clock to the PWT module is enabled.
2 MTIM1	MTIM1 Clock Gate Control This bit controls the clock gate to the MTIM1 module. 0 Bus clock to the MTIM1 module is disabled. 1 Bus clock to the MTIM1 module is enabled.
1 MTIM0	MTIM0 Clock Gate Control This bit controls the clock gate to the MTIM0 module. 0 Bus clock to the MTIM0 module is disabled. 1 Bus clock to the MTIM0 module is enabled.
0 RTC	RTC Clock Gate Control This bit controls the clock gate to the RTC module. 0 Bus clock to the RTC module is disabled. 1 Bus clock to the RTC module is enabled.

7.7.14 System Clock Gating Control 2 Register (SYS_SCGC2)

This high-page register contains control bits to enable or disable the bus clock to the FDS, PMC, DBG, NVM, CRC, and IPC modules. Gating off the clocks to unused peripherals is used to reduce the MCU's run and wait currents.

NOTE

User software should disable the peripheral before disabling the clocks to the peripheral. When clocks are re-enabled to a peripheral, the peripheral registers need to be re-initialized by user software.

Address: 3000h base + Dh offset = 300Dh

Bit	7	6	5	4	3	2	1	0
Read	FDS	PMC	DBG	NVM	IPC	CRC	0	
Write								
Reset	1	1	1	1	1	1	0	0

SYS_SCGC2 field descriptions

Field	Description
7 FDS	FDS Clock Gate Control This bit controls the clock gate to the FDS module. 0 Bus clock to the FDS module is disabled. 1 Bus clock to the FDS module is enabled.
6 PMC	PMC Clock Gate Control This bit controls the clock gate to the PMC module. 0 Bus clock to the PMC module is disabled. 1 Bus clock to the PMC module is enabled.
5 DBG	DBG Clock Gate Control This bit controls the clock gate to the DBG module. 0 Bus clock to the DBG module is disabled. 1 Bus clock to the DBG module is enabled.
4 NVM	NVM Clock Gate Control This bit controls the clock gate to the NVM module. 0 Bus clock to the NVM module is disabled. 1 Bus clock to the NVM module is enabled.
3 IPC	IPC Clock Gate Control This bit controls the clock gate to the IPC module. 0 Bus clock to the IPC module is disabled. 1 Bus clock to the IPC module is enabled.
2 CRC	CRC Clock Gate Control This bit controls the clock gate to the CRC module. 0 Bus clock to the CRC module is disabled. 1 Bus clock to the CRC module is enabled.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

7.7.15 System Clock Gating Control 3 Register (SYS_SCGC3)

This high page register contains control bits to enable or disable the bus clock to the SCI0, IIC modules. Gating off the clocks to unused peripherals is used to reduce the MCU's run and wait currents.

NOTE

User software should disable the peripheral before disabling the clocks to the peripheral. When clocks are re-enabled to a peripheral, the peripheral registers need to be re-initialized by user software.

Address: 3000h base + Eh offset = 300Eh

Bit	7	6	5	4	3	2	1	0
Read	0			SCI0	0		IIC	0
Write								
Reset	0	0	0	1	0	0	1	0

SYS_SCGC3 field descriptions

Field	Description
7–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 SCI0	SCI0 Clock Gate Control This bit controls the clock gate to the SCI0 module. 0 Bus clock to the SCI0 module is disabled. 1 Bus clock to the SCI0 module is enabled.
3–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 IIC	IIC Clock Gate Control This bit controls the clock gate to the IIC module. 0 Bus clock to the IIC module is disabled. 1 Bus clock to the IIC module is enabled.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

7.7.16 System Clock Gating Control 4 Register (SYS_SCGC4)

This high-page register contains control bits to enable or disable the bus clock to the FDS, PMC, DBG, NVM, CRC, and IPC modules. Gating off the clocks to unused peripherals is used to reduce the MCU's run and wait currents.

NOTE

User software should disable the peripheral before disabling the clocks to the peripheral. When clocks are re-enabled to a peripheral, the peripheral registers need to be re-initialized by user software.

Address: 3000h base + Fh offset = 300Fh

Bit	7	6	5	4	3	2	1	0
Read	ACMP0	ACMP1	ADC	0	IRQ	0		KBI0
Write								
Reset	1	1	1	0	1	0	0	1

SYS_SCGC4 field descriptions

Field	Description
7 ACMP0	ACMP0 Clock Gate Control This bit controls the clock gate to the ACMP0 module. 0 Bus clock to the ACMP0 module is disabled. 1 Bus clock to the ACMP0 module is enabled.
6 ACMP1	ACMP1 Clock Gate Control This bit controls the clock gate to the ACMP1 module. 0 Bus clock to the ACMP1 module is disabled. 1 Bus clock to the ACMP1 module is enabled.
5 ADC	ADC Clock Gate Control This bit controls the clock gate to the ADC module. 0 Bus clock to the ADC module is disabled. 1 Bus clock to the ADC module is enabled.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 IRQ	IRQ Clock Gate Control This bit controls the clock gate to the IRQ module. 0 Bus clock to the IRQ module is disabled. 1 Bus clock to the IRQ module is enabled.
2–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 KBI0	KBI0 Clock Gate Control This bit controls the clock gate to the KBI0 module. 0 Bus clock to the KBI0 module is disabled. 1 Bus clock to the KBI0 module is enabled.

7.7.17 Illegal Address Register: High (SYS_ILLAH)

The SYS_ILLAH is a read-only register containing the high 8-bit of the illegal address of ILAD reset.

Address: 3000h base + 4Ah offset = 304Ah

Bit	7	6	5	4	3	2	1	0
Read	ADDR[15:8]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_ILLAH field descriptions

Field	Description
ADDR[15:8]	High 8-bit of illegal address **NOTE:** For ILAD, it reset to the high 8-bit of the illegal address; in other cases, the reset to values are undetermined.

7.7.18 Illegal Address Register: Low (SYS_ILLAL)

The SYS_ILLAL is a read-only register containing the low 8-bit of the illegal address of ILAD reset.

Address: 3000h base + 4Bh offset = 304Bh

Bit	7	6	5	4	3	2	1	0
Read	ADDR[7:0]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_ILLAL field descriptions

Field	Description
ADDR[7:0]	Low 8-bit of illegal address **NOTE:** For ILAD, it resets to the low 8-bit of the illegal address; in other cases, the reset to values are undetermined.

7.7.19 Universally Unique Identifier Register 1 (SYS_UUID1)

The read-only SYS_UUIDx registers contain a series of 64-bit number to identify the unique device in the family.

Address: 3000h base + F8h offset = 30F8h

Bit	7	6	5	4	3	2	1	0
Read	ID[63:56]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_UUID1 field descriptions

Field	Description
ID[63:56]	Universally Unique Identifier

7.7.20 Universally Unique Identifier Register 2 (SYS_UUID2)

The read-only SYS_UUIDx registers contain a series of 63-bit number to identify the unique device in the family.

Address: 3000h base + F9h offset = 30F9h

Bit	7	6	5	4	3	2	1	0
Read	ID[55:48]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_UUID2 field descriptions

Field	Description
ID[55:48]	Universally Unique Identifier

7.7.21 Universally Unique Identifier Register 3 (SYS_UUID3)

The read-only SYS_UUIDx registers contain a series of 63-bit number to identify the unique device in the family.

Address: 3000h base + FAh offset = 30FAh

* Notes:
- x = Undefined at reset.

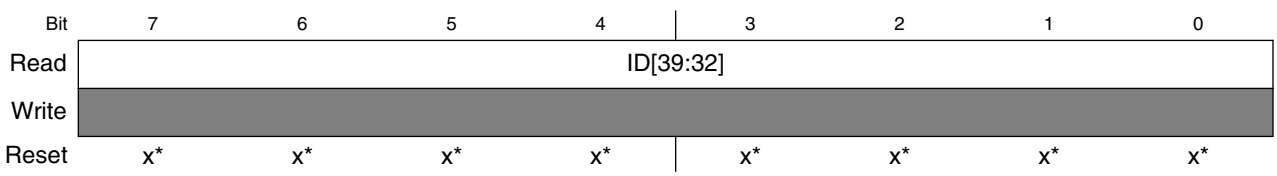
SYS_UUID3 field descriptions

Field	Description
ID[47:40]	Universally Unique Identifier

7.7.22 Universally Unique Identifier Register 4 (SYS_UUID4)

The read-only SYS_UUIDx registers contain a series of 63-bit number to identify the unique device in the family.

Address: 3000h base + FBh offset = 30FBh



* Notes:
- x = Undefined at reset.

SYS_UUID4 field descriptions

Field	Description
ID[39:32]	Universally Unique Identifier

7.7.23 Universally Unique Identifier Register 5 (SYS_UUID5)

The read-only SYS_UUIDx registers contain a series of 64-bit number to identify the unique device in the family.

Address: 3000h base + FCh offset = 30FCh

Bit	7	6	5	4	3	2	1	0
Read	ID[31:24]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_UUID5 field descriptions

Field	Description
ID[31:24]	Universally Unique Identifier

7.7.24 Universally Unique Identifier Register 6 (SYS_UUID6)

The read-only SYS_UUIDx registers contain a series of 64-bit number to identify the unique device in the family.

Address: 3000h base + FDh offset = 30FDh

Bit	7	6	5	4	3	2	1	0
Read	ID[23:16]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_UUID6 field descriptions

Field	Description
ID[23:16]	Universally Unique Identifier

7.7.25 Universally Unique Identifier Register 7 (SYS_UUID7)

The read-only SYS_UUIDx registers contain a series of 64-bit number to identify the unique device in the family.

Address: 3000h base + FEh offset = 30FEh

Bit	7	6	5	4	3	2	1	0
Read	ID[15:8]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_UUID7 field descriptions

Field	Description
ID[15:8]	Universally Unique Identifier

7.7.26 Universally Unique Identifier Register 8 (SYS_UUID8)

The read-only SYS_UUIDx registers contain a series of 64-bit number to identify the unique device in the family.

Address: 3000h base + FFh offset = 30FFh

Bit	7	6	5	4	3	2	1	0
Read	ID[7:0]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_UUID8 field descriptions

Field	Description
ID[7:0]	Universally Unique Identifier

Chapter 8
Clock management

8.1 Clock module

These series contain the following on-chip clock sources:

- Internal clock source (ICS) module — The main clock source generator providing bus clock and other reference clocks to peripherals
- External oscillator (XOSC) module — The external oscillator providing reference clock to internal clock source (ICS), the real-time clock counter clock module (RTC) and other MCU sub-systems.
- Low-power oscillator (LPO) module — The on-chip low-power oscillator providing 1 kHz reference clock to RTC and watchdog (WCOP).

NOTE

For this device, the system clock is the bus clock.

8.2 System clock distribution

The following figure shows a simplified clock connection diagram.

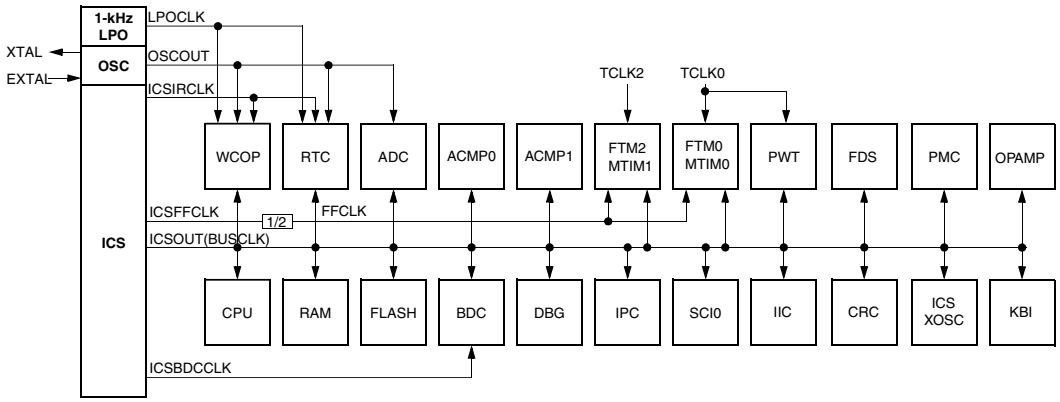


Figure 8-1. System clock distribution diagram

The clock system supplies:

- ICSOUT(BUSCLK) — This clock source is used as the bus clock which is the reference to CPU and all peripherals. Control bits in the ICS control registers determine which of the following clock sources is connected:
  - Internal reference clock
  - External reference clock
  - Frequency-locked loop (FLL) output
- ICSBDCCLK — This clock source is derived from the digitally controlled oscillator (DCO) of the ICS when the ICS is configured to run off of the internal or external reference clock. Development tools can select this internal self-clocked source (16 MHz) to speed up BDC communications in systems where the bus clock is slow.
- ICSIRCLK — This is the internal reference clock and can be selected as the clock source to the WCOP and RTC modules.
- ICSFFCLK — This is the reference clock of the FLL. Its frequency is determined by the setting of the ICS. ICSFFCLK is also used to generate the fixed frequency clock (FFCLK).
- FFCLK — This is the fixed frequency clock which can be selected as the clock source to the FTM and MTIM modules. It is generated by the ICSFFCLK after being synchronized to the bus clock, so the frequency of FFCLK is half of ICSFFCLK..
- LPOCLK — This clock is generated from an internal low power oscillator (≈1 kHz) that is completely independent of the ICS module. The LPOCLK can be selected as the clock source to the RTC or WDOG modules.
- OSCOUT — This is the direct output of the external oscillator module and can be selected as the clock source for RTC, WDOG and ADC.

- TCLK0 — This is an optional external clock source for the FTM0, PWT and MTIM0 modules. The TCLK0 must be limited to 1/4th frequency of the bus clock for synchronization.
- TCLK2 — This is an optional external clock source for the FTM2 and MTIM1 modules. The TCLK2 must be limited to 1/4th frequency of the bus clock for synchronization.

NOTE

Some tools like ProcessorExpert or USB Multilink may use flash memory location, such as 0xFF6F and/or 0xFF6E, to store the temporary trim value.

8.3 Internal clock source (ICS)

The internal clock source (ICS) module provides clock source options for the MCU. The module contains a frequency-locked loop (FLL) as a clock source that is controllable by an internal or external reference clock. The module can provide this FLL clock or the internal reference clock as a source for the MCU system clock, ICSOUT.

Whichever clock source is chosen, ICSOUT is the output from a bus clock divider (BDIV), which allows a lower clock frequency to be derived.

Key features of the ICS module are:

- Frequency-locked loop (FLL) is trimmable for accuracy
- Internal or external reference clocks can be used to control the FLL
- Reference divider is provided for external clock
- Internal reference clock has nine trim bits available
- Internal or external reference clocks can be selected as the clock source for the MCU
- Whichever clock is selected as the source can be divided down by 1, 2, 4, 8, 16, 32, 64 or 128
- FLL Engaged Internal mode is automatically selected out of reset
- A constant divide by 2 of the DCO output that can be select as BDC clock.
- Digitally-controlled oscillator (DCO) optimized for 32 MHz to 40 MHz frequency range
- FLL lock detector and external clock monitor

- FLL lock detector with interrupt capability
- External reference clock monitor with reset capability

8.4 Oscillator (OSC)

The OSC module provides the clock source for the MCU. The OSC module, in conjunction with an external crystal or resonator, generates a clock for the MCU that can be used as reference clock or bus clock.

Key features of the OSC module are:

- Supports 32 kHz crystals (low range mode)
- Supports 4–20 MHz crystals and resonators (high range mode)
- Automatic gain control (AGC) to optimize power consumption in both frequency ranges using low-power mode (low gain mode)
- High gain option in both frequency ranges: 32 kHz, 4–20 MHz
- Voltage and frequency filtering to guarantee clock frequency and stability
- Supports to be enabled by ICS.

8.5 Peripheral clock gating

This device includes a clock gating system to manage the bus clock sources to the individual peripherals. Using this system, the user can enable or disable the bus clock to each of the peripherals at the clock source, eliminating unnecessary clocks to peripherals that are not in use, thereby reducing the overall run and wait mode currents.

Out of reset, all peripheral clocks will be enabled. For lowest possible run or wait currents, user software should disable the clock source to any peripheral not in use. The actual clock will be enabled or disabled immediately following the write to the Clock Gating Control registers (SYS_SCGC1, SYS_SCGC2, SYS_SCGC3, and SYS_SCGC4). Any peripheral with a gated clock can not be used unless its clock is enabled. Writing to the registers of a peripheral with a disabled clock has no effect.

Note

User software must disable the peripheral before disabling the clocks to the peripheral. When clocks to a peripheral are re-enabled, the peripheral registers need to be re-initialized by user software.

In stop modes, the bus clock is disabled for all gated peripherals, regardless of the setting in SYS_SCGCx (x=1,2,3,4) registers.

Chapter 9
Central processor unit

9.1 Introduction

This section provides summary information about the registers, addressing modes, special operations, instructions and exceptions processing of the HCS08 V6 CPU.

The HCS08 V6 CPU is fully source- and object-code-compatible with the HCS08 CPU.

9.1.1 Features

Features of the HCS08 V6 CPU include:

- Object code fully upward-compatible with M68HC05 and M68HC08 families
- 16-bit stack pointer (any size stack anywhere in 64 KB CPU address space)
- 16-bit index register (H:X) with powerful indexed addressing modes
- 8-bit accumulator (A)
- Many instructions treat X as a second general-purpose 8-bit register
- Seven addressing modes:
  - Inherent — Operands in internal registers
  - Relative — 8-bit signed offset to branch destination
  - Immediate — Operand in next object code byte(s)
  - Direct — Operand in memory at 0x0000–0x00FF
  - Extended — Operand anywhere in 64-Kbyte address space

- Indexed relative to H:X — Five submodes including auto increment
- Indexed relative to SP — Improves C efficiency dramatically

- Memory-to-memory data move instructions with four address mode combinations
- Overflow, half-carry, negative, zero, and carry condition codes support conditional branching on the results of signed, unsigned, and binary-coded decimal (BCD) operations
- Efficient bit manipulation instructions
- STOP and WAIT instructions to invoke low-power operating modes

9.2 Programmer's Model and CPU Registers

Figure 9-1 shows the five CPU registers. CPU registers are not part of the memory map.

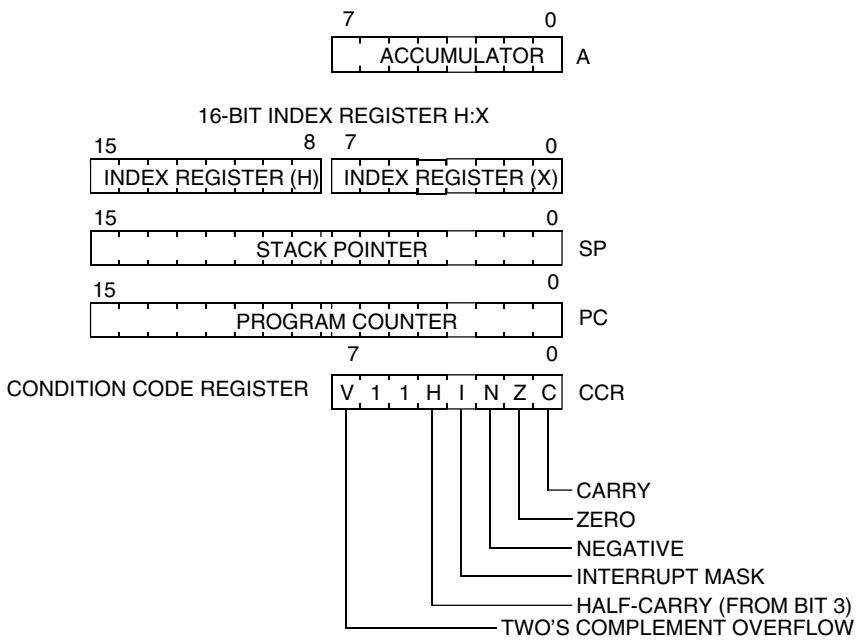


Figure 9-1. CPU Registers

9.2.1 Accumulator (A)

The A accumulator is a general-purpose 8-bit register. One input operand from the arithmetic logic unit (ALU) is connected to the accumulator, and the ALU results are often stored into the A accumulator after arithmetic and logical operations. The

accumulator can be loaded from memory using various addressing modes to specify the address where the loaded data comes from, or the contents of A can be stored to memory using various addressing modes to specify the address where data from A will be stored.

Reset has no effect on the contents of the A accumulator.

9.2.2 Index Register (H:X)

This 16-bit register is actually two separate 8-bit registers (H and X), which often work together as a 16-bit address pointer where H holds the upper byte of an address and X holds the lower byte of the address. All indexed addressing mode instructions use the full 16-bit value in H:X as an index reference pointer; however, for compatibility with the earlier M68HC05 family, some instructions operate only on the low-order 8-bit half (X).

Many instructions treat X as a second general-purpose 8-bit register that can be used to hold 8-bit data values. X can be cleared, incremented, decremented, complemented, negated, shifted, or rotated. Transfer instructions allow data to be transferred from A or transferred to A where arithmetic and logical operations can then be performed.

For compatibility with the earlier M68HC05 family, H is forced to 0x00 during reset. Reset has no effect on the contents of X.

9.2.3 Stack Pointer (SP)

This 16-bit address pointer register points at the next available location on the automatic last-in-first-out (LIFO) stack. The stack may be located anywhere in the 64 KB address space that has RAM, and can be any size up to the amount of available RAM. The stack is used to automatically save the return address for subroutine calls, the return address and CPU registers during interrupts, and for local variables. The AIS (add immediate to stack pointer) instruction adds an 8-bit signed immediate value to SP. This is most often used to allocate or deallocate space for local variables on the stack.

SP is forced to 0x00FF at reset for compatibility with the earlier M68HC05 family. HCS08 V6 programs normally change the value in SP to the address of the last location (highest address) in on-chip RAM during reset initialization to free up direct page RAM (from the end of the on-chip registers to 0x00FF).

The RSP (reset stack pointer) instruction was included for compatibility with the M68HC05 family and is seldom used in new HCS08 V6 programs because it affects only the low-order half of the stack pointer.

9.2.4 Program Counter (PC)

The program counter is a 16-bit register that contains the address of the next instruction or operand to be fetched.

During normal program execution, the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, interrupt, and return operations load the program counter with an address other than that of the next sequential location. This is called a change-of-flow.

During reset, the program counter is loaded with the reset vector that is located at 0xFFFE and 0xFFFF. The vector stored there is the address of the first instruction that will be executed after exiting the reset state.

9.2.5 Condition Code Register (CCR)

The 8-bit condition code register contains the interrupt mask (I) and five flags that indicate the results of the instruction just executed. Bits 6 and 5 are set permanently to 1. The following paragraphs describe the functions of the condition code bits in general terms.

Table 9-1. CCR Register Field Descriptions

Field	Description
7 V	**Two's Complement Overflow Flag** — The CPU sets the overflow flag when a two's complement overflow occurs. The signed branch instructions BGT, BGE, BLE, and BLT use the overflow flag. 0 No overflow 1 Overflow
4 H	**Half-Carry Flag** — The CPU sets the half-carry flag when a carry occurs between accumulator bits 3 and 4 during an add-without-carry (ADD) or add-with-carry (ADC) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations. The DAA instruction uses the states of the H and C condition code bits to automatically add a correction value to the result from a previous ADD or ADC on BCD operands to correct the result to a valid BCD value. 0 No carry between bits 3 and 4 1 Carry between bits 3 and 4
3 I	**Interrupt Mask Bit** — When the interrupt mask is set, all maskable CPU interrupts are disabled. CPU interrupts are enabled when the interrupt mask is cleared. When a CPU interrupt occurs, the interrupt mask is set automatically after the CPU registers are saved on the stack, but before the first instruction of the interrupt service routine is executed. Interrupts are not recognized at the instruction boundary after any instruction that clears I (CLI or TAP). This ensures that the next instruction after a CLI or TAP will always be executed without the possibility of an intervening interrupt, provided I was set. 0 Interrupts enabled

Table continues on the next page...

Table 9-1. CCR Register Field Descriptions (continued)

Field	Description
	1 Interrupts disabled
2 N	**Negative Flag** — The CPU sets the negative flag when an arithmetic operation, logic operation, or data manipulation produces a negative result, setting bit 7 of the result. Simply loading or storing an 8-bit or 16-bit value causes N to be set if the most significant bit of the loaded or stored value was 1. 0 Non-negative result 1 Negative result
1 Z	**Zero Flag** — The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of 0x00 or 0x0000. Simply loading or storing an 8-bit or 16-bit value causes Z to be set if the loaded or stored value was all 0s. 0 Non-zero result 1 Zero result
0 C	**Carry/Borrow Flag** — The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some instructions — such as bit test and branch, shift, and rotate — also clear or set the carry/borrow flag. 0 No carry out of bit 7 1 Carry out of bit 7

9.3 Addressing Modes

Addressing modes define the way the CPU accesses operands and data. In the HCS08 V6, memory, status and control registers, and input/output (I/O) ports share a single 64 KB CPU address space. This arrangement means that the same instructions that access variables in RAM can also be used to access I/O and control registers or nonvolatile program space.

Some instructions use more than one addressing mode. For instance, move instructions use one addressing mode to specify the source operand and a second addressing mode to specify the destination address. Instructions such as BRCLR, BRSET, CBEQ, and DBNZ use one addressing mode to specify the location of an operand for a test and then use relative addressing mode to specify the branch destination address when the tested condition is true. For BRCLR, BRSET, CBEQ, and DBNZ, the addressing mode listed in the instruction set tables is the addressing mode needed to access the operand to be tested, and relative addressing mode is implied for the branch destination.

Every addressing mode, except inherent, generates a 16-bit effective address. The effective address is the address of the memory location that the instruction acts on. Effective address computations do not require extra execution cycles. The HCS08 V6 CPU uses the 16 addressing modes described in the following sections.

9.3.1 Inherent Addressing Mode (INH)

In this addressing mode, instructions either have no operands or all operands are in internal CPU registers. In either case, the CPU does not need to access any memory locations to complete the instruction. Examples:

```
NOP          ;this instruction has no operands
CLRA         ;operand is a CPU register
```

9.3.2 Relative Addressing Mode (REL)

Relative addressing mode is used to specify the destination location for branch instructions. A signed two's complement byte offset value is located in the memory location immediately following the opcode. The offset gives a branching range of -128 to +127 bytes. In most assemblers, the programmer does not need to calculate the offset, because the assembler determines the proper offset and verifies that it is within the span of the branch.

During program execution, if a branch condition is true, the signed offset is sign-extended to a 16-bit value and is added to the current contents of the program counter, which causes program execution to continue at the branch destination address. If a branch condition is false, the CPU executes the next instruction.

9.3.3 Immediate Addressing Mode (IMM)

The operand for instructions with the immediate addressing mode is contained in the byte(s) immediately following the opcode. The byte or bytes that follow the opcode are the value of the statement rather than the address of the value. The pound symbol (#) is used to indicate an immediate addressing mode operand. One very common programming error is to accidentally omit the # symbol. This causes the assembler to misinterpret the following expression as an address rather than explicitly provided data. For example LDA #$55 means to load the immediate value $55 into the accumulator, while LDA $55 means to load the value from address $0055 into the accumulator. Without the # symbol, the instruction is erroneously interpreted as a direct addressing instruction.

Example:

```
LDA       #$55
CPHX      #$FFFF
LDHX      #$67
```

The size of the immediate operand is implied by the instruction context. In the third example, the instruction implies a 16-bit immediate value, but only an 8-bit value is supplied. In this case the assembler generates the 16-bit value $0067 because the CPU expects a 16-bit value in the instruction stream.

9.3.4 Direct Addressing Mode (DIR)

This addressing mode is sometimes called zero-page addressing because it accesses operands in the address range $0000 through $00FF. Since these addresses always begin with $00, only the low byte of the address needs to be included in the instruction, which saves program space and execution time. A system can be optimized by placing the most commonly accessed data in this area of memory. The low byte of the operand address is supplied with the instruction and the high byte of the address is assumed to be zero.

Examples:

```
LDA       $55
```

The value $55 is taken to be the low byte of an address in the range $0000 through $00FF. The high byte of the address is assumed to be zero. During execution, the CPU combines the value $55 from the instruction with the assumed value of $00 to form the address $0055, which is then used to access the data to be loaded into accumulator.

```
LDHX      $20
```

In this example, the value $20 is combined with the assumed value of $00 to form the address $0020. Since the LDHX instruction requires a 16-bit value, a 16-bit word of data is read from addresses $0020 and $0021. After execution, the H:X index register has the value from address $0020 in its high byte and the value from address $0021 in its low byte. The same happens for CPHX and STHX.

```
BRSET     0,$80,foo
```

In this example, direct addressing is used to access the operand and relative addressing is used to identify the destination address of a branch, in case the branch-taken conditions are met. This is also the case for BRCLR.

9.3.5 Extended Addressing Mode (EXT)

In extended addressing, the full 16-bit address of the memory location to be operated on is provided in the instruction. Extended addressing can access any location in the 64 KB memory map.

Example:

```
LDA     $F03B
```

This instruction uses extended addressing because $F03B is above the zero page. In most assemblers, the programmer does not need to specify whether an instruction is direct or extended. The assembler automatically selects the shortest form of the instruction.

9.3.6 Indexed Addressing Mode

Indexed addressing mode has seven variations, including five that use the 16-bit H:X index register pair and two that use the stack pointer as the base reference.

9.3.6.1 Indexed, No Offset (IX)

Instructions using the indexed, no offset addressing mode are one-byte instructions that can access data with variable addresses. The X (Index register low byte) register contains the low byte of the conditional address of the operand and the H (Index register high byte) register contains the high byte of the address.

Indexed, no offset instructions can move a pointer through a table or hold the address of a frequently used RAM or input/output (I/O) location.

9.3.6.2 Indexed, No Offset with Post Increment (IX+)

Instructions using the indexed, no offset with post increment addressing mode are two-byte instructions that address the operands and then increment the Index register (H:X). The X (Index register low byte) register contains the low byte of the conditional address of the operand and the H (Index register high byte) register contains the high byte of the address. This addressing mode is usually used for table searches. MOV and CBEQ instructions use this addressing mode as well.

9.3.6.3 Indexed, 8-Bit Offset (IX1)

Indexed with 8-bit offset instructions are two-byte instructions that can access data with a variable address. The CPU adds the unsigned bytes in the H:X register to the unsigned byte immediately following the opcode. The sum is the effective address.

Indexed, 8-bit offset instructions are useful in selecting the k-th element in an n-element table. The table can begin anywhere and can extend as far as the address map allows. The k value would typically be in H:X, and the address of the beginning of the table would be

in the byte following the opcode. Using H:X in this way, this addressing mode is limited to the first 256 addresses in memory. Tables can be located anywhere in the address map when H:X is used as the base address, and the byte following the opcode is the offset.

9.3.6.4 Indexed, 8-Bit Offset with Post Increment (IX1+)

Indexed, 8-bit offset with post-increment instructions are three-byte instructions that access the operands with variable addresses, then increment H:X. The CPU adds the unsigned bytes in the H:X register to the byte immediately following the opcode. The sum is the effective address. This addressing mode is generally used for table searches. This addressing mode is used for CBEQ instruction.

9.3.6.5 Indexed, 16-Bit Offset (IX2)

Indexed, 16-bit offset instructions are three-byte instructions that can access data with variable addresses at any location in memory. The CPU adds the unsigned contents of H:X to the 16-bit unsigned word formed by the two bytes following the opcode. The sum is the effective address of the operand. The first byte after the opcode is the most significant byte of the 16-bit offset; the second byte is the least significant byte of the 16-bit offset. As with direct and extended addressing, most assemblers determine the shortest form of indexed addressing.

Indexed, 16-bit offset instructions are useful in selecting the k-th element in an n-element table. The table can begin anywhere and can extend as far as the address map allows. The k value would typically be in H:X, and the address of the beginning of the table would be in the bytes following the opcode.

9.3.6.6 SP-Relative, 8-Bit Offset (SP1)

Stack pointer, 8-bit offset instructions are three-byte instructions that address operands in much the same way as indexed 8-bit offset instructions, except that the 8-bit offset is added to the value of the stack pointer instead of the index register.

The stack pointer, 8-bit offset addressing mode permits easy addressing of data on the stack. The CPU adds the unsigned byte in the 16-bit stack pointer (SP) register to the unsigned byte following the opcode. The sum is the effective address of the operand. If interrupts are disabled, this addressing mode allows the stack pointer to be used as a second "index" register.

Stack pointer relative instructions require a pre-byte for access. Consequently, all SP relative instructions take one cycle longer than their index relative counterparts.

9.3.6.7 SP-Relative, 16-Bit Offset (SP2)

Stack pointer, 16-bit offset instructions are four-byte instructions used to access data relative to the stack pointer with variable addresses at any location in memory. The CPU adds the unsigned contents of the 16-bit stack pointer to the 16-bit unsigned word formed by the two bytes following the opcode. The sum is the effective address of the operand.

As with direct and extended addressing, most assemblers determine the shortest form of stack pointer addressing. Due to the pre-byte, stack pointer relative instructions take one cycle longer than their index relative counterparts.

Stack pointer, 16-bit offset instructions are useful in selecting the k-th element a an n-element table. The table can begin anywhere and can extend anywhere in memory. The k value would typically be in the stack pointer register, and the address of the beginning of the table is located in the two bytes following the two-byte opcode.

9.3.7 Memory to memory Addressing Mode

Memory to memory addressing mode has the following four variations.

9.3.7.1 Direct to Direct

This addressing mode is used to move data within the direct page of memory. Both the source operand and the destination operand are in the direct page. The source data is addressed by the first byte immediately following the opcode, and the destination location is addressed by the second byte following the opcode.

9.3.7.2 Immediate to Direct

This addressing mode is used to move an 8-bit constant to any location in the direct page memory. The source data is the byte immediately following the opcode, and the destination is addressed by the second byte following the opcode.

9.3.7.3 Indexed to Direct, Post Increment

Used only by the MOV instruction, this addressing mode accesses a source operand addressed by the H:X register, and a destination location within the direct page addressed by the byte following the opcode. H:X is incremented after the source operand is accessed.

9.3.7.4 Direct to Indexed, Post-Increment

Used only with the MOV instruction, this addressing mode accesses a source operand addressed by the byte following the opcode, and a destination location addressed by the H:X register. H:X is incremented after the destination operand is written.

9.4 Operation modes

The CPU can be placed into the following operation modes: stop, wait, background and security.

9.4.1 Stop mode

Usually, all system clocks, including the crystal oscillator (when used), are halted during stop mode to minimize power consumption. In such systems, external circuitry is needed to control the time spent in stop mode and to issue a signal to wake up the target MCU when it is time to resume processing. Unlike the earlier M68HC05 and M68HC08 MCUs, the HCS08 V6 can be configured to keep a minimum set of clocks running in stop mode. This optionally allows an internal periodic signal to wake the target MCU from stop mode.

When a host debug system is connected to the background debug pin (BKGD) and the ENBDM control bit has been set by a serial command through the background interface (or because the MCU was reset into active background mode), the oscillator is forced to remain active when the MCU enters stop mode. In this case, if a serial BACKGROUND command is issued to the MCU through the background debug interface while the CPU is in stop mode, CPU clocks will resume and the CPU will enter active background mode where other serial background commands can be processed. This ensures that a host development system can still gain access to a target MCU even if it is in stop mode.

9.4.2 Wait mode

The WAIT instruction enables interrupts by clearing the I bit in the CCR. It then halts the clocks to the CPU to reduce overall power consumption while the CPU is waiting for the interrupt or reset event that will wake the CPU from wait mode. When an interrupt or reset event occurs, the CPU clocks will resume and the interrupt or reset event will be processed normally.

If a serial BACKGROUND command is issued to the MCU through the background debug interface while the CPU is in wait mode, CPU clocks will resume and the CPU will enter active background mode where other serial background commands can be processed. This ensures that a host development system can still gain access to a target MCU even if it is in wait mode.

While in wait mode, there are some restrictions on which background debug commands can be used. Only the BACKGROUND command and memory-access-with-status commands are available while in wait mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the CPU is in either stop or wait mode. The BACKGROUND command can be used to wake the CPU from wait mode and enter active background mode.

9.4.3 Background mode

Background instruction (BGND) is not used in normal user programs because it forces the CPU to stop processing user instructions and enter the active background mode waiting for serial background commands. The only way to resume execution of the user program is through reset or by a host debug system issuing a GO, TRACE1, or TAGGO serial command through the background debug interface.

Software-based breakpoints can be set by replacing an opcode at the desired breakpoint address with the BGND opcode. When the program reaches this breakpoint address, the CPU is forced to active background mode rather than continuing the user program.

The active background mode functions are managed through the background debug controller (BDC) in the HCS08 V6 core. The BDC provides the means for analyzing MCU operation during software development. Active background mode is entered in any of the following ways:

- When the BKGD pin is low at the time the MCU exits reset.
- When a BACKGROUND command is received through the BKGD pin.

- When a BGND instruction is executed.
- When encountering a BDC breakpoint.

Background commands are of two types:

- Non-intrusive commands, defined as commands that can be issued while the user program is running. Non-intrusive commands can be issued through the BKGD pin while the MCU is in run mode; non-intrusive commands can also be executed when the MCU is in the active background mode. Non-intrusive commands include:
  - Memory access commands
  - Memory-access-with-status commands
  - BDC register access commands
  - The BACKGROUND command
- Active background commands, which can be executed only while the MCU is in active background mode. Active background commands include commands to:
  - Read or write CPU registers
  - Trace one user program instruction at a time
  - Leave active background mode to return to the user's application program (GO)

The active background mode is used to program a bootloader or user application program into the flash program memory before the MCU is operated in run mode for the first time. The active background mode can also be used to erase and reprogram the flash memory after it has been previously programmed.

9.4.4 Security mode

Usually HCS08 V6 MCUs are implemented with a secure operating mode. When in secure mode, external access to internal memory is restricted, so that only instructions fetched from secure memory can access secure memory.

The method by which the MCU is put into secure mode is not defined by the HCS08 V6 Core. The core receives an external input signal that, when asserted, informs to the core that the MCU is in secure mode.

While in secure mode, the core controls the following set of conditions:

1. The RAM, flash, and EEPROM arrays are considered secure memory. All registers in Direct Page or High Page are considered non-secure memory.
2. Read data is tagged as either secure or non-secure during a program read, depending on whether the read is from secure or non-secure memory.
3. A data read of secure memory returns a value of $00 when the current instruction is tagged as non-secure or the access is a BDC access.
4. A data write to secure memory is blocked and data at the target address does not change state when the current instruction is tagged as non-secure or the access is through BDC.
5. A data write to secure memory is never blocked during the stacking cycles of interrupt service routines.
6. Data accesses to either secure or non-secure memory are allowed when the current instruction is tagged as secure.
7. BDC accesses to non-secure memory are allowed.

When the device is in the non-secure mode, secure memory is treated the same as non-secure memory, and all accesses are allowed.

Table 9-2 details the security conditions for allowing or disabling a read access.

Table 9-2. Security conditions for read access

Inputs conditions					Read control
Security enabled	Ram, flash or EEPROM access	Program or vector read	Current CPU instruction from secure memory	Current access is via BDC	Read access allowed
0	x	x	x	x	1
1	0	x	x	x	1
1	1	1	x	x	1
1	1	0	1	0	1
1	1	0	1	1	0
1	1	0	0	0	0
1	1	0	0	1	0

9.5 HCS08 V6 Opcodes

The HCS08 V6 Core has 254 one-byte opcodes and 47 two-byte opcodes, totaling 301 opcodes. For a more detailed description of the HCS08 V6 instructions please refer to the Instruction Set Summary section.

9.6 Special Operations

The CPU performs a few special operations that are similar to instructions but do not have opcodes like other CPU instructions. This section provides additional information about these operations.

9.6.1 Reset Sequence

Reset can be caused by a power-on-reset (POR) event, internal conditions such as the COP (computer operating properly) watchdog, or by assertion of an external active-low reset pin. When a reset event occurs, the CPU immediately stops whatever it is doing (the MCU does not wait for an instruction boundary before responding to a reset event).

The reset event is considered concluded when the sequence to determine whether the reset came from an internal source is done and when the reset pin is no longer asserted. At the conclusion of a reset event, the CPU performs a 6-cycle sequence to fetch the reset vector from $FFFE and $FFFF and to fill the instruction queue in preparation for execution of the first program instruction.

9.6.2 Interrupt Sequence

When an interrupt is requested, the CPU completes the current instruction before responding to the interrupt. At this point, the program counter is pointing at the start of the next instruction, which is where the CPU should return after servicing the interrupt. The CPU responds to an interrupt by performing the same sequence of operations as for a software interrupt (SWI) instruction, except the address used for the vector fetch is determined by the highest priority interrupt that is pending when the interrupt sequence started.

The CPU sequence for an interrupt is:

1. Store the contents of PCL, PCH, X, A, and CCR on the stack, in that order.
2. Set the I bit in the CCR.
3. Fetch the high-order half of the interrupt vector.
4. Fetch the low-order half of the interrupt vector.
5. Delay for one free bus cycle.

Fetch three bytes of program information starting at the address indicated by the interrupt vector to fill the instruction queue in preparation for execution of the first instruction in the interrupt service routine.

After the CCR contents are pushed onto the stack, the I bit in the CCR is set to prevent other interrupts while in the interrupt service routine. Although it is possible to clear the I bit with an instruction in the interrupt service routine, this would allow nesting of interrupts (which is not recommended because it leads to programs that are difficult to debug and maintain).

For compatibility with the earlier M68HC05 MCUs, the high-order half of the H:X index register pair (H) is not saved on the stack as part of the interrupt sequence. The user must use a PSHH instruction at the beginning of the service routine to save H and then use a PULH instruction just before the RTI that ends the interrupt service routine. It is not necessary to save H if you are certain that the interrupt service routine does not use any instructions or auto-increment addressing modes that might change the value of H.

The software interrupt (SWI) instruction is like a hardware interrupt except that it is not masked by the global I bit in the CCR and it is associated with an instruction opcode within the program so it is not asynchronous to program execution.

9.7 Instruction Set Summary

Table 9-3. Instruction Set Summary

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
ADC #opr8i	Add with Carry	A ← (A) + (M) + (C)	↕	↕	–	↕	↕	↕	IMM	A9	ii	2
ADC opr8a			↕	↕	–	↕	↕	↕	DIR	B9	dd	3
ADC opr16a			↕	↕	–	↕	↕	↕	EXT	C9	hh ll	4
ADC oprx16,X			↕	↕	–	↕	↕	↕	IX2	D9	ee ff	4
ADC oprx8,X			↕	↕	–	↕	↕	↕	IX1	E9	ff	3
ADC ,X			↕	↕	–	↕	↕	↕	IX	F9		3
ADC oprx16,SP			↕	↕	–	↕	↕	↕	SP2	9ED9	ee ff	5
ADC oprx8,SP			↕	↕	–	↕	↕	↕	SP1	9EE9	ff	4

Table continues on the next page...

Table 9-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
ADD #opr8i	Add without Carry	A ← (A) + (M)	↕	↕	–	↕	↕	↕	IMM	AB	ii	2
ADD opr8a			↕	↕	–	↕	↕	↕	DIR	BB	dd	3
ADD opr16a			↕	↕	–	↕	↕	↕	EXT	CB	hh ll	4
ADD oprx16,X			↕	↕	–	↕	↕	↕	IX2	DB	ee ff	4
ADD oprx8,X			↕	↕	–	↕	↕	↕	IX1	EB	ff	3
ADD ,X			↕	↕	–	↕	↕	↕	IX	FB		3
ADD oprx16,SP			↕	↕	–	↕	↕	↕	SP2	9EDB	ee ff	5
ADD oprx8,SP			↕	↕	–	↕	↕	↕	SP1	9EEB	ff	4
AIS #opr8i	Add Immediate Value (Signed) to Stack Pointer	SP ← (SP) + (M) where M is sign extended to a 16-bit value	–	–	–	–	–	–	IMM	A7	ii	2
AIX #opr8i	Add Immediate Value (Signed) to Index Register (H:X)	H:X ← (H:X) + (M) where M is sign extended to a 16-bit value	–	–	–	–	–	–	IMM	AF	ii	2
AND #opr8i	Logical AND	A ← (A) & (M)	0	–	–	↕	↕	–	IMM	A4	ii	2
AND opr8a			0	–	–	↕	↕	–	DIR	B4	dd	3
AND opr16a			0	–	–	↕	↕	–	EXT	C4	hh ll	4
AND oprx16,X			0	–	–	↕	↕	–	IX2	D4	ee ff	4
AND oprx8,X			0	–	–	↕	↕	–	IX1	E4	ff	3
AND ,X			0	–	–	↕	↕	–	IX	F4		3
AND oprx16,SP			0	–	–	↕	↕	–	SP2	9ED4	ee ff	5
AND oprx8,SP			0	–	–	↕	↕	–	SP1	9EE4	ff	4
ASL opr8a	Arithmetic Shift Left (same as LSL)	C ← MSB, LSB ← 0	↕	–	–	↕	↕	↕	DIR	38	dd	5
ASLA			↕	–	–	↕	↕	↕	INH	48		1
ASLX			↕	–	–	↕	↕	↕	INH	58		1
ASL oprx8,X			↕	–	–	↕	↕	↕	IX1	68	ff	5
ASL ,X			↕	–	–	↕	↕	↕	IX	78		4
ASL oprx8,SP			↕	–	–	↕	↕	↕	SP1	9E68	ff	6
ASR opr8a	Arithmetic Shift Right	MSB → MSB, LSB → C	↕	–	–	↕	↕	↕	DIR	37	dd	5
ASRA			↕	–	–	↕	↕	↕	INH	47		1
ASRX			↕	–	–	↕	↕	↕	INH	57		1
ASR oprx8,X			↕	–	–	↕	↕	↕	IX1	67	ff	5
ASR ,X			↕	–	–	↕	↕	↕	IX	77		4
ASR oprx8,SP			↕	–	–	↕	↕	↕	SP1	9E67	ff	6
BCC rel	Branch if Carry Bit Clear	Branch if (C) = 0	–	–	–	–	–	–	REL	24	rr	3
			–	–	–	–	–	–	DIR (b0)	11	dd	5

Table continues on the next page...

Table 9-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
BCLR n,opr8a	Clear Bit n in Memory	Mn ← 0	–	–	–	–	–	–	DIR (b1)	13	dd	5
			–	–	–	–	–	–	DIR (b2)	15	dd	5
			–	–	–	–	–	–	DIR (b3)	17	dd	5
			–	–	–	–	–	–	DIR (b4)	19	dd	
			–	–	–	–	–	–	DIR (b5)	1B	dd	5
			–	–	–	–	–	–	DIR (b6)	1D	dd	5
			–	–	–	–	–	–	DIR (b7)	1F	dd	5
BCS rel	Branch if Carry Bit Set (same as BLO)	Branch if (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BEQ rel	Branch if Equal	Branch if (Z) = 1	–	–	–	–	–	–	REL	27	rr	3
BGE rel	Branch if Greater Than or Equal To (Signed Operands)	Branch if (N ⊕ V) = 0	–	–	–	–	–	–	REL	90	rr	3
BGND	Enter Active Background if ENBDM = 1	Waits For and Processes BDM Commands Until GO, TRACE1, or TAGGO	–	–	–	–	–	–	INH	82		5+
BGT rel	Branch if Greater Than (Signed Operands)	Branch if (Z) ǀ (N ⊕ V) = 0	–	–	–	–	–	–	REL	92	rr	3
BHCC rel	Branch if Half Carry Bit Clear	Branch if (H) = 0	–	–	–	–	–	–	REL	28	rr	3
BHCS rel	Branch if Half Carry Bit Set	Branch if (H) = 1	–	–	–	–	–	–	REL	29	rr	3
BHI rel	Branch if Higher	Branch if (C) ǀ (Z) = 0	–	–	–	–	–	–	REL	22	rr	3
BHS rel	Branch if Higher or Same (same as BCC)	Branch if (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BIH rel	Branch if IRQ Pin High	Branch if IRQ pin = 1	–	–	–	–	–	–	REL	2F	rr	3
BIL rel	Branch if IRQ Pin Low	Branch if IRQ pin = 0	–	–	–	–	–	–	REL	2E	rr	3
BIT #opr8i	Bit Test	(A) & (M), (CCR Updated but Operands Not Changed)	0	–	–	↕	↕	–	IMM	A5	ii	2
BIT opr8a			0	–	–	↕	↕	–	DIR	B5	dd	3
BIT opr16a			0	–	–	↕	↕	–	EXT	C5	hh ll	4
BIT oprx16,X			0	–	–	↕	↕	–	IX2	D5	ee ff	4
BIT oprx8,X			0	–	–	↕	↕	–	IX1	E5	ff	3
BIT ,X			0	–	–	↕	↕	–	IX	F5		3
BIT oprx16,SP			0	–	–	↕	↕	–	SP2	9ED5	ee ff	5
BIT oprx8,SP			0	–	–	↕	↕	–	SP1	9EE5	ff	4

Table continues on the next page...

Table 9-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
BLE rel	Branch if Less Than or Equal To (Signed Operands)	Branch if (Z) | (N ⊕ V) = 1	–	–	–	–	–	–	REL	93	rr	3
BLO rel	Branch if Lower (Same as BCS)	Branch if (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BLS rel	Branch if Lower or Same	Branch if (C) | (Z) = 1	–	–	–	–	–	–	REL	23	rr	3
BLT rel	Branch if Less Than (Signed Operands)	Branch if (N ⊕ V) = 1	–	–	–	–	–	–	REL	91	rr	3
BMC rel	Branch if Interrupt Mask Clear	Branch if (I) = 0	–	–	–	–	–	–	REL	2C	rr	3
BMI rel	Branch if Minus	Branch if (N) = 1	–	–	–	–	–	–	REL	2B	rr	3
BMS rel	Branch if Interrupt Mask Set	Branch if (I) = 1	–	–	–	–	–	–	REL	2D	rr	3
BNE rel	Branch if Not Equal	Branch if (Z) = 0	–	–	–	–	–	–	REL	26	rr	3
BPL rel	Branch if Plus	Branch if (N) = 0	–	–	–	–	–	–	REL	2A	rr	3
BRA rel	Branch Always	No Test	–	–	–	–	–	–	REL	20	rr	3
BRCLR n,opr8a,rel	Branch if Bit n in Memory Clear	Branch if (Mn) = 0	–	–	–	–	–	↕	DIR (b0)	01	dd rr	5
			–	–	–	–	–	↕	DIR (b1)	03	dd rr	5
			–	–	–	–	–	↕	DIR (b2)	05	dd rr	5
			–	–	–	–	–	↕	DIR (b3)	07	dd rr	5
			–	–	–	–	–	↕	DIR (b4)	09	dd rr	5
			–	–	–	–	–	↕	DIR (b5)	0B	dd rr	5
			–	–	–	–	–	↕	DIR (b6)	0D	dd rr	5
			–	–	–	–	–	↕	DIR (b7)	0F	dd rr	5
BRN rel	Branch Never	Uses 3 Bus Cycles	–	–	–	–	–	–	REL	21	rr	3
BRSET n,opr8a,rel	Branch if Bit n in Memory Set	Branch if (Mn) = 1	–	–	–	–	–	↕	DIR (b0)	00	dd rr	5
			–	–	–	–	–	↕	DIR (b1)	02	dd rr	5
			–	–	–	–	–	↕	DIR (b2)	04	dd rr	5
			–	–	–	–	–	↕	DIR (b3)	06	dd rr	5
			–	–	–	–	–	↕	DIR (b4)	08	dd rr	5
			–	–	–	–	–	↕	DIR (b5)	0A	dd rr	5
			–	–	–	–	–	↕	DIR (b6)	0C	dd rr	5
			–	–	–	–	–	↕	DIR (b7)	0E	dd rr	5
			–	–	–	–	–	–	DIR (b0)	10	dd	5
			–	–	–	–	–	–	DIR (b1)	12	dd	5
			–	–	–	–	–	–	DIR (b2)	14	dd	5

Table continues on the next page...

Table 9-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
BSET n,opr8a	Set Bit n in Memory	Mn ← 1	–	–	–	–	–	–	DIR (b3)	16	dd	5
			–	–	–	–	–	–	DIR (b4)	18	dd	5
			–	–	–	–	–	–	DIR (b5)	1A	dd	5
			–	–	–	–	–	–	DIR (b6)	1C	dd	5
			–	–	–	–	–	–	DIR (b7)	1E	dd	5
BSR rel	Branch to Subroutine	PC ← (PC) + 0x0002 push (PCL) SP ← (SP) – 0x0001 push (PCH) SP ← (SP) – 0x0001 PC ← (PC) + rel	–	–	–	–	–	–	REL	AD	rr	5
CBEQ opr8a,rel	Compare and Branch if Equal	Branch if (A) = (M)	–	–	–	–	–	–	DIR	31	dd rr	5
CBEQA #opr8i,rel		Branch if (A) = (M)	–	–	–	–	–	–	IMM	41	ii rr	4
CBEQX #opr8i,rel		Branch if (X) = (M)	–	–	–	–	–	–	IMM	51	ii rr	4
CBEQ oprx8,X+,rel		Branch if (A) = (M)	–	–	–	–	–	–	IX1+	61	ff rr	5
CBEQ ,X+,rel		Branch if (A) = (M)	–	–	–	–	–	–	IX+	71	rr	5
CBEQ oprx8,SP,rel		Branch if (A) = (M)	–	–	–	–	–	–	SP1	9E61	ff rr	6
CLC	Clear Carry Bit	C ← 0	–	–	–	–	–	0	INH	98		1
CLI	Clear Interrupt Mask Bit	I ← 0	–	–	0	–	–	–	INH	9A		1
CLR opr8a	Clear	M ← 0x00	0	–	–	0	1	–	DIR	3F	dd	5
CLRA		A ← 0x00	0	–	–	0	1	–	INH	4F		1
CLRX		X ← 0x00	0	–	–	0	1	–	INH	5F		1
CLRH		H ← 0x00	0	–	–	0	1	–	INH	8C		1
CLR oprx8,X		M ← 0x00	0	–	–	0	1	–	IX1	6F	ff	5
CLR ,X		M ← 0x00	0	–	–	0	1	–	IX	7F		4
CLR oprx8,SP		M ← 0x00	0	–	–	0	1	–	SP1	9E6F	ff	6
CMP #opr8i	Compare Accumulator with Memory	(A) – (M); (CCR Updated But Operands Not Changed)	↕	–	–	↕	↕	↕	IMM	A1	ii	2
CMP opr8a			↕	–	–	↕	↕	↕	DIR	B1	dd	3
CMP opr16a			↕	–	–	↕	↕	↕	EXT	C1	hh ll	4
CMP oprx16,X			↕	–	–	↕	↕	↕	IX2	D1	ee ff	4
CMP oprx8,X			↕	–	–	↕	↕	↕	IX1	E1	ff	3
CMP ,X			↕	–	–	↕	↕	↕	IX	F1		3
CMP oprx16,SP			↕	–	–	↕	↕	↕	SP2	9ED1	ee ff	5

Table continues on the next page...

Table 9-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
CMP oprx8,SP			↕	–	–	↕	↕	↕	SP1	9EE1	ff	4
COM opr8a	One's Complement	M ← (M) = 0xFF – (M)	0	–	–	↕	↕	1	DIR	33	dd	5
COMA		A ← (A) = 0xFF – (A)	0	–	–	↕	↕	1	INH	43		1
COMX		X ← (X) = 0xFF – (X)	0	–	–	↕	↕	1	INH	53		1
COM oprx8,X		M ← (M) = 0xFF – (M)	0	–	–	↕	↕	1	IX1	63	ff	5
COM ,X		M ← (M) = 0xFF – (M)	0	–	–	↕	↕	1	IX	73		4
COM oprx8,SP		M ← (M) = 0xFF – (M)	0	–	–	↕	↕	1	SP1	9E63	ff	6
CPHX opr16a	Compare Index Register (H:X) with Memory	(H:X) – (M:M + 0x0001); (CCR Updated But Operands Not Changed)	↕	–	–	↕	↕	↕	EXT	3E	hh ll	6
CPHX #opr16i			↕	–	–	↕	↕	↕	IMM	65	jj kk	3
CPHX opr8a			↕	–	–	↕	↕	↕	DIR	75	dd	5
CPHX oprx8,SP			↕	–	–	↕	↕	↕	SP1	9EF3	ff	6
CPX #opr8i	Compare X (Index Register Low) with Memory	(X) – (M); (CCR Updated But Operands Not Changed)	↕	–	–	↕	↕	↕	IMM	A3	ii	2
CPX opr8a			↕	–	–	↕	↕	↕	DIR	B3	dd	3
CPX opr16a			↕	–	–	↕	↕	↕	EXT	C3	hh ll	4
CPX oprx16,X			↕	–	–	↕	↕	↕	IX2	D3	ee ff	4
CPX oprx8,X			↕	–	–	↕	↕	↕	IX1	E3	ff	3
CPX ,X			↕	–	–	↕	↕	↕	IX	F3		3
CPX oprx16,SP			↕	–	–	↕	↕	↕	SP2	9ED3	ee ff	5
CPX oprx8,SP			↕	–	–	↕	↕	↕	SP1	9EE3	ff	4
DAA	Decimal Adjust Accumulator After ADD or ADC of BCD Values	$(A)_{10}$	U	–	–	↕	↕	↕	INH	72		1
DBNZ opr8a,rel	Decrement and Branch if Not Zero	Decrement A, X, or M Branch if (result) ≠ 0 Affects X, Not H	–	–	–	–	–	–	DIR	3B	dd rr	7
DBNZA rel			–	–	–	–	–	–	INH	4B	rr	4
DBNZX rel			–	–	–	–	–	–	INH	5B	rr	4
DBNZ oprx8,X,rel			–	–	–	–	–	–	IX1	6B	ff rr	7
DBNZ ,X,rel			–	–	–	–	–	–	IX	7B	rr	6
DBNZ oprx8,SP,rel			–	–	–	–	–	–	SP1	9E6B	ff rr	8
DEC opr8a		M ← (M) – 0x01	↕	–	–	↕	↕	–	DIR	3A	dd	5
DECA		A ← (A) – 0x01	↕	–	–	↕	↕	–	INH	4A		1
DECX		X ← (X) – 0x01	↕	–	–	↕	↕	–	INH	5A		1

Table continues on the next page...

Table 9-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
DEC oprx8,X	Decrement	M ← (M) – 0x01	↕	–	–	↕	↕	–	IX1	6A	ff	5
DEC ,X		M ← (M) – 0x01	↕	–	–	↕	↕	–	IX	7A		4
DEC oprx8,SP		M ← (M) – 0x01	↕	–	–	↕	↕	–	SP1	9E6A	ff	6
DIV	Divide	A ← (H:A)÷(X), H ← Remainder	–	–	–	–	↕	↕	INH	52		6
EOR #opr8i	Exclusive OR Memory with Accumulator	A ← (A ⊕ M)	0	–	–	↕	↕	–	IMM	A8	ii	2
EOR opr8a			0	–	–	↕	↕	–	DIR	B8	dd	3
EOR opr16a			0	–	–	↕	↕	–	EXT	C8	hh ll	4
EOR oprx16,X			0	–	–	↕	↕	–	IX2	D8	ee ff	4
EOR oprx8,X			0	–	–	↕	↕	–	IX1	E8	ff	3
EOR ,X			0	–	–	↕	↕	–	IX	F8		3
EOR oprx16,SP			0	–	–	↕	↕	–	SP2	9ED8	ee ff	5
EOR oprx8,SP			0	–	–	↕	↕	–	SP1	9EE8	ff	4
INC opr8a	Increment	M ← (M) + 0x01	↕	–	–	↕	↕	–	DIR	3C	dd	5
INCA		A ← (A) + 0x01	↕	–	–	↕	↕	–	INH	4C		1
INCX		X ← (X) + 0x01	↕	–	–	↕	↕	–	INH	5C		1
INC oprx8,X		M ← (M) + 0x01	↕	–	–	↕	↕	–	IX1	6C	ff	5
INC ,X		M ← (M) + 0x01	↕	–	–	↕	↕	–	IX	7C		4
INC oprx8,SP		M ← (M) + 0x01	↕	–	–	↕	↕	–	SP1	9E6C	ff	6
JMP opr8a	Jump	PC ← Jump Address							DIR	BC	dd	3
JMP opr16a									EXT	CC	hh ll	4
JMP oprx16,X			–	–	–	–	–	–	IX2	DC	ee ff	4
JMP oprx8,X									IX1	EC	ff	3
JMP ,X									IX	FC		3
JSR opr8a	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL) SP ← (SP) – 0x0001 Push (PCH) SP ← (SP) – 0x0001 PC ← Unconditional Address	–	–	–	–	–	–	DIR	BD	dd	5
JSR opr16a			–	–	–	–	–	–	EXT	CD	hh ll	6
JSR oprx16,X			–	–	–	–	–	–	IX2	DD	ee ff	6
JSR oprx8,X			–	–	–	–	–	–	IX1	ED	ff	5
JSR ,X			–	–	–	–	–	–	IX	FD		5
LDA #opr8i	Load Accumulator from Memory	A ← (M)	0	–	–	↕	↕	–	IMM	A6	ii	2
LDA opr8a									DIR	B6	dd	3
LDA opr16a									EXT	C6	hh ll	4
LDA oprx16,X									IX2	D6	ee ff	4
LDA oprx8,X									IX1	E6	ff	3

Table continues on the next page...

Table 9-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
LDA ,X									IX	F6		3
LDA oprx16,SP									SP2	9ED6	ee ff	5
LDA oprx8,SP									SP1	9EE6	ff	4
LDHX #opr16i	Load Index Register (H:X) from Memory	H:X ← (M:M + 0x0001)	0	–	–	↕	↕	–	IMM	45	jj kk	3
LDHX opr8a			0	–	–	↕	↕	–	DIR	55	dd	4
LDHX opr16a			0	–	–	↕	↕	–	EXT	32	hh ll	5
LDHX ,X			0	–	–	↕	↕	–	IX	9EAE		5
LDHX oprx16,X			0	–	–	↕	↕	–	IX2	9EBE	ee ff	6
LDHX oprx8,X			0	–	–	↕	↕	–	IX1	9ECE	ff	5
LDHX oprx8,SP			0	–	–	↕	↕	–	SP1	9EFE	ff	5
LDX #opr8i	Load X (Index Register Low) from Memory	X ← (M)	0	–	–	↕	↕	–	IMM	AE	ii	2
LDX opr8a			0	–	–	↕	↕	–	DIR	BE	dd	3
LDX opr16a			0	–	–	↕	↕	–	EXT	CE	hh ll	4
LDX oprx16,X			0	–	–	↕	↕	–	IX2	DE	ee ff	4
LDX oprx8,X			0	–	–	↕	↕	–	IX1	EE	ff	3
LDX ,X			0	–	–	↕	↕	–	IX	FE		3
LDX oprx16,SP			0	–	–	↕	↕	–	SP2	9EDE	ee ff	5
LDX oprx8,SP			0	–	–	↕	↕	–	SP1	9EEE	ff	4
LSL opr8a	Logical Shift Left (Same as ASL)	C ← MSB, LSB ← 0	↕	–	–	↕	↕	↕	DIR	38	dd	5
LSLA			↕	–	–	↕	↕	↕	INH	48		1
LSLX			↕	–	–	↕	↕	↕	INH	58		1
LSL oprx8,X			↕	–	–	↕	↕	↕	IX1	68	ff	5
LSL ,X			↕	–	–	↕	↕	↕	IX	78		4
LSL oprx8,SP			↕	–	–	↕	↕	↕	SP1	9E68	ff	6
LSR opr8a	Logical Shift Right	0 → MSB, LSB → C	↕	–	–	0	↕	↕	DIR	34	dd	5
LSRA			↕	–	–	0	↕	↕	INH	44		1
LSRX			↕	–	–	0	↕	↕	INH	54		1
LSR oprx8,X			↕	–	–	0	↕	↕	IX1	64	ff	5
LSR ,X			↕	–	–	0	↕	↕	IX	74		4
LSR oprx8,SP			↕	–	–	0	↕	↕	SP1	9E64	ff	6
MOV oprx8,opr8a	Move	$(M)_{destination} \leftarrow (M)_{source}$	0	–	–	↕	↕	–	DIR/DIR	4E	dd	5
MOV opr8a,X+			0	–	–	↕	↕	–	DIR/IX+	5E	dd	5

Table continues on the next page...

Table 9-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
MOV #opr8i,opr8a		H:X ← (H:X) + 0x0001 in IX+/DIR and DIR/IX+ Modes	0	–	–	↕	↕	–	IMM/DIR	6E	ii	4
MOV ,X+,opr8a			0	–	–	↕	↕	–	IX+/DIR	7E	dd	5
MUL	Unsigned multiply	X:A ← (X) × (A)	–	0	–	–	–	0	INH	42		5
NEG opr8a	Negate (Two's Complement)	M ← – (M) = 0x00 – (M)	↕	–	–	↕	↕	↕	DIR	30	dd	5
NEGA		A ← – (A) = 0x00 – (A)	↕	–	–	↕	↕	↕	INH	40		1
NEGX		X ← – (X) = 0x00 – (X)	↕	–	–	↕	↕	↕	INH	50		1
NEG oprx8,X		M ← – (M) = 0x00 – (M)	↕	–	–	↕	↕	↕	IX1	60	ff	5
NEG ,X		M ← – (M) = 0x00 – (M)	↕	–	–	↕	↕	↕	IX	70		4
NEG oprx8,SP		M ← – (M) = 0x00 – (M)	↕	–	–	↕	↕	↕	SP1	9E60	ff	6
NOP	No Operation	Uses 1 Bus Cycle	–	–	–	–	–	–	INH	9D		1
NSA	Nibble Swap Accumulator	A ← (A[3:0]:A[7:4])	–	–	–	–	–	–	INH	62		1
ORA #opr8i	Inclusive OR Accumulator and Memory	A ← (A) | (M)	0	–	–	↕	↕	–	IMM	AA	ii	2
ORA opr8a			0	–	–	↕	↕	–	DIR	BA	dd	3
ORA opr16a			0	–	–	↕	↕	–	EXT	CA	hh ll	4
ORA oprx16,X			0	–	–	↕	↕	–	IX2	DA	ee ff	4
ORA oprx8,X			0	–	–	↕	↕	–	IX1	EA	ff	3
ORA ,X			0	–	–	↕	↕	–	IX	FA		3
ORA oprx16,SP			0	–	–	↕	↕	–	SP2	9EDA	ee ff	5
ORA oprx8,SP			0	–	–	↕	↕	–	SP1	9EEA	ff	4
PSHA	Push Accumulator onto Stack	Push (A); SP ← (SP) – 0x0001	–	–	–	–	–	–	INH	87		2
PSHH	Push H (Index Register High) onto Stack	Push (H); SP ← (SP) – 0x0001	–	–	–	–	–	–	INH	8B		2
PSHX	Push X (Index Register Low) onto Stack	Push (X); SP ← (SP) – 0x0001	–	–	–	–	–	–	INH	89		2
PULA	Pull Accumulator from Stack	SP ← (SP + 0x0001); Pull (A)	–	–	–	–	–	–	INH	86		3
PULH	Pull H (Index Register High) from Stack	SP ← (SP + 0x0001); Pull (H)	–	–	–	–	–	–	INH	8A		3
PULX	Pull X (Index Register Low) from Stack	SP ← (SP + 0x0001); Pull (X)	–	–	–	–	–	–	INH	88		3
ROL opr8a			↕	–	–	↕	↕	↕	DIR	39	dd	5
ROLA			↕	–	–	↕	↕	↕	INH	49		1

Table continues on the next page...

Table 9-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
ROLX	Rotate Left through Carry	C ← MSB, LSB ← C	↕	–	–	↕	↕	↕	INH	59		1
ROL oprx8,X			↕	–	–	↕	↕	↕	IX1	69	ff	5
ROL ,X			↕	–	–	↕	↕	↕	IX	79		4
ROL oprx8,SP			↕	–	–	↕	↕	↕	SP1	9E69	ff	6
ROR opr8a	Rotate Right through Carry	LSB → C, C → MSB	↕	–	–	↕	↕	↕	DIR	36	dd	5
RORA			↕	–	–	↕	↕	↕	INH	46		1
RORX			↕	–	–	↕	↕	↕	INH	56		1
ROR oprx8,X			↕	–	–	↕	↕	↕	IX1	66	ff	5
ROR ,X			↕	–	–	↕	↕	↕	IX	76		4
ROR oprx8,SP			↕	–	–	↕	↕	↕	SP1	9E66	ff	6
RSP	Reset Stack Pointer	SP ← 0xFF (High Byte Not Affected)	–	–	–	–	–	–	INH	9C		1
RTI	Return from Interrupt	SP ← (SP) + 0x0001, Pull (CCR) SP ← (SP) + 0x0001, Pull (A) SP ← (SP) + 0x0001, Pull (X) SP ← (SP) + 0x0001, Pull (PCH) SP ← (SP) + 0x0001, Pull (PCL)	↕	↕	↕	↕	↕	↕	INH	80		9
RTS	Return from Subroutine	SP ← SP + 0x0001, Pull (PCH) SP ← SP + 0x0001, Pull (PCL)	–	–	–	–	–	–	INH	81		6
SBC #opr8i	Subtract with Carry	A ← (A) – (M) – (C)	↕	–	–	↕	↕	↕	IMM	A2	ii	2
SBC opr8a			↕	–	–	↕	↕	↕	DIR	B2	dd	3
SBC opr16a			↕	–	–	↕	↕	↕	EXT	C2	hh ll	4
SBC oprx16,X			↕	–	–	↕	↕	↕	IX2	D2	ee ff	4
SBC oprx8,X			↕	–	–	↕	↕	↕	IX1	E2	ff	3
SBC ,X			↕	–	–	↕	↕	↕	IX	F2		3
SBC oprx16,SP			↕	–	–	↕	↕	↕	SP2	9ED2	ee ff	5
SBC oprx8,SP			↕	–	–	↕	↕	↕	SP1	9EE2	ff	4
SEC	Set Carry Bit	C ← 1	–	–	–	–	–	1	INH	99		1
SEI	Set Interrupt Mask Bit	I ← 1	–	–	1	–	–	–	INH	9B		1

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Table 9-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
STA opr8a	Store Accumulator in Memory	M ← (A)	0	–	–	↕	↕	–	DIR	B7	dd	3
STA opr16a			0	–	–	↕	↕	–	EXT	C7	hh ll	4
STA oprx16,X			0	–	–	↕	↕	–	IX2	D7	ee ff	4
STA oprx8,X			0	–	–	↕	↕	–	IX1	E7	ff	3
STA ,X			0	–	–	↕	↕	–	IX	F7		2
STA oprx16,SP			0	–	–	↕	↕	–	SP2	9ED7	ee ff	5
STA oprx8,SP			0	–	–	↕	↕	–	SP1	9EE7	ff	4
STHX opr8a	Store H:X (Index Reg.)	(M:M + 0x0001) ← (H:X)	0	–	–	↕	↕	–	DIR	35	dd	4
STHX opr16a			0	–	–	↕	↕	–	EXT	96	hh ll	5
STHX oprx8,SP			0	–	–	↕	↕	–	SP1	9EFF	ff	5
STOP	Enable Interrupts: Stop Processing. Refer to MCU Documentation.	I bit ← 0; Stop Processing	–	–	0	–	–	–	INH	8E		3+
STX opr8a	Store X (Low 8 Bits of Index Register) in Memory	M ← (X)	0	–	–	↕	↕	–	DIR	BF	dd	3
STX opr16a			0	–	–	↕	↕	–	EXT	CF	hh ll	4
STX oprx16,X			0	–	–	↕	↕	–	IX2	DF	ee ff	4
STX oprx8,X			0	–	–	↕	↕	–	IX1	EF	ff	3
STX ,X			0	–	–	↕	↕	–	IX	FF		2
STX oprx16,SP			0	–	–	↕	↕	–	SP2	9EDF	ee ff	5
STX oprx8,SP			0	–	–	↕	↕	–	SP1	9EEF	ff	4
SUB #opr8i	Subtract	A ← (A) – (M)	↕	–	–	↕	↕	↕	IMM	A0	ii	2
SUB opr8a			↕	–	–	↕	↕	↕	DIR	B0	dd	3
SUB opr16a			↕	–	–	↕	↕	↕	EXT	C0	hh ll	4
SUB oprx16,X			↕	–	–	↕	↕	↕	IX2	D0	ee ff	4
SUB oprx8,X			↕	–	–	↕	↕	↕	IX1	E0	ff	3
SUB ,X			↕	–	–	↕	↕	↕	IX	F0		3
SUB oprx16,SP			↕	–	–	↕	↕	↕	SP2	9ED0	ee ff	5
SUB oprx8,SP			↕	–	–	↕	↕	↕	SP1	9EE0	ff	4
		PC ← (PC) + 0x0001 Push (PCL) SP ← (SP) – 0x0001 Push (PCH) SP ← (SP) – 0x0001, Push (X) SP ← (SP) – 0x0001 Push (A)										

Table continues on the next page...

Table 9-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
SWI	Software Interrupt	SP ← (SP) – 0x0001 Push (CCR) SP ← (SP) – 0x0001 I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	–	–	1	–	–	–	INH	83		11
TAP	Transfer Accumulator to CCR	CCR ← (A)	↕	↕	↕	↕	↕	↕	INH	84		1
TAX	Transfer Accumulator to X (Index Register Low)	X ← (A)	–	–	–	–	–	–	INH	97		1
TPA	Transfer CCR to Accumulator	A ← (CCR)	–	–	–	–	–	–	INH	85		1
TST opr8a	Test for Negative or Zero	(M) – 0x00	0	–	–	↕	↕	–	DIR	3D	dd	4
TSTA		(A) – 0x00	0	–	–	↕	↕	–	INH	4D		1
TSTX		(X) – 0x00	0	–	–	↕	↕	–	INH	5D		1
TST oprx8,X		(M) – 0x00	0	–	–	↕	↕	–	IX1	6D	ff	4
TST ,X		(M) – 0x00	0	–	–	↕	↕	–	IX	7D		3
TST oprx8,SP		(M) – 0x00	0	–	–	↕	↕	–	SP1	9E6D	ff	5
TSX	Transfer SP to Index Register	H:X ← (SP) + 0x0001	–	–	–	–	–	–	INH	95		2
TXA	Transfer X (Index Reg. Low) to Accumulator	A ← (X)	–	–	–	–	–	–	INH	9F		1
TXS	Transfer Index Register to SP	SP ← (H:X) – 0x0001	–	–	–	–	–	–	INH	94		2
WAIT	Enable Interrupts Wait for Interrupt	I bit ← 0, Halt CPU	–	–	0	–	–	–	INH	8F		3+

Chapter 10
Flash Memory Module (FTMRH)

10.1 Introduction

The FTMRH module implements the following:

- Program flash (flash) memory

The flash memory is ideal for single-supply applications allowing for field reprogramming without requiring external high voltage sources for program or erase operations. The flash module includes a memory controller that executes commands to modify flash memory contents. The user interface to the memory controller consists of the indexed Flash Common Command Object (FCCOB) register which is written to with the command, global address, data, and any required command parameters. The memory controller must complete the execution of a command before the FCCOB register can be written to with a new command.

CAUTION

A flash byte or longword must be in the erased state before being programmed. Cumulative programming of bits within a flash byte or longword is not allowed.

The flash memory is read as longwords. Read access time is one bus cycle for longwords. For flash memory, an erased bit reads 1 and a programmed bit reads 0.

10.2 Feature

10.2.1 Flash memory features

The flash memory has the following features:

- 16 KB of flash memory composed of one 16 KB flash block divided into 32 sectors of 512 bytes
- Automated program and erase algorithm with verify

- Fast sector erase and longword program operation
- Flexible protection scheme to prevent accidental programming or erasing of flash memory

10.2.2 Other flash module features

The flash memory module has the following other features:

- No external high-voltage power supply required for flash memory program and erase operations
- Interrupt generation on flash command completion and flash error detection
- Security mechanism to prevent unauthorized access to the flash memory

10.3 Functional description

10.3.1 Modes of operation

The flash memory module provides the normal user mode of operation. The operating mode is determined by module-level inputs and affects the FPROT, FCNFG, and FCLKDIV registers.

10.3.1.1 Wait mode

The flash memory module is not affected if the MCU enters Wait mode. The flash module can recover the MCU from Wait via the CCIF interrupt. See Flash interrupts.

10.3.1.2 Stop mode

If a flash command is active, that is, FSTAT[CCIF] = 0, when the MCU requests Stop mode, the current NVM operation will be completed before the MCU is allowed to enter Stop mode.

10.3.2 Flash block read access

If a flash block is read during execution of a command (while FSTAT[CCIF] = 0), the read operation will return invalid data and it will trigger a illegal access exception in the MCU.

10.3.3 Flash memory map

The MCU places the flash memory as shown in the following table.

Table 10-1. Flash memory addressing

Global address	Flash size	Description
0x0000_C000–0x0000_FFFF	16 KB	Flash block contains flash configuration field.

10.3.4 Flash initialization after system reset

On each system reset, the flash module executes an initialization sequence that establishes initial values for the flash block configuration parameters, the FPROT protection register, and the FOPT and FSEC registers. The initialization routine reverts to built-in default values that leave the module in a fully protected and secured state if errors are encountered during execution of the reset sequence. If an error is detected during the reset sequence, both FSTAT[MGSTAT] bits will be set.

FSTAT[CCIF] is cleared throughout the initialization sequence. The NVM module holds off all CPU access for a portion of the initialization sequence. Flash reads are allowed after the hold is removed. Completion of the initialization sequence is marked by setting FSTAT[CCIF] high, which enables user commands. While FSTAT[CCIF] remains cleared, it is not possible to write on registers FCCOBIX or FCCOB.

If a reset occurs while any flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/block being erased is not guaranteed.

10.3.5 Flash command operations

Flash command operations are used to modify flash memory contents.

The command operations contain three steps:

1. Configure the clock for flash program and erase command operations.
2. Use command write sequence to set flash command parameters and launch execution.
3. Execute valid flash commands according to MCU functional mode and MCU security state.

The figure below shows a general flowchart of the flash command write sequence.

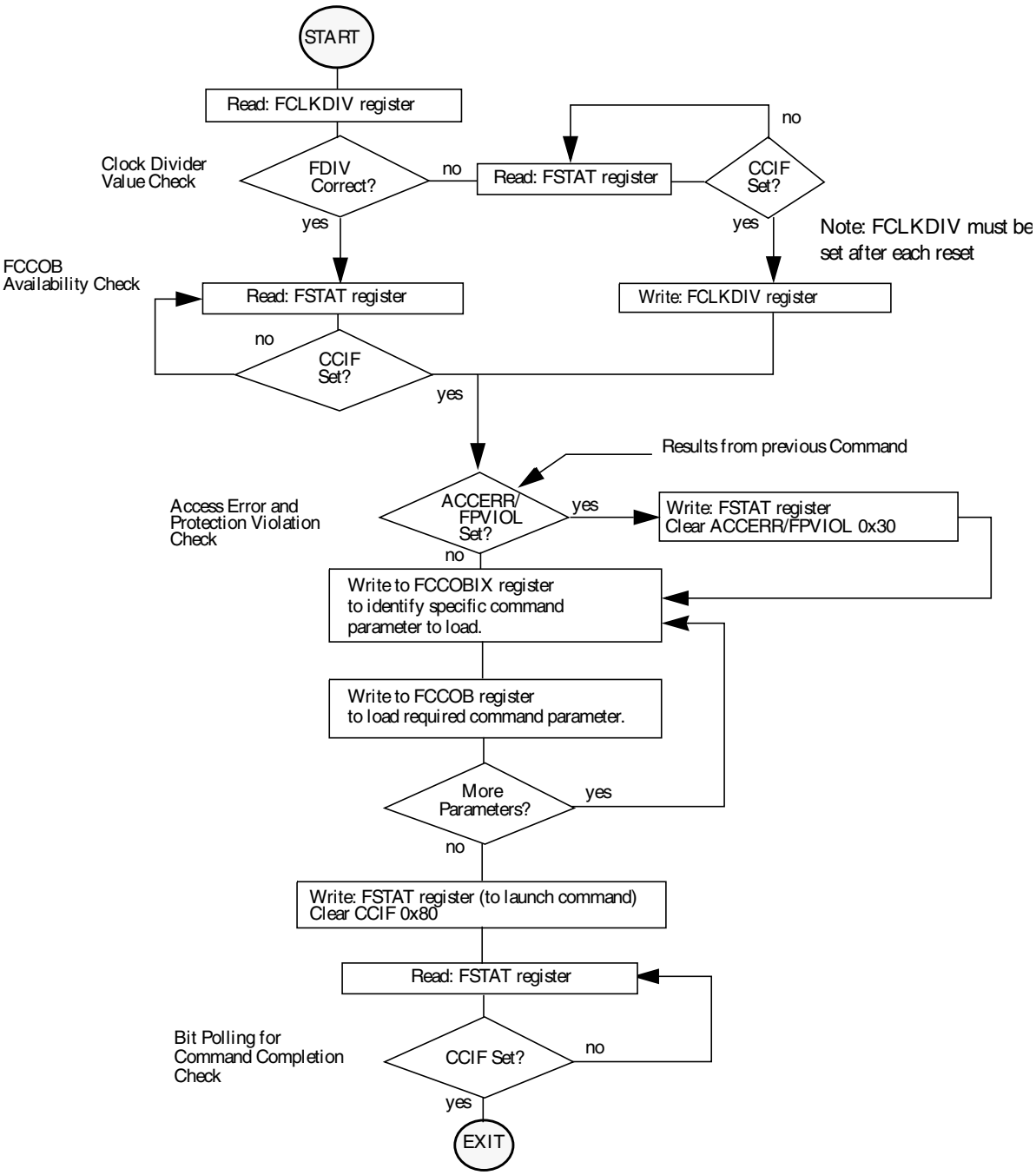


Figure 10-1. Generic flash command write sequence flowchart

10.3.5.1 Writing the FCLKDIV register

Prior to issuing any flash program or erase command after a reset, the user is required to write the FCLKDIV register to divide BUSCLK down to a target FCLK of 1 MHz. The following table shows recommended values for FCLKDIV[FDIV] based on BUSCLK frequency.

Table 10-2. FDIV values for various BUSCLK frequencies

BUSCLK frequency (MHz)		FDIV[5:0]
MIN[1]	MAX[2]	
1.0	1.6	0x00
1.6	2.6	0x01
2.6	3.6	0x02
3.6	4.6	0x03
4.6	5.6	0x04
5.6	6.6	0x05
6.6	7.6	0x06
7.6	8.6	0x07
8.6	9.6	0x08
9.6	10.6	0x09
10.6	11.6	0x0A
11.6	12.6	0x0B
12.6	13.6	0x0C
13.6	14.6	0x0D
14.6	15.6	0x0E
15.6	16.6	0x0F
16.6	17.6	0x10
17.6	18.6	0x11
18.6	19.6	0x12
19.6	20.6	0x13
20.6	21.6	0x14
21.6	22.6	0x15
22.6	23.6	0x16
23.6	24.6	0x17
24.6	25.6	0x18

1. BUSCLK is greater than this value.
2. BUSCLK is less than or equal to this value.

CAUTION

Programming or erasing the flash memory cannot be performed if the bus clock runs at less than 0.8 MHz. Setting FCLKDIV[FDIV] too high can destroy the flash memory due to overstress. Setting FCLKDIV[FDIV] too low can result in incomplete programming or erasure of the flash memory cells.

When the FCLKDIV register is written, FCLKDIV[FDIVLD] is set automatically. If FCLKDIV[FDIVLD] is 0, the FCLKDIV register has not been written since the last reset. If the FCLKDIV register has not been written, any flash program or erase command loaded during a command write sequence will not execute and FSTAT[ACCERR] will be set.

10.3.5.2 Command write sequence

The memory controller will launch all valid flash commands entered using a command write sequence.

Before launching a command, FSTAT[ACCERR] and FSTAT[FPVIOL] must be cleared and the FSTAT[CCIF] flag will be tested to determine the status of the current command write sequence. If FSTAT[CCIF] is 0, indicating that the previous command write sequence is still active, a new command write sequence cannot be started and all writes to the FCCOB register are ignored.

The FCCOB parameter fields must be loaded with all required parameters for the flash command being executed. Access to the FCCOB parameter fields is controlled via FCCOBIX[CCOBIX].

Flash command mode uses the indexed FCCOB register to provide a command code and its relevant parameters to the memory controller. First, the user must set up all required FCCOB fields. Then they can initiate the command's execution by writing a 1 to FSTAT[CCIF]. This action clears the CCIF command completion flag to 0. When the user clears FSTAT[CCIF], all FCCOB parameter fields are locked and cannot be changed by the user until the command completes (evidenced by the memory controller returning FSTAT[CCIF] to1). Some commands return information to the FCCOB register array.

The generic format for the FCCOB parameter fields in flash command mode is shown in the following table. The return values are available for reading after the FSTAT[CCIF] flag has been returned to 1 by the memory controller. Writes to the unimplemented parameter fields, FCCOBIX[CCOBIX] =110b and FCCOBIX[CCOBIX] = 111b, are ignored with read from these fields returning 0x0000.

Table 10-3 shows the generic flash command format. The high byte of the first word in the CCOB array contains the command code, followed by the parameters for this specific flash command. For details on the FCCOB settings required by each command, see the flash command descriptions in Flash command summary .

Table 10-3. FCCOB – flash command mode typical usage

CCOBIX[2:0]	Byte	FCCOB parameter fields in flash command mode
000	HI	FCMD[7:0] defining flash command
	LO	Global address [23:16]
001	HI	Global address [15:8]
	LO	Global address [7:0]
010	HI	Data 0 [15:8]
	LO	Data 0 [7:0]
011	HI	Data 1 [15:8]
	LO	Data 1 [7:0]
100	HI	Data 2 [15:8]
	LO	Data 2 [7:0]
101	HI	Data 3 [15:8]
	LO	Data 3 [7:0]

The contents of the FCCOB parameter fields are transferred to the memory controller when the user clears the FSTAT[CCIF] command completion flag by writing 1. The CCIF flag will remain clear until the flash command has completed. Upon completion, the memory controller will return FSTAT[CCIF] to 1 and the FCCOB register will be used to communicate any results.

The following table presents the valid flash commands, as enabled by the combination of the functional MCU mode with the MCU security state of unsecured or secured.

MCU secured state is selected by FSEC[SEC].

Table 10-4. Flash commands by mode and security state

FCMD	Command	Unsecured	Secured
		U[1]	U[2]
0x01	Erase verify all blocks	*	*
0x02	Erase verify block	*	*
0x03	Erase verify flash section	*	*
0x04	Read once	*	*
0x06	Program flash	*	*
0x07	Program once	*	*
0x08	Erase all block	*	*
0x09	Erase flash block	*	*

Table continues on the next page...

Table 10-4. Flash commands by mode and security state (continued)

FCMD	Command	Unsecured	Secured
		U[1]	U[2]
0x0A	Erase flash sector	*	*
0x0B	Unsecure flash	*	*
0x0C	Verify backdoor access key	*	*
0x0D	Set user margin level	*	*
0x0E	Set factory margin level	*	*

1. Unsecured User mode
2. Secured User mode

10.3.6 Flash interrupts

The flash module can generate an interrupt when a flash command operation has completed.

Table 10-5. Flash interrupt source

Interrupt source	Interrupt flag	Local enable	Global (CCR) mask
Flash command complete	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit

10.3.6.1 Description of flash interrupt operation

The flash module uses the FSTAT[CCIF] flag in combination with the FCNFG[CCIE] interrupt enable bit to generate the flash command interrupt request.

The logic used for generating the flash module interrupts is shown in the following figure.

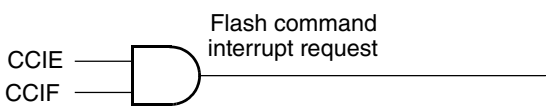


Figure 10-2. Flash module interrupts implementation

10.3.7 Protection

The FPROT register can be set to protect regions in the flash memory from accidental programing or erasing. Two separate memory regions, one growing downward from global address 0x0_FFFF in the flash memory, called the higher region, and the remaining addresses in the flash memory, can be activated for protection. The flash memory addresses covered by these protectable regions are shown in the flash memory map.

Default protection settings as well as security information that allows the MCU to restrict access to the flash module are stored in the flash configuration field as described in the table below.

Table 10-6. Flash configuration field

Global address	Size (Bytes)	Description
0xFF70–0xFF77	8	Backdoor comparison key. See Verify backdoor access key command and Unsecuring the MCU using backdoor key access.
0xFF78–0xFF7B [1]	4	Reserved
0xFF7C[1]	1	Flash protection byte
0xFF7D[1]	1	Reserved
0xFF7E[1]	1	Flash nonvolatile byte
0xFF7F[1]	1	Flash security byte

1. 0x0_FF78-0x0_FF7F form a Flash phrase and must be programmed in a single command write sequence. Each byte in the 0x0_FF78 - 0x0_FF7B reserved field should be programmed to 0xFF.

The flash module provides protection to the MCU. During the reset sequence, the FPROT register is loaded with the contents of the flash protection byte in the flash configuration field at global address FF7C in flash memory. The protection functions depend on the configuration of bit settings in FPROT register.

Table 10-7. Flash protection function

FPOPEN	FPHDIS	Function[1]
1	1	No flash protection
1	0	Protected high range
0	1	Full flash memory protected
0	0	Unprotected high range

1. For range sizes, see Table 4.

The flash protection scheme can be used by applications requiring reprogramming in single chip mode while providing as much protection as possible if reprogramming is not required.

All possible flash protection scenarios are shown in the following figure. Although the protection scheme is loaded from the flash memory at global address 0xFF7C during the reset sequence, it can be changed by the user.

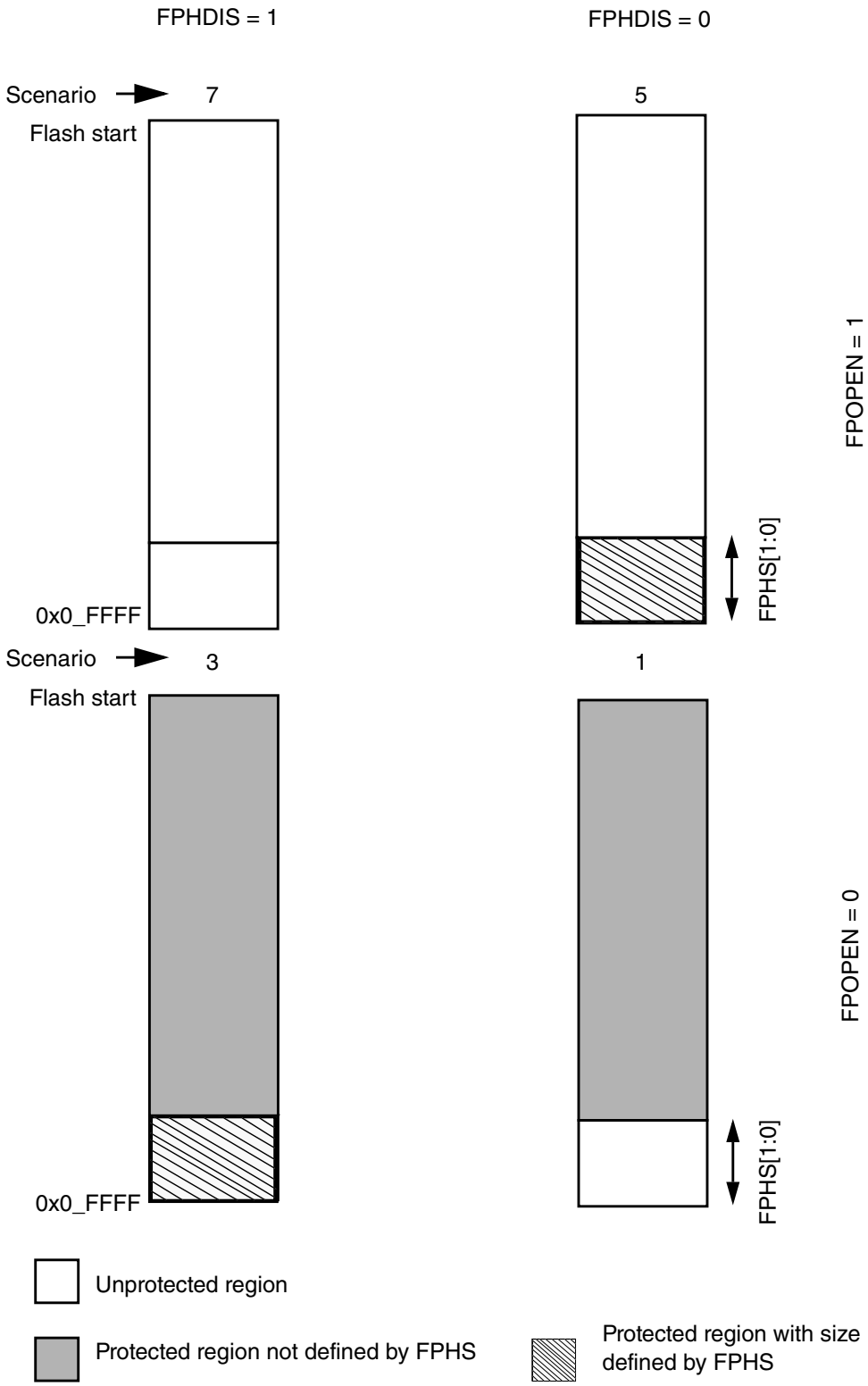


Figure 10-3. Flash protection scenarios

The general guideline is that flash protection can only be added and not removed. The following table specifies all valid transitions between flash protection scenarios. Any attempt to write an invalid scenario to the FPROT register will be ignored. The contents of the FPROT register reflect the active protection scenario. See the FPROT[FPHS] field descriptions for additional restrictions.

Table 10-8. Flash protection scenario transitions

From protection scenario	To protection scenario[1]			
	1	3	5	7
1	×	×		
3		×		
5		×	×	
7	×	×	×	×

1. Allowed transitions marked with X.

The flash protection address range is listed in the following two tables regarding the scenarios in the table above.

Table 10-9. Flash protection higher address range

FPHS[1:0]	Global address range	Protected size
00	0xF800–0xFFFF	2 KB
01	0xF000–0xFFFF	4 KB
10	0xE000–0xFFFF	8 KB
11	0xC000–0xFFFF	16 KB

10.3.8 Security

The flash module provides security information to the MCU. The flash security state is defined by FSEC[SEC]. During reset, the flash module initializes the FSEC register using data read from the security byte of the flash configuration field. The security state out of reset can be permanently changed by programming the security byte, assuming that the MCU is starting from a mode where the necessary flash erase and program commands are available and that the upper region of the flash is unprotected. If the flash security byte is successfully programmed, its new value will take effect after the next MCU reset.

The following subsections describe these security-related subjects:

- Unsecuring the MCU using backdoor key access

- Unsecuring the MCU using BDM
- Mode and security effects on flash command availability

10.3.8.1 Unsecuring the MCU using backdoor key access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys, which are four 16-bit words programmed at addresses 0xFF70–0xFF77. If the KEYEN[1:0] bits are in the enabled state, the verify backdoor access key command – see Verify backdoor access key command, allows the user to present four prospective keys for comparison to the keys stored in the flash memory via the memory controller. If the keys presented in the verify backdoor access key command match the backdoor keys stored in the flash memory, FSEC[SEC] will be changed to unsecure the MCU. Key values of 0x0000 and 0xFFFF are not permitted as backdoor keys. While the Verify Backdoor Access Key command is active, flash memory will not be available for read access and will return invalid data.

The user code stored in the flash memory must have a method of receiving the backdoor keys from an external stimulus. This external stimulus would typically be through one of the on-chip serial ports.

If the KEYEN[1:0] bits are in the enabled state, the MCU can be unsecured by the backdoor key access sequence described below:

1. Follow the command sequence for the verify backdoor access key command as explained in Verify backdoor access key command.
2. If the verify backdoor access key command is successful, the MCU is unsecured and FSEC[SEC] is forced to the unsecure state of 10.

The verify backdoor access key command is monitored by the memory controller and an illegal key will prohibit future use of the verify backdoor access key command. A reset of the MCU is the only method to re-enable the verify backdoor access key command. The security as defined in the flash security byte is not changed by using the verify backdoor access key command sequence. The backdoor keys stored in addresses 0xFF70–0xFF77 are unaffected by the verify backdoor access key command sequence. The verify backdoor access key command sequence has no effect on the program and erase protections defined in the flash protection register, FPROT.

After the backdoor keys have been correctly matched, the MCU will be unsecured. After the MCU is unsecured, the sector containing the flash security byte can be erased and the flash security byte can be reprogrammed to the unsecure state, if desired. In the unsecure state, the user has full control of the contents of the backdoor keys by programming addresses 0xFF70–0xFF77 in the flash configuration field.

10.3.8.2 Unsecuring the MCU using BDM

A secured MCU can be unsecured by using the following method to erase the flash memory:

1. Reset the MCU.
2. Set FCDIV register as described in Writing the FCLKDIV register
3. Configure FPROT register to disable protection in the flash memory.
4. Execute the Erase All Blocks command write sequence to erase the flash memory. Alternatively the Unsecure Flash command can be executed.

   If theflash memory is verified as erased, the MCU will be unsecured. All BDM commands will now be enabled and the flash security byte may be programmed to the unsecure state by continuing with the following steps:
5. Execute the Program Flash command write sequence to program the flash security byte to the unsecured state
6. Reset the MCU

10.3.8.3 Mode and security effects on flash command availability

The availability of flash module commands depends on the MCU operating mode and security state as shown in Table 10-4.

10.3.9 Flash commands

10.3.9.1 Flash commands

The following table summarizes the valid flash commands as well as the effects of the commands on the flash block and other resources within the flash module.

NOTE

All commands in the following table, regardless of MCU mode or security state, cannot be launched while the flash array is

being read (i.e. the commands must not be executed if the core is fetching code from the flash). If the core attempts to read the flash while any command is running that may result in an illegal access. Refer to Flash block read access for details.

Table 10-10. Flash commands

FCMD	Command	Function on flash memory
0x01	Erase Verify All Blocks	Verifies that all flash blocks are erased
0x02	Erase Verify Block	Verifies that a flash block is erased
0x03	Erase Verify Flash Section	Verifies that a given number of words starting at the address provided are erased
0x04	Read Once	Reads a dedicated 64-byte field in the nonvolatile information register in flash block that was previously programmed using the program once command
0x06	Program Flash	Programs up to two longwords in a flash block
0x07	Program Once	Programs a dedicated 64 byte field in the nonvolatile information register in flash block that is allowed to be programmed only once
0x08	Erase All Block	Erases all flash blocks An erase of all flash blocks is possible only when the FPROT[FPHDIS] and FPROT[FPOEN] and the bit are set prior to launching the command
0x09	Erase Flash Block	Erases a flash block An erase of the full flash block is possible only when FPROT[FPHDIS] and FPROT[FPOEN] are set prior to launching the command.
0x0A	Erase Flash Sector	Erases all bytes in a flash sector
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all flash blocks and verifying that all flash blocks are erased
0x0C	Verify Backdoor Access key	Supports a method of releasing MCU security by verifying a set of security keys
0x0D	Set User Margin Level	Specifies a user margin read level for all flash blocks
0x0E	Set Factory Margin Level	Specifies a factory margin read level for all flash blocks

10.3.10 Flash command summary

This section provides details of all available flash commands launched by a command write sequence. The FSTAT[ACCERR] will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the memory controller:

- Starting any command write sequence that programs or erases flash memory before initializing the FLCKDIV register.
- Writing an invalid command as part of the command write sequence.
- For additional possible errors, refer to the error handling table provided for each command.

If a flash block is read during the execution of an algorithm (FSTAT[CCIF] = 0) on that same block, the read operation will return invalid data.

If FSTAT[ACCERR] or FSTAT[FPVIOL] are set, the user must clear these fields before starting any command write sequence.

CAUTION

An flash longword must be in the erased state before being programmed. Cumulative programming of bits within an flash longword is not allowed.

10.3.10.1 Erase Verify All Blocks command

The Erase Verify All Blocks command will verify that all flash blocks have been erased.

Table 10-11. Erase Verify All Blocks command FCCOB requirements

CCOBIX[2:0]	FCCOBHI parameters	FCCOBLO parameters
000	0x01	Not required

Upon clearing FSTAT[CCIF] to launch the Erase Verify All Blocks command, the memory controller will verify that the entire flash memory space is erased. The FSTAT[CCIF] flag will set after the erase verify all blocks operation has completed. If all blocks are not erased, it means blank check failed and both FSTAT[MGSTAT] bits will be set.

Table 10-12. Erase verify all blocks command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[1] or if blank check failed
	MGSTAT0	Set if any errors have been encountered during the read or if blank check failed

1. As found in the memory map for NVM

10.3.10.2 Erase Verify Block command

The Erase Verify Block command allows the user to verify that an entire flash block has been erased. The FCCOB global address [23:0] bits determine which block must be verified.

Table 10-13. Erase Verify Block Command FCCOB requirements

CCOBIX[2:0]	FCCOBHI parameters	FCCOBLO parameters
000	0x02	Global address [23:16] to identify flash block
001	Global address [15:0] in flash block to be verified	

Upon clearing FSTAT[CCIF] to launch the erase verify block command, the memory controller will verify that the selected flash block is erased. The FSTAT[CCIF] flag will set after the erase verify block operation has completed. If the block is not erased, it means blank check failed and both FSTAT[MGSTAT] bits will be set.

Table 10-14. Erase Verify Block command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if an invalid global address [23:0] is supplied[1]
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed
	MGSTAT0	Set if any errors have been encountered during the read or if blank check failed

1. As found in the memory map for NVM

10.3.10.3 Erase Verify Flash Section command

The Erase Verify Flash Section command will verify that a section of code in the flash memory is erased. The Erase Verify Flash Section command defines the starting point of the code to be verified and the number of longwords.

Table 10-15. Erase verify flash section command FCCOB requirements

CCOBIX[2:0]	FCCOBHI parameters	FCCOBLO parameters
000	0x03	Global address [23:16] of flash block
001	Global address [15:0] of the first longwords to be verified	
010	Number of long words to be verified	

Upon clearing FSTAT[CCIF] to launch the erase verify flash section command, the memory controller will verify that the selected section of flash memory is erased. The FSTAT[CCIF] flag will set after the erase verify flash section operation has completed. If the section is not erased, it means blank check failed and both FSTAT[MGSTAT] bits will be set.

Table 10-16. Erase Verify Flash Section command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 10-4)
		Set if an invalid global address [23:0] is supplied (see Table 10-1)[1]
		Set if a misaligned long words address is supplied (global address[1:0] != 00)
		Set if the requested section crosses flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[2] or if blank check failed
	MGSTAT0	Set if any errors have been encountered during the read[2] or if blank check failed

1. As defined by the memory map for NVM
2. As found in the memory map for NVM

10.3.10.4 Read once command

The read once command provides read access to a reserved 64-byte field (8 phrase) located in the nonvolatile information register of flash. The read once field can only be programmed once and can not be erased. It can be used to store the product ID or any other information that can be written only once. It is programmed using the program once command described in Program Once command. To avoid code runaway, the read once command must not be executed from the flash block containing the program once reserved field.

Table 10-17. Read Once command FCCOB requirements

CCOBIX[2:0]	FCCOB parameters	
000	0x04	Not required
001	Read once phrase index (0x0000 – 0x0007)	
010	Read once word 0 value	
011	Read once word 1 value	
100	Read once word 2 value	
101	Read once word 3 value	

Upon clearing FSTAT[CCIF] to launch the read once command, a read once phrase is fetched and stored in the FCCOB indexed register. The FSTAT[CCIF] flag will set after the read once operation has completed. Valid phrase index values for the read once command range from 0x0000 to 0x0007. During execution of the read once command, any attempt to read addresses within flash block will return invalid data.

Table 10-18. Read Once command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command is not available in current mode (see Table 10-4)
		Set if an invalid phrase index is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any errors have been encountered during the read

10.3.10.5 Program Flash command

The program flash operation will program up to two previously erased longwords in the flash memory using an embedded algorithm.

Note

A flash longword must be in the erased state before being programmed. Cumulative programming of bits within a flash longword is not allowed.

Table 10-19. Program Flash command FCCOB requirements

CCOBIX[2:0]	FCCOBHI parameters	FCCOBLO parameters
000	0x06	Global address [23:16] to identify flash block
001	Global address [15:0] of longwords location to be programmed[1]	
010	Word 0 (longword 0) program value	
011	Word 1 (longword 0) program value	
100	Word 2 (longword 1) program value	
101	Word 3 (longword 1) program value	

1. Global address [1:0] must be 00.

Upon clearing FSTAT[CCIF] to launch the Program Flash command, the memory controller will program the data longwords to the supplied global address and will then proceed to verify the data longwords read back as expected. The FSTAT[CCIF] flag will set after the program flash operation has completed.

Table 10-20. Program Flash command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] ≠ 011 or 101 at command launch
		Set if command not available in current mode (see Table 10-4)
		Set if an invalid global address [23:0] is supplied (see Table 10-1.[1]

Table continues on the next page...

Table 10-20. Program Flash command error handling (continued)

Register	Error bit	Error condition
		Set if a misaligned longword address is supplied (global address [1:0] != 00)
		Set if the requested group of words breaches the end of the flash block.
	FPVIOL	Set if the global address [23:0] points to a protected data
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any errors have been encountered during the verify operation

1. As defined by the memory map of NVM.

10.3.10.6 Program Once command

The Program Once command restricts programming to a reserved 64-byte field (8 phrases) in the nonvolatile information register located in flash. The program once reserved field can be read using the read once command as described in Read once command. The program once command must be issued only once because the nonvolatile information register in flash cannot be erased. To avoid code runaway, the program once command must not be executed from the flash block containing the program once reserved field.

Table 10-21. Program Once command FCCOB requirements

CCOBIX[2:0]	FCCOB parameters	
000	0x07	Not required
001	Program Once phrase index (0x000 – 0x0007)	
010	Program once Word 0 value	
011	Program once Word 1value	
100	Program once Word 2 value	
101	Program once Word 3 value	

Upon clearing FSTAT[CCIF] to launch the program once command, the memory controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The FSTAT[CCIF] flag will remain clear, setting only after the program once operation has completed.

The reserved nonvolatile information register accessed by the Program Once command cannot be erased, and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the program once command range from 0x0000 to 0x0007. During execution of the program once command, any attempt to read addresses within flash will return invalid data.

Table 10-22. Program Once ommand error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 10-4)
		Set if an invalid phrase index is supplied
		Set if the requested phrase has already been programmed[1]
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any errors have been encountered during the verify operation

1. If a program once phrase is initially programmed to 0xFFFF_FFFF_FFFF_FFFF, the program once command will be allowed to execute again on that same phrase.

10.3.10.7 Erase All Blocks command

The Erase All Blocks operation will erase the entire flash memory space.

Table 10-23. Erase All Blocks command FCCOB requirements

CCOBIX[2:0]	FCCOBHI parameters	FCCOBLO parameters
000	0x08	Not required

Upon clearing FSTAT[CCIF] to launch the Erase All Blocks command, the memory controller will erase the entire NVM memory space and verify that it is erased. If the memory controller verifies that the entire NVM memory space was properly erased, security will be released. Therefore, the device is in unsecured state. During the execution of this command (FSTAT[CCIF] = 0) the user must not write to any NVM module register. The FSTAT[CCIF] flag will set after the erase all blocks operation has completed.

Table 10-24. Erase All Blocks command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] ≠ 000 at command launch
		Set if command not available in current mode (see Table 10-4)
	FPVIOL	Set if any area of the flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[1]
	MGSTAT0	Set if any errors have been encountered during the verify operation[1]

1. As found in the memory map for NVM.

10.3.10.8 Erase flash block command

The erase flash block operation will erase all addresses in a flash block.

Table 10-25. Erase flash block command FCCOB requirements

CCOBIX[2:0]	FCCOB parameters	
000	0x09	Global address [23:16] to identify flash block
001	Global address[15:0] in flash block to be erased	

Upon clearing FSTAT[CCIF] to launch the erase flash block command, the memory controller will erase the selected flash block and verify that it is erased. The FSTAT[CCIF] flag will set after the erase flash block operation has completed.

Table 10-26. Erase flash block command error handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 10-4)
		Set if an invalid global address [23:0] is supplied[1]
	FPVIOL	Set if an area of the selected flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[2]
	MGSTAT0	Set if any errors have been encountered during the verify operation[2]

1. As defined by the memory map for NVM.
2. As found in the memory map for NVM.

10.3.10.9 Erase flash sector command

The erase flash sector operation will erase all addresses in a flash sector.

Table 10-27. Erase flash sector command FCCOB requirements

CCOBIX[2:0]	FCCOB parameters	
000	0x0A	Global address [23:16] to identify flash block to be erased
001	Global address [15:0] anywhere within the sector to be erased. Refer to Overview for the flash sector size	

Upon clearing FSTAT[CCIF] to launch the erase flash sector command, the memory controller will erase the selected flash sector and then verify that it is erased. The FSTAT[CCIF] flag will be set after the erase flash sector operation has completed.

Table 10-28. Erase flash sector command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 10-4)
		Set if an invalid global address [23:0] is supplied.[1] (see Table 10-1)
		Set if a misaligned longword address is supplied (global address [1:0] != 00)
	FPVIOL	Set if the selected flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any errors have been encountered during the verify operation

1. As defined by the memory map for NVM

10.3.10.10 Unsecure flash command

The unsecure flash command will erase the entire flash memory space, and if the erase is successful, will release security.

Table 10-29. Unsecure flash command FCCOB requirements

CCOBIX[2:0]	FCCOB parameters	
000	0x0B	Not required

Upon clearing FSTAT[CCIF] to launch the unsecure flash command, the memory controller will erase the entire flash memory space and verify that it is erased. If the memory controller verifies that the entire flash memory space was properly erased, security will be released. If the erase verify is not successful, the unsecure flash operation sets FSTAT[MGSTAT1] and terminates without changing the security state. During the execution of this command (FSTAT[CCIF] = 0), the user must not write to any flash module register. The FSTAT[CCIF] flag is set after the unsecure flash operation has completed.

Table 10-30. Unsecure flash command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command is not available in current mode (see Table 10-4)
	FPVIOL	Set if any area of the flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[1]
	MGSTAT0	Set if any errors have been encountered during the verify operation[1]

1. As found in the memory map for NVM

10.3.10.11 Verify backdoor access key command

The verify backdoor access key command will execute only if it is enabled by the FSEC[KEYEN] bits. The verify backdoor access key command releases security if user-supplied keys match those stored in the flash security bytes of the flash configuration field. See Table 10-1 for details. The code that performs verifying backdoor access command must be running from RAM.

Table 10-31. Verify backdoor access key command FCCOB requirements

CCOBIX[2:0]	FCCOBHI parameters	FCCOBLO parameters
000	0x0C	Not required
001	Key 0	
010	Key 1	
011	Key 2	
100	Key 3	

Upon clearing FSTAT[CCIF] to launch the verify backdoor access key command, the memory controller will check the FSEC[KEYEN] bits to verify that this command is enabled. If not enabled, the memory controller sets the FSTAT[ACCERR] bit. If the command is enabled, the memory controller compares the key provided in FCCOB to the backdoor comparison key in the flash configuration field with Key 0 compared to 0x0400, and so on. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the verify backdoor access key command are aborted (set FSTAT[ACCERR]) until a reset occurs. The FSTAT[CCIF] flag is set after the verify backdoor access key operation has completed.

Table 10-32. Verify backdoor access key command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] ≠ 100 at command launch
		Set if an incorrect backdoor key is supplied
		Set if backdoor key access has not been enabled (KEYEN[1:0] ≠ 10
		Set if the backdoor key has mismatched since the last reset
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

10.3.10.12 Set user margin level command

The user margin is a small delta to the normal read reference level and, in effect, is a minimum safety margin. That is, if the reads pass at the tighter tolerances of the user margins, the normal reads have at least that much safety margin before users experience data loss.

The set user margin level command causes the memory controller to set the margin level for future read operations of the flash block.

Table 10-33. Set user margin level command FCCOB requirements

CCOBIX[2:0]	FCCOBHI parameters	FCCOBLO parameters
000	0x0D	Global address [23:16] to identify flash block
001	Global address [15:0] to identify flash block	
010	Margin level setting	

Upon clearing FSTAT[CCIF] to launch the set user margin level command, the memory controller will set the user margin level for the targeted block and then set the FSTAT[CCIF] flag.

Note

Valid margin level settings for the set user margin level command are defined in the following tables.

Table 10-34. Valid set user margin level settings

CCOB (CCOBIX = 010)	Level description
0x0000	Return to normal level
0x0001	User margin-1 level[1]
0x0002	User margin-0 level[2]

1. Read margin to the erased state
2. Read margin to the programmed state

Table 10-35. Set user margin level command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command is not available in current mode (see Table 10-4)
		Set if an invalid global address [23:0] is supplied
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

Note

User margin levels can be used to check that NVM memory contents have adequate margin for normal level read operations. If unexpected results are encountered when checking NVM memory contents at user margin levels, a potential loss of information has been detected.

10.3.10.13 Set factory margin level command

The set factory margin Level command causes the memory controller to set the margin level specified for future read operations of the flash block.

Table 10-36. Set factory margin level command FCCOB requirements

CCOBIX[2:0]	FCCOBHI parameters	FCCOBLO parameters
000	0x0E	Global address [23:16] to identify flash block
001	Global address [15:0] to identify flash block	
010	Margin level setting	

Upon clearing FSTAT[CCIF] to launch the set factory margin level command, the memory controller will set the factory margin level for the targeted block and then set the FSTAT[CCIF] flag.

Note

Valid margin level settings for the set factory margin level command are defined in the following tables.

Table 10-37. Valid set factory margin level settings

CCOB (CCOBIX = 010)	Level description
0x0000	Return to normal level
0x0001	User margin-1 level[1]
0x0002	User margin-0 level[2]
0x0003	Factory margin-1 level[1]
0x0004	Factory margin-0 level[2]

1. Read margin to the erased state
2. Read margin to the programmed state

Table 10-38. Set factory margin level command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command is not available in current mode (see Table 10-4)
		Set if an invalid global address [23:0] is supplied
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

CAUTION

Factory margin levels must only be used during verify of the initial factory programming.

Note

Factory margin levels can be used to check that Flash memory contents have adequate margin for data retention at the normal level setting. If unexpected results are encountered when checking flash memory contents at factory margin levels, the fash memory contents must be erased and reprogrammed.

10.4 Memory map and register definition

This section presents a high-level summary of the registers and how they are mapped. The registers can be accessed in 32-bits, 16-bits (aligned on data[31:16] or on data[15:0]) or 8-bits. In the case of the writable registers, the write accesses are forbidden during flash command execution. For more details, see Caution note in Flash memory map.

FTMRH memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3020	Flash Clock Divider Register (FTMRH_FCLKDIV)	8	R/W	00h	10.4.1/167
3021	Flash Security Register (FTMRH_FSEC)	8	R	Undefined	10.4.2/168
3022	Flash CCOB Index Register (FTMRH_FCCOBIX)	8	R/W	00h	10.4.3/169
3024	Flash Configuration Register (FTMRH_FCNFG)	8	R/W	00h	10.4.4/169
3026	Flash Status Register (FTMRH_FSTAT)	8	R/W	80h	10.4.5/170
3028	Flash Protection Register (FTMRH_FPROT)	8	R/W	See section	10.4.6/171
302A	Flash Common Command Object Register:High (FTMRH_FCCOBHI)	8	R/W	00h	10.4.7/172

Table continues on the next page...

FTMRH memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
302B	Flash Common Command Object Register: Low (FTMRH_FCCOBLO)	8	R/W	00h	10.4.8/173
302C	Flash Option Register (FTMRH_FOPT)	8	R/W	Undefined	10.4.9/173

10.4.1 Flash Clock Divider Register (FTMRH_FCLKDIV)

The FCLKDIV register is used to control timed events in program and erase algorithms.

All bits in the FCLKDIV register are readable, bit 7 is not writable, bit 6 is write-once-high and controls the writability of the FDIV field in user mode. In BDM mode, bits 6-0 are writable any number of times but bit 7 remains unwritable.

NOTE

The FCLKDIV register must not be written while a flash command is executing (FSTAT[CCIF] = 0)

Address: 3020h base + 0h offset = 3020h

Bit	7	6	5	4	3	2	1	0
Read	FDIVLD	FDIVLCK	FDIV					
Write								
Reset	0	0	0	0	0	0	0	0

FTMRH_FCLKDIV field descriptions

Field	Description
7 FDIVLD	Clock Divider Loaded 0 FCLKDIV register has not been written since the last reset. 1 FCLKDIV register has been written since the last reset.
6 FDIVLCK	Clock Divider Locked 0 FDIV field is open for writing. 1 FDIV value is locked and cannot be changed. After the lock bit is set high, only reset can clear this bit and restore writability to the FDIV field in user mode.
FDIV	Clock Divider Bits FDIV[5:0] must be set to effectively divide BUSCLK down to 1MHz to control timed events during flash program and erase algorithms. Refer to the table in the Writing the FCLKDIV register for the recommended values of FDIV based on the BUSCLK frequency.

10.4.2 Flash Security Register (FTMRH_FSEC)

The FSEC register holds all bits associated with the security of the MCU and NVM module. All fields in the FSEC register are readable but not writable. During the reset sequence, the FSEC register is loaded with the contents of the flash security byte in the flash configuration field located in flash memory.

See Security for security function.

Address: 3020h base + 1h offset = 3021h

Bit	7	6	5	4	3	2	1	0
Read	KEYEN		Reserved				SEC	
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

FTMRH_FSEC field descriptions

Field	Description
7–6 KEYEN	Backdoor Key Security Enable Bits The KEYEN[1:0] bits define the enabling of backdoor key access to the flash module. **NOTE:** 01 is the preferred KEYEN state to disable backdoor key access. 00 Disabled 01 Disabled 10 Enabled 11 Disabled
5–2 Reserved	This field is reserved.
SEC	Flash Security Bits Defines the security state of the MCU. If the flash module is unsecured using backdoor key access, the SEC field is forced to 10. **NOTE:** 01 is the preferred SEC state to set MCU to secured state. 00 Secured 01 Secured 10 Unsecured 11 Secured

10.4.3 Flash CCOB Index Register (FTMRH_FCCOBIX)

The FCCOBIX register is used to index the FCCOB register for NVM memory operations.

Address: 3020h base + 2h offset = 3022h

Bit	7	6	5	4	3	2	1	0
Read	0					CCOBIX		
Write								
Reset	0	0	0	0	0	0	0	0

FTMRH_FCCOBIX field descriptions

Field	Description
7–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CCOBIX	Common Command Register Index Selects which word of the FCCOB register array is being read or written to.

10.4.4 Flash Configuration Register (FTMRH_FCNFG)

The FCNFG register enables the flash command complete interrupt.

Address: 3020h base + 4h offset = 3024h

Bit	7	6	5	4	3	2	1	0
Read	CCIE	0			0			
Write								
Reset	0	0	0	0	0	0	0	0

FTMRH_FCNFG field descriptions

Field	Description
7 CCIE	Command Complete Interrupt Enable Controls interrupt generation when a flash command has completed. 0 Command complete interrupt is disabled. 1 An interrupt will be requested whenever the CCIF flag in the FSTAT register is set.
6–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

10.4.5 Flash Status Register (FTMRH_FSTAT)

The FSTAT register reports the operational status of the flash module.

Address: 3020h base + 6h offset = 3026h

Bit	7	6	5	4	3	2	1	0
Read	CCIF	0	ACCERR	FPVIOL	MGBUSY	0	MGSTAT	
Write								
Reset	1	0	0	0	0	0	0	0

FTMRH_FSTAT field descriptions

Field	Description
7 CCIF	Command Complete Interrupt Flag Indicates that a flash command has completed. The CCIF flag is cleared by writing a 1 to CCIF to launch a command and CCIF will stay low until command completion or command violation. 0 Flash command is in progress. 1 Flash command has completed.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 ACCERR	Flash Access Error Flag Indicates an illegal access has occurred to the flash memory caused by either a violation of the command write sequence or issuing an illegal flash command. While ACCERR is set, the CCIF flag cannot be cleared to launch a command. Writing 1 to this field clears it while writing a 0 to this field has no effect. 0 No access error is detected. 1 Access error is detected.
4 FPVIOL	Flash Protection Violation Flag Indicates an attempt was made to program or erase an address in a protected area of flash memory during a command write sequence. Writing 1 to FPVIOL clears this field while writing 0 to this field has no effect. While FPIOL is set, it is not possible to launch a command or start a command write sequence. 0 No protection violation is detected. 1 Protection violation is detected.
3 MGBUSY	Memory Controller Busy Flag Reflects the active state of the memory controller. 0 Memory controller is idle. 1 Memory controller is busy executing a flash command (CCIF = 0).
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
MGSTAT	Memory Controller Command Completion Status Flag

Table continues on the next page...

FTMRH_FSTAT field descriptions (continued)

Field	Description
	One or more MGSTAT flag bits are set if an error is detected during execution of a flash command or during the flash reset sequence. **NOTE:** Reset value can deviate from the value shown if a double bit fault is detected during the reset sequence.

10.4.6 Flash Protection Register (FTMRH_FPROT)

The FPROT register defines which flash sectors are protected against program and erase operations.

The unreserved bits of the FPROT register are writable with the restriction that the size of the protected region can only be increased (see Protection). All the unreserved bits of the FPROT register are writable without restriction in active Background Debug Mode (BDM).

During the reset sequence, the FPROT register is loaded with the contents of the flash protection byte in the flash configuration field at global address 0x40D located in flash memory. To change the flash protection that will be loaded during the reset sequence, the upper sector of the flash memory must be unprotected, then the flash protection byte must be reprogrammed.

Trying to alter data in any protected area in the flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. The block erase of a flash block is not possible if any of the flash sectors contained in the same flash block are protected.

Address: 3020h base + 8h offset = 3028h

Bit	7	6	5	4	3	2	1	0
Read	FPOPEN	RNV6	FPHDIS	FPHS		RNV		
Write								
Reset	x*	x*	x*	x*	x*	0	0	0

FTMRH_FPROT field descriptions

Field	Description
7 FPOPEN	Flash Protection Operation Enable The FPOPEN bit determines the protection function for program or erase operations. 0 When FPOPEN is clear, the FPHDIS fields defines unprotected address ranges as specified by the corresponding FPHS field. 1 When FPOPEN is set, the FPHDIS fields enables protection for the address range specified by the corresponding FPHS field.

Table continues on the next page...

FTMRH_FPROT field descriptions (continued)

Field	Description
6 RNV6	Reserved Nonvolatile Bit The RNV bit must remain in the erased state.
5 FPHDIS	Flash Protection Higher Address Range Disable The FPHDIS bit determines whether there is a protected/unprotected area in a specific region of the flash memory ending with global address 0x7FFF. 0 Protection/Unprotection enabled. 1 Protection/Unprotection disabled.
4–3 FPHS	Flash Protection Higher Address Size The FPHS bits determine the size of the protected/unprotected area in flash memory. The FPHS bits can be written to only while the FPHDIS bit is set.
RNV	Reserved Nonvolatile Bit The RNV bit must remain in the erased state.

10.4.7 Flash Common Command Object Register:High (FTMRH_FCCOBHI)

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte-wide reads and writes are allowed to the FCCOB register.

Address: 3020h base + Ah offset = 302Ah

Bit	7	6	5	4	3	2	1	0
Read Write	CCOB							
Reset	0	0	0	0	0	0	0	0

FTMRH_FCCOBHI field descriptions

Field	Description
CCOB	Common Command Object Bit 15:8 High 8 bits of Common Command Object register

10.4.8 Flash Common Command Object Register: Low (FTMRH_FCCOBLO)

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte-wide reads and writes are allowed to the FCCOB register.

Address: 3020h base + Bh offset = 302Bh

Bit	7	6	5	4	3	2	1	0
Read Write	CCOB							
Reset	0	0	0	0	0	0	0	0

FTMRH_FCCOBLO field descriptions

Field	Description
CCOB	Common Command Object Bit 7:0 Low 8 bits of Common Command Object register

10.4.9 Flash Option Register (FTMRH_FOPT)

The FOPT register is the flash option register.

In active Background Debug Mode (BDM), all bits in the FOPT register are readable and writable. In other modes, all bits in the FOPT register are readable but not writable.

During the reset sequence, the FOPT register is loaded from the flash nonvolatile byte in the flash configuration field at global address 0x040F located in flash memory as indicated by reset condition.

Address: 3020h base + Ch offset = 302Ch

Bit	7	6	5	4	3	2	1	0
Read Write	NV							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

FTMRH_FOPT field descriptions

Field	Description
NV	Nonvolatile Bits The NV[7:0] bits are available as nonvolatile bits. During the reset sequence, the FOPT register is loaded from the flash nonvolatile byte in the flash configuration field at global address 0x40F located in flash memory.

Chapter 11
Port Control (PORT)

11.1 Introduction

This device has three sets of I/O ports, which include up to 18 general-purpose I/O pins.

Not all pins are available on all devices. See Table 3-1 to determine which functions are available for a specific device.

Many of the I/O pins are shared with on-chip peripheral functions, as shown in Table 3-1 . The peripheral modules have priority over the I/O, so when a peripheral is enabled, the associated I/O functions are disabled.

After reset, the shared peripheral functions are disabled so that the pins are controlled by the parallel I/O except PTA4 and PTA5 that are default to BKGD/MS and $\overline{\text{RESET}}$ function. All of the parallel I/O are configured as high-impedance (Hi-Z). The pin control functions for each pin are configured as follows:

- input disabled (PTxIEn = 0),
- output disabled (PTxOEn = 0), and
- internal pullups disabled (PTxPEn = 0).

The following figures show the structures of each I/O pin.

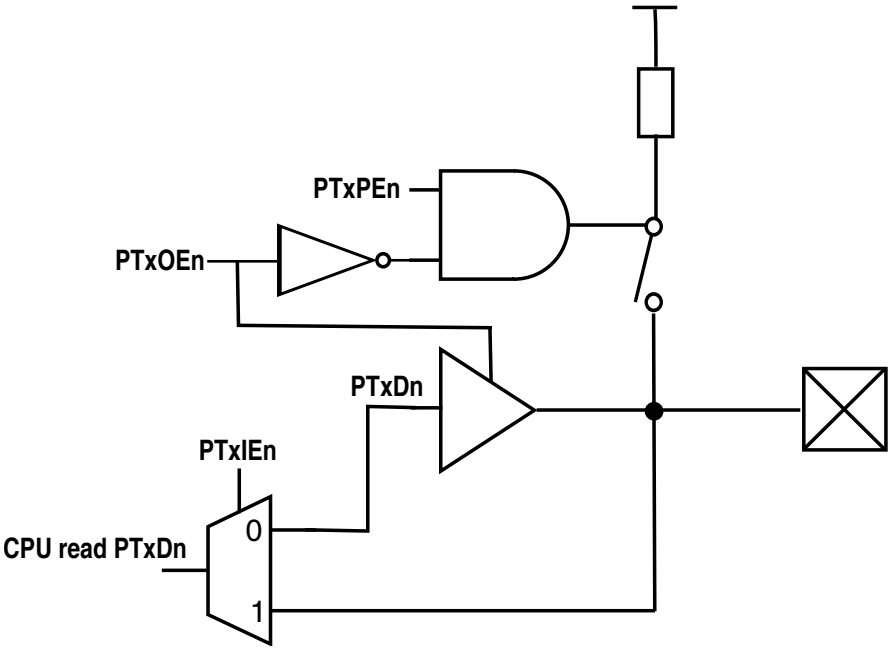


Figure 11-1. Normal I/O structure

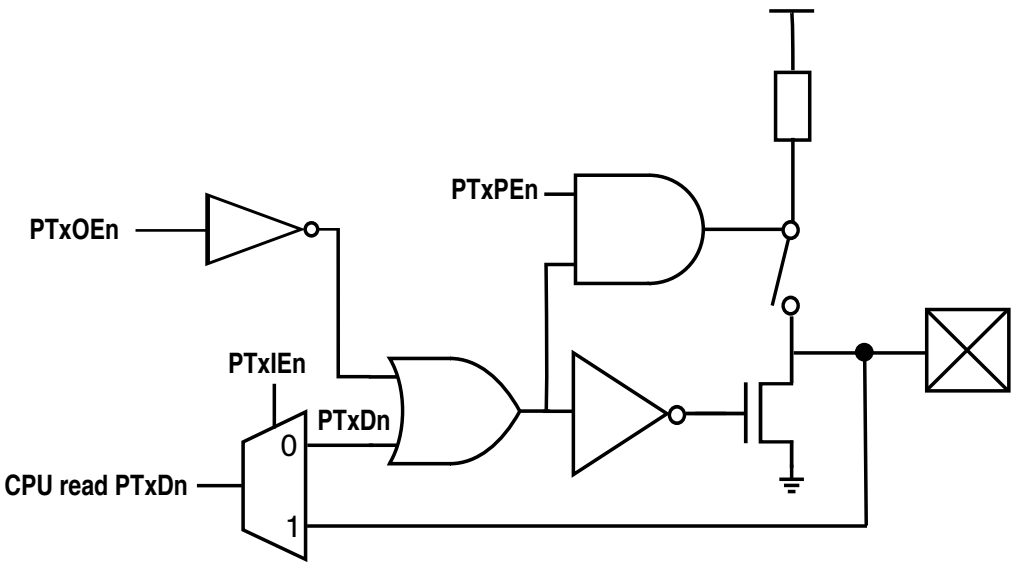


Figure 11-2. I/O structure when I^2C functions SDA/SCL is enabled

11.2 Port data and data direction

Reading and writing of parallel I/O is accomplished through the port data registers (PTxD). The direction, input or output, is controlled through the input enable or output enable registers.

After reset, all parallel I/O default to the Hi-Z state. The corresponding bit in output enable register (PTxOE) or input enable register (PTxIE) must be configured for output or input operation. Each port pin has an input enable bit and an output enable bit. When PTxIEn = 1, a read from PTxDn returns the input value of the associated pin; when PTxIEn = 0, a read from PTxDn returns the last value written to the port data register.

NOTE

The PTxOE must be clear when the corresponding pin is used as input function to avoid contention. If set the corresponding PTxOE and PTxIE bits at same time, read from PTxDn will always return the output data.

When a peripheral module or system function is in control of a port pin, the data direction register bit still controls what is returned for reads of the port data register, even though the peripheral system has overriding control of the actual pin direction.

When a shared analog function is enabled for a pin, all digital pin functions are disabled. A read of the port data register returns a value of 0 for any bits that have shared analog functions enabled. In general, whenever a pin is shared with both an alternate digital function and an analog function, the analog function has priority such that if both of the digital and analog functions are enabled, the analog function controls the pin.

A write of valid data to a port data register must occur before setting the output enable bit of an associated port pin. This ensures that the pin will not be driven with an incorrect data value.

11.3 Internal pullup enable

An internal pullup device can be enabled for each port pin by setting the corresponding bit in one of the pullup enable registers (PTxPEn). The internal pullup device is disabled if the pin is configured as an output by the parallel I/O control logic, or by any shared peripheral function, regardless of the state of the corresponding pullup enable register bit. The internal pullup device is also disabled if the pin is controlled by an analog function.

11.4 Input glitch filter setting

A filter is implemented for each port pin that is configured as a digital input. It can be used as a simple low-pass filter to filter any glitch that is introduced from the pins of GPIO, IRQ,$\overline{\text{RESET}}$, and KBI. The glitch width threshold can be adjusted easily by

setting registers PORT_IOFLTn and PORT_FCLKDIV between 1~4096 BUSCLKs (or 1~128 LPOCLKs). This configurable glitch filter can take the place of an on board external analog filter, and greatly improve the EMC performance.

Setting register PORT_IOFLTn can configure the filter of the whole port, etc. set PORT_IOFLT0[FLTA] will affect all PTAn pins.

11.5 Pin behavior in stop mode

In stop3 mode, all I/O is maintained because internal logic circuitry stays powered up. Upon recovery, normal I/O function is available to the user.

11.6 Port data registers

PORT memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	Port A Data Register (PORT_PTAD)	8	R/W	00h	11.6.1/179
1	Port B Data Register (PORT_PTBD)	8	R/W	00h	11.6.2/179
2	Port C Data Register (PORT_PTCD)	8	R/W	00h	11.6.3/180
30B0	Port A Output Enable Register (PORT_PTAOE)	8	R/W	00h	11.6.4/180
30B1	Port B Output Enable Register (PORT_PTBOE)	8	R/W	00h	11.6.5/181
30B2	Port C Output Enable Register (PORT_PTCOE)	8	R/W	00h	11.6.6/182
30B8	Port A Input Enable Register (PORT_PTAIE)	8	R/W	00h	11.6.7/183
30B9	Port B Input Enable Register (PORT_PTBIE)	8	R/W	00h	11.6.8/184
30BA	Port C Input Enable Register (PORT_PTCIE)	8	R/W	00h	11.6.9/185
30EC	Port Filter Register 0 (PORT_IOFLT0)	8	R/W	00h	11.6.10/186
30EE	Port Filter Register 2 (PORT_IOFLT2)	8	R/W	00h	11.6.11/187
30EF	Port Clock Division Register (PORT_FCLKDIV)	8	R/W	00h	11.6.12/188
30F0	Port A Pullup Enable Register (PORT_PTAPE)	8	R/W	00h	11.6.13/189
30F1	Port B Pullup Enable Register (PORT_PTBPE)	8	R/W	00h	11.6.14/190
30F2	Port C Pullup Enable Register (PORT_PTCPE)	8	R/W	00h	11.6.15/191

11.6.1 Port A Data Register (PORT_PTAD)

Address: 0h base + 0h offset = 0h

Bit	7	6	5	4	3	2	1	0
Read	0		PTAD					
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTAD field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
PTAD	Port A Data Register Bits For port A pins that are configured as inputs, a read returns the logic level on the pin. For port A pins that are configured as outputs, a read returns the last value that was written to this register. For port A pins that are configured as Hi-Z, a read returns uncertainty data. Writes are latched into all bits of this register. For port A pins that are configured as outputs, the logic level is driven out of the corresponding MCU pin. Reset forces PTAD to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

11.6.2 Port B Data Register (PORT_PTBD)

Address: 0h base + 1h offset = 1h

Bit	7	6	5	4	3	2	1	0
Read Write	PTBD							
Reset	0	0	0	0	0	0	0	0

PORT_PTBD field descriptions

Field	Description
PTBD	Port B Data Register Bits For port B pins that are configured as inputs, a read returns the logic level on the pin. For port B pins that are configured as outputs, a read returns the last value that was written to this register. For port B pins that are configured as Hi-Z, a read returns uncertainty data. Writes are latched into all bits of this register. For port B pins that are configured as outputs, the logic level is driven out of the corresponding MCU pin. Reset forces PTBD to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

11.6.3 Port C Data Register (PORT_PTCD)

Address: 0h base + 2h offset = 2h

Bit	7	6	5	4	3	2	1	0
Read	0				PTCD			
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTCD field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
PTCD	Port C Data Register Bits For port C pins that are configured as inputs, a read returns the logic level on the pin. For port C pins that are configured as outputs, a read returns the last value that was written to this register. For port C pins that are configured as Hi-Z, a read returns uncertainty data. Writes are latched into all bits of this register. For port C pins that are configured as outputs, the logic level is driven out of the corresponding MCU pin. Reset forces PTCD to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

11.6.4 Port A Output Enable Register (PORT_PTAOE)

Address: 0h base + 30B0h offset = 30B0h

Bit	7	6	5	4	3	2	1	0
Read	0		PTAOE5	PTAOE4	PTAOE3	PTAOE2	PTAOE1	PTAOE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTAOE field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 PTAOE5	Output Enable for Port A Bit 5 This read/write bit enables the port A pin as an output. 0 Output Disabled for port A bit 5. 1 Output Enabled for port A bit 5.
4 PTAOE4	Output Enable for Port A Bit 4 This read/write bit enables the port A pin as an output.

Table continues on the next page...

PORT_PTAOE field descriptions (continued)

Field	Description
	0 Output Disabled for port A bit 4. 1 Output Enabled for port A bit 4.
3 PTAOE3	Output Enable for Port A Bit 3 This read/write bit enables the port A pin as an output. 0 Output Disabled for port A bit 3. 1 Output Enabled for port A bit 3.
2 PTAOE2	Output Enable for Port A Bit 2 This read/write bit enables the port A pin as an output. 0 Output Disabled for port A bit 2. 1 Output Enabled for port A bit 2.
1 PTAOE1	Output Enable for Port A Bit 1 This read/write bit enables the port A pin as an output. 0 Output Disabled for port A bit 1. 1 Output Enabled for port A bit 1.
0 PTAOE0	Output Enable for Port A Bit 0 This read/write bit enables the port A pin as an output. 0 Output Disabled for port A bit 0. 1 Output Enabled for port A bit 0.

11.6.5 Port B Output Enable Register (PORT_PTBOE)

Address: 0h base + 30B1h offset = 30B1h

Bit	7	6	5	4	3	2	1	0
Read Write	PTBOE7	PTBOE6	PTBOE5	PTBOE4	PTBOE3	PTBOE2	PTBOE1	PTBOE0
Reset	0	0	0	0	0	0	0	0

PORT_PTBOE field descriptions

Field	Description
7 PTBOE7	Output Enable for Port B Bit 7 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 7. 1 Output Enabled for port B bit 7.
6 PTBOE6	Output Enable for Port B Bit 6 This read/write bit enables the port B pin as an output.

Table continues on the next page...

PORT_PTBOE field descriptions (continued)

Field	Description
	0 Output Disabled for port B bit 6. 1 Output Enabled for port B bit 6.
5 PTBOE5	Output Enable for Port B Bit 5 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 5. 1 Output Enabled for port B bit 5.
4 PTBOE4	Output Enable for Port B Bit 4 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 4. 1 Output Enabled for port B bit 4.
3 PTBOE3	Output Enable for Port B Bit 3 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 3. 1 Output Enabled for port B bit 3.
2 PTBOE2	Output Enable for Port B Bit 2 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 2. 1 Output Enabled for port B bit 2.
1 PTBOE1	Output Enable for Port B Bit 1 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 1. 1 Output Enabled for port B bit 1.
0 PTBOE0	Output Enable for Port B Bit 0 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 0. 1 Output Enabled for port B bit 0.

11.6.6 Port C Output Enable Register (PORT_PTCOE)

Address: 0h base + 30B2h offset = 30B2h

Bit	7	6	5	4	3	2	1	0
Read	0				PTCOE3	PTCOE2	PTCOE1	PTCOE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTCOE field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 PTCOE3	Output Enable for Port C Bit 3 This read/write bit enables the port C pin as an output. 0 Output Disabled for port C bit 3. 1 Output Enabled for port C bit 3.
2 PTCOE2	Output Enable for Port C Bit 2 This read/write bit enables the port C pin as an output. 0 Output Disabled for port C bit 2. 1 Output Enabled for port C bit 2.
1 PTCOE1	Output Enable for Port C Bit 1 This read/write bit enables the port C pin as an output. 0 Output Disabled for port C bit 1. 1 Output Enabled for port C bit 1.
0 PTCOE0	Output Enable for Port C Bit 0 This read/write bit enables the port C pin as an output. 0 Output Disabled for port C bit 0. 1 Output Enabled for port C bit 0.

11.6.7 Port A Input Enable Register (PORT_PTAIE)

Address: 0h base + 30B8h offset = 30B8h

Bit	7	6	5	4	3	2	1	0
Read	0		PTAIE5	0	PTAIE3	PTAIE2	PTAIE1	PTAIE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTAIE field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 PTAIE5	Input Enable for Port A Bit 5 This read/write bit enables the port A pin as an input. 0 Input disabled for port A bit 5. 1 Input enabled for port A bit 5.

Table continues on the next page...

PORT_PTAIE field descriptions (continued)

Field	Description
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 PTAIE3	Input Enable for Port A Bit 3 This read/write bit enables the port A pin as an input. 0 Input disabled for port A bit 3. 1 Input enabled for port A bit 3.
2 PTAIE2	Input Enable for Port A Bit 2 This read/write bit enables the port A pin as an input. 0 Input disabled for port A bit 2. 1 Input enabled for port A bit 2.
1 PTAIE1	Input Enable for Port A Bit 1 This read/write bit enables the port A pin as an input. 0 Input disabled for port A bit 1. 1 Input enabled for port A bit 1.
0 PTAIE0	Input Enable for Port A Bit 0 This read/write bit enables the port A pin as an input. 0 Input disabled for port A bit 0. 1 Input enabled for port A bit 0.

11.6.8 Port B Input Enable Register (PORT_PTBIE)

Address: 0h base + 30B9h offset = 30B9h

Bit	7	6	5	4	3	2	1	0
Read Write	PTBIE7	PTBIE6	PTBIE5	PTBIE4	PTBIE3	PTBIE2	PTBIE1	PTBIE0
Reset	0	0	0	0	0	0	0	0

PORT_PTBIE field descriptions

Field	Description
7 PTBIE7	Input Enable for Port B Bit 7 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 7. 1 Input enabled for port B bit 7.
6 PTBIE6	Input Enable for Port B Bit 6 This read/write bit enables the port B pin as an input.

Table continues on the next page...

PORT_PTBIE field descriptions (continued)

Field	Description
	0 Input disabled for port B bit 6. 1 Input enabled for port B bit 6.
5 PTBIE5	Input Enable for Port B Bit 5 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 5. 1 Input enabled for port B bit 5.
4 PTBIE4	Input Enable for Port B Bit 4 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 4. 1 Input enabled for port B bit 4.
3 PTBIE3	Input Enable for Port B Bit 3 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 3. 1 Input enabled for port B bit 3.
2 PTBIE2	Input Enable for Port B Bit 2 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 2. 1 Input enabled for port B bit 2.
1 PTBIE1	Input Enable for Port B Bit 1 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 1. 1 Input enabled for port B bit 1.
0 PTBIE0	Input Enable for Port B Bit 0 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 0. 1 Input enabled for port B bit 0.

11.6.9 Port C Input Enable Register (PORT_PTCIE)

Address: 0h base + 30BAh offset = 30BAh

Bit	7	6	5	4	3	2	1	0
Read	0				PTCIE3	PTCIE2	PTCIE1	PTCIE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTCIE field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 PTCIE3	Input Enable for Port C Bit 3 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 3. 1 Input enabled for port C bit 3.
2 PTCIE2	Input Enable for Port C Bit 2 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 2. 1 Input enabled for port C bit 2.
1 PTCIE1	Input Enable for Port C Bit 1 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 1. 1 Input enabled for port C bit 1.
0 PTCIE0	Input Enable for Port C Bit 0 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 0. 1 Input enabled for port C bit 0.

11.6.10 Port Filter Register 0 (PORT_IOFLT0)

This register sets the filters for input.

Address: 0h base + 30ECh offset = 30ECh

Bit	7	6	5	4	3	2	1	0
Read	0		FLTC		FLTB		FLTA	
Write								
Reset	0	0	0	0	0	0	0	0

PORT_IOFLT0 field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5–4 FLTC	Filter selection for input from PTC 00 BUSCLK 01 FLTDIV1

Table continues on the next page...

PORT_IOFLT0 field descriptions (continued)

Field	Description
	10 FLTDIV2 11 FLTDIV3
3–2 FLTB	Filter selection for input from PTB 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3
FLTA	Filter selection for input from PTA 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3

11.6.11 Port Filter Register 2 (PORT_IOFLT2)

This register sets the filters for input.

Address: 0h base + 30EEh offset = 30EEh

Bit	7	6	5	4	3	2	1	0
Read Write	FLTFDS		FLTPWT		FLTKBI0		FLTRST	
Reset	0	0	0	0	0	0	0	0

PORT_IOFLT2 field descriptions

Field	Description
7–6 FLTFDS	Filter selection for input from FDS 00 BUSCLK 01 Select FLTDIV1, and will switch to FLTDIV3 in stop mode automatically. 10 Select FLTDIV2, and will switch to FLTDIV3 in stop mode automatically. 11 FLTDIV3
5–4 FLTPWT	Filter selection for input from PWT 00 BUSCLK 01 Select FLTDIV1, and will switch to FLTDIV3 in stop mode automatically. 10 Select FLTDIV2, and will switch to FLTDIV3 in stop mode automatically. 11 FLTDIV3
3–2 FLTKBI0	Filter selection for input from KBI0 00 BUSCLK 01 Select FLTDIV1, and will switch to FLTDIV3 in stop mode automatically. 10 Select FLTDIV2, and will switch to FLTDIV3 in stop mode automatically. 11 FLTDIV3

Table continues on the next page...

PORT_IOFLT2 field descriptions (continued)

Field	Description
FLTRST	Filter selection for input from RESET/IRQ 00 BUSCLK 01 Select FLTDIV1, and will switch to FLTDIV3 in stop mode automatically. 10 Select FLTDIV2, and will switch to FLTDIV3 in stop mode automatically. 11 FLTDIV3

11.6.12 Port Clock Division Register (PORT_FCLKDIV)

Configure the high/low level glitch width threshold. Glitches that are shorter than the selected clock width will be filtered out; glitches that are more than twice the selected clock width will not be filtered out (they will pass to the internal circuitry).

Address: 0h base + 30EFh offset = 30EFh

Bit	7	6	5	4	3	2	1	0
Read Write	FLTDIV3			FLTDIV2			FLTDIV1	
Reset	0	0	0	0	0	0	0	0

PORT_FCLKDIV field descriptions

Field	Description
7–5 FLTDIV3	Filter Division Set 3 Port Filter Division Set 3 000 LPOCLK. 001 LPOCLK/2. 010 LPOCLK/4. 011 LPOCLK/8. 100 LPOCLK/16. 101 LPOCLK/32. 110 LPOCLK/64. 111 LPOCLK/128.
4–2 FLTDIV2	Filter Division Set 2 Port Filter Division Set 2 000 BUSCLK/32. 001 BUSCLK/64. 010 BUSCLK/128. 011 BUSCLK/256. 100 BUSCLK/512. 101 BUSCLK/1024. 110 BUSCLK/2048. 111 BUSCLK/4096.

Table continues on the next page...

PORT_FCLKDIV field descriptions (continued)

Field	Description
FLTDIV1	Filter Division Set 1 Port Filter Division Set 1 00 BUSCLK/2. 01 BUSCLK/4. 10 BUSCLK/8. 11 BUSCLK/16.

11.6.13 Port A Pullup Enable Register (PORT_PTAPE)

Address: 0h base + 30F0h offset = 30F0h

Bit	7	6	5	4	3	2	1	0
Read	0		PTAPE5	0	PTAPE3	PTAPE2	PTAPE1	PTAPE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTAPE field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 PTAPE5	Pull Enable for Port A Bit 5 This control bit determines if the internal pullup device is enabled for the associated PTA pin. For port A pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port A bit 5. 1 Pullup enabled for port A bit 5.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 PTAPE3	Pull Enable for Port A Bit 3 This control bit determines if the internal pullup device is enabled for the associated PTA pin. For port A pins that are configured as outputs or Hi-Z, these bits have no effect. **NOTE:** When configuring to use this pin as output high for IIC, the internal pullup device remains active when PTAPE3 is set. It is automatically disabled to save power when output low. 0 Pullup disabled for port A bit 3. 1 Pullup enabled for port A bit 3.
2 PTAPE2	Pull Enable for Port A Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTA pin. For port A pins that are configured as outputs or Hi-Z, these bits have no effect. **NOTE:** When configuring to use this pin as output high for IIC, the internal pullup device remains active when PTAPE2 is set. It is automatically disabled to save power when output low.

Table continues on the next page...

PORT_PTAPE field descriptions (continued)

Field	Description
	0 Pullup disabled for port A bit 2. 1 Pullup enabled for port A bit 2.
1 PTAPE1	Pull Enable for Port A Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTA pin. For port A pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port A bit 1. 1 Pullup enabled for port A bit 1.
0 PTAPE0	Pull Enable for Port A Bit 0 This control bit determines if the internal pullup device is enabled for the associated PTA pin. For port A pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port A bit 0. 1 Pullup enabled for port A bit 0.

11.6.14 Port B Pullup Enable Register (PORT_PTBPE)

Address: 0h base + 30F1h offset = 30F1h

Bit	7	6	5	4	3	2	1	0
Read Write	PTBPE7	PTBPE6	PTBPE5	PTBPE4	PTBPE3	PTBPE2	PTBPE1	PTBPE0
Reset	0	0	0	0	0	0	0	0

PORT_PTBPE field descriptions

Field	Description
7 PTBPE7	Pull Enable for Port B Bit 7 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 7. 1 Pullup enabled for port B bit 7.
6 PTBPE6	Pull Enable for Port B Bit 6 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 6. 1 Pullup enabled for port B bit 6.
5 PTBPE5	Pull Enable for Port B Bit 5 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 5. 1 Pullup enabled for port B bit 5.

Table continues on the next page...

PORT_PTBPE field descriptions (continued)

Field	Description
4 PTBPE4	Pull Enable for Port B Bit 4 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 4. 1 Pullup enabled for port B bit 4.
3 PTBPE3	Pull Enable for Port B Bit 3 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 3. 1 Pullup enabled for port B bit 3.
2 PTBPE2	Pull Enable for Port B Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 2. 1 Pullup enabled for port B bit 2.
1 PTBPE1	Pull Enable for Port B Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 1. 1 Pullup enabled for port B bit 1.
0 PTBPE0	Pull Enable for Port B Bit 0 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 0. 1 Pullup enabled for port B bit 0.

11.6.15 Port C Pullup Enable Register (PORT_PTCPE)

Address: 0h base + 30F2h offset = 30F2h

Bit	7	6	5	4	3	2	1	0
Read	0				PTCPE3	PTCPE2	PTCPE1	PTCPE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTCPE field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 PTCPE3	Pull Enable for Port C Bit 3 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 3. 1 Pullup enabled for port C bit 3.
2 PTCPE2	Pull Enable for Port C Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 2. 1 Pullup enabled for port C bit 2.
1 PTCPE1	Pull Enable for Port C Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 1. 1 Pullup enabled for port C bit 1.
0 PTCPE0	Pull Enable for Port C Bit 0 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 0. 1 Pullup enabled for port C bit 0.

Chapter 12
Keyboard Interrupts (KBI)

12.1 Introduction

12.1.1 Features

The KBI features include:

- Up to eight keyboard interrupt pins with individual pin enable bits
- Each keyboard interrupt pin is programmable as:
  - falling-edge sensitivity only
  - rising-edge sensitivity only
  - both falling-edge and low-level sensitivity
  - both rising-edge and high-level sensitivity
- One software-enabled keyboard interrupt
- Exit from low-power modes

12.1.2 Modes of Operation

This section defines the KBI operation in:

- Wait mode
- Stop mode
- Background debug mode

12.1.2.1 KBI in Wait mode

Executing the Wait instruction places the MCU into Wait mode. The KBI interrupt should be enabled (KBI_SC[KBIE] = 1), if desired, before executing the Wait instruction, allowing the KBI to continue to operate while the MCU is in Wait mode. An enabled KBI pin (KBI_PE[KBIPEn] = 1) can be used to bring the MCU out of Wait mode if the KBI interrupt is enabled (KBI_SC[KBIE] = 1).

12.1.2.2 KBI in Stop modes

Executing the Stop instruction places the MCU into Stop mode (when Stop is selected), where the KBI can operate asynchronously. If this is the desired behavior, the KBI interrupt must be enabled (KBI_SC[KBIE] = 1) before executing the Stop instruction, allowing the KBI to continue to operate while the MCU is in Stop mode. An enabled KBI pin (KBI_PE[KBIPEn] = 1) can be used to bring the MCU out of Stop mode if the KBI interrupt is enabled (KBI_SC[KBIE] = 1).

12.1.3 Block Diagram

The block diagram for the keyboard interrupt module is shown below..

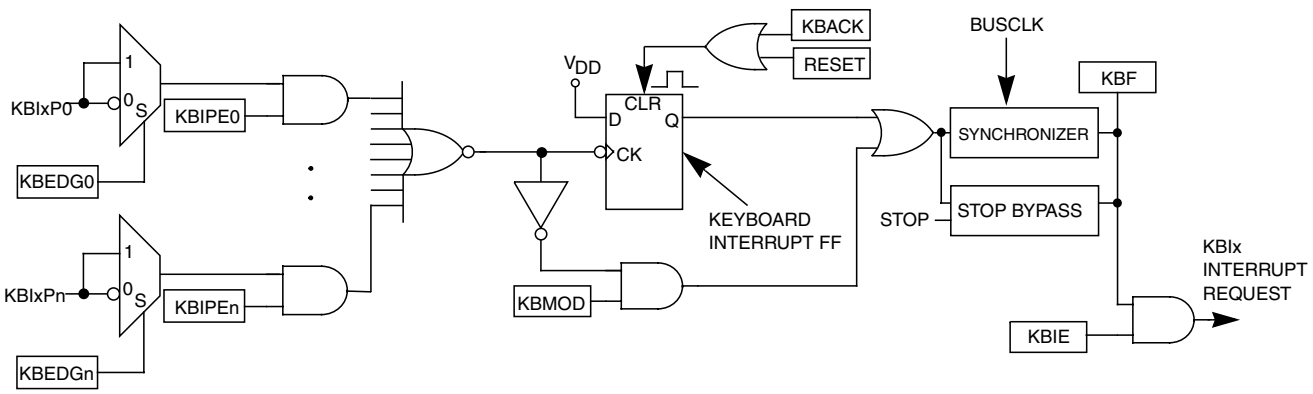


Figure 12-1. KBI block diagram

12.2 External signals description

The KBI input pins can be used to detect either falling edges, or both falling edge and low-level interrupt requests. The KBI input pins can also be used to detect either rising edges, or both rising edge and high-level interrupt requests.

The signal properties of KBI are shown in the following table:

Table 12-1. External signals description

Signal	Function	I/O
KBIPn	Keyboard interrupt pins	I

12.3 Register definition

The KBI includes following registers:

- A pin status and control register, KBI_SC
- A pin enable register, KBI_PE
- An edge select register, KBI_ES

See the direct-page register summary in the Memory chapter for the absolute address assignments for all KBI registers. This section refers to registers and control bits only by their names.

Some MCUs may have more than one KBI, so register names include placeholder characters to identify which KBI is being referenced.

12.4 Memory Map and Registers

KBI memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3C	KBI Status and Control Register (KBI0_SC)	8	R/W	00h	12.4.1/196
307C	KBI Pin Enable Register (KBI0_PE)	8	R/W	00h	12.4.2/197
307D	KBI Edge Select Register (KBI0_ES)	8	R/W	00h	12.4.3/197

12.4.1 KBI Status and Control Register (KBIx_SC)

KBI_SC contains the status flag and control bits, which are used to configure the KBI.

Address: 3Ch base + 0h offset = 3Ch

Bit	7	6	5	4	3	2	1	0
Read	0				KBF		KBIE	KBMOD
Write						KBACK		
Reset	0	0	0	0	0	0	0	0

KBIx_SC field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 KBF	KBI Interrupt Flag KBF indicates when a KBI interrupt request is detected. Writes have no effect on KBF. 0 KBI interrupt request not detected. 1 KBI interrupt request detected.
2 KBACK	KBI Acknowledge Writing a 1 to KBACK is part of the flag clearing mechanism.
1 KBIE	KBI Interrupt Enable KBIE determines whether a KBI interrupt is enabled or not. 0 KBI interrupt not enabled. 1 KBI interrupt enabled.
0 KBMOD	KBI Detection Mode KBMOD (along with the KBEDG bits) controls the detection mode of the KBI interrupt pins. 0 Keyboard detects edges only. 1 Keyboard detects both edges and levels.

12.4.2 KBI Pin Enable Register (KBIx_PE)

KBI_PE contains the pin enable control bits.

Address: 3Ch base + 3040h offset = 307Ch

Bit	7	6	5	4	3	2	1	0
Read Write	KBIPE							
Reset	0	0	0	0	0	0	0	0

KBIx_PE field descriptions

Field	Description
KBIPE	KBI Pin Enables Each of the KBIPEn bits enable the corresponding KBI interrupt pin. 0 Pin is not enabled as KBI interrupt. 1 Pin is enabled as KBI interrupt.

12.4.3 KBI Edge Select Register (KBIx_ES)

KBI_ES contains the edge select control bits.

Address: 3Ch base + 3041h offset = 307Dh

Bit	7	6	5	4	3	2	1	0
Read Write	KBEDG							
Reset	0	0	0	0	0	0	0	0

KBIx_ES field descriptions

Field	Description
KBEDG	KBI Edge Selects Each of the KBEDGn bits selects the falling edge/low-level or rising edge/high-level function of the corresponding pin. 0 Falling edge/low level. 1 Rising edge/high level.

12.5 Functional Description

This on-chip peripheral module is called a keyboard interrupt module because originally it was designed to simplify the connection and use of row-column matrices of keyboard switches. However, these inputs are also useful as extra external interrupt inputs and as an external means of waking the MCU from stop or wait low-power modes.

The KBI module allows up to eight pins to act as additional interrupt sources. Writing to the KBI_PE[KBIPEn] bits independently enables or disables each KBI pin. Each KBI pin can be configured as edge sensitive or edge and level sensitive based on the KBI_SC[KBMOD] bit. Edge sensitive can be software programmed to be either falling or rising; the level can be either low or high. The polarity of the edge or edge and level sensitivity is selected using the KBI_ES[KBEDGn] bits.

12.5.1 Edge-only sensitivity

Synchronous logic is used to detect edges. A falling edge is detected when an enabled keyboard interrupt (KBI_PE[KBIPEn]=1) input signal is seen as a logic 1 (the deasserted level) during one bus cycle and then a logic 0 (the asserted level) during the next cycle. A rising edge is detected when the input signal is seen as a logic 0 (the deasserted level) during one bus cycle and then a logic 1 (the asserted level) during the next cycle.

Before the first edge is detected, all enabled keyboard interrupt input signals must be at the deasserted logic levels. After any edge is detected, all enabled keyboard interrupt input signals must return to the deasserted level before any new edge can be detected.

A valid edge on an enabled KBI pin will set KBI_SC[KBF]. If KBI_SC[KBIE] is set, an interrupt request will be presented to the MPU. Clearing of KBI_SC[KBF] is accomplished by writing a 1 to KBI_SC[KBACK].

12.5.2 Edge and level sensitivity

A valid edge or level on an enabled KBI pin will set KBI_SC[KBF]. If KBI_SC[KBIE] is set, an interrupt request will be presented to the MCU. Clearing of KBI_SC[KBF] is accomplished by writing a 1 to KBI_SC[KBACK], provided all enabled keyboard inputs are at their deasserted levels. KBI_SC[KBF] will remain set if any enabled KBI pin is asserted while attempting to clear KBI_SC[KBF] by writing a 1 to KBI_SC[KBACK].

12.5.3 KBI Pullup Resistor

Each KBI pin, if enabled by KBI_PE, can be configured via the associated I/O port pull enable register, see chapter, to use:

- an internal pullup resistor, or
- no resistor

If an internal pullup resistor is enabled for an enabled KBI pin, the associated I/O port pull select register (see I/O Port chapter) can be used to select an internal pullup resistor.

12.5.4 KBI initialization

When a keyboard interrupt pin is first enabled, it is possible to get a false keyboard interrupt flag. To prevent a false interrupt request during keyboard initialization, the user should do the following:

1. Mask keyboard interrupts by clearing KBI_SC[KBIE].
2. Enable the KBI polarity by setting the appropriate KBI_ES[KBEDGn] bits.
3. Before using internal pullup resistors, configure the associated bits in PORT_.
4. Enable the KBI pins by setting the appropriate KBI_PE[KBIPEn] bits.
5. Write to KBI_SC[KBACK] to clear any false interrupts.
6. Set KBI_SC[KBIE] to enable interrupts.

Chapter 13
Internal Clock Source (ICS)

13.1 Chip specific ICS information

If ICS is in FEI or FEE mode, the ICS_C2[BDIV] cannot be set to 000.

13.2 Introduction

The internal clock source (ICS) module provides clock source choices for the MCU. The module contains a frequency-locked loop (FLL) as a clock source that is controllable by either an internal or an external reference clock. The module can provide this FLL clock or either of the internal or external reference clocks as a source for the MCU system clock. There are also signals provided to control a low-power oscillator (OSC) module for glitch-free clock modes transitions. These signals configure and enable the OSC module to generate its external crystal/resonator clock (OSC_OUT) used by peripheral modules and as the ICS external reference clock source. The ICS external reference clock can be the external crystal/resonator (OSC_OUT) supplied by an OSC, or it can be another external clock source.

The ICS clock source chosen is passed through a reduced bus divider (BDIV) which allows a lower final output clock frequency to be derived.

13.2.1 Features

The key features of the ICS module are given below:

- Internal reference clock has 9 trim bits for accuracy
- Internal or external reference clocks can be used to control the FLL.
- Selectable dividers for external reference clock to ensure proper input frequency to FLL.
- Internal or external reference clocks can be selected as the clock source for the MCU.
- FLL Engaged Internal mode is automatically selected out of reset.

- FLL lock detector and external clock monitor
  - FLL lock detector with interrupt capability
  - External reference clock monitor with reset capability
- Digitally controlled oscillator optimized for 32-40 MHz frequency range

13.2.2 Block diagram

The following figure is the ICS block diagram.

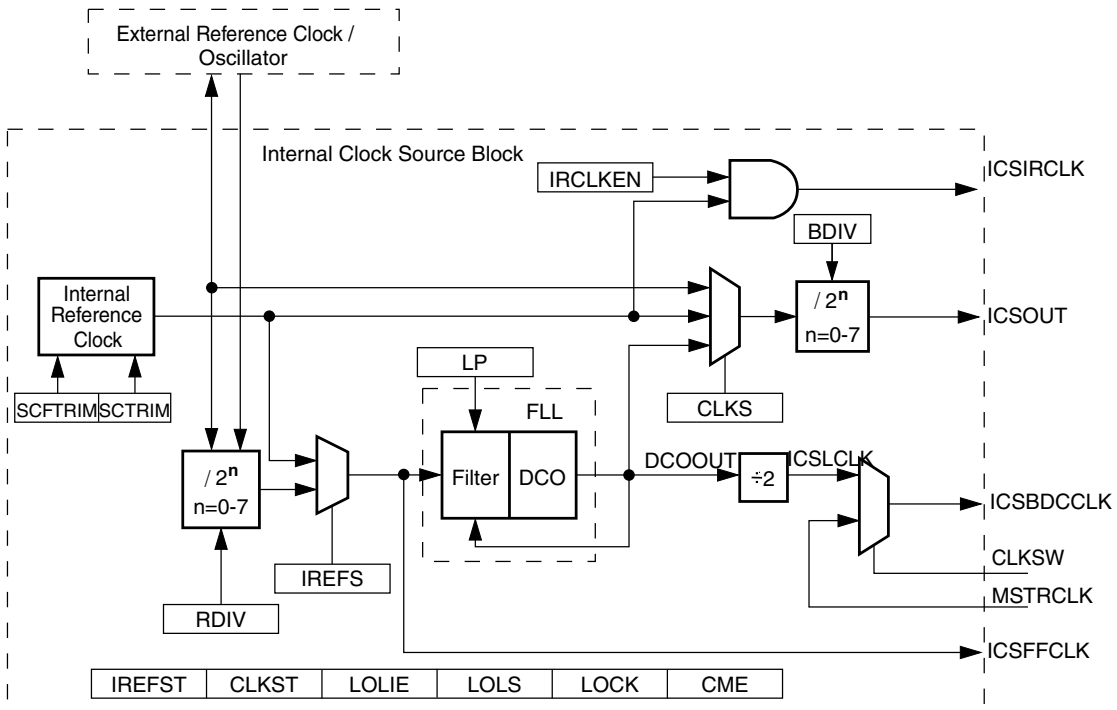


Figure 13-1. Internal clock source (ICS) block diagram

13.2.3 Modes of operation

There are seven modes of operation for the ICS: FEI, FEE, FBI, FBILP, FBE, FBELP, and STOP. Each of these modes is explained briefly in the following subsections.

13.2.3.1 FLL engaged internal (FEI)

In FLL engaged internal mode, which is the default mode, the ICS supplies a clock derived from the FLL which is controlled by the internal reference clock.

13.2.3.2 FLL engaged external (FEE)

In FLL engaged external mode, the ICS supplies a clock derived from the FLL which is controlled by an external reference clock source.

13.2.3.3 FLL bypassed internal (FBI)

In FLL bypassed internal mode, the FLL is enabled and controlled by the internal reference clock, but is bypassed. The ICS supplies a clock derived from the internal reference clock.

13.2.3.4 FLL bypassed internal low power (FBILP)

In FLL bypassed internal low power mode, the FLL is disabled and bypassed, and the ICS supplies a clock derived from the internal reference clock.

13.2.3.5 FLL bypassed external (FBE)

In FLL bypassed external mode, the FLL is enabled and controlled by an external reference clock, but is bypassed. The ICS supplies a clock derived from the external reference clock source.

13.2.3.6 FLL bypassed external low power (FBELP)

In FLL bypassed external low power mode, the FLL is disabled and bypassed, and the ICS supplies a clock derived from the external reference clock.

13.2.3.7 Stop (STOP)

In Stop mode, the FLL is disabled and the internal or the ICS external reference clocks source (OSC_OUT) can be selected to be enabled or disabled. The ICS does not provide any MCU clock sources.

NOTE

The DCO frequency changes from the pre-stop value to its reset value and the FLL needs to reacquire the lock before the

frequency is stable. Timing sensitive operations must wait for the FLL acquisition time, $t_{Acquire}$, before executing.

13.3 External signal description

There are no ICS signals that connect off chip.

13.4 Register definition

ICS memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3038	ICS Control Register 1 (ICS_C1)	8	R/W	04h	13.4.1/204
3039	ICS Control Register 2 (ICS_C2)	8	R/W	20h	13.4.2/205
303A	ICS Control Register 3 (ICS_C3)	8	R/W	See section	13.4.3/206
303B	ICS Control Register 4 (ICS_C4)	8	R/W	00h	13.4.4/207
303C	ICS Status Register (ICS_S)	8	R/W	10h	13.4.5/207

13.4.1 ICS Control Register 1 (ICS_C1)

Address: 3038h base + 0h offset = 3038h

Bit	7	6	5	4	3	2	1	0
Read Write	CLKS		RDIV			IREFS	IRCLKEN	IREFSTEN
Reset	0	0	0	0	0	1	0	0

ICS_C1 field descriptions

Field	Description
7–6 CLKS	Clock Source Select Selects the clock source that controls the bus frequency. The actual bus frequency depends on the value of ICS_C2[BDIV]. 00 Output of FLL is selected. 01 Internal reference clock is selected. 10 External reference clock is selected. 11 Reserved, defaults to 00.
5–3 RDIV	Reference Divider Changing RDIV will cause the change of reference clock frequency of FLL, RDIV is not allowed to be changed in FEE/FBE mode.

Table continues on the next page...

ICS_C1 field descriptions (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td></td><td>Selects the amount to divide down the FLL reference clock selected by the IREFS bits. Resulting frequency must be in the range 31.25 kHz to 39.0625 kHz.

<table><tr><th>RDIV</th><th>OSC_CR[RANGE]= 0</th><th>OSC_CR[RANGE]= 1</th></tr><tr><td>000</td><td>1[1]</td><td>32</td></tr><tr><td>001</td><td>2</td><td>64</td></tr><tr><td>010</td><td>4</td><td>128</td></tr><tr><td>011</td><td>8</td><td>256</td></tr><tr><td>100</td><td>16</td><td>512</td></tr><tr><td>101</td><td>32</td><td>1024</td></tr><tr><td>110</td><td>64</td><td>Reserved</td></tr><tr><td>111</td><td>128</td><td>Reserved</td></tr></table>
1. Reset default</td></tr>
<tr><td>2
IREFS</td><td>Internal Reference Select

Selects the reference clock source for the FLL.

0 External reference clock is selected.
1 Internal reference clock is selected.</td></tr>
<tr><td>1
IRCLKEN</td><td>Internal Reference Clock Enable

Enables the internal reference clock for use as ICSIRCLK.

0 ICSIRCLK is inactive.
1 ICSIRCLK is active.</td></tr>
<tr><td>0
IREFSTEN</td><td>Internal Reference Stop Enable

Controls whether or not the internal reference clock remains enabled when the ICS enters Stop mode.

0 Internal reference clock is disabled in Stop mode.
1 Internal reference clock stays enabled in Stop mode if IRCLKEN is set, or if ICS is in FEI, FBI, or FBILP mode before entering Stop.</td></tr>
</table>

1. Reset default

13.4.2 ICS Control Register 2 (ICS_C2)

Address: 3038h base + 1h offset = 3039h

Bit	7	6	5	4	3	2	1	0
Read	BDIV			LP	0			
Write								
Reset	0	0	1	0	0	0	0	0

ICS_C2 field descriptions

Field	Description
7–5 BDIV	Bus Frequency Divider Selects the amount to divide down the clock source selected by ICS_C1[CLKS]. This controls the bus frequency. 000 Encoding 0—Divides the selected clock by 1. 001 Encoding 1—Divides the selected clock by 2 (reset default). 010 Encoding 2—Divides the selected clock by 4. 011 Encoding 3—Divides the selected clock by 8. 100 Encoding 4—Divides the selected clock by 16. 101 Encoding 5—Divides the selected clock by 32. 110 Encoding 6—Divides the selected clock by 64. 111 Encoding 7—Divides the selected clock by 128.
4 LP	Low Power Select Controls whether the FLL is disabled in FLL bypassed modes. 0 FLL is not disabled in bypass mode. 1 FLL is disabled in bypass modes unless debug is active.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

13.4.3 ICS Control Register 3 (ICS_C3)

Address: 3038h base + 2h offset = 303Ah

Bit	7	6	5	4	3	2	1	0
Read Write	SCTRIM							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- SCTRIM is loaded during reset from a factory programmed location when not in BDM mode. If in a BDM mode, SCTRIM gets loaded with a value of 0x80. x = Undefined at reset.

ICS_C3 field descriptions

Field	Description
SCTRIM	Slow Internal Reference Clock Trim Setting Controls the slow internal reference clock frequency by controlling the internal reference clock period. The bits are binary weighted. In other words, bit 1 adjusts twice as much as bit 0. Increasing the binary value of SCTRIM will increase the period, and decreasing the value will decrease the period. An additional fine trim bit is available as the ICS_C4[SCFTRIM]. ICS_C3 is automatically loaded during reset from a factory programmed location when not in a debug mode. The factory programmed trim value adjusts the internal oscillator frequency to fint_ft as specified in the datasheet. The user can provide a custom trim value to attain other internal reference clock frequencies within the fint_t range. The custom trim value must be programmed into reserved flash location and copied to ICS_C3 during code initialization.

13.4.4 ICS Control Register 4 (ICS_C4)

Address: 3038h base + 3h offset = 303Bh

Bit	7	6	5	4	3	2	1	0
Read	LOLIE	0	CME	0				SCFTRIM
Write								
Reset	0	0	0	0	0	0	0	0

ICS_C4 field descriptions

Field	Description
7 LOLIE	Loss of Lock Interrupt Determines if an interrupt request is made following a loss of lock indication. This field has an effect only when ICS_S[LOLS] is set. 0 No request on loss of lock. 1 Generates an interrupt request on loss of lock.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 CME	Clock Monitor Enable Determines if a reset request is made following a loss of external clock indication. This field must be set to a logic 1 only when the ICS is in an operational mode that uses the external clock (FEE, FBE, or FBELP). 0 Clock monitor is disabled. 1 Generates a reset request on loss of external clock.
4–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 SCFTRIM	Slow Internal Reference Clock Fine Trim Controls the smallest adjustment of the internal reference clock frequency. Setting SCFTRIM will increase the period and clearing SCFTRIM will decrease the period by the smallest amount possible. ICS_C4[SCFTRIM] is automatically loaded during reset from a factory programmed location when not in a debug mode. The factory programmed trim value adjusts the internal oscillator frequency to fint_ft as specified in the datasheet. The user can provide a custom trim value to attain other internal reference clock frequencies within the fint_t range. The custom fine trim bit value must be programmed into reserved flash location and copied to ICS_C4 during code initialization.

13.4.5 ICS Status Register (ICS_S)

Address: 3038h base + 4h offset = 303Ch

Bit	7	6	5	4	3	2	1	0
Read	LOLS	LOCK	0	IREFST	CLKST		0	
Write	w1c							
Reset	0	0	0	1	0	0	0	0

ICS_S field descriptions

Field	Description
7 LOLS	Loss of Lock Status Indicates the lock status for the FLL. LOLS is set when lock detection is enabled and after acquiring lock, the FLL output frequency has fallen outside the lock exit frequency tolerance, from ±4.7% to ±5.97%. ICS_C4[LOLIE] determines whether an interrupt request is made when set. LOLS is cleared by reset or by writing a logic 1 to LOLS when LOLS is set. Writing a logic 0 to LOLS has no effect. 0 FLL has not lost lock since LOLS was last cleared. 1 FLL has lost lock since LOLS was last cleared.
6 LOCK	Lock Status Indicates whether the FLL has acquired lock. Lock detection is disabled when FLL is disabled. If the lock status bit is set then changing the value of any of the following fields IREFS, RDIV[2:0], or, if in FEI or FBI modes, SCTRIM[7:0] will cause the lock status bit to clear and stay cleared until the FLL has reacquired lock. Stop mode entry will also cause the lock status bit to clear and stay cleared until the FLL has reacquired lock. 0 FLL is currently unlocked. 1 FLL is currently locked.
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 IREFST	Internal Reference Status Indicates the current source for the reference clock. This field does not update immediately after a write to ICS_C1[IREFS] due to internal synchronization between clock domains. 0 Source of reference clock is external clock. 1 Source of reference clock is internal clock.
3–2 CLKST	Clock Mode Status Indicates the current clock mode. This field doesn't update immediately after a write to ICS_C1[CLKS] due to internal synchronization between clock domains. 00 Output of FLL is selected. 01 FLL Bypassed, internal reference clock is selected. 10 FLL Bypassed, external reference clock is selected. 11 Reserved.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

13.5 Functional description

13.5.1 Operational modes

The seven states of the ICS are shown as a state diagram and are described below. The arrows indicate the allowed movements among the states.

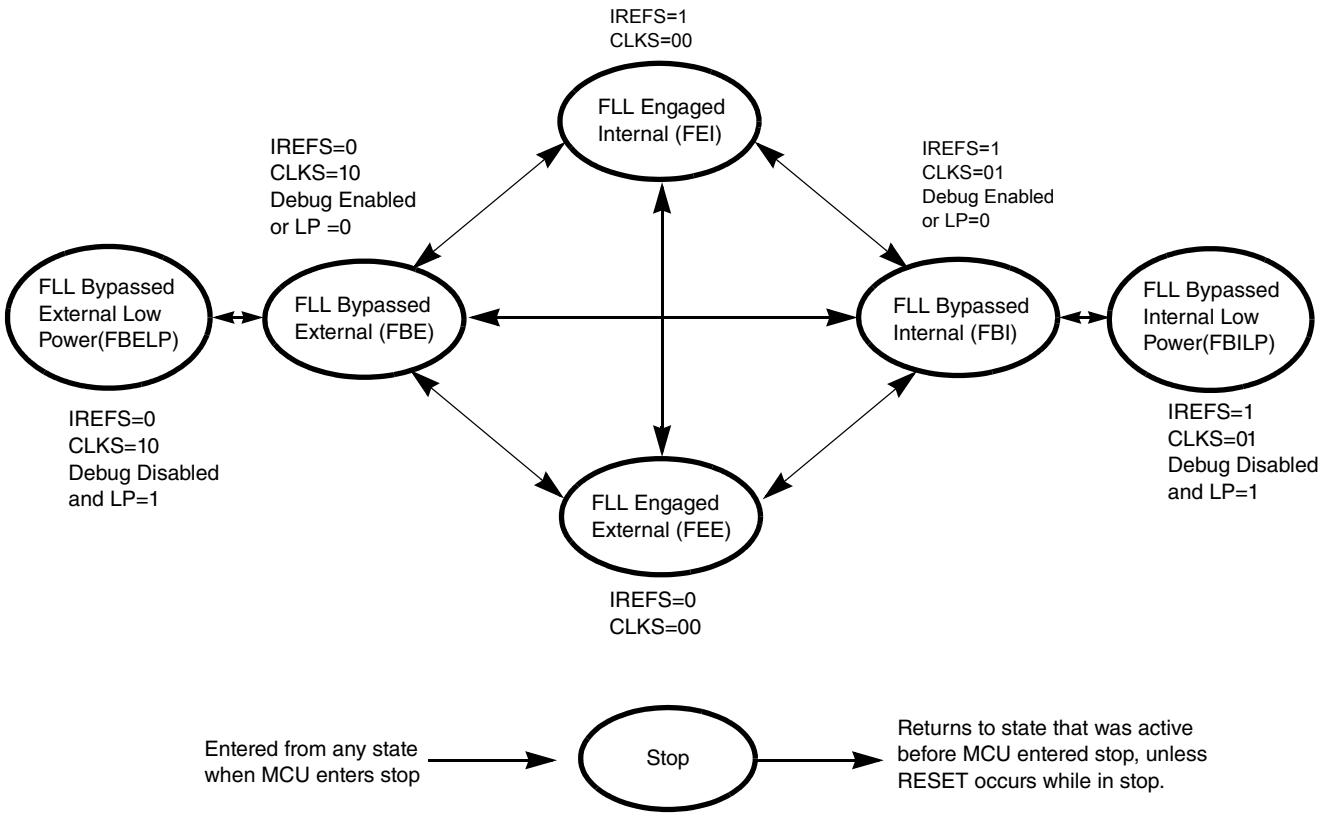


Figure 13-2. Clock switching modes

13.5.1.1 FLL engaged internal (FEI)

FLL engaged internal (FEI) is the default mode of operation and is entered when all the following conditions occur:

- 00b is written to ICS_C1[CLKS].
- 1b is written to ICS_C1[IREFS].

In FLL engaged internal mode, the ICSOUT clock is derived from the FLL clock, which is controlled by the internal reference clock. The FLL loop locks the frequency to 1024 times the internal reference frequency. The internal reference clock is enabled.

13.5.1.2 FLL engaged external (FEE)

The FLL engaged external (FEE) mode is entered when all the following conditions occur:

- 00b is written to ICS_C1[CLKS].
- 0b is written to ICS_C1[IREFS].
- ICS_C1[RDIV] and OSC_CR[RANGE] are written to divide external reference clock to be within the range of 31.25 kHz to 39.0625 kHz.

In FLL engaged external mode, the ICSOUT clock is derived from the FLL clock which is controlled by the external reference clock source.The FLL loop locks the frequency to 1024 times the external reference frequency, as selected by ICS_C1[RDIV] and OSC_CR[RANGE]. The external reference clock is enabled.

13.5.1.3 FLL bypassed internal (FBI)

The FLL bypassed internal (FBI) mode is entered when all the following conditions occur:

- 01b is written to ICS_C1[CLKS].
- 1b is written to ICS_C1[IREFS].
- BDM mode is active or ICS_C2[LP] bit is written to 0.

In FLL bypassed internal mode, the ICSOUT clock is derived from the internal reference clock. The FLL clock is controlled by the internal reference clock, and the FLL loop locks the FLL frequency to 1024 times the internal reference frequency. The internal reference clock is enabled.

13.5.1.4 FLL bypassed internal low power (FBILP)

The FLL bypassed internal low power (FBILP) mode is entered when all the following conditions occur:

- 01b is written to ICS_C1[CLKS].
- 1b is written to ICS_C1[IREFS].
- BDM mode is not active and ICS_C2[LP] bit is written to 1b.

In FLL bypassed internal low-power mode, the ICSOUT clock is derived from the internal reference clock and the FLL is disabled. The internal reference clock is enabled.

13.5.1.5 FLL bypassed external (FBE)

The FLL bypassed external (FBE) mode is entered when all the following conditions occur:

- 10b is written to ICS_C1[CLKS].
- 0b is written to ICS_C1[IREFS].
- ICS_C1[RDIV] and OSC_CR[RANGE] fields are written to divide external reference clock to be within the range of 31.25 kHz to 39.0625 kHz.
- BDM mode is active or 0b is written to ICS_C2[LP].

In FLL bypassed external mode, the ICSOUT clock is derived from the external reference clock source. The FLL clock is controlled by the external reference clock, and the FLL loop locks the FLL frequency to 1024 times the external reference frequency, as selected by ICS_C1[RDIV] and OSC_CR[RANGE], the external reference clock is enabled.

13.5.1.6 FLL bypassed external low power (FBELP)

The FLL bypassed external low-power (FBELP) mode is entered when all the following conditions occur:

- 10b is written to ICS_C1[CLKS].
- 0b is written to ICS_C1[IREFS].
- BDM mode is not active and ICS_C2[LP] bit is written to 1b.

In FLL bypassed external low-power mode, the ICSOUT clock is derived from the external reference clock source and the FLL is disabled. The external reference clock source is enabled.

13.5.1.7 Stop

NOTE

The DCO frequency changes from the pre-stop value to its reset value and the FLL need to re-acquire the lock before the frequency is stable. Timing sensitive operations must wait for the FLL acquisition time, $t_{Acquire}$, before executing.

Stop mode is entered whenever the MCU enters a STOP state. In this mode, all ICS clock signals are static except in the following cases:

ICSIRCLK will be active in Stop mode when all the following conditions occur:

- 1b is written to ICS_C1[IRCLKEN].
- 1b is written to ICS_C1[IREFSTEN].

13.5.2 Mode switching

ICS_C1[IREFS] can be changed at anytime, but the actual switch to the newly selected clock is shown by ICS_S[IREFST]. When switching between FLL engaged internal (FEI) and FLL engaged external (FEE) modes, the FLL begins locking again after the switch is completed.

ICS_C1[CLKS] can also be changed at anytime, but the actual switch to the newly selected clock is shown by ICS_S[CLKST]. If the newly selected clock is not available, the previous clock remains selected.

NOTE

When mode switching is from FEE, FBE or FBELP to FEI, it is suggested to wait IREFST switch completion, then change ICS_C1[CLKS].

13.5.3 Bus frequency divider

ICS_C2[BDIV] can be changed anytime and the actual switch to the new frequency occurs immediately.

13.5.4 Low-power field usage

The Low-Power (LP) field in the ICS_C2 register is provided to allow the FLL to be disabled and thus conserve power when it is not being used.

However, in some applications it may be desirable to allow the FLL to be enabled and to lock for maximum accuracy before switching to an FLL engaged mode. To do this, write 0b to ICS_C2[LP].

13.5.5 Internal reference clock

When ICS_C1[IRCLKEN] is set, the internal reference clock signal is presented as ICSIRCLK, which can be used as an additional clock source. To re-target the ICSIRCLK frequency, write a new value to the ICS_C3[SCTRIM] bits to trim the period of the internal reference clock:

- Writing a larger value slows down the ICSIRCLK frequency.
- Writing a smaller value to the ICS_C3 register speeds up the ICSIRCLK frequency.

The trim bits affect the ICSOUT frequency if the ICS is in FLL engaged internal (FEI), FLL bypassed internal (FBI), or FLL bypassed internal low power (FBILP) mode.

Until ICSIRCLK is trimmed, programming low bus divider (ICS_C2[BDIV]) factors may result in ICSOUT frequencies that exceed the maximum chip-level frequency and violate the chip-level clock timing specifications.

If ICS_C1[IREFSTEN] is set and 1b is written to ICS_C1[IRCLKEN], the internal reference clock keeps running during Stop mode in order to provide a fast recovery upon exiting Stop mode.

All MCU devices are factory programmed with a trim value in a reserved memory location. This value is uploaded to the ICS_C3 register and ICS_C4[SCFTRIM] during any reset initialization. For finer precision, trim the internal oscillator in the application and set ICS_C4[SCFTRIM] accordingly.

13.5.6 Fixed frequency clock

The ICS presents the divided FLL reference clock as ICSFFCLK for use as an additional clock source. ICSFFCLK frequency must be no more than 1/4 of the ICSOUT frequency to be valid. Because of this requirement, in bypass modes, the ICSFFCLK is valid only in bypass external modes (FBE and FBELP) for the following conditions of ICS_C2[BDIV], and divider factor of ICS_C1[RDIV] and OSC_CR[RANGE] values:

if OSC_CR[RANGE] is high,

- ICS_C2[BDIV] = 000, ICS_C1[RDIV] ≥ 010
- ICS_C2[BDIV] = 001 (divide by 2), ICS_C1[RDIV] ≥ 011
- ICS_C2[BDIV] = 010 (divide by 4), ICS_C1[RDIV] ≥ 100
- ICS_C2[BDIV] = 011 (divide by 8), ICS_C1[RDIV] ≥ 101

13.5.7 FLL lock and clock monitor

13.5.7.1 FLL clock lock

In FBE and FEE modes, the clock detector source uses the external reference as the reference. When FLL is detected from lock to unlock, ICS_S[LOLS] is set. An interrupt will be generated if ICS_C4[LOLIE] is set. ICS_S[LOLS] is cleared by reset or by writing a logic 1 to ICS_S[LOLS] when ICS_S[LOLS] is set. Writing a logic 0 to ICS_S[LOLS] has no effect.

In FBI and FEI modes, the lock detector source uses the internal reference as the reference. When FLL is detected from lock to unlock, ICS_S[LOLS] is set. An interrupt will be generated if ICS_C4[LOLIE] is set. ICS_S[LOLS] is cleared by reset or by writing a logic 1 to ICS_S[LOLS] when ICS_S[LOLS] is set. Writing a logic 0 to ICS_S[LOLS] has no effect.

In FBELP and FBILP modes, the FLL is not on so that lock detect function is not applicable.

13.5.7.2 External reference clock monitor

In FBE, FEE, or FBELP modes, if 1 is written to ICS_C4[CME], the clock monitor is enabled. If the external reference falls below a certain frequency, the MCU will reset. The will be set to indicate the error.

Chapter 14
Oscillator (OSC)

14.1 Chip specific OSC information

NOTE

The OSC_OUT in this chapter is the OSCOUT from chip specific view.

14.2 Introduction

14.2.1 Overview

The OSC module provides the clock source for the MCU. The OSC module, in conjunction with an external crystal or resonator, generates a clock for the MCU that can be used as reference clock or bus clock.

14.2.2 Features and modes

Key features of the OSC module are:

- Supports 32 kHz crystals (low range mode)
- Supports 4–20 MHz crystals and resonators (high range mode)
- Automatic gain control (AGC) to optimize power consumption in both frequency ranges using low-power mode (low gain mode)
- High gain option in both frequency ranges: 32 kHz, 4–20 MHz
- Voltage and frequency filtering to guarantee clock frequency and stability
- Supports to be enabled by ICS.

14.2.3 Block diagram

See the following figure for OSC module block diagram.

The OSC module uses a crystal or resonator to generate three filtered oscillator clock signals(XTL_CLK). The XTL_CLK can work in Stop mode since they come from Hard block which always has power.

The OSCOS decides whether OSC_OUT comes from internal oscillators(XTL_CLK) or directly from external clock driven on EXTAL pin. The OSCOS signal allows the XTAL pad to be used as I/O or test clock.

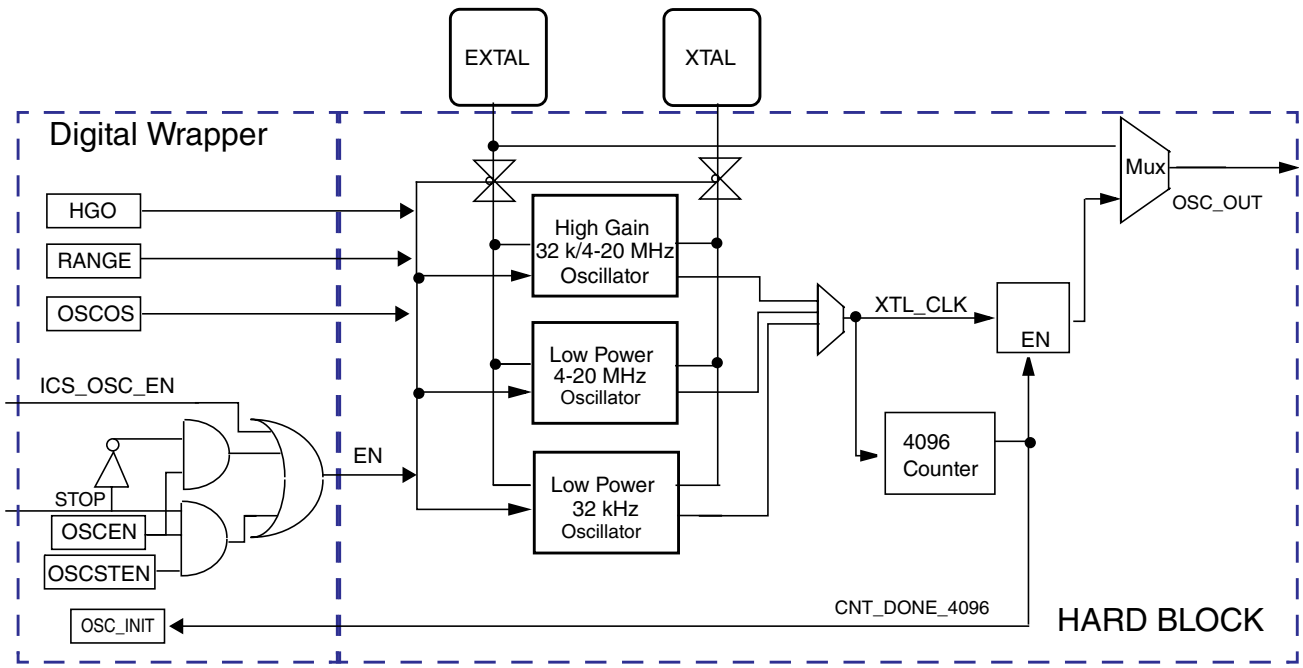


Figure 14-1. OSC module block diagram

14.3 Signal description

The following table shows the user-accessible signals available for the OSC module. See the chip-level specification to find out which signals are actually connected to external pins.

Table 14-1. OSC signal descriptions

Signal	Description	I/O
EXTAL	External clock/oscillator input	Analog input
XTAL	Oscillator output	Analog output

14.4 External crystal / resonator connections

The connections for a crystal/resonator frequency reference are shown in Figure 14-2 and Figure 14-3. When using low-frequency, low-power mode, the only external component is the crystal or resonator itself. In the other oscillator modes, load capacitors (C_x, C_y) and feedback resistor (R_F) are required. In addition, a series resistor (R_S) may be used in high-gain modes. Recommended component values are listed in the data sheet.

Table 14-2. External crystal/resonator connections

Oscillator mode	Connections
Low frequency, high gain	Connection2
Low frequency, low-power	Connection1
High frequency, high gain (4–20 MHz)	Connection2
High frequency, low-power (4–20 MHz)	Connection2

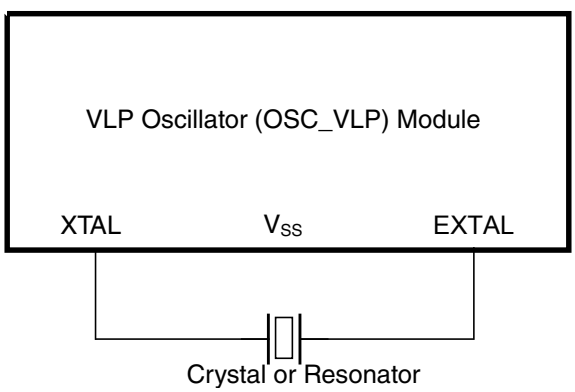


Figure 14-2. Crystal/resonator connections - connection 1

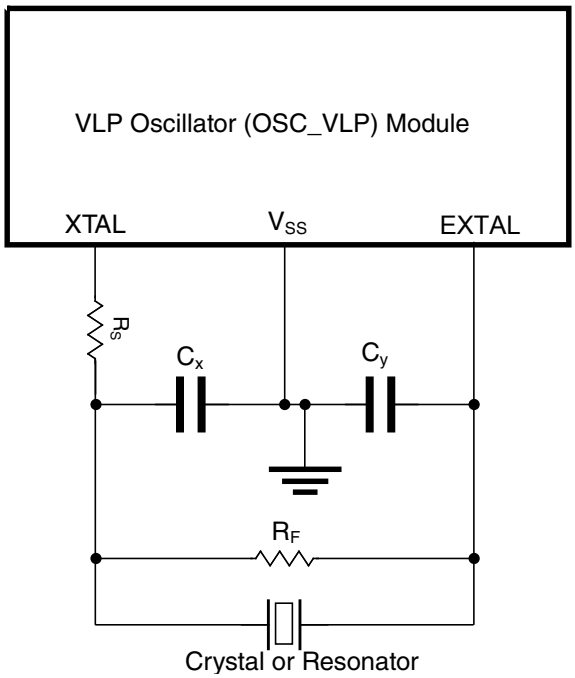


Figure 14-3. Crystal/resonator connections - connection 2

14.5 External clock connections

In external clock mode (OSC_CR[OSCOS] = 0), the pins can be connected as shown in the following figure.

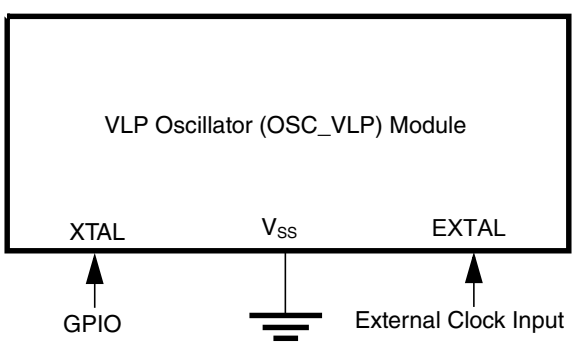


Figure 14-4. External clock connections

14.6 Memory map and register descriptions

OSC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
303E	OSC Control Register (OSC_CR)	8	R/W	00h	14.6.1/219

14.6.1 OSC Control Register (OSC_CR)

Address: 303Eh base + 0h offset = 303Eh

Bit	7	6	5	4	3	2	1	0
Read	OSCEN	0	OSCSTEN	OSCOS	0	RANGE	HGO	OSCINIT
Write								
Reset	0	0	0	0	0	0	0	0

OSC_CR field descriptions

Field	Description
7 OSCEN	OSC Enable Enables the OSC module. The OSC module can also be enabled by the ICS module. 0 OSC module is disabled. 1 OSC module is enabled.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 OSCSTEN	OSC Enable in Stop mode Controls whether or not the OSC clock remains enabled when MCU enters Stop mode and OSCEN is set. OSCSTEN has no effect if ICS requests OSC enable. 0 OSC clock is disabled in Stop mode. 1 OSC clock stays enabled in Stop mode.
4 OSCOS	OSC Output Select Selects the output clock of the OSC module. 0 External clock source from EXTAL pin is selected. 1 Oscillator clock source is selected.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 RANGE	Frequency Range Select Selects the frequency range for the OSC module. This bit must be configured before the OSC is enabled and DO NOT change it after the OSC is enabled

Table continues on the next page...

OSC_CR field descriptions (continued)

Field	Description
	0 Low frequency range of 32 kHz. 1 High frequency range of 4–20 MHz.
1 HGO	High Gain Oscillator Select Controls the OSC mode of operation. 0 Low-power mode 1 High-gain mode
0 OSCINIT	OSC Initialization This field is set after the initialization cycles of oscillator are completed. 0 Oscillator initialization is not complete. 1 Oscillator initialization is completed.

14.7 Functional description

14.7.1 OSC module states

There are three states of the OSC module. A state diagram is shown in Figure 14-5. The states and the transitions among each other are described in this section.

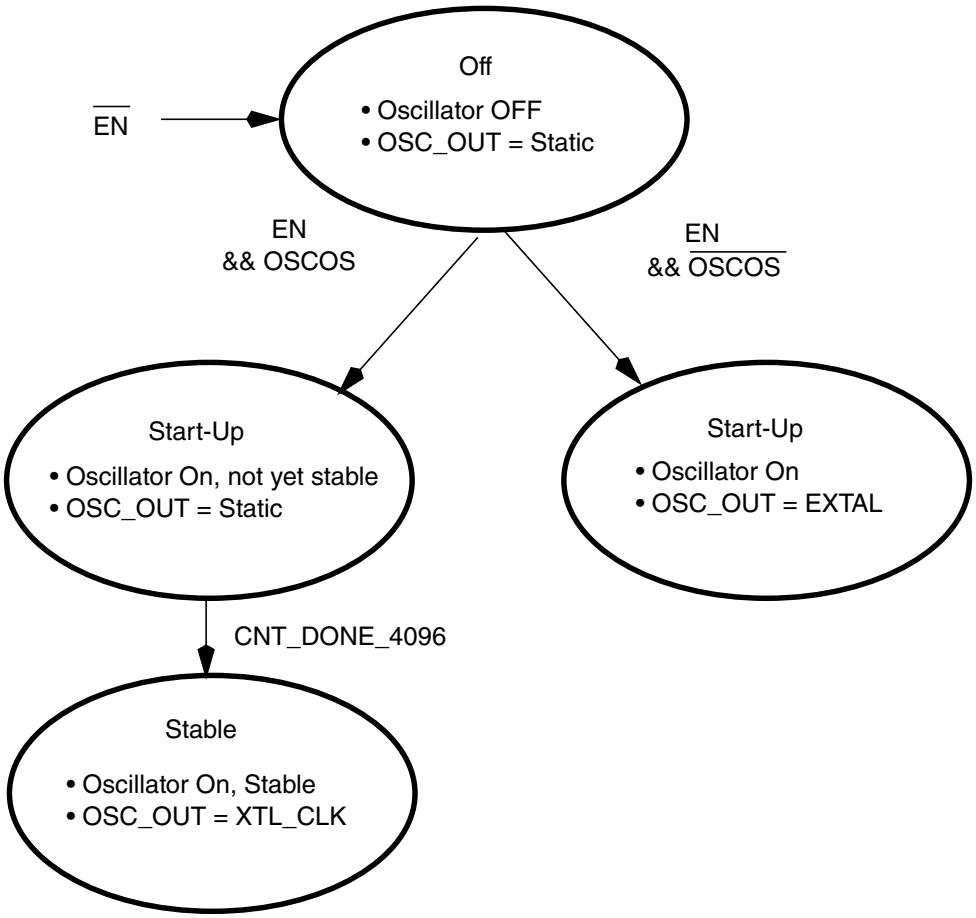


Figure 14-5. OSC module state diagram

EN is decided by OSC_CR[OSCEN], Stop, OSC_CR[OSCSTEN], and external request (ICS_OSC_EN). See the following table for details.

Table 14-3. EN status

EN	ICS_OSC_EN	OSC_CR[OSCEN]	OSC_CR[OSCSTEN]	Stop
1	1	-	-	-
1	0	1	-	0
1	0	1	1	1
0	0	1	0	1
0	0	0	-	-

14.7.1.1 Off

The off state is entered whenever the EN signal is negated. Upon entering this state, XTL_CLK and OSC_OUT is static. The EXTAL and XTAL pins are also decoupled from all other oscillator circuitry in this state. The OSC module circuitry is configured to draw minimal current.

14.7.1.2 Oscillator startup

The oscillator startup state is entered whenever the oscillator is first enabled (EN transitions high) and OSC_CR[OSCOS] is high. In this state, the OSC module is enabled and oscillations are starting up, but have not yet stabilized. When the oscillation amplitude becomes large enough to pass through the input buffer, XTL_CLK begins clocking the counter. When the counter has seen 4096 cycles of XTL_CLK, the oscillator is considered stable and XTL_CLK is passed to the output clock OSC_OUT.

14.7.1.3 Oscillator stable

The oscillator stable state is entered whenever the oscillator is enabled (EN is high), OSC_CR[OSCOS] is high, and the counter has seen 4096 cycles of XTL_CLK (CNT_DONE_4096 is high). In this state, the OSC module is producing a stable output clock on OSC_OUT. Its frequency is determined by the external components being used.

14.7.1.4 External clock mode

The external clock state is entered when the oscillator is enabled(EN is high) and OSC_CR[OSCOS] is low. In this state, the OSC module is set up to buffer (with hysteresis) a clock from EXTAL onto the OSC_OUT. Its frequency is determined by the external clock being supplied.

14.7.2 OSC module modes

The oscillator is a Pierce-type oscillator that supports external crystals or resonators operating over the frequency ranges shown in the following table. These modes assume EN = 1, OSC_CR[OSCOS] = 1.

Table 14-4. Oscillator modes

RANGE	HGO	Mode	Frequency range
0	1	Low-frequency, high-gain	f_{lo}(min) up to f_{lo}(max)
0	0	Low-frequency, low-power (VLP)	
1	1	High-frequency mode1, high-gain	f_{hi}(min) up to f_{hi}(max)
1	0	High-frequency mode1, low-power	

14.7.2.1 Low-frequency, high-gain mode

In low-frequency, high-gain mode (OSC_CR[RANGE] = 0, OSC_CR[HGO] = 1) the oscillator uses a simple inverter-style amplifier. The gain is set to achieve rail-to-rail oscillation amplitudes. The oscillator input buffer in this mode is single-ended. It provides low pass frequency filtering as well as hysteresis for voltage filtering and converts the output to logic levels.

14.7.2.2 Low-frequency, low-power mode

In low-frequency, low-power mode (OSC_CR[RANGE] = 0, OSC_CR[HGO] = 0), the oscillator uses a gain control loop to minimize power consumption. As the oscillation amplitude increases, the amplifier current is reduced. This continues until a desired amplitude is achieved at steady-state.

The oscillator input buffer in this mode is single-ended. It provides low pass frequency filtering as well as hysteresis for voltage filtering and converts the output to logic levels.

In this mode, the amplifier inputs, gain-control input, and input buffer input are all capacitively coupled for leakage tolerance (not sensitive to the DC level of EXTAL).

Also in this mode, all external components except for the resonator itself are integrated, which includes the load capacitors and feeback resistor which biases EXTAL.

14.7.2.3 High-frequency, high-gain mode

In high-frequency, high-gain Mode (OSC_CR[RANGE] = 1, OSC_CR[HGO] = 1), the oscillator uses a simple inverter-style amplifier. The gain is set to achieve rail-to-rail oscillation amplitudes.

The oscillator input buffer in this mode is single-ended. It provides low pass frequency filtering as well as hysteresis for voltage filtering and converts the output to logic levels.

14.7.2.4 High-frequency, low-power mode

In high-frequency, low-power mode (OSC_CR[RANGE] = 1, OSC_CR[HGO] = 0) the oscillator uses a gain control loop to minimize power consumption. As the oscillation amplitude increases, the amplifier current is reduced. This continues until a desired amplitude is achieved at steady-state.

The oscillator input buffer in this mode is differential. It provides low pass frequency filtering as well as hysteresis for voltage filtering and converts the output to logic levels.

14.7.3 Counter

The oscillator output clock (OSC_OUT) is gated off until the counter has detected 4096 cycles of its input clock (XTL_CLK). Once 4096 cycles are complete, the counter passes XTL_CLK onto OSC_OUT. This counting timeout is used to guarantee output clock stability.

14.7.4 Reference clock pin requirements

The OSC module requires use of both the EXTAL and XTAL pins to generate an output clock in oscillator mode but requires only the EXTAL pin in external clock mode. The EXTAL and XTAL pins can be used for I/O or test clock purposes as long as the specifications listed in the data sheet are met.

Chapter 15
FlexTimer Module (FTM)

15.1 Chip specific FTM information

This device contains up to two FTM modules of one 6-channel FTM2 and one 2-channel FTM0. Each FTM module has independent external clock input. Both FTM0 and FTM2 are fully compatible with the TPM.

The fault shutdown function for PWM output is implemented in the FDS module, please refer to the Fault Detection and Shutdown (FDS) for more detail. Software controlled PWM output function is also implemented in this chip, please refer to the FTM software controlled output and System Control for more detail.

Table 15-1. FTM module external signals

FTM	Functions	Default	Alternate
FTM0	Channel 0	PTA0/FTM0CH0	PTA5/FTM0CH0
	Channel 1	PTA1/FTM0CH1	PTA4/FTM0CH1
	alternate clock	PTA5/TCLK0	
FTM2	Channel 0	PTC0/FTM2CH0	
	Channel 1	PTC1/FTM2CH1	
	Channel 2	PTC2/FTM2CH2	
	Channel 3	PTC3/FTM2CH3	
	Channel 4	PTB4/FTM2CH4	
	Channel 5	PTB5/FTM2CH5	
	alternate clock	PTB3/TCLK2	

The memory map in this chapter shows the whole registers the FTM modules can support, but for this device, only the following registers take effect.

Table 15-2. FTM module registers

FTM	Registers
FTM0	SC, CNTH, CNTL, MODH, MODL, C0SC, C0VH, C0VL,C1SC, C1VH, C1VL

Table continues on the next page...

Table 15-2. FTM module registers (continued)

FTM	Registers
FTM2	All the FTM2 registers

15.2 Introduction

NOTE

For the chip-specific implementation details of this module's instances, see the chip configuration information.

The FlexTimer module is a two to eight channel timer which supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The FTM time reference is a 16-bit unsigned counter.

15.2.1 FlexTimer philosophy

The FlexTimer is built upon a very simple timer used for many years on NXP's 8-bit microcontrollers, the HCS08 Timer PWM Module – TPM. The FlexTimer extends the functionality to meet the demands of motor control, digital lighting solutions, and power conversion, while providing low cost and backwards compatibility with the TPM module.

All of the features common with the TPM module have fully backwards compatible register assignments and the FlexTimer can use code on the same core platform without change to perform the same functions.

15.2.2 Features

The FTM features include:

- Selectable FTM source clock:
  - Source clock can be the system clock, the fixed frequency clock, or an external clock
  - Fixed frequency clock is an additional clock input to allow the selection of an on chip clock source other than the system clock
  - Selecting external clock connects FTM clock to a chip level input pin therefore allowing to synchronize the FTM counter with an off chip clock source

- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- FTM has a 16-bit counter
  - It can be a free-running counter or a counter with selectable final value
  - The counting can be up or up-down
- Each channel can be configured for input capture, output compare, or edge-aligned PWM mode
- In input capture mode:
  - The capture can occur on rising edges, falling edges or both edges
- In output compare mode the output signal can be set, cleared, or toggled on match
- All channels can be configured for center-aligned PWM mode
- The generation of an interrupt per channel
- The generation of an interrupt when the counter overflows
- Backwards compatible with TPM

15.2.3 Modes of operation

When the MCU is in active BDM background or BDM foreground mode, the FTM temporarily suspends all counting until the MCU returns to normal user operating mode. During stop mode, all FTM input clocks are stopped, so the FTM is effectively disabled until clocks resume. During wait mode, the FTM continues to operate normally. If the FTM does not need to produce a real time reference or provide the interrupt sources needed to wake the MCU from wait mode, the power can then be saved by disabling FTM functions before entering wait mode.

15.2.4 Block diagram

The FTM uses one input/output (I/O) pin per channel, CHn (FTM channel (n)) where n is the channel number (0–7).

The following figure shows the FTM structure. The central component of the FTM is the 16-bit counter with programmable final value and its counting can be up or up-down.

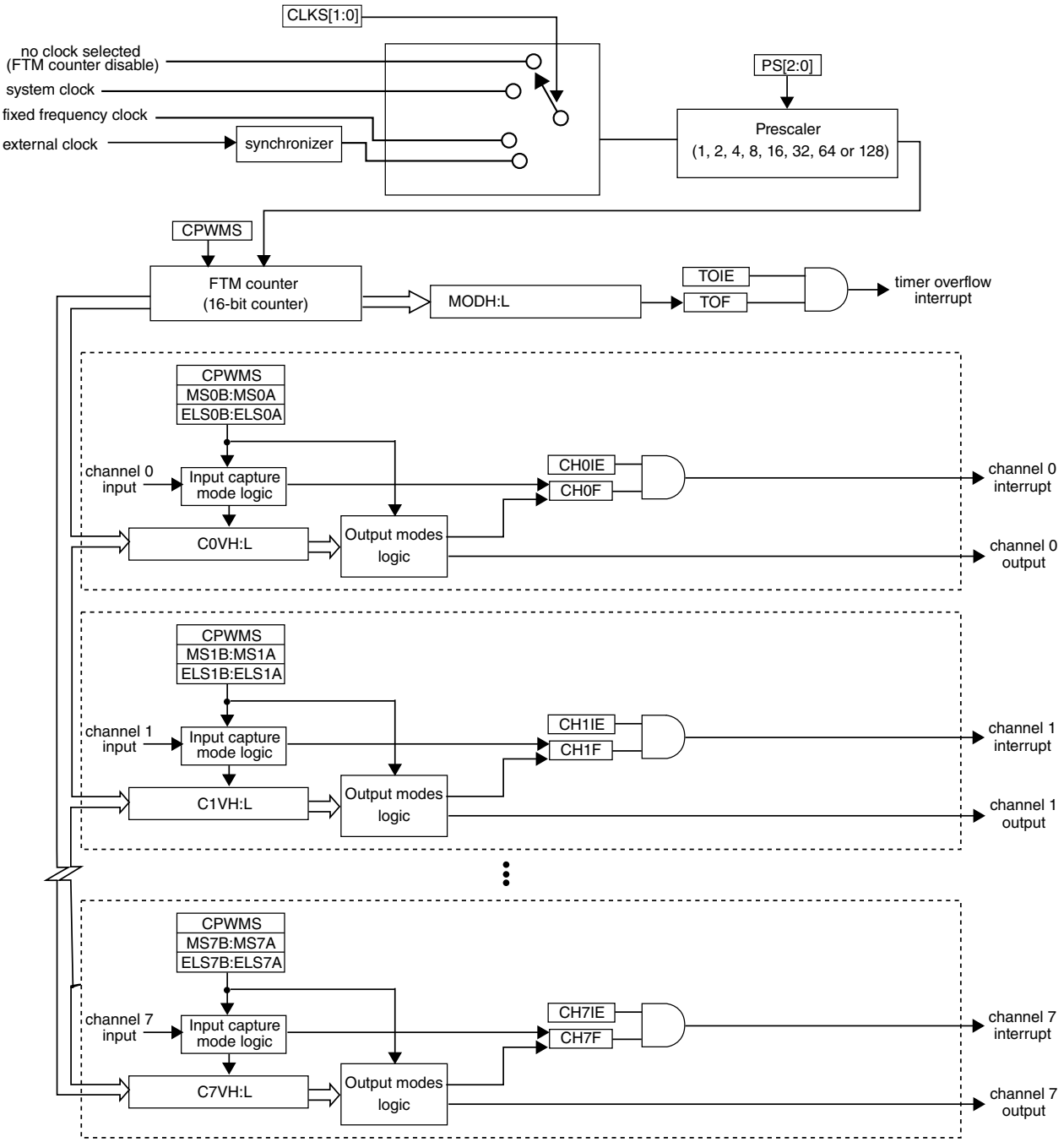


Figure 15-1. FTM block diagram

15.3 Signal description

The following table shows the user-accessible signals for the FTM.

Table 15-3. Signal properties

Name	Function
EXTCLK	External clock – FTM external clock can be selected to drive the FTM counter.
CHn[1]	Channel (n) – I/O pin associated with FTM channel (n).

1. n = channel number (0 to 7)

15.3.1 EXTCLK — FTM external clock

The external clock input signal is used as the FTM counter clock if selected by CLKS[1:0] bits in the SC register. This clock signal must not exceed 1/4 of system clock frequency. The FTM counter prescaler selection and settings are also used when an external clock is selected.

15.3.2 CHn — FTM channel (n) I/O pin

Each FTM channel can be configured to operate either as input or output. The direction associated with each channel, input or output, is selected according to the mode assigned for that channel.

15.4 Memory map and register definition

This section provides a detailed description of all FTM registers.

15.4.1 Module memory map

This section presents a high-level summary of the FTM registers and how they are mapped.

15.4.2 Register descriptions

This section consists of register descriptions in address order.

FTM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
20	Status and Control (FTM0_SC)	8	R/W	00h	15.4.3/231
21	Counter High (FTM0_CNTH)	8	R/W	00h	15.4.4/232
22	Counter Low (FTM0_CNTL)	8	R/W	00h	15.4.5/233
23	Modulo High (FTM0_MODH)	8	R/W	00h	15.4.6/233
24	Modulo Low (FTM0_MODL)	8	R/W	00h	15.4.7/234
25	Channel Status and Control (FTM0_C0SC)	8	R/W	00h	15.4.8/235
26	Channel Value High (FTM0_C0VH)	8	R/W	00h	15.4.9/236
27	Channel Value Low (FTM0_C0VL)	8	R/W	00h	15.4.10/237
28	Channel Status and Control (FTM0_C1SC)	8	R/W	00h	15.4.8/235
29	Channel Value High (FTM0_C1VH)	8	R/W	00h	15.4.9/236
2A	Channel Value Low (FTM0_C1VL)	8	R/W	00h	15.4.10/237
2B	Channel Status and Control (FTM0_C2SC)	8	R/W	00h	15.4.8/235
2C	Channel Value High (FTM0_C2VH)	8	R/W	00h	15.4.9/236
2D	Channel Value Low (FTM0_C2VL)	8	R/W	00h	15.4.10/237
2E	Channel Status and Control (FTM0_C3SC)	8	R/W	00h	15.4.8/235
2F	Channel Value High (FTM0_C3VH)	8	R/W	00h	15.4.9/236
30	Channel Value Low (FTM0_C3VL)	8	R/W	00h	15.4.10/237
31	Channel Status and Control (FTM0_C4SC)	8	R/W	00h	15.4.8/235
32	Channel Value High (FTM0_C4VH)	8	R/W	00h	15.4.9/236
33	Channel Value Low (FTM0_C4VL)	8	R/W	00h	15.4.10/237
34	Channel Status and Control (FTM0_C5SC)	8	R/W	00h	15.4.8/235
35	Channel Value High (FTM0_C5VH)	8	R/W	00h	15.4.9/236
36	Channel Value Low (FTM0_C5VL)	8	R/W	00h	15.4.10/237
30C0	Status and Control (FTM2_SC)	8	R/W	00h	15.4.3/231
30C1	Counter High (FTM2_CNTH)	8	R/W	00h	15.4.4/232
30C2	Counter Low (FTM2_CNTL)	8	R/W	00h	15.4.5/233
30C3	Modulo High (FTM2_MODH)	8	R/W	00h	15.4.6/233
30C4	Modulo Low (FTM2_MODL)	8	R/W	00h	15.4.7/234
30C5	Channel Status and Control (FTM2_C0SC)	8	R/W	00h	15.4.8/235
30C6	Channel Value High (FTM2_C0VH)	8	R/W	00h	15.4.9/236
30C7	Channel Value Low (FTM2_C0VL)	8	R/W	00h	15.4.10/237
30C8	Channel Status and Control (FTM2_C1SC)	8	R/W	00h	15.4.8/235
30C9	Channel Value High (FTM2_C1VH)	8	R/W	00h	15.4.9/236
30CA	Channel Value Low (FTM2_C1VL)	8	R/W	00h	15.4.10/237
30CB	Channel Status and Control (FTM2_C2SC)	8	R/W	00h	15.4.8/235
30CC	Channel Value High (FTM2_C2VH)	8	R/W	00h	15.4.9/236
30CD	Channel Value Low (FTM2_C2VL)	8	R/W	00h	15.4.10/237
30CE	Channel Status and Control (FTM2_C3SC)	8	R/W	00h	15.4.8/235

Table continues on the next page...

FTM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
30CF	Channel Value High (FTM2_C3VH)	8	R/W	00h	15.4.9/236
30D0	Channel Value Low (FTM2_C3VL)	8	R/W	00h	15.4.10/237
30D1	Channel Status and Control (FTM2_C4SC)	8	R/W	00h	15.4.8/235
30D2	Channel Value High (FTM2_C4VH)	8	R/W	00h	15.4.9/236
30D3	Channel Value Low (FTM2_C4VL)	8	R/W	00h	15.4.10/237
30D4	Channel Status and Control (FTM2_C5SC)	8	R/W	00h	15.4.8/235
30D5	Channel Value High (FTM2_C5VH)	8	R/W	00h	15.4.9/236
30D6	Channel Value Low (FTM2_C5VL)	8	R/W	00h	15.4.10/237

15.4.3 Status and Control (FTMx_SC)

SC contains the overflow status flag and control bits used to configure the interrupt enable, FTM configuration, clock source, and prescaler factor. These controls relate to all channels within this module.

Address: Base address + 0h offset

Bit	7	6	5	4	3	2	1	0
Read	TOF	TOIE	CPWMS	CLKS		PS		
Write	0							
Reset	0	0	0	0	0	0	0	0

FTMx_SC field descriptions

Field	Description
7 TOF	Timer Overflow Flag Set by hardware when the FTM counter passes the value in the Counter Modulo registers. The TOF bit is cleared by reading the SC register while TOF is set and then writing a 0 to TOF bit. Writing a 1 to TOF has no effect. If another FTM overflow occurs between the read and write operations, the write operation has no effect; therefore, TOF remains set indicating an overflow has occurred. In this case a TOF interrupt request is not lost due to the clearing sequence for a previous TOF. 0 FTM counter has not overflowed. 1 FTM counter has overflowed.
6 TOIE	Timer Overflow Interrupt Enable Enables FTM overflow interrupts. 0 Disable TOF interrupts. Use software polling. 1 Enable TOF interrupts. An interrupt is generated when TOF equals one.

Table continues on the next page...

FTMx_SC field descriptions (continued)

Field	Description
5 CPWMS	Center-aligned PWM Select Selects CPWM mode. This mode configures the FTM to operate in up-down counting mode. 0 FTM counter operates in up counting mode. 1 FTM counter operates in up-down counting mode.
4–3 CLKS	Clock Source Selection Selects one of the three FTM counter clock sources. 00 No clock selected (this in effect disables the FTM counter). 01 System clock 10 Fixed frequency clock 11 External clock
PS	Prescale Factor Selection Selects one of 8 division factors for the clock source selected by CLKS. The new prescaler factor affects the clock source on the next system clock cycle after the new value is updated into the register bits. 000 Divide by 1 001 Divide by 2 010 Divide by 4 011 Divide by 8 100 Divide by 16 101 Divide by 32 110 Divide by 64 111 Divide by 128

15.4.4 Counter High (FTMx_CNTH)

The Counter registers contain the high and low bytes of the counter value. Reading either byte latches the contents of both bytes into a buffer where they remain latched until the other half is read. This allows coherent 16-bit reads in either big-endian or little-endian order which makes this more friendly to various compiler implementations. The coherency mechanism is automatically restarted by an MCU reset or any write to the Status and Control register.

Writing any value to COUNT_H or COUNT_L updates the FTM counter with its initial 16-bit value (all zeroes) and resets the read coherency mechanism, regardless of the data involved in the write.

When BDM is active, the FTM counter is frozen (this is the value that you may read); the read coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active, even if one or both counter bytes are read while

BDM is active. This assures that if you were in the middle of reading a 16-bit register when BDM became active, it reads the appropriate value from the other half of the 16-bit value after returning to normal execution.

Address: Base address + 1h offset

Bit	7	6	5	4	3	2	1	0
Read Write	COUNT_H							
Reset	0	0	0	0	0	0	0	0

FTMx_CNTH field descriptions

Field	Description
COUNT_H	Counter value high byte

15.4.5 Counter Low (FTMx_CNTL)

See the description for the Counter High register.

Address: Base address + 2h offset

Bit	7	6	5	4	3	2	1	0
Read Write	COUNT_L							
Reset	0	0	0	0	0	0	0	0

FTMx_CNTL field descriptions

Field	Description
COUNT_L	Counter value low byte

15.4.6 Modulo High (FTMx_MODH)

The Modulo registers contain the high and low bytes of the modulo value for the FTM counter. After the FTM counter reaches the modulo value, the overflow flag (TOF) becomes set at the next clock, and the next value of FTM counter depends on the selected counting method (Counter).

Writing to either byte latches the value into a buffer. The register is updated with the value of their write buffer according to Update of the registers with write buffers.

This write coherency mechanism may be manually reset by writing to the SC register whether BDM is active or not.

When BDM is active, this write coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active, even if one or both bytes of the modulo register are written while BDM is active. Any write to the modulo register bypasses the buffer latches and directly writes to the modulo register while BDM is active.

It is recommended to initialize the FTM counter, by writing to CNTH or CNTL, before writing to the FTM modulo register to avoid confusion about when the first counter overflow will occur.

Address: Base address + 3h offset

Bit	7	6	5	4	3	2	1	0
Read Write	MOD_H							
Reset	0	0	0	0	0	0	0	0

FTMx_MODH field descriptions

Field	Description
MOD_H	High byte of the modulo value

15.4.7 Modulo Low (FTMx_MODL)

See the description for the Modulo High register.

Address: Base address + 4h offset

Bit	7	6	5	4	3	2	1	0
Read Write	MOD_L							
Reset	0	0	0	0	0	0	0	0

FTMx_MODL field descriptions

Field	Description
MOD_L	Low byte of the modulo value

15.4.8 Channel Status and Control (FTM*x*_C*n*SC)

CnSC contains the channel-interrupt-status flag and control bits used to configure the interrupt enable, channel configuration, and pin function.

Table 15-4. Mode, edge, and level selection

CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration
X	XX	00	None	Pin not used for FTM
0	00	01	Input capture	Capture on Rising Edge Only
		10		Capture on Falling Edge Only
		11		Capture on Rising or Falling Edge
	01	01	Output compare	Toggle Output on match
		10		Clear Output on match
		11		Set Output on match
	1X	10	Edge-aligned PWM	High-true pulses (clear Output on match)
		X1		Low-true pulses (set Output on match)
1	XX	10	Center-aligned PWM	High-true pulses (clear Output on match-up)
		X1		Low-true pulses (set Output on match-up)

Address: Base address + 5h offset + (3d × i), where i=0d to 5d

Bit	7	6	5	4	3	2	1	0
Read	CHF	CHIE	MSB	MSA	ELSB	ELSA	0	0
Write	0							
Reset	0	0	0	0	0	0	0	0

FTM*x*_C*n*SC field descriptions

Field	Description
7 CHF	Channel Flag Set by hardware when an event occurs on the channel. CHF is cleared by reading the CnSC register while CHnF is set and then writing a 0 to the CHF bit. Writing a 1 to CHF has no effect. If another event occurs between the read and write operations, the write operation has no effect; therefore, CHF remains set indicating an event has occurred. In this case a CHF interrupt request is not lost due to the clearing sequence for a previous CHF.

Table continues on the next page...

FTMx_C*n*SC field descriptions (continued)

Field	Description
	0 No channel event has occurred. 1 A channel event has occurred.
6 CHIE	Channel Interrupt Enable Enables channel interrupts. 0 Disable channel interrupts. Use software polling. 1 Enable channel interrupts.
5 MSB	Channel Mode Select Used for further selections in the channel logic. Its functionality is dependent on the channel mode. See the table in the register description.
4 MSA	Channel Mode Select Used for further selections in the channel logic. Its functionality is dependent on the channel mode. See the table in the register description.
3 ELSB	Edge or Level Select The functionality of ELSB and ELSA depends on the channel mode. See the table in the register description.
2 ELSA	Edge or Level Select The functionality of ELSB and ELSA depends on the channel mode. See the table in the register description.
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

15.4.9 Channel Value High (FTMx_C*n*VH)

These registers contain the captured FTM counter value of the input capture function or the match value for the output modes.

In input capture mode, reading a single byte in CnV latches the contents into a buffer where they remain latched until the other byte is read. This latching mechanism also resets, or becomes unlatched, when the CnSC register is written whether BDM mode is active or not. Any write to the channel registers is ignored during this mode.

When BDM is active, the read coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active, even if one or both bytes of the channel value register are read while BDM is active. This ensures that if you were in the middle of reading a 16-bit register when BDM became active, it reads the appropriate value from the other half of the 16-bit value after returning to normal execution. Any read of the CnV registers in BDM mode bypasses the buffer latches and returns the value of these registers and not the value of their read buffer.

In output modes, writing to CnV latches the value into a buffer. The registers are updated with the value of their write buffer according to Update of the registers with write buffers.

This write coherency mechanism may be manually reset by writing to the CnSC register whether BDM mode is active or not.

When BDM is active, the write coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active even if one or both bytes of the channel value register are written while BDM is active. Any write to the CnV registers bypasses the buffer latches and writes directly to the register while BDM is active. The values written to the channel value registers while BDM is active are used in output modes operation after normal execution resumes. Writes to the channel value registers while BDM is active do not interfere with the partial completion of a coherency sequence. After the write coherency mechanism has been fully exercised, the channel value registers are updated using the buffered values while BDM was not active.

Address: Base address + 6h offset + (3d × i), where i=0d to 5d

Bit	7	6	5	4	3	2	1	0
Read Write	VAL_H							
Reset	0	0	0	0	0	0	0	0

FTMx_C*n*VH field descriptions

Field	Description
VAL_H	Channel Value High Byte Captured FTM counter value of the input capture function or the match value for the output modes

15.4.10 Channel Value Low (FTMx_C*n*VL)

See the description for the Channel Value High register.

Address: Base address + 7h offset + (3d × i), where i=0d to 5d

Bit	7	6	5	4	3	2	1	0
Read Write	VAL_L							
Reset	0	0	0	0	0	0	0	0

FTMx_C*n*VL field descriptions

Field	Description
VAL_L	Channel Value Low Byte Captured FTM counter value of the input capture function or the match value for the output modes

FTMx_C*n*VL field descriptions (continued)

Field	Description

15.5 Functional Description

The following sections describe the FTM features.

The notation used in this document to represent the counters and the generation of the signals is shown in the following figure.

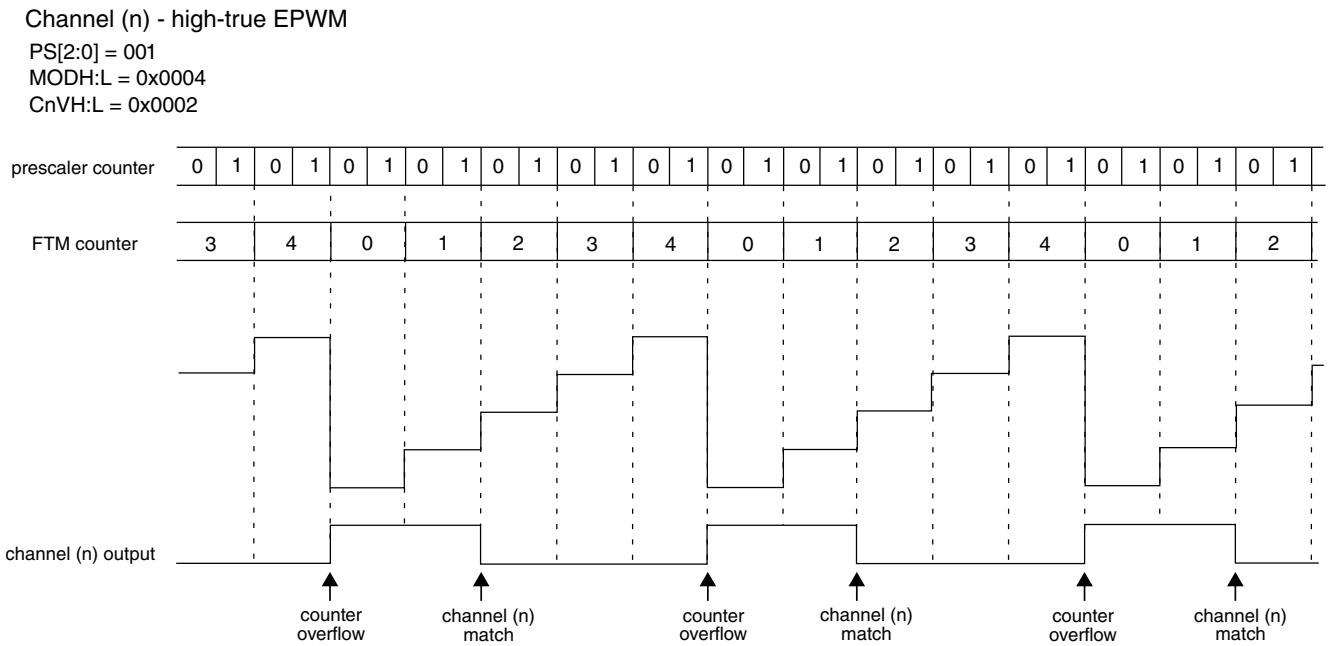


Figure 15-2. Notation used

15.5.1 Clock Source

FTM module has only one clock domain that is the system clock.

15.5.1.1 Counter Clock Source

The CLKS[1:0] bits in the SC register select one of three possible clock sources for the FTM counter or disable the FTM counter. After any MCU reset, CLKS[1:0] = 0:0 so no clock source is selected.

The CLKS[1:0] bits may be read or written at any time. Disabling the FTM counter by writing 0:0 to the CLKS[1:0] bits does not affect the FTM counter value or other registers.

The fixed frequency clock is an alternative clock source for the FTM counter that allows the selection of a clock other than the system clock or an external clock. This clock input is defined by chip integration. Refer to chip specific documentation for further information. Due to FTM hardware implementation limitations, the frequency of the fixed frequency clock must not exceed the system clock frequency.

The external clock passes through a synchronizer clocked by the system clock to ensure that counter transitions are properly aligned to system clock transitions. Therefore, to meet the Nyquist criteria and account for jitter, the frequency of the external clock source must not exceed 1/4 of the system clock frequency.

15.5.2 Prescaler

The selected counter clock source passes through a prescaler that is a 7-bit counter. The value of the prescaler is selected by the PS[2:0] bits. The following figure shows an example of the prescaler counter and FTM counter.

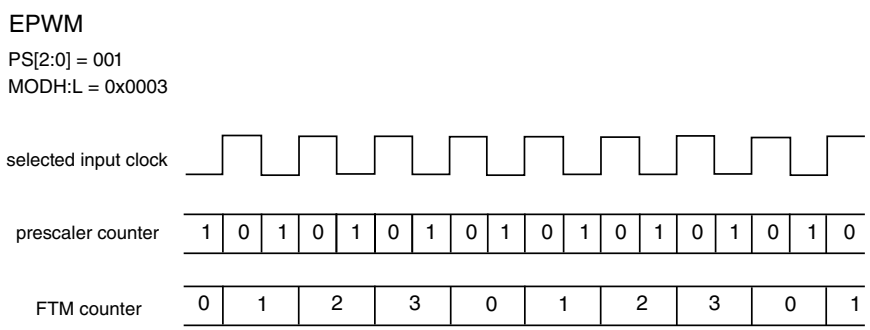


Figure 15-3. Example of the prescaler counter

15.5.3 Counter

The FTM has a 16-bit counter that is used by the channels either for input or output modes. The FTM counter clock is the selected clock divided by the prescaler (see Prescaler).

The FTM counter has these modes of operation:

- up counting (see Up counting)
- up-down counting (see Up-down counting)

15.5.3.1 Up counting

Up counting is selected when (CPWMS = 0).

The starting value of the count is 0x0000 and MODH:L defines the final value of the count; see the following figure. The value of 0x0000 is loaded into the FTM counter, and the counter increments until the value of MODH:L is reached, at which point the counter is reloaded with 0x0000.

The FTM period when using up counting is (MODH:L + 0x0001) × period of the FTM counter clock.

The TOF bit is set when the FTM counter changes from MODH:L to 0x0000.

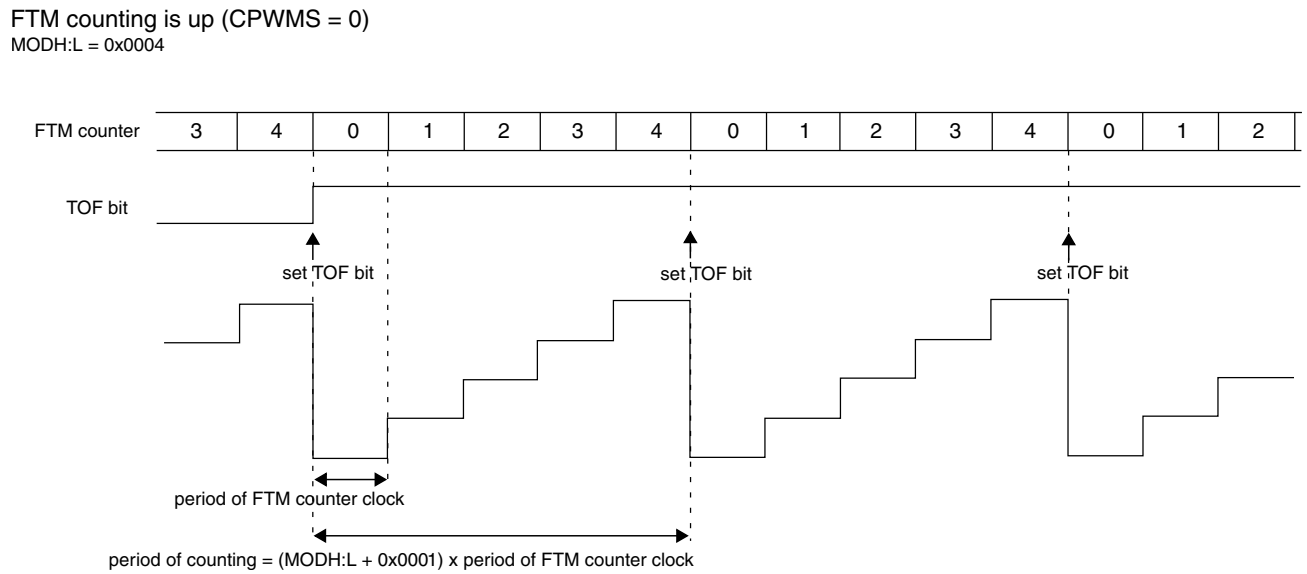


Figure 15-4. Example of FTM up counting

15.5.3.2 Up-down counting

Up-down counting is selected when (CPWMS = 1).

The starting value of the count is 0x0000 and MODH:L defines the final value of the count. The value of 0x0000 is loaded into the FTM counter, and the counter increments until the value of MODH:L is reached, at which point the counter is decremented until it returns to the value of 0x0000 and the up-down counting restarts.

The FTM period when using up-down counting is 2 × (MODH:L) × period of the FTM counter clock.

The TOF bit is set when the FTM counter changes from MODH:L to (MODH:L – 1).

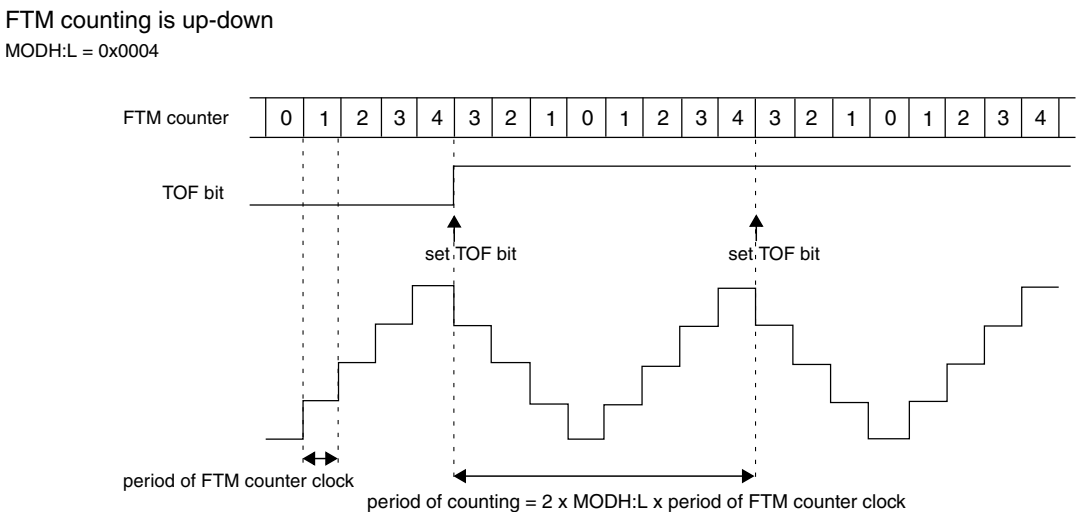


Figure 15-5. Example of up-down counting

15.5.3.3 Free running counter

If (MODH:L = 0x0000 or MODH:L = 0xFFFF), the FTM counter is a free running counter. In this case, the FTM counter runs free from 0x0000 through 0xFFFF and the TOF bit is set when the FTM counter changes from 0xFFFF to 0x0000 See the following figure.

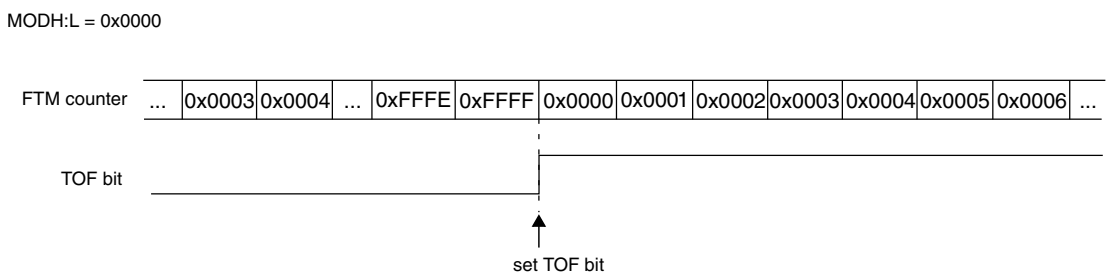


Figure 15-6. Example when the FTM counter is a free running

15.5.3.4 Counter reset

Any write to CNTH or CNTL register resets the FTM counter to the value of 0x0000 and the channels output to its initial value, except for channels in output compare mode.

15.5.4 Input capture mode

The input capture mode is selected when (CPWMS = 0), (MSnB:MSnA = 0:0), and (ELSnB:ELSnA ≠ 0:0).

When a selected edge occurs on the channel input, the current value of the FTM counter is captured into the CnVH:L registers. At the same time, the CHnF bit is set and the channel interrupt is generated if enabled by CHnIE = 1. See the following figure.

When a channel is configured for input capture, the CHn pin is an edge-sensitive input. ELSnB:ELSnA control bits determine which edge, falling or rising, triggers input-capture event. Note that the maximum frequency for the channel input signal to be detected correctly is system clock divided by four, which is required to meet Nyquist criteria for signal sampling.

When either half of the 16-bit capture register (CnVH:L) is read, the other half is latched into a buffer to support coherent 16-bit access in big-endian or little-endian order. This read coherency mechanism can be manually reset by writing to CnSC register.

Writes to the CnVH:L registers are ignored in input capture mode.

While in BDM, the input capture function works as configured. When a selected edge event occurs, the FTM counter value, which is frozen because of BDM, is captured into the CnVH:L registers and the CHnF bit is set.

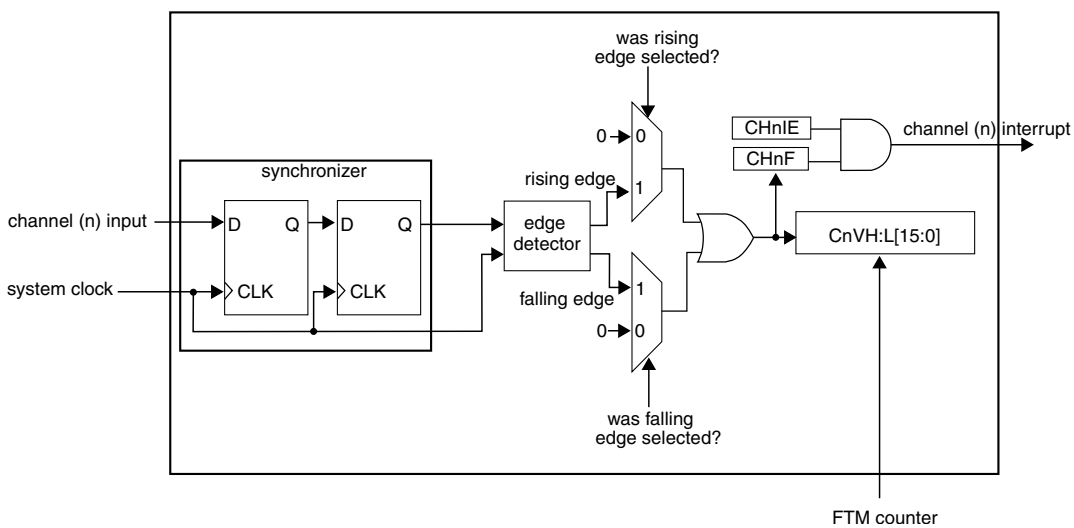


Figure 15-7. Input capture mode

The input signal is always delayed three rising edges of the system clock; that is, two rising edges to the synchronizer plus one more rising edge to the edge detector. In other words, the CHnF bit is set on the third rising edge of the system clock after a valid edge occurs on the channel input.

15.5.5 Output compare mode

The output compare mode is selected when (CPWMS = 0) and (MSnB:MSnA = 0:1).

In output compare mode, the FTM can generate timed pulses with programmable position, polarity, duration, and frequency. When the counter matches the value in the CnVH:CnVL registers of an output compare channel, the channel (n) output can be set, cleared, or toggled.

When a channel is initially configured to toggle mode, the previous value of the channel output is held until the first output compare event occurs.

The CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (FTM counter = CnVH:CnVL).

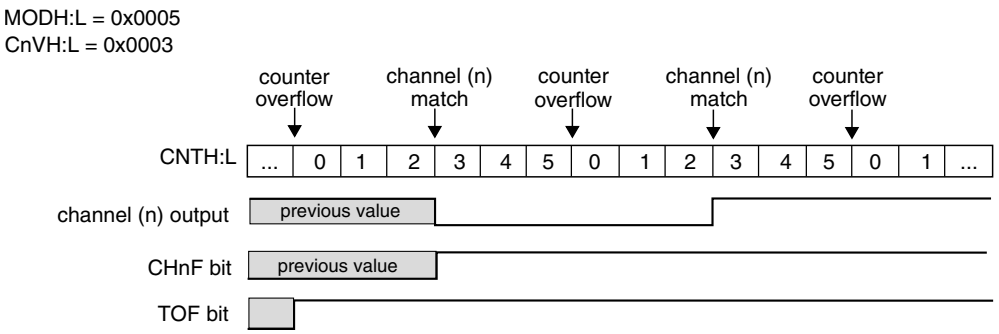


Figure 15-8. Example of the output compare mode when the match toggles the channel output

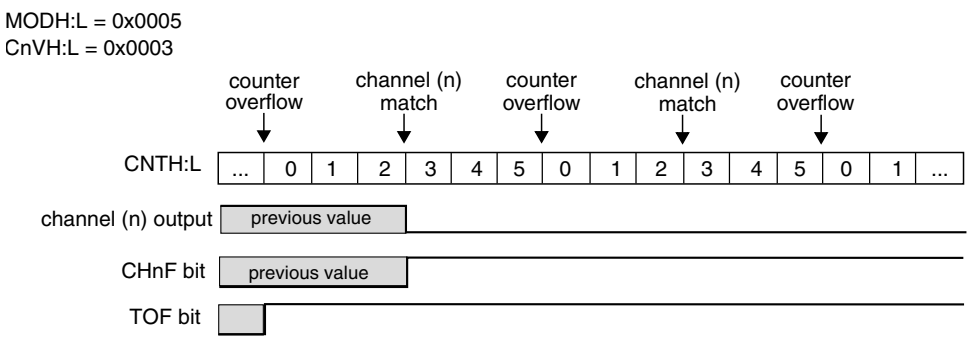


Figure 15-9. Example of the output compare mode when the match clears the channel output

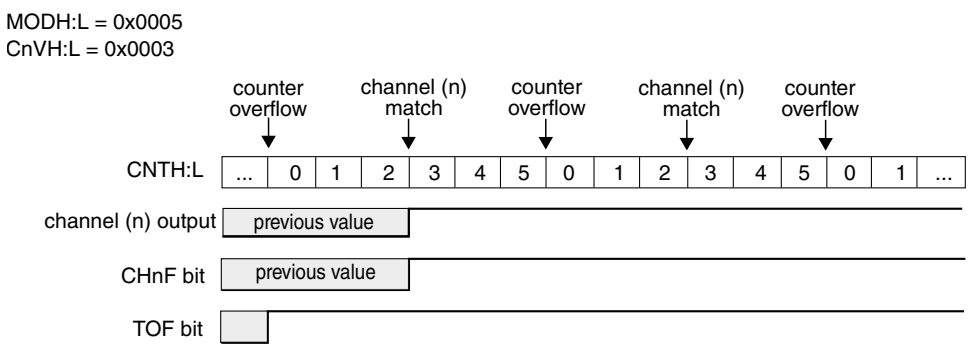


Figure 15-10. Example of the output compare mode when the match sets the channel output

It is possible to use the output compare mode with (ELSnB:ELSnA = 0:0). In this case, when the counter reaches the value in the CnVH:CnVL registers, the CHnF bit is set and the channel (n) interrupt is generated, if CHnIE = 1. However, the channel (n) output is not modified and controlled by FTM.

15.5.6 Edge-aligned PWM (EPWM) mode

The edge-aligned mode is selected when all of the following apply:

- (CPWMS = 0)
- (MSnB = 1)

The EPWM period is determined by (MODH:L + 0x0001) and the pulse width (duty cycle) is determined by (CnVH:L).

The CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (FTM counter = CnVH:L), that is, at the end of the pulse width.

This type of PWM signal is called edge-aligned because the leading edges of all PWM signals are aligned with the beginning of the period, which is the same for all channels within an FTM.

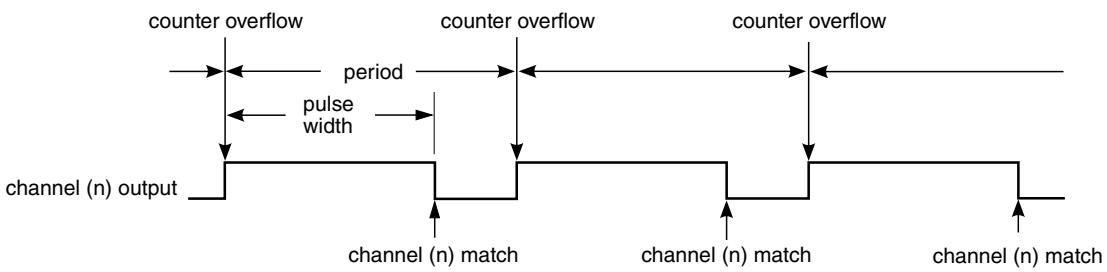


Figure 15-11. EPWM period and pulse width with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = 0:0) when the counter reaches the value in the CnVH:L registers, the CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1), however, the channel (n) output is not controlled by FTM.

If (ELSnB:ELSnA = 1:0), then the channel (n) output is forced high at the counter overflow, when the value of 0x0000 is loaded into the FTM counter. Additionally, it is forced low at the channel (n) match, when the FTM counter = CnVH:L. See the following figure.

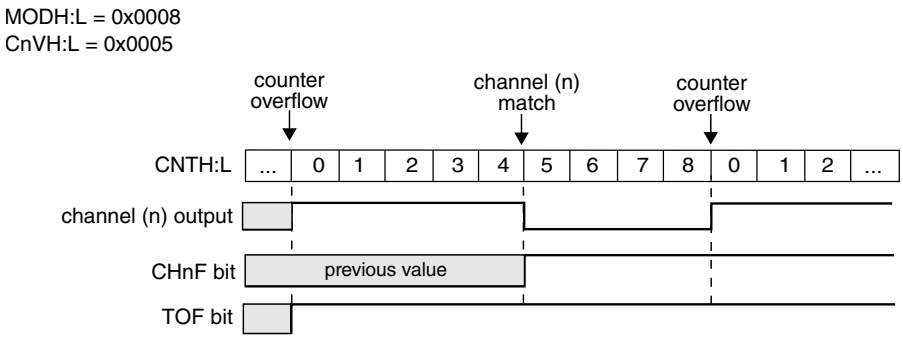


Figure 15-12. EPWM signal with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = X:1), then the channel (n) output is forced low at the counter overflow, when the value of 0x0000 is loaded into the FTM counter. Additionally, it is forced high at the channel (n) match, when the FTM counter = CnVH:L. See the following figure.

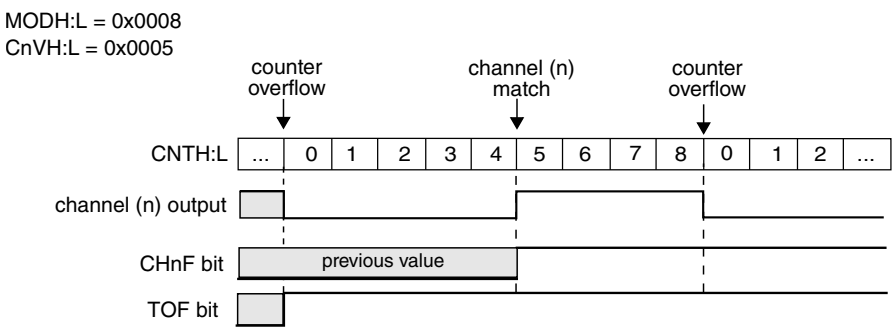


Figure 15-13. EPWM signal with ELSnB:ELSnA = X:1

If (CnVH:L = 0x0000), then the channel (n) output is a 0% duty cycle EPWM signal and CHnF bit is not set, even when there is the channel (n) match. If (CnVH:L > MODH:L), then the channel (n) output is a 100% duty cycle EPWM signal and CHnF bit is not set, even when there is the channel (n) match. Therefore, MODH:MODL must be less than 0xFFFF in order to get a 100% duty cycle EPWM signal.

15.5.7 Center-aligned PWM (CPWM) mode

The center-aligned mode is selected when:

- (CPWMS = 1)

The CPWM pulse width (duty cycle) is determined by 2 × (CnVH:L). The period is determined by 2 × (MODH:L). See the following figure. MODH:L must be kept in the range of 0x0001 to 0x7FFF because values outside this range can produce ambiguous results.

In the CPWM mode, the FTM counter counts up until it reaches MODH:L and then counts down until it reaches the value of 0x0000.

The CHnF bit is set and channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (FTM counter = CnVH:L) when the FTM counting is down, at the begin of the pulse width, and when the FTM counting is up, at the end of the pulse width.

This type of PWM signal is called center-aligned because the pulse width centers for all channels are aligned with the value of 0x0000.

The other channel modes are not compatible with the up-down counter (CPWMS = 1). Therefore, all FTM channels must be used in CPWM mode when (CPWMS = 1).

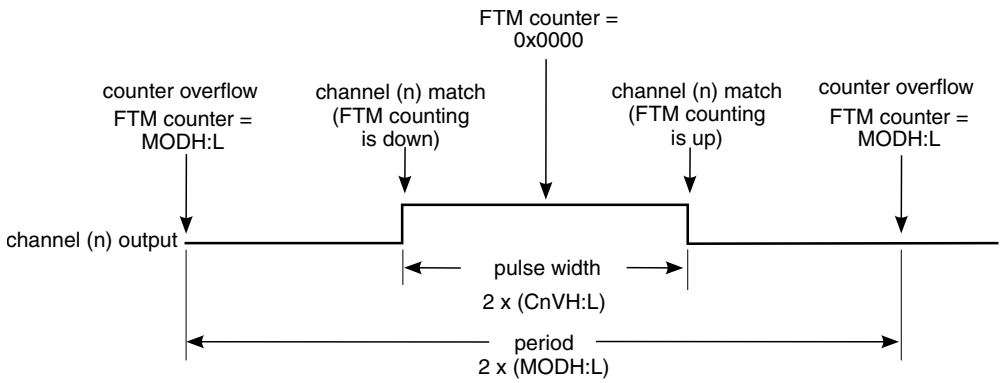


Figure 15-14. CPWM period and pulse width with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = 0:0) when the counter reaches the value in the CnVH:L registers, the CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1), however the channel (n) output is not controlled by FTM.

If (ELSnB:ELSnA = 1:0), then the channel (n) output is forced high at the channel (n) match (FTM counter = CnVH:L) when counting down, and it is forced low at the channel (n) match when counting up; see the following figure.

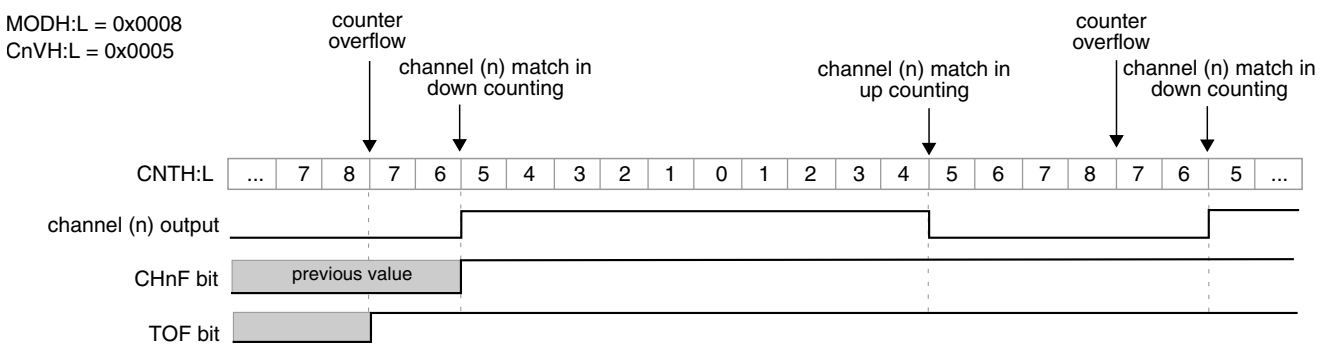


Figure 15-15. CPWM signal with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = X:1), then the channel (n) output is forced low at the channel (n) match (FTM counter = CnVH:L) when counting down, and it is forced high at the channel (n) match when counting up; see the following figure.

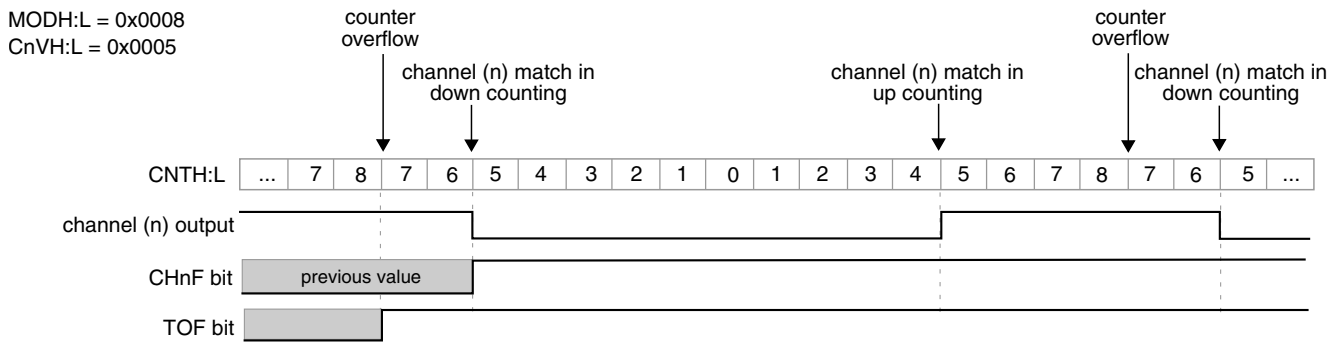


Figure 15-16. CPWM signal with ELSnB:ELSnA = X:1

If (CnVH:L = 0x0000) or (CnVH:L is a negative value, that is, CnVH[7] = 1) then the channel (n) output is a 0% duty cycle CPWM signal and CHnF bit is not set even when there is the channel (n) match.

If (CnVH:L is a positive value, that is, CnVH[7] = 0), (CnVH:L ≥ MODH:L), and (MODH:L ≠ 0x0000), then the channel (n) output is a 100% duty cycle CPWM signal and CHnF bit is not set even when there is the channel (n) match. This implies that the usable range of periods set by MODH:L is 0x0001 through 0x7FFE, or 0x7FFF if you do not need to generate a 100% duty cycle CPWM signal. This is not a significant limitation because the resulting period is much longer than required for normal applications.

The CPWM mode must not be used when the FTM counter is a free running counter.

15.5.8 Update of the registers with write buffers

This section describes the updating of registers that have write buffers.

15.5.8.1 MODH:L registers

If (CLKS[1:0] = 0:0), then MODH:L registers are updated when their second byte is written.

If (CLKS[1:0] ≠ 0:0), then MODH:L registers are updated according to the CPWMS bit:

- If the selected mode is not CPWM mode, then MODH:L registers are updated after both bytes have been written and the FTM counter changes from (MODH:L) to (all zeroes). If the FTM counter is a free-running counter, then this update is made when the FTM counter changes from 0xFFFF to 0x0000.
- If the selected mode is CPWM mode, then MODH:L registers are updated after both bytes have been written and the FTM counter changes from MODH:L to (MODH:L – 0x0001).

15.5.8.2 CnVH:L registers

If (CLKS[1:0] = 0:0), then CnVH:L registers are updated when their second byte is written.

If (CLKS[1:0] ≠ 0:0), then CnVH:L registers are updated according to the selected mode:

- If the selected mode is output compare mode, then CnVH:L registers are updated after their second byte is written and on the next change of the FTM counter.
- If the selected mode is EPWM mode, the CnVH:L registers are updated after both bytes have been written and the FTM counter changes from MODH:L to all zeroes. If the FTM counter is a free running counter, then this update is made when the FTM counter changes from 0xFFFF to 0x0000.
- If the selected mode is CPWM mode, then CnVH:L registers are updated after both bytes have been written and the FTM counter changes from MODH:L to (MODH:L – 0x0001).

15.5.9 BDM mode

When BDM mode is active, the FlexTimer counter and the channels output are frozen.

However, the value of FlexTimer counter or the channels output are modified in BDM mode when:

- A write of any value to the CNTH or CNTL registers (Counter reset) resets the FTM counter to the value of 0x0000 and the channels output to their initial value, except for channels in output compare mode.

15.6 Reset overview

The FTM is reset whenever any chip reset occurs.

When the FTM exits from reset:

- The FTM counter and the prescaler counter are zero and are stopped (CLKS[1:0] = 0b00)
- The timer overflow interrupt is zero (Timer overflow interrupt)
- The channels interrupts are zero (Channel (n) interrupt)

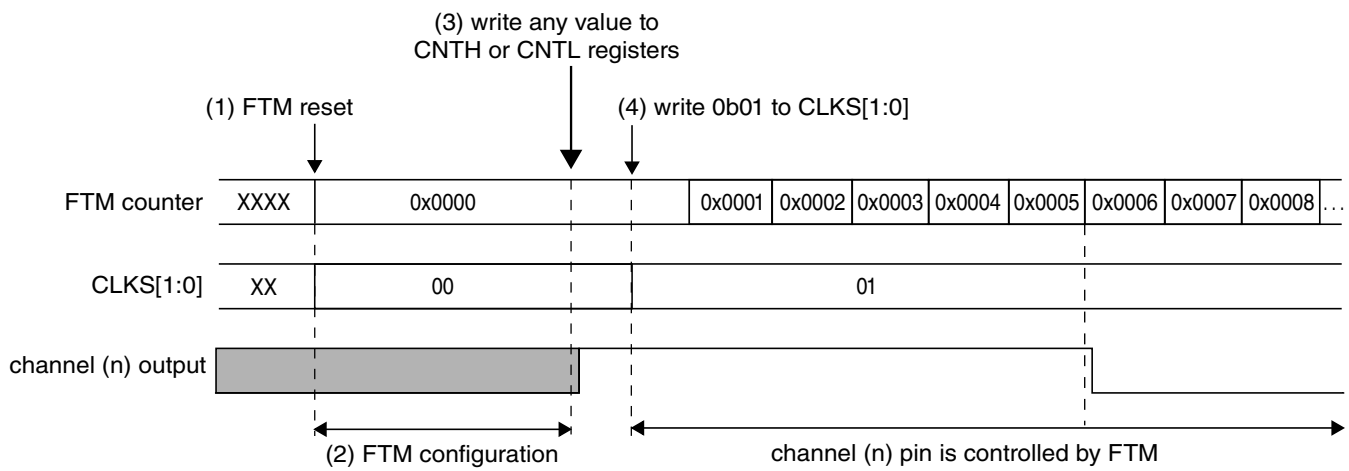
- The channels are in input capture mode (Input capture mode)
- The channels outputs are zero
- The channels pins are not controlled by FTM (ELS(n)B:ELS(n)A = 0b00). See table "Mode, Edge, and Level Selection"

The following figure shows the FTM behavior after the reset. At the reset (item 1), the FTM counter is disabled (see table "FTM Clock Source Selection"), its value is updated to zero and the pins are not controlled by FTM (table "Mode, Edge, and Level Selection").

After the reset, the FTM should be configured (item 2). It is necessary to define the FTM counter mode, the FTM counting limit (MODH:L registers value), the channels mode and CnVH:L registers value according to the channels mode.

Because of this, you should write any value to CNTH or CNTL registers (item 3). This write updates the FTM counter with the value of 0x0000 and the channels output with its initial value (except for channels in output compare mode) (Counter reset).

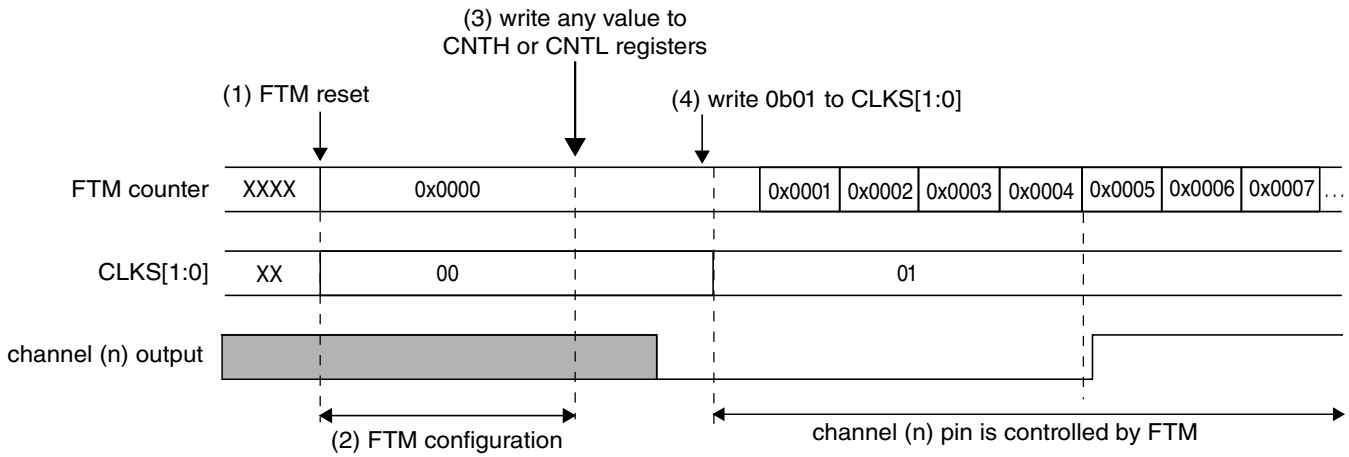
The next step is to select the FTM counter clock by the CLKS[1:0] bits (item 4). It is important to highlight that the pins are controlled only by FTM when CLKS[1:0] bits are different from zero (table "Mode, Edge, and Level Selection").



Note
– Channel (n) is in high-true EPWM mode with 0 < C(n)VH:L < MODH:L
– C(n)VH:L = 0x0005

Figure 15-17. FTM behavior after the reset when the channel (n) is in EPWM mode

The following figure shows an example when the channel (n) is in output compare mode and the channel (n) output is toggled when there is a match. In the output compare mode, the channel output is not updated to its initial value when there is a write to CNTH or CNTL registers (item 3).



Note
– Channel (n) is in output compare and the channel (n) output is toggled when there is a match
– C(n)VH:L = 0x0004

Figure 15-18. FTM behavior after the reset when the channel (n) is in output compare mode

15.7 FTM Interrupts

15.7.1 Timer overflow interrupt

The timer overflow interrupt is generated when (TOIE = 1) and (TOF = 1).

15.7.2 Channel (n) interrupt

The channel (n) interrupt is generated when (CHnIE = 1) and (CHnF = 1).

Chapter 16
8-bit modulo timer (MTIM)

16.1 Chip specific MTIM information

The modulo timer module (MTIM) provides a circuit of selectable clock sources and a programmable interrupt. The MTIM module contains a 8-bit modulo counter, which can operate as a free-running counter or a modulo counter. A timer overflow interrupt can be enabled to generate periodic interrupts for time-based software events. MTIM module may use external clock source. Following table summarizes the external signals of MTIM modules.

Table 16-1. MTIM clocks

MTIM Module Clock Interface	Chip Specific Clock Source
Bus clock (BUSCLK)	BUSCLK
Fixed frequncy clock (XCLK)	FFCLK
TCLK	TCLK0 for MTIM0 and TCLK2 for MTIM1

The MTIM module can be used for ADC hardware trigger, refer to System Control for more details.

16.2 Introduction

The MTIM is a simple 8-bit timer with several software selectable clock sources and a programmable interrupt.

For MCUs that have more than one MTIM, the MTIMs are collectively called MTIMx. For example, MTIMx for an MCU with two MTIMs would refer to MTIM0 and MTIM1. For MCUs that have exactly one MTIM, it is always referred to as MTIM.

16.3 Features

Timer system features include:

- 8-bit up-counter:
  - Free-running or 8-bit modulo limit
  - Software controllable interrupt on overflow
  - Counter reset bit (TRST)
  - Counter stop bit (TSTP)
- Four software selectable clock sources for input to prescaler:
  - System bus clock - rising edge
  - Fixed frequency clock (XCLK) - rising edge
  - External clock source on the TCLK pin - rising edge
  - External clock source on the TCLK pin - falling edge
- Nine selectable clock prescale values:
  - Clock source divide by 1, 2, 4, 8, 16, 32, 64, 128, or 256

16.4 Modes of operation

This section defines the MTIM's operation in stop, wait, and background debug modes.

16.4.1 MTIM in wait mode

The MTIM continues to run in wait mode if enabled before executing the WAIT instruction. Therefore, the MTIM can be used to bring the MCU out of wait mode if the timer overflow interrupt is enabled. For lowest possible current consumption, the MTIM must be stopped by software if not needed as an interrupt source during wait mode.

16.4.2 MTIM in stop mode

The MTIM is disabled in stop mode, regardless of the settings before executing the STOP instruction. Therefore, the MTIM cannot be used as a wakeup source from stop modes.

If stop3 is exited with a reset, the MTIM will be put into its reset state. If stop3 is exited with an interrupt, the MTIM continues from the state it was in when stop3 was entered. If the counter was active upon entering stop3, the count will resume from the current value.

16.4.3 MTIM in active background mode

The MTIM suspends all counting until the microcontroller returns to normal user operating mode. Counting resumes from the suspended value as long as an MTIM reset did not occur, MTIM_SC[TRST] written to a 1 or MTIM_MOD written.

16.5 Block diagram

The block diagram for the modulo timer module is shown in the following figure.

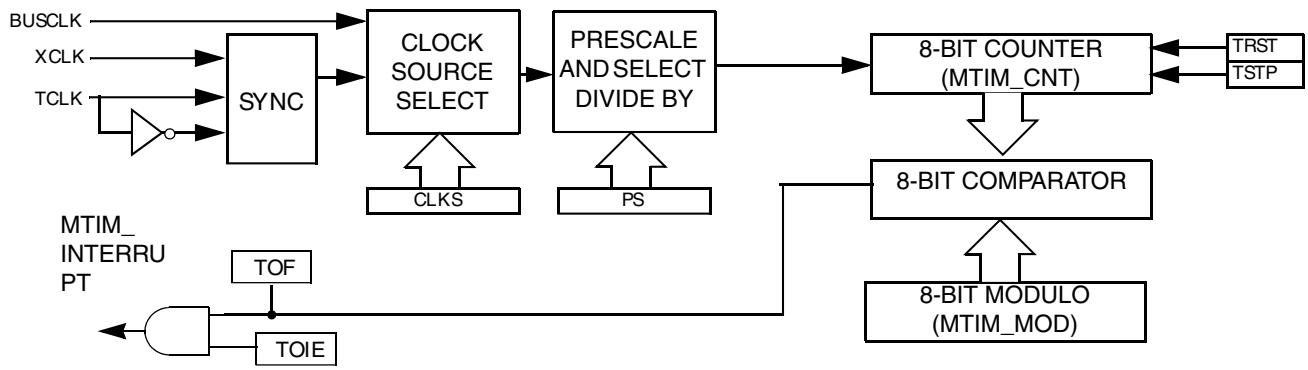


Figure 16-1. Modulo timer (MTIM) block diagram

16.6 External signal description

The MTIM includes one external signal, TCLK, used to input an external clock when selected as the MTIM clock source. The signal properties of TCLK are shown in the following table.

Table 16-2. MTIM external signal

Signal	Function	I/O
TCLK	External clock source input into MTIM	I

The TCLK input must be synchronized by the bus clock. Also, variations in duty cycle and clock jitter must be accommodated. Therefore, the TCLK signal must be limited to one-fourth of the bus frequency.

The TCLK pin can be muxed with a general-purpose port pin.

16.7 Register definition

MTIM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
18	MTIM Status and Control Register (MTIM0_SC)	8	R/W	10h	16.7.1/254
19	MTIM Clock Configuration Register (MTIM0_CLK)	8	R/W	00h	16.7.2/255
1A	MTIM Counter Register (MTIM0_CNT)	8	R	00h	16.7.3/256
1B	MTIM Modulo Register (MTIM0_MOD)	8	R/W	00h	16.7.4/256
1C	MTIM Status and Control Register (MTIM1_SC)	8	R/W	10h	16.7.1/254
1D	MTIM Clock Configuration Register (MTIM1_CLK)	8	R/W	00h	16.7.2/255
1E	MTIM Counter Register (MTIM1_CNT)	8	R	00h	16.7.3/256
1F	MTIM Modulo Register (MTIM1_MOD)	8	R/W	00h	16.7.4/256

16.7.1 MTIM Status and Control Register (MTIMx_SC)

MTIM_SC contains the overflow status flag and control bits that are used to configure the interrupt enable, reset the counter, and stop the counter.

Address: Base address + 0h offset

Bit	7	6	5	4	3	2	1	0
Read	TOF	TOIE	0	TSTP	0			
Write			TRST					
Reset	0	0	0	1	0	0	0	0

MTIMx_SC field descriptions

Field	Description
7 TOF	MTIM Overflow Flag This bit is set when the MTIM counter register overflows to 0x00 after reaching the value in the MTIM modulo register. Clear TOF by reading the MTIM_SC register while TOF is set, then write a 0 to TOF. TOF is also cleared when TRST is written to a 1 or when any value is written to the MTIM_MOD register. 0 MTIM counter has not reached the overflow value in the MTIM modulo register. 1 MTIM counter has reached the overflow value in the MTIM modulo register.
6 TOIE	MTIM Overflow Interrupt Enable This read/write bit enables MTIM overflow interrupts. If TOIE is set, then an interrupt is generated when TOF = 1. Reset clears TOIE. Do not set TOIE if TOF = 1. Clear TOF first, then set TOIE. 0 TOF interrupts are disabled. Use software polling. 1 TOF interrupts are enabled.

Table continues on the next page...

MTIMx_SC field descriptions (continued)

Field	Description
5 TRST	MTIM Counter Reset When a 1 is written to this write-only bit, the MTIM counter register resets to 0x00 and TOF is cleared. Reading this bit always returns 0. 0 No effect. MTIM counter remains at current state. 1 MTIM counter is reset to 0x00.
4 TSTP	MTIM Counter Stop When set, this read/write bit stops the MTIM counter at its current value. Counting resumes from the current value when TSTP is cleared. Reset sets TSTP to prevent the MTIM from counting. 0 MTIM counter is active. 1 MTIM counter is stopped.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

16.7.2 MTIM Clock Configuration Register (MTIMx_CLK)

MTIM_CLK contains the clock select bits (CLKS) and the prescaler select bits (PS).

Address: Base address + 1h offset

Bit	7	6	5	4	3	2	1	0
Read	0		CLKS		PS			
Write								
Reset	0	0	0	0	0	0	0	0

MTIMx_CLK field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5–4 CLKS	Clock Source Select These two read/write bits select one of four different clock sources as the input to the MTIM prescaler. Changing the clock source while the counter is active does not clear the counter. The count continues with the new clock source. Reset clears CLKS to 000b. 00 Encoding 0. Bus clock (BUSCLK). 01 Encoding 1. Fixed-frequency clock (XCLK). 10 Encoding 2. External source (TCLK pin), falling edge. 11 Encoding 3. External source (TCLK pin), rising edge.
PS	Clock Source Prescaler These four read/write bits select one of nine outputs from the 8-bit prescaler. Changing the prescaler value while the counter is active does not clear the counter. The count continues with the new prescaler value. Reset clears PS to 0000b.

Table continues on the next page...

MTIMx_CLK field descriptions (continued)

Field	Description	
	0000	Encoding 0. MTIM clock source.
	0001	Encoding 1. MTIM clock source/2.
	0010	Encoding 2. MTIM clock source/4.
	0011	Encoding 3. MTIM clock source/8.
	0100	Encoding 4. MTIM clock source/16.
	0101	Encoding 5. MTIM clock source/32.
	0110	Encoding 6. MTIM clock source/64.
	0111	Encoding 7. MTIM clock source/128.
	1000	Encoding 8. MTIM clock source/256.
	Others	Default to MTIM clock source/256.

16.7.3 MTIM Counter Register (MTIMx_CNT)

MTIM_CNT is the read-only value of the current MTIM count of the 8-bit counter.

Address: Base address + 2h offset

Bit	7	6	5	4	3	2	1	0
Read	COUNT							
Write								
Reset	0	0	0	0	0	0	0	0

MTIMx_CNT field descriptions

Field	Description
COUNT	MTIM Count These eight read-only bits contain the current value of the 8-bit counter. Writes have no effect to this register. Reset clears the count to 0x00.

16.7.4 MTIM Modulo Register (MTIMx_MOD)

Address: Base address + 3h offset

Bit	7	6	5	4	3	2	1	0
Read Write	MOD							
Reset	0	0	0	0	0	0	0	0

MTIMx_MOD field descriptions

Field	Description
MOD	MTIM Modulo

MTIMx_MOD field descriptions (continued)

Field	Description
	These eight read/write bits contain the modulo value used to reset the count and set TOF. A value of 0x00 puts the MTIM in free-running mode. Writing to MTIM_MOD resets the COUNT to 0x00 and clears TOF. Reset sets the modulo to 0x00.

16.8 Functional description

The MTIM consists of a main 8-bit up-counter with an 8-bit modulo register, a clock source selector, and a prescaler block with nine selectable values. The module also contains software-selectable interrupt logic.

The MTIM counter (MTIM_CNT) has three modes of operation: stopped, free-running, and modulo. Out of reset, the counter is stopped. If the counter is started without writing a new value to the modulo register, then the counter will be in free-running mode. The counter is in modulo mode when a value other than 0x00 is in the modulo register while the counter is running.

After any MCU reset, the counter is stopped and reset to 0x00, and the modulus is set to 0x00. The bus clock is selected as the default clock source and the prescale value is divide by 1. To start the MTIM in free-running mode, simply write to the MTIM status and control register (MTIM_SC), and clear the MTIM stop bit (TSTP).

Four clock sources are software selectable: the internal bus clock, the fixed frequency clock (XCLK), and an external clock on the TCLK pin, selectable as incrementing on either rising or falling edges. The MTIM clock select bits, CLKS1:CLKS0, in MTIM_CLK are used to select the desired clock source. If the counter is active (SC[TSTP] = 0) when a new clock source is selected, the counter will continue counting from the previous value using the new clock source.

Nine prescale values are software selectable: clock source divided by 1, 2, 4, 8, 16, 32, 64, 128, or 256. The prescaler select bits (CLK[PS]) in MTIM_CLK select the desired prescale value. If the counter is active (SC[TSTP] = 0) when a new prescaler value is selected, the counter will continue counting from the previous value using the new prescaler value.

The MTIM modulo register (MTIM_MOD) allows the overflow compare value to be set to any value from 0x01 to 0xFF. Reset clears the modulo value to 0x00, which results in a free running counter.

When the counter is active (SC[TSTP] = 0), the counter increments at the selected rate until the count matches the modulo value. When these values match, the counter overflows to 0x00 and continues counting. The MTIM overflow flag (SC[TOF]) is set

whenever the counter overflows. The flag sets on the transition from the modulo value to 0x00. Writing to MTIM_MOD while the counter is active resets the counter to 0x00 and clears SC[TOF].

Clearing SC[TOF] is a two-step process. The first step is to read the MTIM_SC register while SC[TOF] is set. The second step is to write a 0 to SC[TOF]. If another overflow occurs between the first and second step, the clearing process is reset and SC[TOF] will remain set after the second step is performed. This will prevent the second occurrence from being missed. SC[TOF] is also cleared when a 1 is written to SC[TRST] or when any value is written to the MTIM_MOD register.

The MTIM allows for an optional interrupt to be generated whenever SC[TOF] is set. To enable the MTIM overflow interrupt, set the MTIM overflow interrupt enable bit (SC[TOIE]). SC[TOIE] must never be written to a 1 while SC[TOF] = 1. Instead, SC[TOF] must be cleared first, then the SC[TOIE] can be set to 1.

16.8.1 MTIM operation example

This section shows an example of the MTIM operation as the counter reaches a matching value from the modulo register.

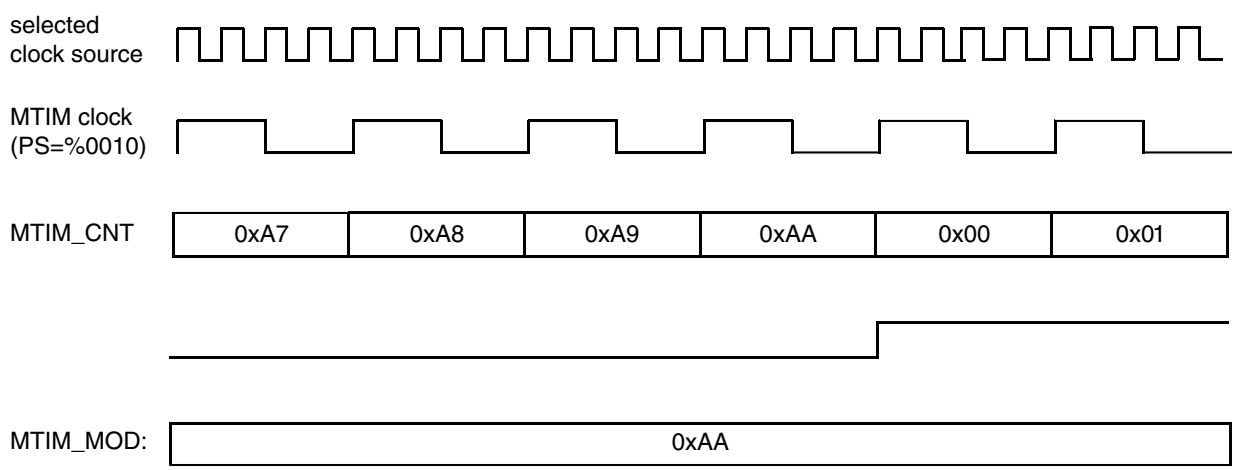


Figure 16-2. MTIM counter overflow example

In the above example, the selected clock source could be any of the four possible choices. The prescaler is set to CLK[PS] = 0010b or divide-by-4. The modulo value in the MTIM_MOD register is set to 0xAA. When the counter, MTIM_CNT, reaches the modulo value of 0xAA, it overflows to 0x00 and continues counting. The timer overflow flag, SC[TOF], sets when the counter value changes from 0xAA to 0x00. An MTIM overflow interrupt is generated when SC[TOF] is set, if SC[TOIE] = 1.

Chapter 17
Pulse Width Timer (PWT)

17.1 Chip specific PWT information

This device has one pulse width timer (PWT). The PWT is used to captures a pulse width and pulse period. PWT has four input, which is stated in below table:

Table 17-1. PWT input signals

PWT Input	Signals
Input 0	NC
Input 1	External Pad (PTA2)
Input 2	ACMP0 Output
Input 3	ACMP1 Output

The following clocks used in this chapter are from the chip:

Table 17-2. PWT clocks

PWT clocks	Chip clocks
PWT_CLK	BUSCLK
ALTCLK	TCLK0

17.2 Introduction

17.2.1 Features

The pulse width timer (PWT) includes the following features:

- Automatic measurement of pulse width with 16-bit resolution
- Separate positive and negative pulse width measurements
- Programmable triggering edge for starting measurement

- Programmable measuring time between successive alternating edges, rising edges or falling edges
- Programmable prescaler from clock input as 16-bit counter time base
- Two selectable clock sources—PWT_CLK and alternative clock
- Four selectable pulse inputs
- Programmable interrupt generation upon pulse width value updated and counter overflow

17.2.2 Modes of operation

The following table describes the operation of the PWT module in various modes.

Modes	Description
Run	When enabled, the pulse width timer module is active.
Wait	When enabled, the pulse width timer module is active and can perform the waking up function if the corresponding interrupt is enabled.
Stop	The pulse width timer module is halted when entering stop and the register contents and operating status is preserved. If stop exits with reset then the module resets. If stop exits with another source, the module resumes operation based on module status upon exit.
Active background	Upon entering Debug mode, the PWT suspends all counting and pulse edge detection until the microcontroller returns to normal user operating mode. Counting and edge detection resume from the suspended value when normal user operating mode returns as long as the PWTSR bit (PWT software reset) is not written to 1 and the PWT module is still enabled.

17.2.3 Block diagram

The following is the block diagram of the pulse width timer module (PWT).

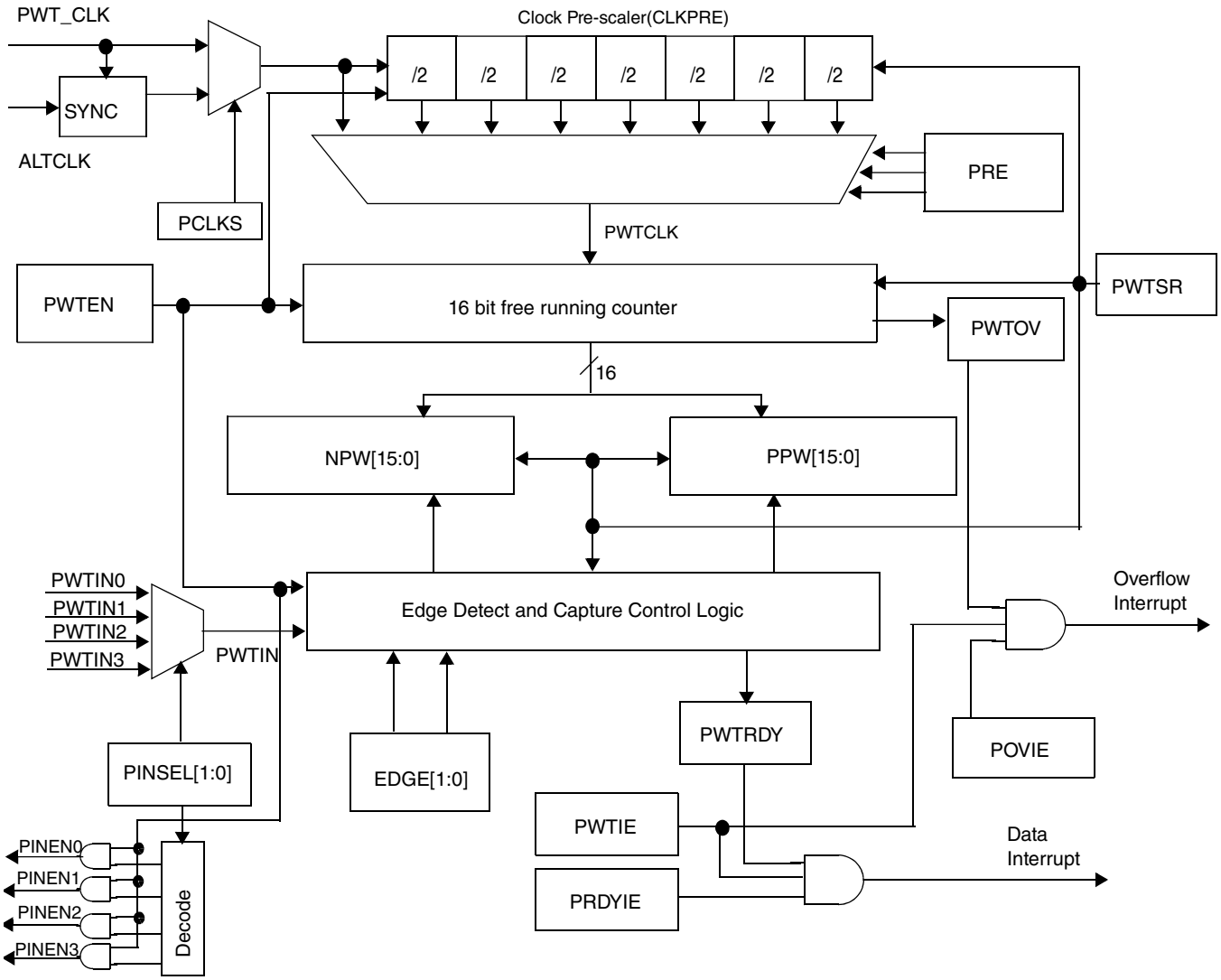


Figure 17-1. Pulse width timer (PWT) block diagram

17.3 PWT signal description

Table 17-3. PWT signal description

Signal	I/O	Pullup	Description
PWTIN[3:0]	I	No	Pulse Inputs
ALTCLK	I	No	Alternative clock source for the counter

17.3.1 PWTIN[3:0] - Pulse Width Timer Capture Inputs

The input signals are pulse capture inputs which can come from internal or external sources. The PWT input is selected by CR[PINSEL] to be routed to the pulse width timer. If the input comes from external source and is selected as the PWT input, the input port is enabled for PWT function by CR[PINSEL] automatically. The minimum pulse width to be measured is 1 PWTCLK cycle, any pulse narrower than this value is ignored by PWT module. The PWTCLK cycle time depends on the PWT clock source selection and prescaler rate setting.

17.3.2 ALTCLK- Alternative Clock Source for Counter

The PWT has an alternative clock input ALTCLK which can be selected as the clock source of the counter when CR[PCLKS] is set. The ALTCLK input must be synchronized by the bus clock. Variations in duty cycle and clock jitter must also be accommodated so that the ALTCLK signal must not exceed one-fourth of the bus frequency. The ALTCLK pin can be shared with a general-purpose port pin. See the Pins and Connections chapter for the pin location and priority of this function.

17.4 Memory Map and Register Descriptions

PWT memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3030	Pulse Width Timer Control and Status Register (PWT_CS)	8	R/W	00h	17.4.1/263
3031	Pulse Width Timer Control Register (PWT_CR)	8	R/W	00h	17.4.2/264
3032	Pulse Width Timer Positive Pulse Width Register: High (PWT_PPH)	8	R	00h	17.4.3/265
3033	Pulse Width Timer Positive Pulse Width Register: Low (PWT_PPL)	8	R	00h	17.4.4/265
3034	Pulse Width Timer Negative Pulse Width Register: High (PWT_NPH)	8	R	00h	17.4.5/266
3035	Pulse Width Timer Negative Pulse Width Register: Low (PWT_NPL)	8	R	00h	17.4.6/266
3036	Pulse Width Timer Counter Register: High (PWT_CNTH)	8	R	00h	17.4.7/267
3037	Pulse Width Timer Counter Register: Low (PWT_CNTL)	8	R	00h	17.4.8/267

17.4.1 Pulse Width Timer Control and Status Register (PWT_CS)

Address: 3030h base + 0h offset = 3030h

Bit	7	6	5	4	3	2	1	0
Read	PWTEN	PWTIE	PRDYIE	POVIE	0	0	PWTRDY	PWTOV
Write					PWTSR			
Reset	0	0	0	0	0	0	0	0

PWT_CS field descriptions

Field	Description
7 PWTEN	PWT Module Enable Enables/disables the PWT module. To avoid unexpected behavior, do not change any PWT configurations as long as PWTEN is set. 0 The PWT is disabled. 1 The PWT is enabled.
6 PWTIE	PWT Module Interrupt Enable Enables the PWT module to generate an interrupt. 0 Disables the PWT to generate interrupt. 1 Enables the PWT to generate interrupt.
5 PRDYIE	PWT Pulse Width Data Ready Interrupt Enable Enables/disables the PWT to generate an interrupt when PWTRDY is set as long as PWTIE is set. 0 Disable PWT to generate interrupt when PWTRDY is set. 1 Enable PWT to generate interrupt when PWTRDY is set.
4 POVIE	PWT Counter Overflow Interrupt Enable Enables/disables the PWT to generate an interrupt when PWTOV is set due to PWT counter overflow. 0 Disable PWT to generate interrupt when PWTOV is set. 1 Enable PWT to generate interrupt when PWTOV is set.
3 PWTSR	PWT Soft Reset Performs a soft reset to the PWT. This field always reads as 0. 0 No action taken. 1 Writing 1 to this field will perform soft reset to PWT.
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 PWTRDY	PWT Pulse Width Valid Indicates that the PWT Pulse Width register(s) has been updated and is ready to be read. This field is cleared by reading PWTRDY and then writing 0 to PWTRDY bit when PWTRDY is set.Writing 1 to this field has no effect.

Table continues on the next page...

PWT_CS field descriptions (continued)

Field	Description
	0 PWT pulse width register(s) is not up-to-date. 1 PWT pulse width register(s) has been updated.
0 PWTOV	PWT Counter Overflow Indicates that the PWT counter has run from 0x0000_0xFFFF to 0x0000_0x0000. This field is cleared by writing 0 to PWTOV when PWTOV is set. Writing 1 to this field has no effect. If another overflow occurs when this field is being cleared, the clearing fails. 0 PWT counter no overflow. 1 PWT counter runs from 0xFFFF to 0x0000.

17.4.2 Pulse Width Timer Control Register (PWT_CR)

Address: 3030h base + 1h offset = 3031h

Bit	7	6	5	4	3	2	1	0
Read Write	PCLKS	PINSEL		EDGE		PRE		
Reset	0	0	0	0	0	0	0	0

PWT_CR field descriptions

Field	Description
7 PCLKS	PWT Clock Source Selection Controls the selection of clock source for the PWT counter. 0 PWT_CLK is selected as the clock source of PWT counter. 1 Alternative clock is selected as the clock source of PWT counter.
6–5 PINSEL	PWT Pulse Inputs Selection Enables the corresponding PWT input port, if this PWT input comes from an external source. 00 PWTIN[0] is enabled. 01 PWTIN[1] is enabled. 10 PWTIN[2] enabled. 11 PWTIN[3] enabled.
4–3 EDGE	PWT Input Edge Sensitivity Selects which edge triggers the pulse width measurement and which edges trigger the capture. If user needs to change the trigger and capture mode by changing the value of EDGE[1:0], a PWT software reset is required after changing the EDGE[1:0] value. Clearing PWTEN and then setting it has the same effect. 00 The first falling-edge starts the pulse width measurement, and on all the subsequent falling edges, the pulse width is captured. 01 The first rising edge starts the pulse width measurement, and on all the subsequent rising and falling edges, the pulse width is captured.

Table continues on the next page...

PWT_CR field descriptions (continued)

Field	Description
	10 The first falling edge starts the pulse width measurement, and on all the subsequent rising and falling edges, the pulse width is captured. 11 The first-rising edge starts the pulse width measurement, and on all the subsequent rising edges, the pulse width is captured.
PRE	PWT Clock Prescaler (CLKPRE) Setting Selects the value by which the clock is divided to clock the PWT counter. 000 Clock divided by 1. 001 Clock divided by 2. 010 Clock divided by 4. 011 Clock divided by 8. 100 Clock divided by 16. 101 Clock divided by 32. 110 Clock divided by 64. 111 Clock divided by 128.

17.4.3 Pulse Width Timer Positive Pulse Width Register: High (PWT_PPH)

Address: 3030h base + 2h offset = 3032h

Bit	7	6	5	4	3	2	1	0
Read	PPWH							
Write								
Reset	0	0	0	0	0	0	0	0

PWT_PPH field descriptions

Field	Description
PPWH	Positive Pulse Width[15:8] High byte of captured positive pulse width value.

17.4.4 Pulse Width Timer Positive Pulse Width Register: Low (PWT_PPL)

Address: 3030h base + 3h offset = 3033h

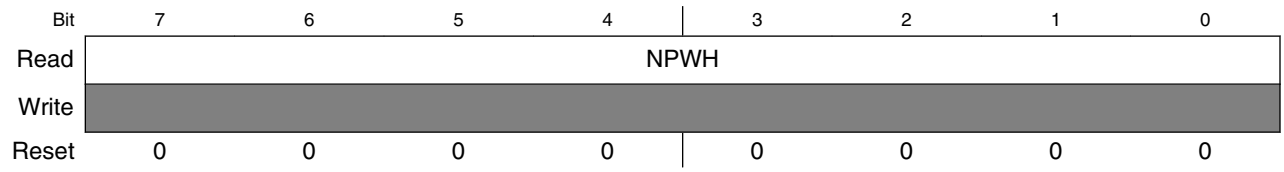
Bit	7	6	5	4	3	2	1	0
Read	PPWL							
Write								
Reset	0	0	0	0	0	0	0	0

PWT_PPL field descriptions

Field	Description
PPWL	Positive Pulse Width[7:0] Low byte of captured positive pulse width value.

17.4.5 Pulse Width Timer Negative Pulse Width Register: High (PWT_NPH)

Address: 3030h base + 4h offset = 3034h

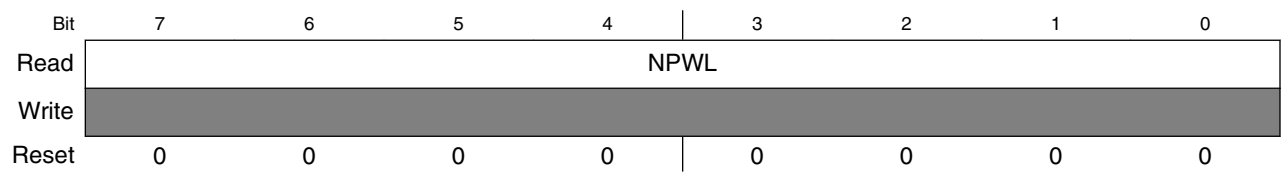


PWT_NPH field descriptions

Field	Description
NPWH	Negative Pulse Width[15:8] High byte of captured negative pulse width value.

17.4.6 Pulse Width Timer Negative Pulse Width Register: Low (PWT_NPL)

Address: 3030h base + 5h offset = 3035h



PWT_NPL field descriptions

Field	Description
NPWL	Negative Pulse Width[7:0] Low byte of captured negative pulse width value.

17.4.7 Pulse Width Timer Counter Register: High (PWT_CNTH)

Address: 3030h base + 6h offset = 3036h

Bit	7	6	5	4	3	2	1	0
Read	PWTH							
Write								
Reset	0	0	0	0	0	0	0	0

PWT_CNTH field descriptions

Field	Description
PWTH	PWT counter[15:8] High byte of PWT counter register.

17.4.8 Pulse Width Timer Counter Register: Low (PWT_CNTL)

Address: 3030h base + 7h offset = 3037h

Bit	7	6	5	4	3	2	1	0
Read	PWTL							
Write								
Reset	0	0	0	0	0	0	0	0

PWT_CNTL field descriptions

Field	Description
PWTL	PWT counter[7:0] Low byte of PWT counter register.

17.5 Functional Description

17.5.1 PWT Counter and PWT Clock Prescaler

The pulse width timer (PWT) measures duration of a pulse or the period of a signal input to the PWTIN by a 16-bit free running counter (CNTH[PWTH] and CNTL[PWTL]). There is a clock prescaler of CLKPRE(CR[PRE]) in PWT module that provides the frequency divided clock to CNTH[PWTH] and CNTL[PWTL]. The clock prescaler can select clock input from bus clock and alternative clock by CR[PCLKS].

The PWT counter uses the frequency divided clock from CR[PRE] for counter advancing. The frequency of prescaler is programmable as the clock frequency divided by 1, 2, 4, 8, 16, 32, 64, 128 (depending on the setting of CR[PRE]).

As soon as the PWT counter is enabled, it starts counting using the selected and divided clock source; the counter is cleared without loading to the registers when the first valid edge (trigger edge) is detected. If no valid trigger edge is detected for a long time, it is possible for the counter to overflow. When 16-bit free running counter is running, any edge to be measured after the trigger edge causes the value of CNTH[PWTH] and CNTL[PWTL] to be uploaded to the appropriate pulse width registers. At the same time, CNTH[PWTH] and CNTL[PWTL] will be reset to 0x0000 and the clock prescaler output will also be reset together. CNTH[PWTH] and CNTL[PWTL] will then start advancing again with the input clock. If the CNTH[PWTH] and CNTL[PWTL] runs from 0xFFFF to 0x0000, the CS[PWTOV] bit is set.

17.5.2 Edge detection and capture control

The edge detection and capture control part detects measurement trigger edges and controls when and which pulse width register(s) will be updated.

Based on the setting of CR[EDGE], the edge detection logic determines the starting and ending edge of the pulse width to be measured on PWTIN, and the registers fields to be updated.

The PWTIN can be selected from one of four sources by configuring CR[PINSEL].

It must be noted that inside the edge detection and capture logic, the system slave clock is used for PWT to sample and synchronize the PWTIN pulse, therefore the minimal PWTIN pulse width is determined by this slave clock frequency. For example, if this clock frequency is 50 MHz, the minimal PWTIN pulse width must be longer than 20 ns(the period of 50 MHz), otherwise, PWT won't be able to capture this pulse and the counter would overflow. See the chip configuration chapters to check the slave clock frequency to PWT. Also, if there isn't any valid edge of the PWTIN width for a long time, the PWT counter would overflow as well.

When CR[EDGE] is 00, the first falling edge is the trigger edge from which the pulse width begins to be measured. The counter value is uploaded to PPH[PPWH] and PPL[PPWL] upon each of the subsequent falling edges. When CR[EDGE] is 11, the first rising edge is the trigger edge from which the pulse width begins to be measured. The counter value is uploaded to NPH[NPWH] and NPL[NPWL] upon each successive rising-edge. In these two cases, the period of PWTIN is measured.

When CR[EDGE] is 01, the first rising edge is the trigger edge. The pulse width begins to be measured from this edge. PPH[PPWH] and PPL[PPWL] are uploaded upon each of the subsequent falling edges. NPH[NPWH] and NPL[NPWL] are uploaded upon each successive rising edge. When CR[EDGE] is 10, the first falling edge is the trigger edge from which the pulse width is measured. NPH[NPWH] and NPL[NPWL] are uploaded on each successive rising edge and PPH[PPWH] and PPL[PPWL] are uploaded on each successive falling edge. In these two cases, the positive pulse and negative pulse are measured separately and the positive pulse width is uploaded into PPH[PPWH] and PPL[PPWL]. The negative pulse width is uploaded into NPH[NPWH] and NPL[NPWL].

The following figure illustrates the trigger edge detection and pulse width registers update of PWT.

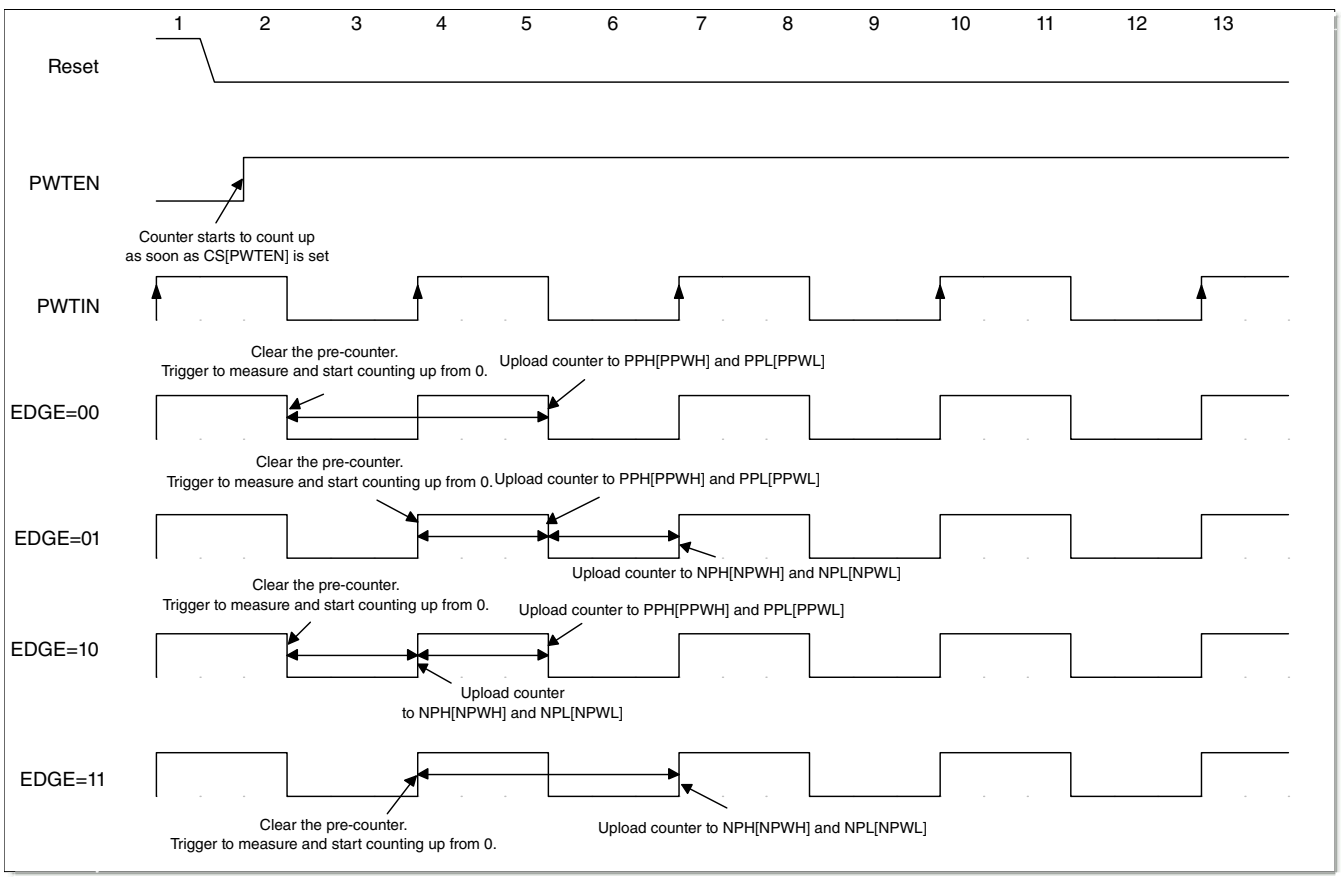


Figure 17-2. Trigger edge detection and pulse width registers update

CS[PWTRDY] indicates that the data can be read in PPH[PPWH], PPL[PPWL], NPH[NPWH] and NPL[NPWL], based on the setting of CR[EDGE].

- When CR[EDGE] is 00, CS[PWTRDY] is set whenever PPH[PPWH] and PPL[PPWL] are updated.
- When CR[EDGE] is 11, CS[PWTRDY] is set whenever NPH[NPWH] and NPL[NPWL] are updated.

- When CR[EDGE] is 01, CS[PWTRDY] is set whenever PPH[PPWH] and PPL[PPWL] are updated, followed by NPH[NPWH] and NPL[NPWL]'s update.
- When CR[EDGE] is 10, CS[PWTRDY] is set whenever NPH[NPWH] and NPL[NPWL] are updated, followed by PPH[PPWH] and PPL[PPWL]'s update.

When CS[PWTRDY] is set, the updated pulse width register(s) transfers the data to corresponding 16-bit read buffer(s). The read value of pulse width registers actually comes from the corresponding read buffers, whenever the chip is in normal run mode or Debug mode. Reading followed by writing 0 to CS[PWTRDY] flag clears this field. Until CS[PWTRDY] is cleared, the 16-bit read buffer(s) cannot be updated. But this does not affect the upload of pulse width registers from the PWT counter.

If another pulse measurement is completed and the pulse width registers are updated, the clearing of the CS[PWTRDY] flag fails, that is, CS[PWTRDY] will still be set, but the 16-bit read buffer(s) will be updated again as long as the action is cleared.. The user should complete the pulse width data reading before clearing CS[PWTRDY] to avoid missing data. This mechanism assures that the second pulse measurement will not be lost in case the MCU does not have enough time to read the first one ready for read. The mechanism is automatically restarted by an MCU reset , writing 1 to CS[PWTSR] or writing a 0 to CS[PWTEN] followed by writing a 1 to it.

The following figure illustrates the buffering mechanism of pulse width register:

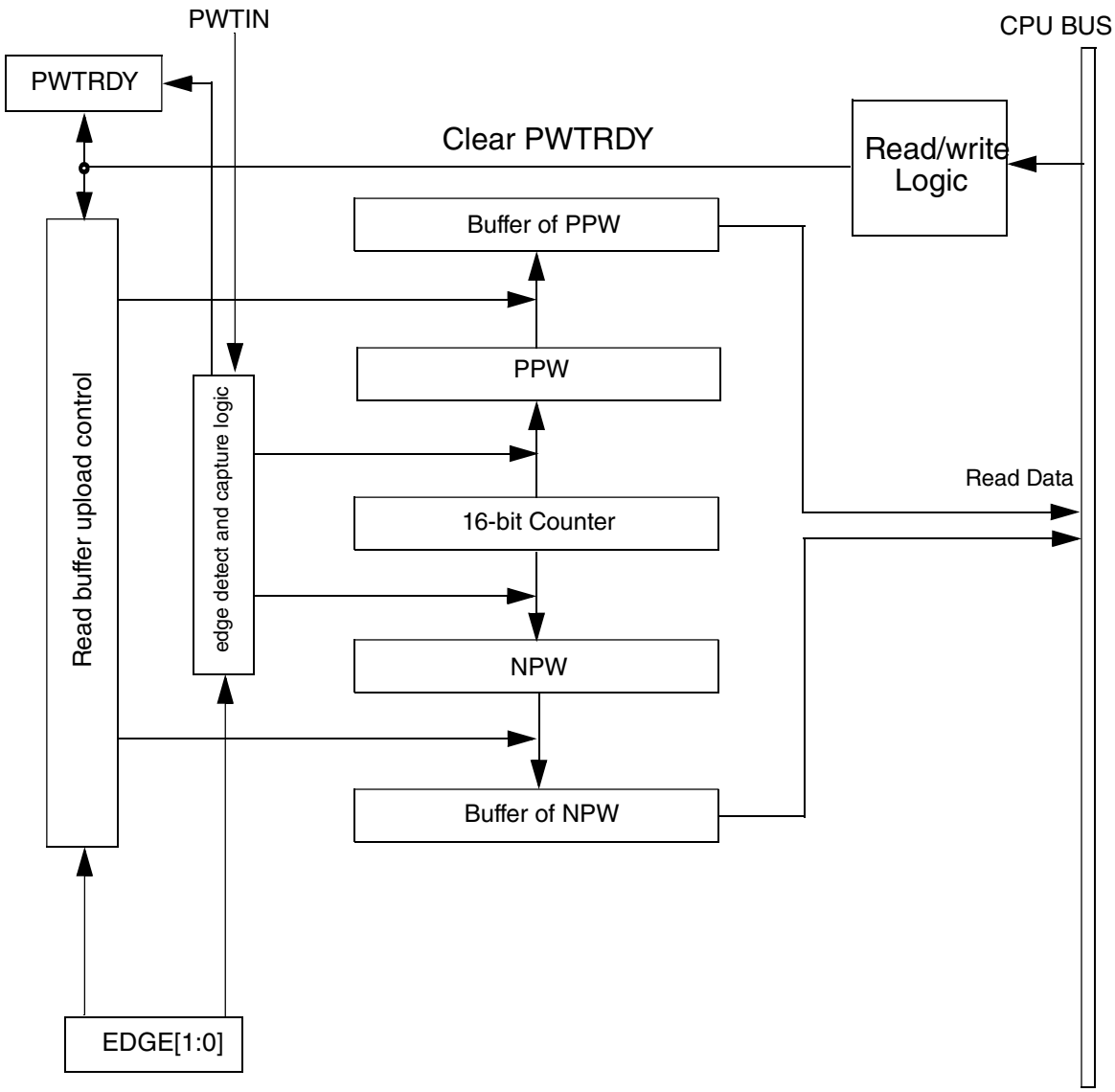


Figure 17-3. Buffering mechanism of Pulse Width register

When PWT completes any pulse width measurement, a signal is generated to reset CNTH[PWTH] and CNTL[PWTL], and the clock prescaler output after the data has been uploaded to the pulse width registers. To assure that there is no missing count, CNTH[PWTH], CNTL[PWTL] and the clock prescaler output are reset in a bus clock cycle after the completion of a pulse width measurement.

17.5.3 Counter overflow function

After PWT counter is enabled, the counter overflow occurs if no valid trigger edge is detected for a long time.

The following figure illustrates the counter overflow and different PWTIN pin states of PWT.

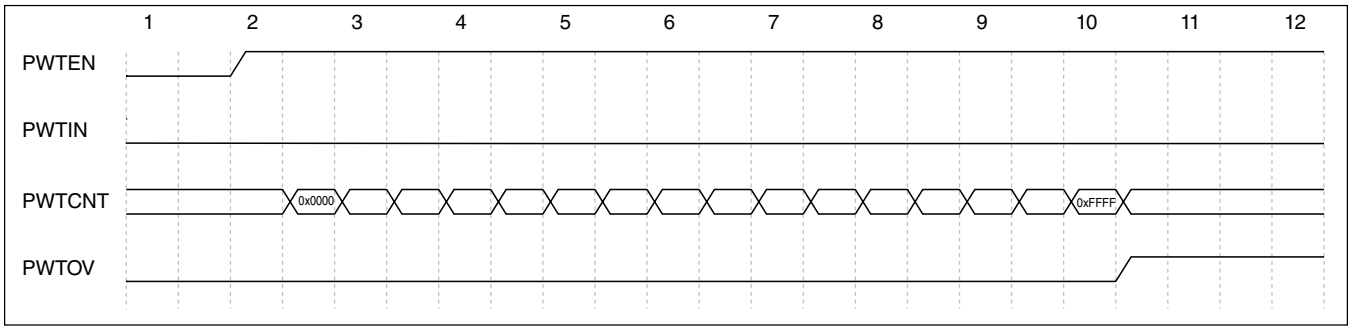


Figure 17-4. PWT counter overflow with low PWTIN

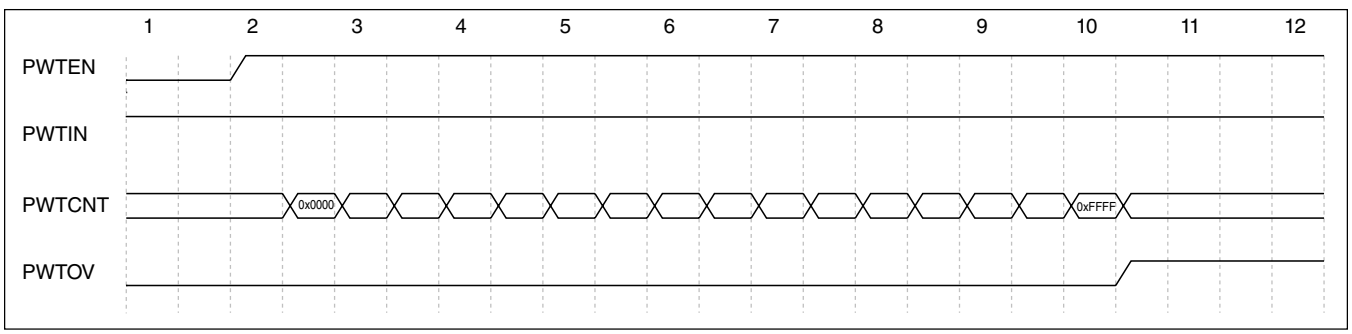


Figure 17-5. PWT counter overflow with high PWTIN

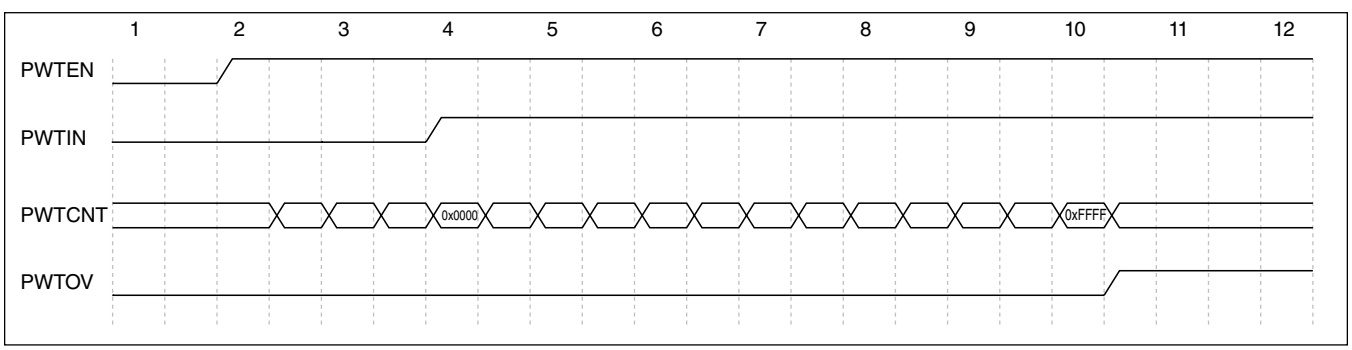


Figure 17-6. PWT counter overflow with PWTIN positive edge

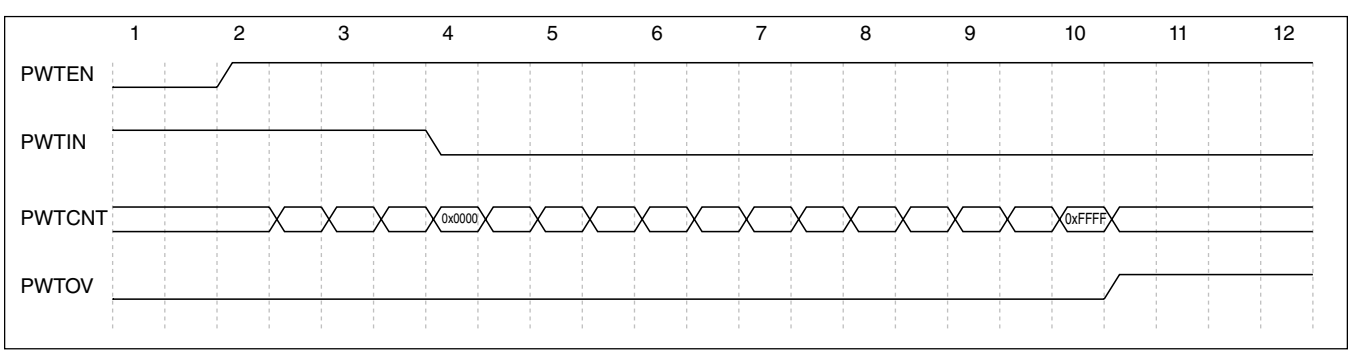


Figure 17-7. PWT counter overflow with PWTIN negative edge

17.6 Reset

17.6.1 Description of reset operation

PWT soft reset is built into PWT as a mechanism used to reset/restart the pulse width timer. The PWT soft reset is triggered by writing 1 to CS[PWTSR]. (This field always reads 0). Unlike reset by the CPU, the PWT reset does not restore everything in the PWT to its reset state. The following steps can be used to describe the reset operation.

1. The PWT counter is set to 0x0000.
2. The 16-bit buffer of PWT counter is reset.
3. The PWT clock prescaler output is reset.
4. The edge detection logic is reset.
5. The capture logic is reset and the latching mechanism of pulse width registers is also restarted.
6. PPH[PPWH], PPL[PPWL], NPH[NPWH] and NPL[NPWL] are set to 0x0000.
7. CS[PWTOV] and CS[PWTRDY] are set to 0.
8. All other PWT register settings are not changed.

Writing a 0 to CS[PWTEN] also has the above effects except that the reset state will be held until CS[PWTEN] is set to 1.

17.7 Interrupts

17.7.1 Description of interrupt operation

The other major component of the PWT is the interrupts control logic. When CS[PWTOV] and CS[POVIE] are set, a PWT overflow interrupt can be generated. When CS[PWTRDY] bit and CS[PRDYIE] are set, a pulse width data ready interrupt can be generated. CS[PWTIE] controls the interrupt generation of the PWT module. The functionality of the PWT is not affected while the interrupt is being generated.

17.8 Applications

17.8.1 Initialization/Application Information

Following are the recommended steps to initialize the PWT module:

1. Configure PCLKS, PRE, PINSEL and EDGE bits to select clock source, set pre-scaler rate, select PWT input pin and edge detection mode.
2. Set PWTIE, PRDYIE and POVIE bits if corresponding interrupt is desired to be generated.
3. Set PWTEN bit to enable the pulse width measurement.

The step 1 and 2 can be sequential or not, but they must be completed before step 3 to ensure all settings are ready before pulse width measurement is enabled.

17.8.2 Application examples

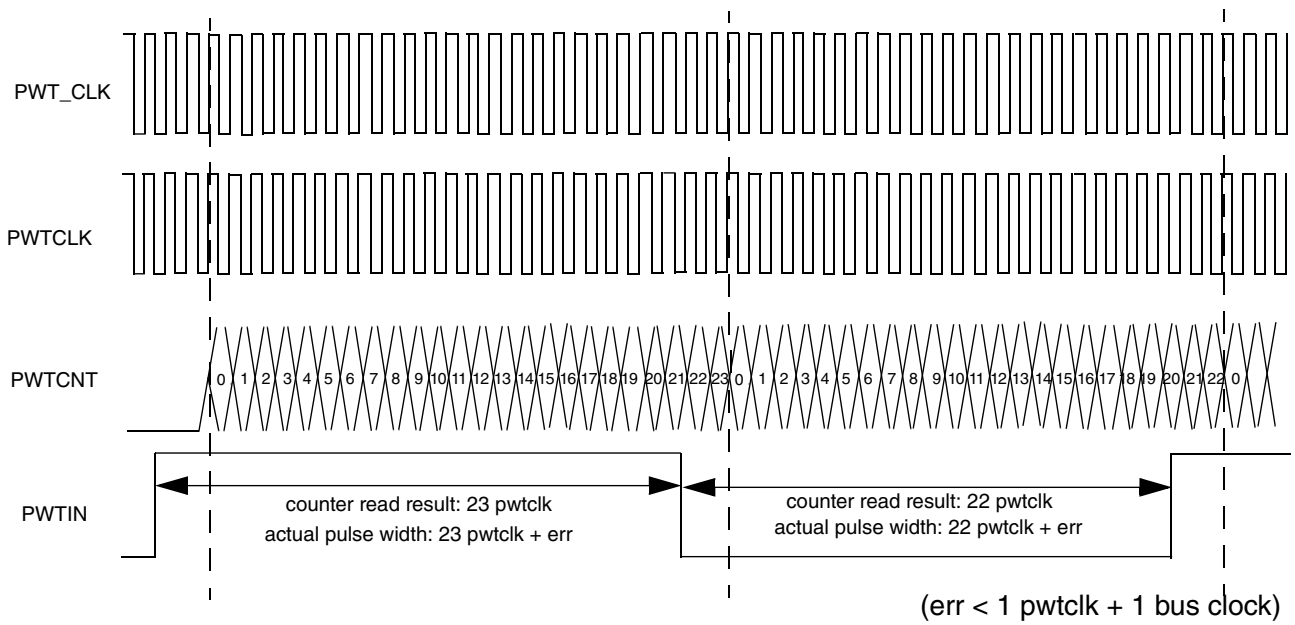


Figure 17-8. Example at PWTCLK is Bus Clock divided by 1

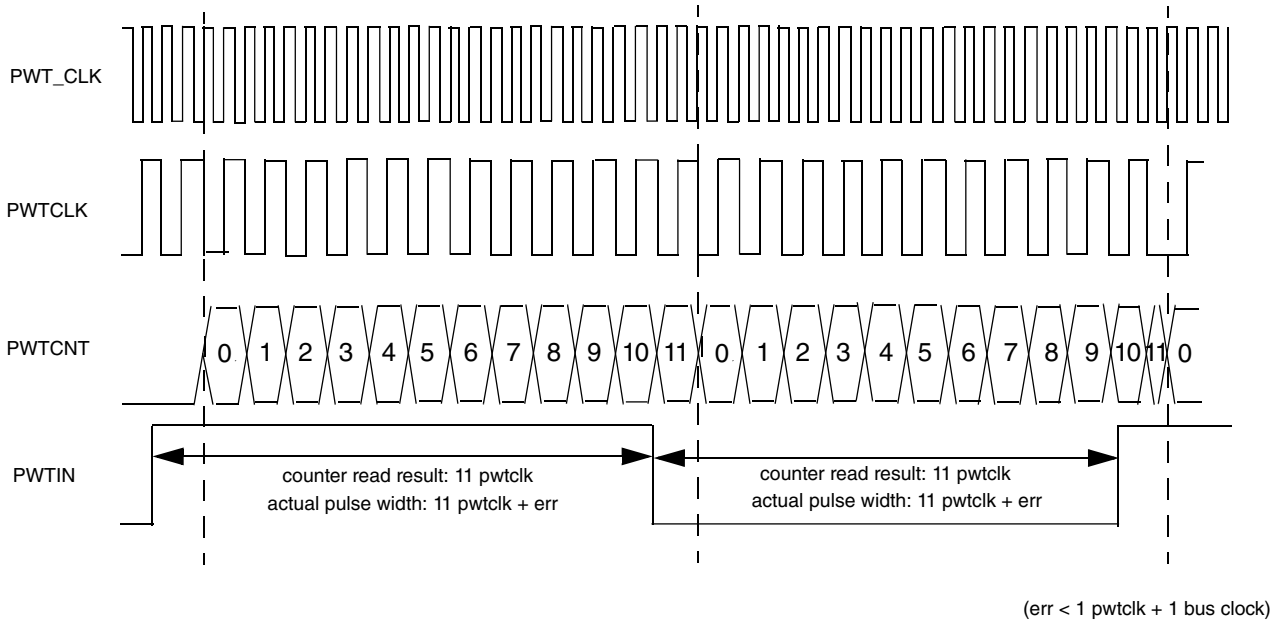


Figure 17-9. Example at PWTCLK is Bus Clock divided by 2

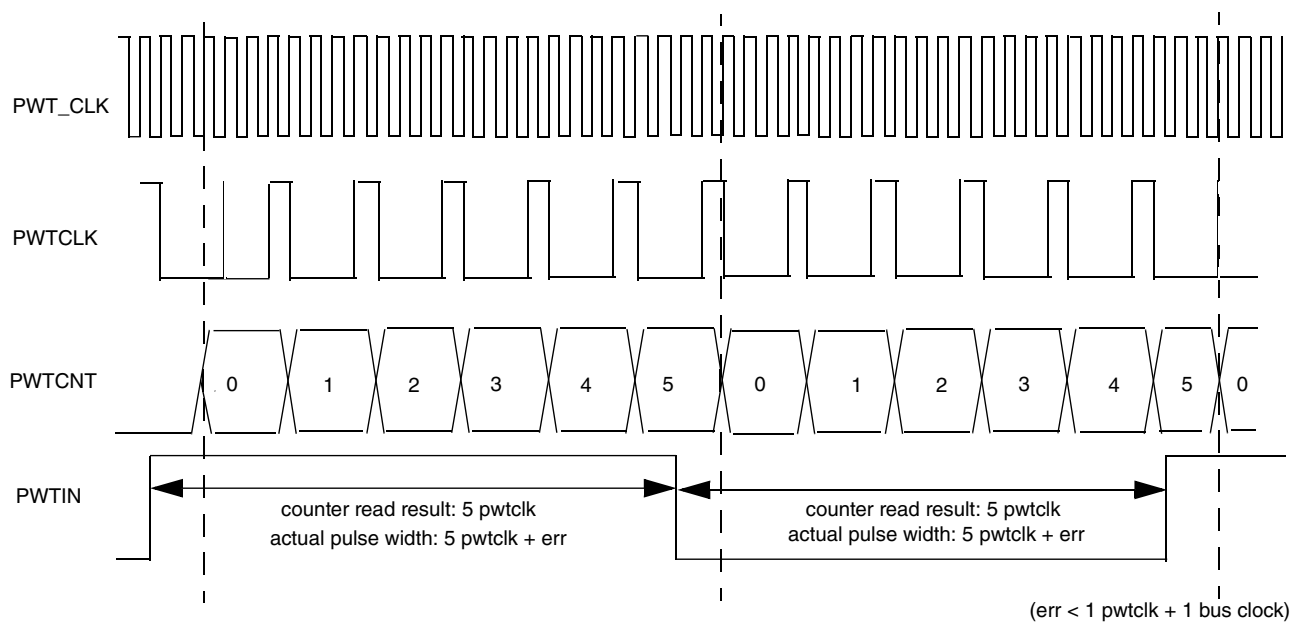


Figure 17-10. Example at PWTCLK is Bus Clock divided by 4

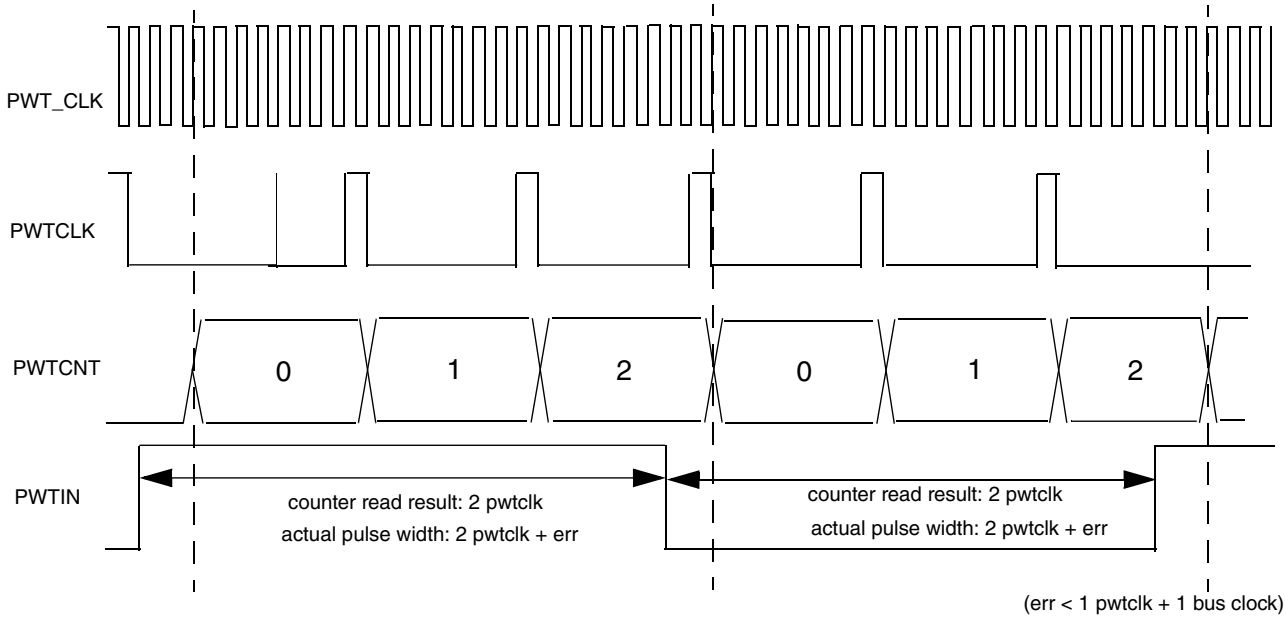


Figure 17-11. Example at PWTCLK is Bus Clock divided by 8

Chapter 18
Real-time counter (RTC)

18.1 Chip specific RTC information

This device contains a Real-Time Counter (RTC) module, which can work with other peripherals like ADC and FTM to realize flexible trigger and capture functions, refer to System Control for more details.

The RTC has the following clock options:

Table 18-1. RTC clock options

RTC Module Clock Interface	Chip Specific Clock Source
Bus clock (BUS CLK)	BUSCLK
Internal LPO clock (LPO CLK)	LPOCLK (1 kHz)
Internal RC oscillator clock (IRC CLK)	ICSIRCLK (up to the 32 kHz)
External clock (EXT CLK)	OSCOUT

18.2 Introduction

The real-time counter (RTC) consists of one 16-bit counter, one 16-bit comparator, several binary-based and decimal-based prescaler dividers, three clock sources, one programmable periodic interrupt. This module can be used for time-of-day, calendar or any task scheduling functions. It can also serve as a cyclic wake-up from low-power modes, Stop and Wait without the need of external components.

18.3 Features

Features of the RTC module include:

- 16-bit up-counter

- 16-bit modulo match limit
- Software controllable periodic interrupt on match

- Software selectable clock sources for input to prescaler with programmable 16 bit prescaler
  - OSC 32.768KHz nominal.
  - LPO (~1 kHz)
  - Bus clock
  - Internal reference clock

18.3.1 Modes of operation

This section defines the RTC operation in Stop, Wait, and Background Debug modes.

18.3.1.1 Wait mode

The RTC continues to run in Wait mode if enabled before executing the WAIT instruction. Therefore, the RTC can be used to bring the MCU out of Wait mode if the real-time interrupt is enabled. For lowest possible current consumption, the RTC must be stopped by software if not needed as an interrupt source during Wait mode.

18.3.1.2 Stop modes

The RTC continues to run in Stop mode if the RTC is enabled before executing the STOP instruction. Therefore, the RTC can be used to bring the MCU out of stop modes with no external components, if the real-time interrupt is enabled.

18.3.2 Block diagram

The block diagram for the RTC module is shown in the following figure.

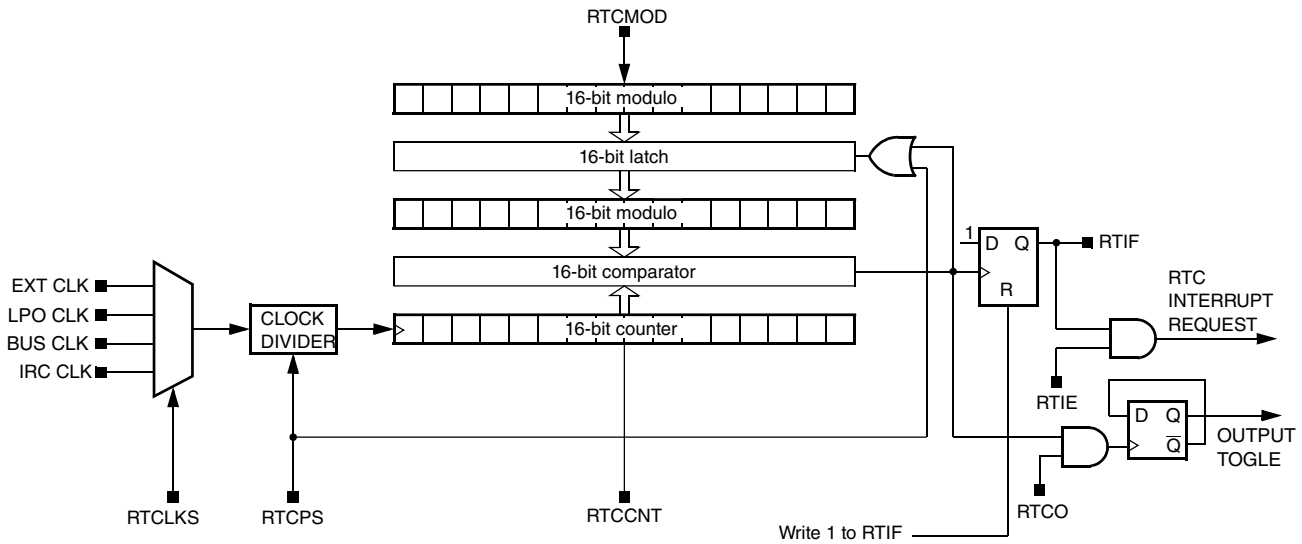


Figure 18-1. Real-time counter (RTC) block diagram

18.4 Register definition

The RTC includes a status and control register, a 16-bit counter register, and a 16-bit modulo register.

RTC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
306A	RTC Status and Control Register 1 (RTC_SC1)	8	R/W	00h	18.4.1/280
306B	RTC Status and Control Register 2 (RTC_SC2)	8	R/W	00h	18.4.2/280
306C	RTC Modulo Register: High (RTC_MODH)	8	R/W	00h	18.4.3/281
306D	RTC Modulo Register: Low (RTC_MODL)	8	R/W	00h	18.4.4/282
306E	RTC Counter Register: High (RTC_CNTH)	8	R	00h	18.4.5/282
306F	RTC Counter Register: Low (RTC_CNTL)	8	R	00h	18.4.6/283

18.4.1 RTC Status and Control Register 1 (RTC_SC1)

RTC_SC1 contains the real-time interrupt status flag (RTIF).

Address: 306Ah base + 0h offset = 306Ah

Bit	7	6	5	4	3	2	1	0
Read	RTIF	RTIE	0	Reserved	0			
Write								
Reset	0	0	0	0	0	0	0	0

RTC_SC1 field descriptions

Field	Description
7 RTIF	Real-Time Interrupt Flag This status bit indicates the RTC counter register reached the value in the RTC modulo register. Writing a logic 0 has no effect. Writing a logic 1 clears the bit and the real-time interrupt request. Reset clears RTIF to 0. 0 RTC counter has not reached the value in the RTC modulo register. 1 RTC counter has reached the value in the RTC modulo register.
6 RTIE	Real-Time Interrupt Enable This read/write bit enables real-time interrupts. If RTIE is set, then an interrupt is generated when RTIF is set. Reset clears RTIE to 0. 0 Real-time interrupt requests are disabled. Use software polling. 1 Real-time interrupt requests are enabled.
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 Reserved	This field is reserved.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

18.4.2 RTC Status and Control Register 2 (RTC_SC2)

RTC_SC2 contains the clock select bits (RTCLKS) and the prescaler select bits (RTCPS).

Address: 306Ah base + 1h offset = 306Bh

Bit	7	6	5	4	3	2	1	0
Read	RTCLKS		0		RTCPS			
Write								
Reset	0	0	0	0	0	0	0	0

RTC_SC2 field descriptions

Field	Description
7–6 RTCLKS	Real-Time Clock Source Select These two read/write bits select the clock source input to the RTC prescaler. Changing the clock source clears the prescaler and RTCCNT counters. Reset clears RTCLKS to 00. 00 External clock source. 01 Real-time clock source is 1 kHz. 10 Internal clock. 11 Bus clock.
5–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
RTCPS	Real-Time Clock Prescaler Select These four read/write bits select binary-based or decimal-based divide-by values for the clock source. Changing the prescaler value clears the prescaler and RTCCNT counters. Reset clears RTCPS to 0000. 000 Off 001 If RTCLKS = x0, it is 1; if RTCLKS = x1, it is 128. 010 If RTCLKS = x0, it is 2; if RTCLKS = x1, it is 256. 011 If RTCLKS = x0, it is 4; if RTCLKS = x1, it is 512. 100 If RTCLKS = x0, it is 8; if RTCLKS = x1, it is 1024. 101 If RTCLKS = x0, it is 16; if RTCLKS = x1, it is 2048. 110 If RTCLKS = x0, it is 32; if RTCLKS = x1, it is 100. 111 If RTCLKS = x0, it is 64; if RTCLKS = x1, it is 1000.

18.4.3 RTC Modulo Register: High (RTC_MODH)

RTC_MODH, together with RTC_MODL, indicates the value of the 16-bit modulo value.

Address: 306Ah base + 2h offset = 306Ch

Bit	7	6	5	4	3	2	1	0
Read Write	MODH							
Reset	0	0	0	0	0	0	0	0

RTC_MODH field descriptions

Field	Description
MODH	RTC Modulo High These sixteen read/write bits, MODH and MODL, contain the modulo value used to reset the count to 0x0000 upon a compare match and set the RTIF status bit. A value of 0x00 of the MODH an MODL sets the RTIF bit on each rising edge of the prescaler output. Reset sets the modulo to 0x00.

18.4.4 RTC Modulo Register: Low (RTC_MODL)

RTC_MODL, together with RTC_MODH, indicates the value of the 16-bit modulo value.

Address: 306Ah base + 3h offset = 306Dh

Bit	7	6	5	4	3	2	1	0
Read Write	MODL							
Reset	0	0	0	0	0	0	0	0

RTC_MODL field descriptions

Field	Description
MODL	RTC Modulo Low These sixteen read/write bits, MODH and MODL, contain the modulo value used to reset the count to 0x0000 upon a compare match and set the RTIF status bit. A value of 0x00 of the MODH an MODL sets the RTIF bit on each rising edge of the prescaler output. Reset sets the modulo to 0x00.

18.4.5 RTC Counter Register: High (RTC_CNTH)

RTC_CNTH, together with RTC_CNTL, indicates the read-only value of the current RTC count of the 16-bit counter.

NOTE

The RTC_CNTL must be read first to lock the counter and then read RTC_CNTH to correctly read 16-bit counter.

Address: 306Ah base + 4h offset = 306Eh

Bit	7	6	5	4	3	2	1	0
Read	CNTH							
Write								
Reset	0	0	0	0	0	0	0	0

RTC_CNTH field descriptions

Field	Description
CNTH	RTC Count High CNTH and CNTL contain the current value of the 16-bit counter. Writes have no effect to this register. Reset or writing different values to RTCLKS and RTCPS clear the count to 0x00.

18.4.6 RTC Counter Register: Low (RTC_CNTL)

RTC_CNTL, together with RTC_CNTH, indicates the read-only value of the current RTC count of the 16-bit counter.

Address: 306Ah base + 5h offset = 306Fh

Bit	7	6	5	4	3	2	1	0
Read	CNTL							
Write								
Reset	0	0	0	0	0	0	0	0

RTC_CNTL field descriptions

Field	Description
CNTL	RTC Count Low CNTH and CNTL contain the current value of the 16-bit counter. Writes have no effect to this register. Reset or writing different values to RTCLKS and RTCPS clear the count to 0x00.

18.5 Functional description

The RTC is composed of a main 16-bit up-counter with a 16-bit modulo register, a clock source selector, and a prescaler block with binary-based and decimal-based selectable values. The module also contains software selectable interrupt logic .

After any MCU reset, the counter is stopped and reset to 0x0000, the modulus register is set to 0x0000, and the prescaler is off. The external oscillator clock is selected as the default clock source. To start the prescaler, write any value other than 0 to the Prescaler Select field (RTC_SC2[RTCPS]).

The clock sources are software selectable: the external oscillator (OSC), on-chip low power oscillator (LPO), internal reference clock, and bus clock. The RTC Clock Select field (RTC_SC2[RTCLKS]) is used to select the desired clock source to the prescaler dividers. If a different value is written to RTC_SC2[RTCLKS], the prescaler and CNTH and RTC_CNTL counters are reset to 0x00.

RTC_SC2[RTCPS] and RTC_SC2[RTCLKS] select the desired divide-by value. If a different value is written to RTC_SC2[RTCPS], the prescaler and RTCCNT counters are reset to 0x00. The following table shows different prescaler period values.

Table 18-2. Prescaler period

RTCPS	32768Hz OSC clock source prescaler period (RTCLKS = 00)	LPO clock (1 kHz) source prescaler period (RTCLKS = 01)	Internal reference clock source prescaler period (RTCLKS = 10)	Bus clock (8 MHz) source prescaler period (RTCLKS = 11)
000	Off	Off	Off	Off
001	30.5176 µs	128 ms	30.5176 µs	16 µs
010	61.0351 µs	256 ms	61.0351 µs	32 µs
011	122.0703 µs	512 ms	122.0703 µs	64 µs
100	244.1406 µs	1024 ms	244.1406 µs	128 µs
101	488.28125 µs	2048 ms	488.28125 µs	256 µs
110	976.5625 µs	100 ms	976.5625 µs	12.5 µs
111	1.9531 ms	1 s	1.9531 ms	125 µs

The RTC Modulo register (RTC_MODH and RTC_MODL) allows the compare value to be set to any value from 0x0000 to 0xFFFF. When the counter is active, the counter increments at the selected rate until the count matches the modulo value. When these values match, the counter resets to 0x0000 and continues counting. The Real-Time Interrupt Flag (RTC_SC1[RTIF]) is set whenever a match occurs. The flag sets on the transition from the modulo value to 0x0000. The modulo value written to RTC_MODH and RTC_MODL is latched until the RTC counter overflows or RTC_SC2[RTCPS] is selected nonzero.

The RTC allows for an interrupt to be generated whenever RTC_SC1[RTIF] is set. To enable the real-time interrupt, set the Real-Time Interrupt Enable field (RTC_SC1[RTIE]). RTC_SC1[RTIF] is cleared by writing a 1 to RTC_SC1[RTIF].

18.5.1 RTC operation example

This section shows an example of the RTC operation as the counter reaches a matching value from the modulo register.

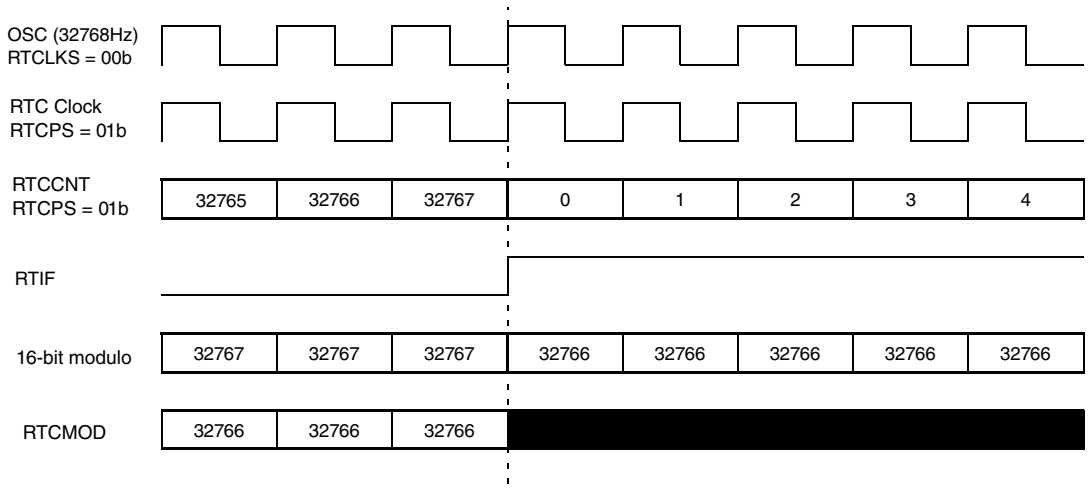


Figure 18-2. RTC counter overflow example

In the above example, the external clock source is selected. The prescaler is set to RTC_SC2[RTCPS] = 001b or passthrough. The actual modulo value used by 16-bit comparator is 32767, when the modulo value in the RTC_MODH and RTC_MODL registers is set to 32766. When the counter, RTC_CNTH and RTC_CNTL, reaches the modulo value of 32767, the counter overflows to 0x00 and continues counting. The modulo value is updated by fetching from RTC_MODH and RTC_MODL registers. The real-time interrupt flag, RTC_SC1[RTIF], sets when the counter value changes from 0x7FFF to 0x0000.

18.6 Initialization/application information

This section provides example code to give some basic direction to a user on how to initialize and configure the RTC module. The example software is implemented in C language.

The example below shows how to implement time of day with the RTC using the OSC clock source to achieve the lowest possible power consumption.

Example: 18.6.1 Software calendar implementation in RTC ISR

```
/* Initialize the elapsed time counters */
Seconds = 0;
Minutes = 0;
Hours = 0;
Days=0;

/* Configure RTC to interrupt every 1 second from OSC (32.768KHz) clock source */
RTC_MOD = 511; // overflow every 512 times
```

Initialization/application information

```
RTC_SC2 = RTC_SC2_RTCPS_MASK; // external 32768 clock selected with 1/64 predivider.
RTC_SC1 = RTC_SC1_RTIF_MASK | RTC_SC1_RTIE_MASK; // interrupt cleared and enabled

/*********************************************************************
Function Name : RTC_ISR
Notes : Interrupt service routine for RTC module.
*********************************************************************/
void RTC_ISR(void)
{
/* Clears the interrupt flag, RTIF, and interrupt request */
RTC_SC1 |= RTC_SC1_RTIF_MASK;

/* RTC interrupts every 1 Second */
Seconds++;

/* 60 seconds in a minute */
if (Seconds > 59)
{
Minutes++;
Seconds = 0;
}

/* 60 minutes in an hour */
if (Minutes > 59)
{
Hours++;
Minutes = 0;
}

/* 24 hours in a day */
if (Hours > 23)
{
Days ++;
Hours = 0;
}
}
```

Chapter 19
Serial communications interface (SCI)

19.1 Chip specific SCI information

This device includes one independent serial communications interface (SCI) module, which can work with FTM, ACMP to realize more complicated functions, refer to System Control for more details.

The following table summarizes the external signals of SCIs modules

Table 19-1. SCI modules external signals

SCI	Functions	Default	Alternate
SCI0	TxD	PTB1/TxD	PTA3/TxD
	RxD	PTB0/RxD	PTA2/RxD

SCI0 channels can be configured on different pinouts by setting SYS_SOPT1[SCI0PS].

19.2 Introduction

19.2.1 Features

Features of SCI module include:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Double-buffered transmitter and receiver with separate enables
- Programmable baud rates (13-bit modulo divider)
- Interrupt-driven or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error

  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length
- Programmable 1-bit or 2-bit stop bits
- Receiver wakeup by idle-line or address-mark
- Optional 13-bit break character generation / 11-bit break character detection
- Selectable transmitter output polarity

19.2.2 Modes of operation

See Section Functional description for details concerning SCI operation in these modes:

- 8- and 9-bit data modes
- Stop mode operation
- Loop mode
- Single-wire mode

19.2.3 Block diagram

The following figure shows the transmitter portion of the SCI.

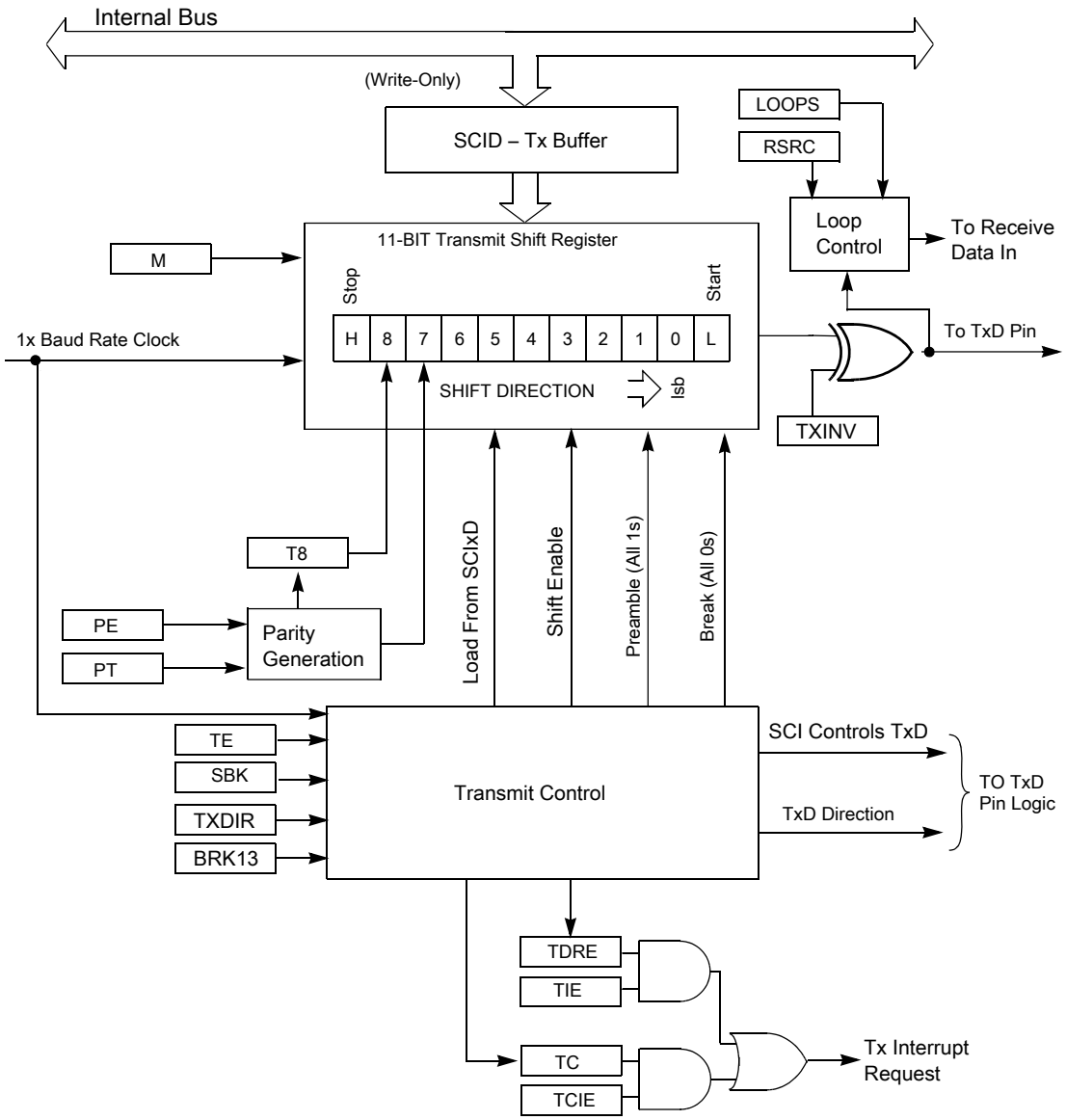


Figure 19-1. SCI transmitter block diagram

The following figure shows the receiver portion of the SCI.

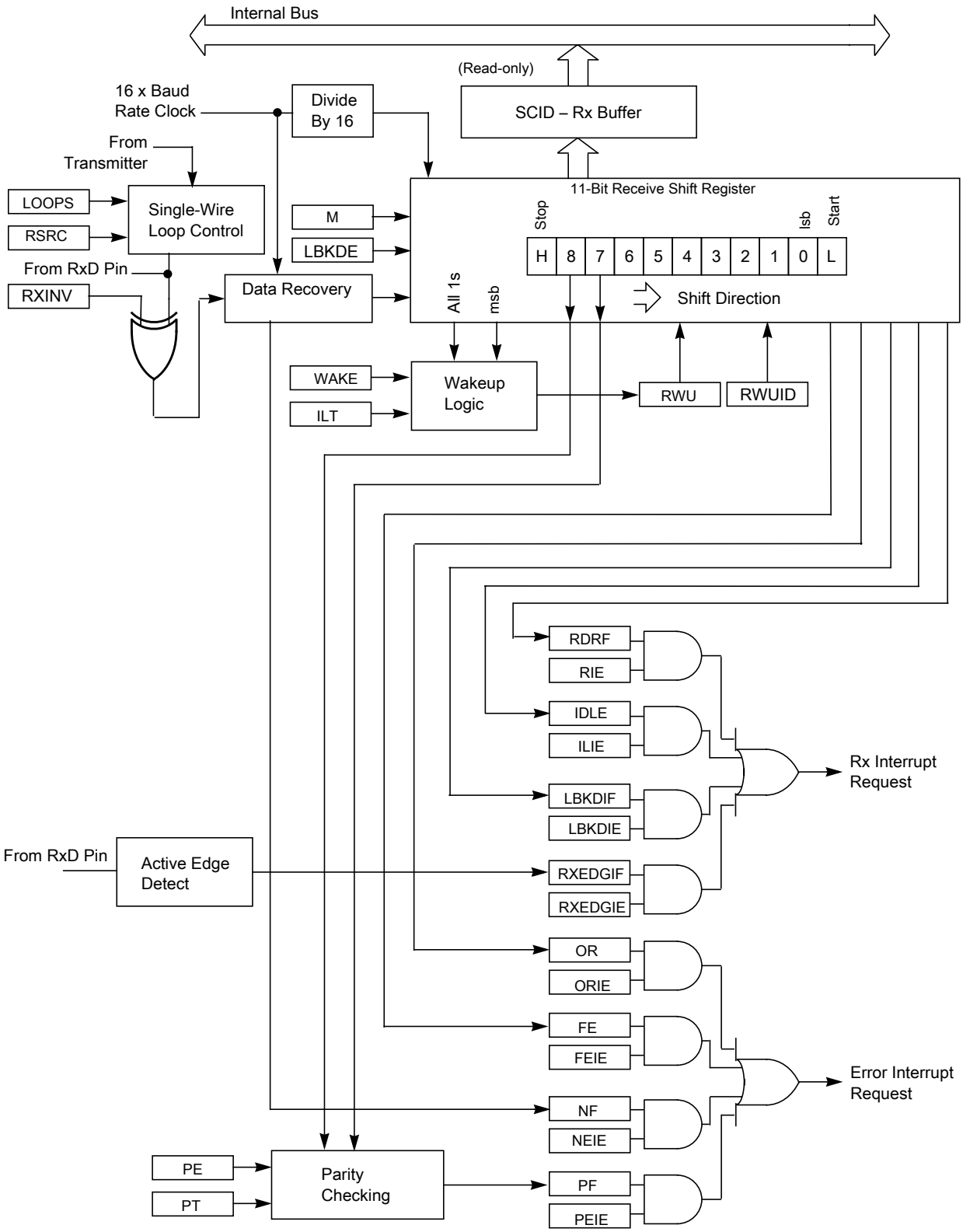


Figure 19-2. SCI receiver block diagram

19.3 SCI signal descriptions

The SCI signals are shown in the table found here.

Table 19-2. SCI signal descriptions

Signal	Description	I/O
RxD	Receive data	I
TxD	Transmit data	I/O

19.3.1 Detailed signal descriptions

The detailed signal descriptions of the SCI are shown in the following table.

Table 19-3. SCI—Detailed signal descriptions

Signal	I/O	Description	
RxD	I	Receive data. Serial data input to receiver.	
		State meaning	Whether RxD is interpreted as a 1 or 0 depends on the bit encoding method along with other configuration settings.
		Timing	Sampled at a frequency determined by the module clock divided by the baud rate.
TxD	I/O	Transmit data. Serial data output from transmitter.	
		State meaning	Whether TxD is interpreted as a 1 or 0 depends on the bit encoding method along with other configuration settings.
		Timing	Driven at the beginning or within a bit time according to the bit encoding method along with other configuration settings. Otherwise, transmissions are independent of reception timing.

19.4 Register definition

The SCI has 8-bit registers to control baud rate, select SCI options, report SCI status, and for transmit/receive data.

Refer to the direct-page register summary in the memory chapter of this document or the absolute address assignments for all SCI registers. This section refers to registers and control bits only by their names. An NXP-provided equate or header file is used to translate these names into the appropriate absolute addresses.

SCI memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3080	SCI Baud Rate Register: High (SCI0_BDH)	8	R/W	00h	19.4.1/292
3081	SCI Baud Rate Register: Low (SCI0_BDL)	8	R/W	04h	19.4.2/293
3082	SCI Control Register 1 (SCI0_C1)	8	R/W	00h	19.4.3/293
3083	SCI Control Register 2 (SCI0_C2)	8	R/W	00h	19.4.4/295
3084	SCI Status Register 1 (SCI0_S1)	8	R	C0h	19.4.5/296
3085	SCI Status Register 2 (SCI0_S2)	8	R/W	00h	19.4.6/298
3086	SCI Control Register 3 (SCI0_C3)	8	R/W	00h	19.4.7/299
3087	SCI Data Register (SCI0_D)	8	R/W	00h	19.4.8/301

19.4.1 SCI Baud Rate Register: High (SCIx_BDH)

This register, along with SCI_BDL, controls the prescale divisor for SCI baud rate generation. To update the 13-bit baud rate setting [SBR12:SBR0], first write to SCI_BDH to buffer the high half of the new value and then write to SCI_BDL. The working value in SCI_BDH does not change until SCI_BDL is written.

Address: 3080h base + 0h offset = 3080h

Bit	7	6	5	4	3	2	1	0
Read Write	LBKDIE	RXEDGIE	SBNS	SBR				
Reset	0	0	0	0	0	0	0	0

SCIx_BDH field descriptions

Field	Description
7 LBKDIE	LIN Break Detect Interrupt Enable (for LBKDIF) 0 Hardware interrupts from SCI_S2[LBKDIF] disabled (use polling). 1 Hardware interrupt requested when SCI_S2[LBKDIF] flag is 1.
6 RXEDGIE	RxD Input Active Edge Interrupt Enable (for RXEDGIF) 0 Hardware interrupts from SCI_S2[RXEDGIF] disabled (use polling). 1 Hardware interrupt requested when SCI_S2[RXEDGIF] flag is 1.
5 SBNS	Stop Bit Number Select SBNS determines whether data characters are one or two stop bits. 0 One stop bit. 1 Two stop bit.
SBR	Baud Rate Modulo Divisor.

Table continues on the next page...

SCIx_BDH field descriptions (continued)

Field	Description
	The 13 bits in SBR[12:0] are referred to collectively as BR, and they set the modulo divide rate for the SCI baud rate generator. When BR is cleared, the SCI baud rate generator is disabled to reduce supply current. When BR is 1 - 8191, the SCI baud rate equals BUSCLK/(16×BR).

19.4.2 SCI Baud Rate Register: Low (SCIx_BDL)

This register, along with SCI_BDH, control the prescale divisor for SCI baud rate generation. To update the 13-bit baud rate setting [SBR12:SBR0], first write to SCI_BDH to buffer the high half of the new value and then write to SCI_BDL. The working value in SCI_BDH does not change until SCI_BDL is written.

SCI_BDL is reset to a non-zero value, so after reset the baud rate generator remains disabled until the first time the receiver or transmitter is enabled; that is, SCI_C2[RE] or SCI_C2[TE] bits are written to 1.

Address: 3080h base + 1h offset = 3081h

Bit	7	6	5	4	3	2	1	0
Read Write	SBR							
Reset	0	0	0	0	0	1	0	0

SCIx_BDL field descriptions

Field	Description
SBR	Baud Rate Modulo Divisor These 13 bits in SBR[12:0] are referred to collectively as BR. They set the modulo divide rate for the SCI baud rate generator. When BR is cleared, the SCI baud rate generator is disabled to reduce supply current. When BR is 1 - 8191, the SCI baud rate equals BUSCLK/(16×BR).

19.4.3 SCI Control Register 1 (SCIx_C1)

This read/write register controls various optional features of the SCI system.

Address: 3080h base + 2h offset = 3082h

Bit	7	6	5	4	3	2	1	0
Read Write	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
Reset	0	0	0	0	0	0	0	0

SCIx_C1 field descriptions

Field	Description
7 LOOPS	Loop Mode Select Selects between loop back modes and normal 2-pin full-duplex modes. When LOOPS is set, the transmitter output is internally connected to the receiver input. 0 Normal operation - RxD and TxD use separate pins. 1 Loop mode or single-wire mode where transmitter outputs are internally connected to receiver input. (See RSRC bit.) RxD pin is not used by SCI.
6 SCISWAI	SCI Stops in Wait Mode 0 SCI clocks continue to run in wait mode so the SCI can be the source of an interrupt that wakes up the CPU. 1 SCI clocks freeze while CPU is in wait mode.
5 RSRC	Receiver Source Select This bit has no meaning or effect unless the LOOPS bit is set to 1. When LOOPS is set, the receiver input is internally connected to the TxD pin and RSRC determines whether this connection is also connected to the transmitter output. 0 Provided LOOPS is set, RSRC is cleared, selects internal loop back mode and the SCI does not use the RxD pins. 1 Single-wire SCI mode where the TxD pin is connected to the transmitter output and receiver input.
4 M	9-Bit or 8-Bit Mode Select 0 Normal - start + 8 data bits (lsb first) + stop. 1 Receiver and transmitter use 9-bit data characters start + 8 data bits (lsb first) + 9th data bit + stop.
3 WAKE	Receiver Wakeup Method Select 0 Idle-line wakeup. 1 Address-mark wakeup.
2 ILT	Idle Line Type Select Setting this bit to 1 ensures that the stop bits and logic 1 bits at the end of a character do not count toward the 10 or 11 bit times of logic high level needed by the idle line detection logic. 0 Idle character bit count starts after start bit. 1 Idle character bit count starts after stop bit.
1 PE	Parity Enable Enables hardware parity generation and checking. When parity is enabled, the most significant bit (msb) of the data character, eighth or ninth data bit, is treated as the parity bit. 0 No hardware parity generation or checking. 1 Parity enabled.
0 PT	Parity Type Provided parity is enabled (PE = 1), this bit selects even or odd parity. Odd parity means the total number of 1s in the data character, including the parity bit, is odd. Even parity means the total number of 1s in the data character, including the parity bit, is even. 0 Even parity. 1 Odd parity.

19.4.4 SCI Control Register 2 (SCIx_C2)

This register can be read or written at any time.

Address: 3080h base + 3h offset = 3083h

Bit	7	6	5	4	3	2	1	0
Read Write	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset	0	0	0	0	0	0	0	0

SCIx_C2 field descriptions

Field	Description
7 TIE	Transmit Interrupt Enable for TDRE 0 Hardware interrupts from TDRE disabled; use polling. 1 Hardware interrupt requested when TDRE flag is 1.
6 TCIE	Transmission Complete Interrupt Enable for TC 0 Hardware interrupts from TC disabled; use polling. 1 Hardware interrupt requested when TC flag is 1.
5 RIE	Receiver Interrupt Enable for RDRF 0 Hardware interrupts from RDRF disabled; use polling. 1 Hardware interrupt requested when RDRF flag is 1.
4 ILIE	Idle Line Interrupt Enable for IDLE 0 Hardware interrupts from IDLE disabled; use polling. 1 Hardware interrupt requested when IDLE flag is 1.
3 TE	Transmitter Enable TE must be 1 to use the SCI transmitter. When TE is set, the SCI forces the TxD pin to act as an output for the SCI system. When the SCI is configured for single-wire operation (LOOPS = RSRC = 1), TXDIR controls the direction of traffic on the single SCI communication line (TxD pin). TE can also queue an idle character by clearing TE then setting TE while a transmission is in progress. When TE is written to 0, the transmitter keeps control of the port TxD pin until any data, queued idle, or queued break character finishes transmitting before allowing the pin to revert to a general-purpose I/O pin. 0 Transmitter off. 1 Transmitter on.
2 RE	Receiver Enable When the SCI receiver is off, the RxD pin reverts to being a general-purpose port I/O pin. If LOOPS is set the RxD pin reverts to being a general-purpose I/O pin even if RE is set. 0 Receiver off. 1 Receiver on.
1 RWU	Receiver Wakeup Control

Table continues on the next page...

SCIx_C2 field descriptions (continued)

Field	Description
	This bit can be written to 1 to place the SCI receiver in a standby state where it waits for automatic hardware detection of a selected wakeup condition. The wakeup condition is an idle line between messages, WAKE = 0, idle-line wakeup, or a logic 1 in the most significant data bit in a character, WAKE = 1, address-mark wakeup. Application software sets RWU and, normally, a selected hardware condition automatically clears RWU. 0 Normal SCI receiver operation. 1 SCI receiver in standby waiting for wakeup condition.
0 SBK	Send Break Writing a 1 and then a 0 to SBK queues a break character in the transmit data stream. Additional break characters of 10 or 11 or 12, 13 or 14 or 15 if BRK13 = 1, bit times of logic 0 are queued as long as SBK is set. Depending on the timing of the set and clear of SBK relative to the information currently being transmitted, a second break character may be queued before software clears SBK. 0 Normal transmitter operation. 1 Queue break character(s) to be sent.

19.4.5 SCI Status Register 1 (SCIx_S1)

This register has eight read-only status flags. Writes have no effect. Special software sequences, which do not involve writing to this register, clear these status flags.

Address: 3080h base + 4h offset = 3084h

Bit	7	6	5	4	3	2	1	0
Read	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
Write								
Reset	1	1	0	0	0	0	0	0

SCIx_S1 field descriptions

Field	Description
7 TDRE	Transmit Data Register Empty Flag TDRE is set out of reset and when a transmit data value transfers from the transmit data buffer to the transmit shifter, leaving room for a new character in the buffer. To clear TDRE, read SCI_S1 with TDRE set and then write to the SCI data register (SCI_D). 0 Transmit data register (buffer) full. 1 Transmit data register (buffer) empty.
6 TC	Transmission Complete Flag TC is set out of reset and when TDRE is set and no data, preamble, or break character is being transmitted. TC is cleared automatically by reading SCI_S1 with TC set and then doing one of the following: • Write to the SCI data register (SCI_D) to transmit new data • Queue a preamble by changing TE from 0 to 1 • Queue a break character by writing 1 to SCI_C2[SBK]

Table continues on the next page...

SCIx_S1 field descriptions (continued)

Field	Description
	0 Transmitter active (sending data, a preamble, or a break). 1 Transmitter idle (transmission activity complete).
5 RDRF	Receive Data Register Full Flag RDRF becomes set when a character transfers from the receive shifter into the receive data register (SCI_D). To clear RDRF, read SCI_S1 with RDRF set and then read the SCI data register (SCI_D). 0 Receive data register empty. 1 Receive data register full.
4 IDLE	Idle Line Flag IDLE is set when the SCI receive line becomes idle for a full character time after a period of activity. When ILT is cleared, the receiver starts counting idle bit times after the start bit. If the receive character is all 1s, these bit times and the stop bits time count toward the full character time of logic high, 10 or 11 bit times depending on the M control bit, needed for the receiver to detect an idle line. When ILT is set, the receiver doesn't start counting idle bit times until after the stop bits. The stop bits and any logic high bit times at the end of the previous character do not count toward the full character time of logic high needed for the receiver to detect an idle line. To clear IDLE, read SCI_S1 with IDLE set and then read the SCI data register (SCI_D). After IDLE has been cleared, it cannot become set again until after a new character has been received and RDRF has been set. IDLE is set only once even if the receive line remains idle for an extended period. 0 No idle line detected. 1 Idle line was detected.
3 OR	Receiver Overrun Flag OR is set when a new serial character is ready to be transferred to the receive data register (buffer), but the previously received character has not been read from SCI_D yet. In this case, the new character, and all associated error information, is lost because there is no room to move it into SCI_D. To clear OR, read SCI_S1 with OR set and then read the SCI data register (SCI_D). 0 No overrun. 1 Receive overrun (new SCI data lost).
2 NF	Noise Flag The advanced sampling technique used in the receiver takes seven samples during the start bit and three samples in each data bit and the stop bits. If any of these samples disagrees with the rest of the samples within any bit time in the frame, the flag NF is set at the same time as RDRF is set for the character. To clear NF, read SCI_S1 and then read the SCI data register (SCI_D). 0 No noise detected. 1 Noise detected in the received character in SCI_D.
1 FE	Framing Error Flag FE is set at the same time as RDRF when the receiver detects a logic 0 where the stop bits was expected. This suggests the receiver was not properly aligned to a character frame. To clear FE, read SCI_S1 with FE set and then read the SCI data register (SCI_D). 0 No framing error detected. This does not guarantee the framing is correct. 1 Framing error.
0 PF	Parity Error Flag

Table continues on the next page...

SCIx_S1 field descriptions (continued)

Field	Description
	PF is set at the same time as RDRF when parity is enabled (PE = 1) and the parity bit in the received character does not agree with the expected parity value. To clear PF, read SCI_S1 and then read the SCI data register (SCI_D). 0 No parity error. 1 Parity error.

19.4.6 SCI Status Register 2 (SCIx_S2)

This register contains one read-only status flag.

When using an internal oscillator in a LIN system, it is necessary to raise the break detection threshold one bit time. Under the worst case timing conditions allowed in LIN, it is possible that a 0x00 data character can appear to be 10.26 bit times long at a slave running 14% faster than the master. This would trigger normal break detection circuitry designed to detect a 10-bit break symbol. When the LBKDE bit is set, framing errors are inhibited and the break detection threshold changes from 10 bits to 11 bits, preventing false detection of a 0x00 data character as a LIN break symbol.

Address: 3080h base + 5h offset = 3085h

Bit	7	6	5	4	3	2	1	0
Read	LBKDIF	RXEDGIF	0	RXINV	RWUID	BRK13	LBKDE	RAF
Write								
Reset	0	0	0	0	0	0	0	0

SCIx_S2 field descriptions

Field	Description
7 LBKDIF	LIN Break Detect Interrupt Flag LBKDIF is set when the LIN break detect circuitry is enabled and a LIN break character is detected. LBKDIF is cleared by writing a 1 to it. 0 No LIN break character has been detected. 1 LIN break character has been detected.
6 RXEDGIF	RxD Pin Active Edge Interrupt Flag RXEDGIF is set when an active edge, falling if RXINV = 0, rising if RXINV=1, on the RxD pin occurs. RXEDGIF is cleared by writing a 1 to it. 0 No active edge on the receive pin has occurred. 1 An active edge on the receive pin has occurred.
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

SCIx_S2 field descriptions (continued)

Field	Description
4 RXINV	Receive Data Inversion Setting this bit reverses the polarity of the received data input. **NOTE:** Setting RXINV inverts the RxD input for all cases: data bits, start and stop bits, break, and idle. 0 Receive data not inverted. 1 Receive data inverted.
3 RWUID	Receive Wake Up Idle Detect RWUID controls whether the idle character that wakes up the receiver sets the IDLE bit. 0 During receive standby state (RWU = 1), the IDLE bit does not get set upon detection of an idle character. 1 During receive standby state (RWU = 1), the IDLE bit gets set upon detection of an idle character.
2 BRK13	Break Character Generation Length BRK13 selects a longer transmitted break character length. Detection of a framing error is not affected by the state of this bit. 0 Break character is transmitted with length of 10 bit times (if M = 0, SBNS = 0) or 11 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 12 (if M = 1, SBNS = 1). 1 Break character is transmitted with length of 13 bit times (if M = 0, SBNS = 0) or 14 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 15 (if M = 1, SBNS = 1).
1 LBKDE	LIN Break Detection Enable LBKDE selects a longer break character detection length. While LBKDE is set, framing error (FE) and receive data register full (RDRF) flags are prevented from setting. 0 Break character is detected at length 10 bit times (if M = 0, SBNS = 0) or 11 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 12 (if M = 1, SBNS = 1). 1 Break character is detected at length of 11 bit times (if M = 0, SBNS = 0) or 12 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 13 (if M = 1, SBNS = 1).
0 RAF	Receiver Active Flag RAF is set when the SCI receiver detects the beginning of a valid start bit, and RAF is cleared automatically when the receiver detects an idle line. This status flag can be used to check whether an SCI character is being received before instructing the MCU to go to stop mode. 0 SCI receiver idle waiting for a start bit. 1 SCI receiver active (RxD input not idle).

19.4.7 SCI Control Register 3 (SCIx_C3)

Address: 3080h base + 6h offset = 3086h

Bit	7	6	5	4	3	2	1	0
Read	R8	T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE
Write								
Reset	0	0	0	0	0	0	0	0

SCIx_C3 field descriptions

Field	Description
7 R8	Ninth Data Bit for Receiver When the SCI is configured for 9-bit data (M = 1), R8 can be thought of as a ninth receive data bit to the left of the msb of the buffered data in the SCI_D register. When reading 9-bit data, read R8 before reading SCI_D because reading SCI_D completes automatic flag clearing sequences that could allow R8 and SCI_D to be overwritten with new data.
6 T8	Ninth Data Bit for Transmitter When the SCI is configured for 9-bit data (M = 1), T8 may be thought of as a ninth transmit data bit to the left of the msb of the data in the SCI_D register. When writing 9-bit data, the entire 9-bit value is transferred to the SCI shift register after SCI_D is written so T8 should be written, if it needs to change from its previous value, before SCI_D is written. If T8 does not need to change in the new value, such as when it is used to generate mark or space parity, it need not be written each time SCI_D is written.
5 TXDIR	TxD Pin Direction in Single-Wire Mode When the SCI is configured for single-wire half-duplex operation (LOOPS = RSRC = 1), this bit determines the direction of data at the TxD pin. 0 TxD pin is an input in single-wire mode. 1 TxD pin is an output in single-wire mode.
4 TXINV	Transmit Data Inversion Setting this bit reverses the polarity of the transmitted data output. **NOTE:** Setting TXINV inverts the TxD output for all cases: data bits, start and stop bits, break, and idle. 0 Transmit data not inverted. 1 Transmit data inverted.
3 ORIE	Overrun Interrupt Enable This bit enables the overrun flag (OR) to generate hardware interrupt requests. 0 OR interrupts disabled; use polling. 1 Hardware interrupt requested when OR is set.
2 NEIE	Noise Error Interrupt Enable This bit enables the noise flag (NF) to generate hardware interrupt requests. 0 NF interrupts disabled; use polling). 1 Hardware interrupt requested when NF is set.
1 FEIE	Framing Error Interrupt Enable This bit enables the framing error flag (FE) to generate hardware interrupt requests. 0 FE interrupts disabled; use polling). 1 Hardware interrupt requested when FE is set.
0 PEIE	Parity Error Interrupt Enable This bit enables the parity error flag (PF) to generate hardware interrupt requests. 0 PF interrupts disabled; use polling). 1 Hardware interrupt requested when PF is set.

19.4.8 SCI Data Register (SCIx_D)

This register is actually two separate registers. Reads return the contents of the read-only receive data buffer and writes go to the write-only transmit data buffer. Reads and writes of this register are also involved in the automatic flag clearing mechanisms for the SCI status flags.

Address: 3080h base + 7h offset = 3087h

Bit	7	6	5	4	3	2	1	0
Read Write	R7T7	R6T6	R5T5	R4T4	R3T3	R2T2	R1T1	R0T0
Reset	0	0	0	0	0	0	0	0

SCIx_D field descriptions

Field	Description
7 R7T7	Read receive data buffer 7 or write transmit data buffer 7.
6 R6T6	Read receive data buffer 6 or write transmit data buffer 6.
5 R5T5	Read receive data buffer 5 or write transmit data buffer 5.
4 R4T4	Read receive data buffer 4 or write transmit data buffer 4.
3 R3T3	Read receive data buffer 3 or write transmit data buffer 3.
2 R2T2	Read receive data buffer 2 or write transmit data buffer 2.
1 R1T1	Read receive data buffer 1 or write transmit data buffer 1.
0 R0T0	Read receive data buffer 0 or write transmit data buffer 0.

19.5 Functional description

The SCI allows full-duplex, asynchronous, NRZ serial communication among the MCU and remote devices, including other MCUs.

The SCI comprises a baud rate generator, transmitter, and receiver block. The transmitter and receiver operate independently, although they use the same baud rate generator. During normal operation, the MCU monitors the status of the SCI, writes the data to be transmitted, and processes received data. The following describes each of the blocks of the SCI.

19.5.1 Baud rate generation

As shown in the figure found here, the clock source for the SCI baud rate generator is the bus-rate clock.

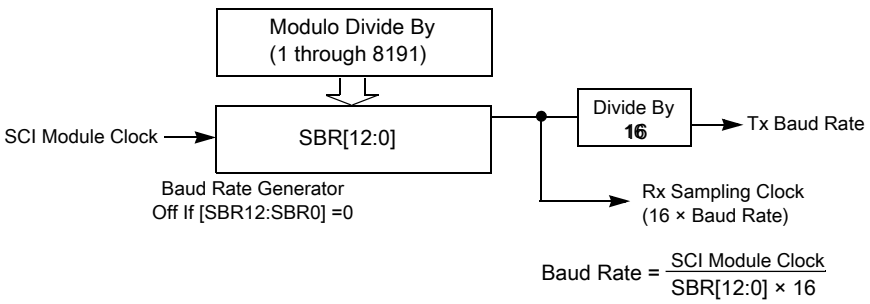


Figure 19-3. SCI baud rate generation

SCI communications require the transmitter and receiver, which typically derive baud rates from independent clock sources, to use the same baud rate. Allowed tolerance on this baud frequency depends on the details of how the receiver synchronizes to the leading edge of the start bit and how bit sampling is performed.

The MCU resynchronizes to bit boundaries on every high-to-low transition. In the worst case, there are no such transitions in the full 10- or 11-bit or 12-bittime character frame so any mismatch in baud rate is accumulated for the whole character time. For an NXP SCI system whose bus frequency is driven by a crystal, the allowed baud rate mismatch is about ±4.5 percent for 8-bit data format and about ±4 percent for 9-bit data format. Although baud rate modulo divider settings do not always produce baud rates that exactly match standard rates, it is normally possible to get within a few percent, which is acceptable for reliable communications.

19.5.2 Transmitter functional description

This section describes the overall block diagram for the SCI transmitter, as well as specialized functions for sending break and idle characters.

The transmitter output (TxD) idle state defaults to logic high, SCI_C3[TXINV] is cleared following reset. The transmitter output is inverted by setting SCI_C3[TXINV]. The transmitter is enabled by setting the TE bit in SCI_C2. This queues a preamble character that is one full character frame of the idle state. The transmitter then remains idle until data is available in the transmit data buffer. Programs store data into the transmit data buffer by writing to the SCI data register (SCI_D).

The central element of the SCI transmitter is the transmit shift register that is 10 or 11 or 12 bits long depending on the setting in the SCI_C1[M] control bit and SCI_BDH[SBNS] bit. For the remainder of this section, assume SCI_C1[M] is cleared, SCI_BDH[SBNS] is also cleared, selecting the normal 8-bit data mode. In 8-bit data mode, the shift register holds a start bit, eight data bits, and a stop bit. When the transmit shift register is available for a new SCI character, the value waiting in the transmit data register is transferred to the shift register, synchronized with the baud rate clock, and the transmit data register empty (SCI_S1[TDRE]) status flag is set to indicate another character may be written to the transmit data buffer at SCI_D.

NOTE

Always read SCI_S1 before writing to SCI_D to allow data to be transmitted.

If no new character is waiting in the transmit data buffer after a stop bit is shifted out the TxD pin, the transmitter sets the transmit complete flag and enters an idle mode, with TxD high, waiting for more characters to transmit.

Writing 0 to SCI_C2[TE] does not immediately release the pin to be a general-purpose I/O pin. Any transmit activity in progress must first be completed. This includes data characters in progress, queued idle characters, and queued break characters.

19.5.2.1 Send break and queued idle

SCI_C2[SBK] sends break characters originally used to gain the attention of old teletype receivers. Break characters are a full character time of logic 0, 10 bit times including the start and stop bits. A longer break of 13 bit times can be enabled by setting SCI_S2[BRK13]. Normally, a program would wait for SCI_S1[TDRE] to become set to indicate the last character of a message has moved to the transmit shifter, write 1, and then write 0 to SCI_C2[SBK]. This action queues a break character to be sent as soon as the shifter is available. If SCI_C2[SBK] remains 1 when the queued break moves into the shifter, synchronized to the baud rate clock, an additional break character is queued. If the receiving device is another NXP SCI, the break characters are received as 0s in all eight data bits and a framing error (SCI_S1[FE] = 1) occurs.

When idle-line wake-up is used, a full character time of idle (logic 1) is needed between messages to wake up any sleeping receivers. Normally, a program would wait for SCI_S1[TDRE] to become set to indicate the last character of a message has moved to the transmit shifter, then write 0 and then write 1 to the SCI_C2[TE] bit. This action queues an idle character to be sent as soon as the shifter is available. As long as the character in the shifter does not finish while SCI_C2[TE] is cleared, the SCI transmitter never actually releases control of the TxD pin. If there is a possibility of the shifter finishing while SCI_C2[TE] is cleared, set the general-purpose I/O controls so the pin shared with TxD is an output driving a logic 1. This ensures that the TxD line looks like a normal idle line even if the SCI loses control of the port pin between writing 0 and then 1 to SCI_C2[TE].

The length of the break character is affected by the SCI_S2[BRK13] and SCI_C1[M] as shown below.

Table 19-4. Break character length

BRK13	M	SBNS	Break character length
0	0	0	10 bit times
0	0	1	11 bit times
0	1	0	11 bit times
0	1	1	12 bit times
1	0	0	13 bit times
1	0	1	14 bit times
1	1	0	14 bit times
1	1	1	15 bit times

19.5.3 Receiver functional description

In this section, the receiver block diagram is a guide for the overall receiver functional description.

Next, the data sampling technique used to reconstruct receiver data is described in more detail. Finally, two variations of the receiver wakeup function are explained.

The receiver input is inverted by setting SCI_S2[RXINV]. The receiver is enabled by setting the SCI_C2[RE] bit. Character frames consist of a start bit of logic 0, eight (or nine) data bits (lsb first), and one (or two) stop bits of logic 1. For information about 9-bit data mode, refer to 8- and 9-bit data modes. For the remainder of this discussion, assume the SCI is configured for normal 8-bit data mode.

After receiving the stop bit into the receive shifter, and provided the receive data register is not already full, the data character is transferred to the receive data register and the receive data register full (SCI_S1[RDRF]) status flag is set. If SCI_S1[RDRF] was already set indicating the receive data register (buffer) was already full, the overrun (OR) status flag is set and the new data is lost. Because the SCI receiver is double-buffered, the program has one full character time after SCI_S1[RDRF] is set before the data in the receive data buffer must be read to avoid a receiver overrun.

When a program detects that the receive data register is full (SCI_S1[RDRF] = 1), it gets the data from the receive data register by reading SCI_D. The SCI_S1[RDRF] flag is cleared automatically by a two-step sequence normally satisfied in the course of the user's program that manages receive data. Refer to Interrupts and status flags for more details about flag clearing.

19.5.3.1 Data sampling technique

The SCI receiver uses a 16× baud rate clock for sampling. The oversampling ratio is fixed at 16. The receiver starts by taking logic level samples at 16 times the baud rate to search for a falling edge on the RxD serial data input pin. A falling edge is defined as a logic 0 sample after three consecutive logic 1 samples. The 16× baud rate clock divides the bit time into 16 segments labeled SCI_D[RT1] through SCI_D[RT16]. When a falling edge is located, three more samples are taken at SCI_D[RT3], SCI_D[RT5], and SCI_D[RT7] to make sure this was a real start bit and not merely noise. If at least two of these three samples are 0, the receiver assumes it is synchronized to a receive character.

The receiver then samples each bit time, including the start and stop bits, at SCI_D[RT8], SCI_D[RT9], and SCI_D[RT10] to determine the logic level for that bit. The logic level is interpreted to be that of the majority of the samples taken during the bit time. In the case of the start bit, the bit is assumed to be 0 if at least two of the samples at SCI_D[RT3], SCI_D[RT5], and SCI_D[RT7] are 0 even if one or all of the samples taken at SCI_D[RT8], SCI_D[RT9], and SCI_D[RT10] are 1s. If any sample in any bit time, including the start and stop bits, in a character frame fails to agree with the logic level for that bit, the noise flag (SCI_S1[NF]) is set when the received character is transferred to the receive data buffer.

The falling edge detection logic continuously looks for falling edges. If an edge is detected, the sample clock is resynchronized to bit times. This improves the reliability of the receiver in the presence of noise or mismatched baud rates. It does not improve worst case analysis because some characters do not have any extra falling edges anywhere in the character frame.

In the case of a framing error, provided the received character was not a break character, the sampling logic that searches for a falling edge is filled with three logic 1 samples so that a new start bit can be detected almost immediately.

In the case of a framing error, the receiver is inhibited from receiving any new characters until the framing error flag is cleared. The receive shift register continues to function, but a complete character cannot transfer to the receive data buffer if SCI_S1[FE] remains set.

19.5.3.2 Receiver wake-up operation

Receiver wake-up is a hardware mechanism that allows an SCI receiver to ignore the characters in a message intended for a different SCI receiver. In such a system, all receivers evaluate the first character(s) of each message, and as soon as they determine the message is intended for a different receiver, they write logic 1 to the receiver wake up control field (SCI_C2[RWU]). When SCI_C2[RWU] is set, the status flags associated with the receiver, (with the exception of the idle bit, IDLE, when SCI_S2[RWUID] is set), are inhibited from setting, thus eliminating the software overhead for handling the unimportant message characters. At the end of a message, or at the beginning of the next message, all receivers automatically force SCI_C2[RWU] to 0, so all receivers wake up in time to look at the first character(s) of the next message.

19.5.3.2.1 Idle-line wakeup

When wake is cleared, the receiver is configured for idle-line wakeup. In this mode, SCI_C2[RWU] is cleared automatically when the receiver detects a full character time of the idle-line level. The SCI_C1[M] control field selects 8-bit or 9-bit data mode and SCI_BDH[SBNS] selects 1-bit or 2-bit stop bit number that determines how many bit times of idle are needed to constitute a full character time, 10 or 11 or 12 bit times because of the start and stop bits.

When SCII_C2[RWU] is 1 and SCI_S2[RWUID] is 0, the idle condition that wakes up the receiver does not set SCI_S1[IDLE]. The receiver wakes up and waits for the first data character of the next message that sets SCI_S1[RDRF] and generates an interrupt, if enabled. When SCI_S2[RWUID] is 1, any idle condition sets SCI_S1[IDLE] flag and generates an interrupt if enabled, regardless of whether SCI_C2[RWU] is 0 or 1.

The idle-line type (SCI_C1[ILT]) control bit selects one of two ways to detect an idle line. When SCI_C1[ILT] is cleared, the idle bit counter starts after the start bit so the stop bit and any logic 1s at the end of a character count toward the full character time of idle. When SCI_C1[ILT] is set, the idle bit counter does not start until after a stop bit time, so the idle detection is not affected by the data in the last character of the previous message.

19.5.3.2.2 Address-mark wakeup

When wake is set, the receiver is configured for address-mark wakeup. In this mode, SCI_C2[RWU] is cleared automatically when the receiver detects a, or two, if SCI_BDH[SBNS] = 1, logic 1 in the most significant bits of a received character, eighth bit when SCI_C1[M] is cleared and ninth bit when SCI_C1[M] is set.

Address-mark wakeup allows messages to contain idle characters, but requires the msb be reserved for use in address frames. The one, or two, if SCI_BDH[SBNS] = 1, logic 1s msb of an address frame clears the SCI_C2[RWU] bit before the stop bits are received and sets the SCI_S1[RDRF] flag. In this case, the character with the msb set is received even though the receiver was sleeping during most of this character time.

19.5.4 Interrupts and status flags

The SCI system has three separate interrupt vectors to reduce the amount of software needed to isolate the cause of the interrupt.

One interrupt vector is associated with the transmitter for SCI_S1[TDRE] and SCI_S1[TC] events. Another interrupt vector is associated with the receiver for RDRF, IDLE, RXEDGIF, and LBKDIF events. A third vector is used for OR, NF, FE, and PF error conditions. Each of these ten interrupt sources can be separately masked by local interrupt enable masks. The flags can be polled by software when the local masks are cleared to disable generation of hardware interrupt requests.

The SCI transmitter has two status flags that can optionally generate hardware interrupt requests. Transmit data register empty (SCI_S1[TDRE]) indicates when there is room in the transmit data buffer to write another transmit character to SCI_D. If the transmit interrupt enable (SCI_C2[TIE]) bit is set, a hardware interrupt is requested when SCI_S1[TDRE] is set. Transmit complete (SCI_S1[TC]) indicates that the transmitter is finished transmitting all data, preamble, and break characters and is idle with TxD at the inactive level. This flag is often used in systems with modems to determine when it is safe to turn off the modem. If the transmit complete interrupt enable (SCI_C2[TCIE]) bit is set, a hardware interrupt is requested when SCI_S1[TC] is set. Instead of hardware interrupts, software polling may be used to monitor the SCI_S1[TDRE] and SCI_S1[TC] status flags if the corresponding SCI_C2[TIE] or SCI_C2[TCIE] local interrupt masks are cleared.

When a program detects that the receive data register is full (SCI_S1[RDRF] = 1), it gets the data from the receive data register by reading SCI_D. The SCI_S1[RDRF] flag is cleared by reading SCI_S1 while SCI_S1[RDRF] is set and then reading SCI_D.

When polling is used, this sequence is naturally satisfied in the normal course of the user program. If hardware interrupts are used, SCI_S1 must be read in the interrupt service routine (ISR). Normally, this is done in the ISR anyway to check for receive errors, so the sequence is automatically satisfied.

The IDLE status flag includes logic that prevents it from getting set repeatedly when the RxD line remains idle for an extended period of time. IDLE is cleared by reading SCI_S1 while SCI_S1[IDLE] is set and then reading SCI_D. After SCI_S1[IDLE] has been cleared, it cannot become set again until the receiver has received at least one new character and has set SCI_S1[RDRF].

If the associated error was detected in the received character that caused SCI_S1[RDRF] to be set, the error flags - noise flag (SCI_S1[NF]), framing error (SCI_S1[FE]), and parity error flag (SCI_S1[PF]) - are set at the same time as SCI_S1[RDRF]. These flags are not set in overrun cases.

If SCI_S1[RDRF] was already set when a new character is ready to be transferred from the receive shifter to the receive data buffer, the overrun (SCI_S1[OR]) flag is set instead of the data along with any associated NF, FE, or PF condition is lost.

At any time, an active edge on the RxD serial data input pin causes the SCI_S2[RXEDGIF] flag to set. The SCI_S2[RXEDGIF] flag is cleared by writing a 1 to it. This function depends on the receiver being enabled (SCI_C2[RE] = 1).

19.5.5 Baud rate tolerance

A transmitting device may operate at a baud rate below or above that of the receiver.

Accumulated bit time misalignment can cause one of the three stop bit data samples (RT8, RT9, and RT10) to fall outside the actual stop bit. A noise error will occur if the RT8, RT9, and RT10 samples are not all the same logical values. A framing error will occur if the receiver clock is misaligned in such a way that the majority of the RT8, RT9, and RT10 stop bit samples are a logic zero.

As the receiver samples an incoming frame, it re-synchronizes the RT clock on any valid falling edge within the frame. Resynchronization within frames will correct a misalignment between transmitter bit times and receiver bit times.

19.5.5.1 Slow data tolerance

Figure 19-4 shows how much a slow received frame can be misaligned without causing a noise error or a framing error. The slow stop bit begins at RT8 instead of RT1 but arrives in time for the stop bit data samples at RT8, RT9, and RT10.

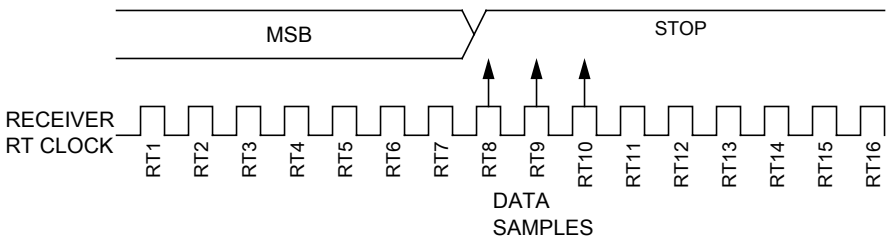


Figure 19-4. Slow data

For an 8-bit data and 1 stop bit character, data sampling of the stop bit takes the receiver 9 bit times x 16 RT cycles +10 RT cycles =154 RT cycles.

With the misaligned character shown in Figure 19-4, the receiver counts 154 RT cycles at the point when the count of the transmitting device is 9 bit times x 16 RT cycles + 3 RT cycles = 147 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 8-bit data and 1 stop bit character with no errors is:

((154 - 147) / 154) x 100 = 4.54%

For a 9-bit data or 2 stop bits character, data sampling of the stop bit takes the receiver 10 bit times x 16 RT cycles + 10 RT cycles = 170 RT cycles.

With the misaligned character shown in Figure 19-4, the receiver counts 170 RT cycles at the point when the count of the transmitting device is 10 bit times x 16 RT cycles + 3 RT cycles = 163 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 9-bit or 2 stop bits character with no errors is:

((170 - 163) / 170) X 100 = 4.12%

For a 9-bit data and 2 stop bit character, data sampling of the stop bit takes the receiver 11 bit times x 16 RT cycles + 10 RT cycles = 186 RT cycles.

With the misaligned character shown in Figure 19-4, the receiver counts 186 RT cycles at the point when the count of the transmitting device is 11 bit times x 16 RT cycles + 3 RT cycles = 179 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 9-bit and 2 stop bits character with no errors is: ((186 - 179) / 186) X 100 = 3.76%

19.5.5.2 Fast data tolerance

Figure 19-5 shows how much a fast received frame can be misaligned. The fast stop bit ends at RT10 instead of RT16 but is still sampled at RT8, RT9, and RT10.

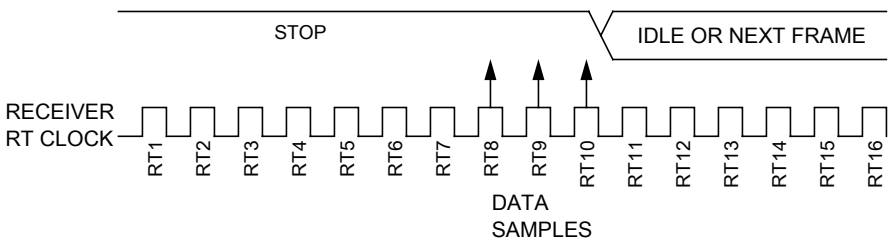


Figure 19-5. Fast data

For an 8-bit data and 1 stop bit character, data sampling of the stop bit takes the receiver 9 bit times x 16 RT cycles + 10 RT cycles = 154 RT cycles.

With the misaligned character shown in Figure 19-5, the receiver counts 154 RT cycles at the point when the count of the transmitting device is 10 bit times x 16 RT cycles = 160 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 8-bit and 1 stop bit character with no errors is:

((154 - 160) / 154) x 100 = 3.90%

For a 9-bit data or 2 stop bits character, data sampling of the stop bit takes the receiver 10 bit times x 16 RT cycles + 10 RT cycles = 170 RT cycles.

With the misaligned character shown in, the receiver counts 170 RT cycles at the point when the count of the transmitting device is 11 bit times x 16 RT cycles = 176 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit or 2 stop bits character with no errors is:

((170 - 176) / 170) x 100 = 3.53%

For a 9-bit data and 2 stop bits character, data sampling of the stop bit takes the receiver 11 bit times x 16 RT cycles + 10 RT cycles = 186 RT cycles.

With the misaligned character shown in, the receiver counts 186 RT cycles at the point when the count of the transmitting device is 12 bit times x 16 RT cycles = 192 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit and 2 stop bits character with no errors is:

((186 - 192) / 186) x 100 = 3.23%

19.5.6 Additional SCI functions

The following sections describe additional SCI functions.

19.5.6.1 8- and 9-bit data modes

The SCI system, transmitter and receiver, can be configured to operate in 9-bit data mode by setting SCI_C1[M]. In 9-bit mode, there is a ninth data bit to the left of the most significant bit of the SCI data register. For the transmit data buffer, this bit is stored in T8 in SCI_C3. For the receiver, the ninth bit is held in SCI_C3[R8].

For coherent writes to the transmit data buffer, write to SCI_C3[T8] before writing to SCI_D.

If the bit value to be transmitted as the ninth bit of a new character is the same as for the previous character, it is not necessary to write to SCI_C3[T8] again. When data is transferred from the transmit data buffer to the transmit shifter, the value in SCI_C3[T8] is copied at the same time data is transferred from SCI_D to the shifter.

The 9-bit data mode is typically used with parity to allow eight bits of data plus the parity in the ninth bit, or it is used with address-mark wake-up so the ninth data bit can serve as the wakeup bit. In custom protocols, the ninth bit can also serve as a software-controlled marker.

19.5.6.2 Stop mode operation

During all stop modes, clocks to the SCI module are halted.

No SCI module registers are affected in Stop mode.

The receive input active edge detect circuit remains active in Stop mode. An active edge on the receive input brings the CPU out of Stop mode if the interrupt is not masked (SCI_BDH[RXEDGIE] = 1).

Because the clocks are halted, the SCI module resumes operation upon exit from stop, only in Stop mode. Software must ensure stop mode is not entered while there is a character (including preamble, break and normal data) being transmitted out of or received into the SCI module, that means SCI_S1[TC] =1, SCI_S1[TDRE] = 1, and SCI_S2[RAF] = 0 must all meet before entering stop mode.

19.5.6.3 Loop mode

When SCI_C1[LOOPS] is set, the SCI_C1[RSRC] bit in the same register chooses between loop mode (SCI_C1[RSRC] = 0) or single-wire mode (SCI_C1[RSRC] = 1). Loop mode is sometimes used to check software, independent of connections in the external system, to help isolate system problems. In this mode, the internal loop back connection from the transmitter to the receiver causes the receiver to receive characters that are sent out by the transmitter.

19.5.6.4 Single-wire operation

When SCI_C1[LOOPS] is set, SCI_C1[RSRC] chooses between loop mode (SCI_C1[RSRC] = 0) or single-wire mode (SCI_C1[RSRC] = 1). Single-wire mode implements a half-duplex serial connection. The receiver is internally connected to the transmitter output and to the TxD pin. The RxD pin is not used and reverts to a general-purpose port I/O pin.

In single-wire mode, the SCI_C3[TXDIR] bit controls the direction of serial data on the TxD pin. When SCI_C3[TXDIR] is cleared, the TxD pin is an input to the SCI receiver and the transmitter is temporarily disconnected from the TxD pin so an external device can send serial data to the receiver. When SCI_C3[TXDIR] is set, the TxD pin is an output driven by the transmitter. In single-wire mode, the transmitter output is internally connected to the receiver input and the RxD pin is not used by the SCI, so it reverts to a general-purpose port I/O pin.

Chapter 20
Inter-Integrated Circuit (I2C)

20.1 Chip specific I2C information

This device contains an inter-integrated circuit (I2C) module.

The following table summarizes the external signals of I2C module:

Table 20-1. I2C module external signals

Functions	Default	Alternate 0	Alternate 1
SCL	PTA3/SCL	PTB7/SCL	PTB3/SCL
SDA	PTA2/SDA	PTB6/SDA	PTB2/SDA

I2C channels can be reconfigured on different pinout by setting SYS_SOPT1[IICPS].

20.2 Introduction

NOTE

For the chip-specific implementation details of this module's instances, see the chip configuration information.

The inter-integrated circuit (I^2C, I2C, or IIC) module provides a method of communication between a number of devices.

The interface is designed to operate up to at least 400 kbit/s with maximum bus loading and timing. The I2C device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF. The I2C module also complies with the *System Management Bus (SMBus) Specification, version 2*.

20.2.1 Features

The I2C module has the following features:

- Compatible with *The I^2C-Bus Specification*
- Multimaster operation
- Software programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation and detection
- Repeated START signal generation and detection
- Acknowledge bit generation and detection
- Bus busy detection
- General call recognition
- 10-bit address extension
- Support for *System Management Bus (SMBus) Specification, version 2*
- Programmable input glitch filter
- Low power mode wakeup on slave address match
- Range slave address support

20.2.2 Modes of operation

The I2C module's operation in various low power modes is as follows:

- Run mode: This is the basic mode of operation. To conserve power in this mode, disable the module.
- Wait mode: The module continues to operate when the core is in Wait mode and can provide a wakeup interrupt.
- Stop mode: The module is inactive in Stop3 mode for reduced power consumption, except that address matching is enabled in Stop3 mode. The STOP instruction does not affect the I2C module's register states.

20.2.3 Block diagram

The following figure is a functional block diagram of the I2C module.

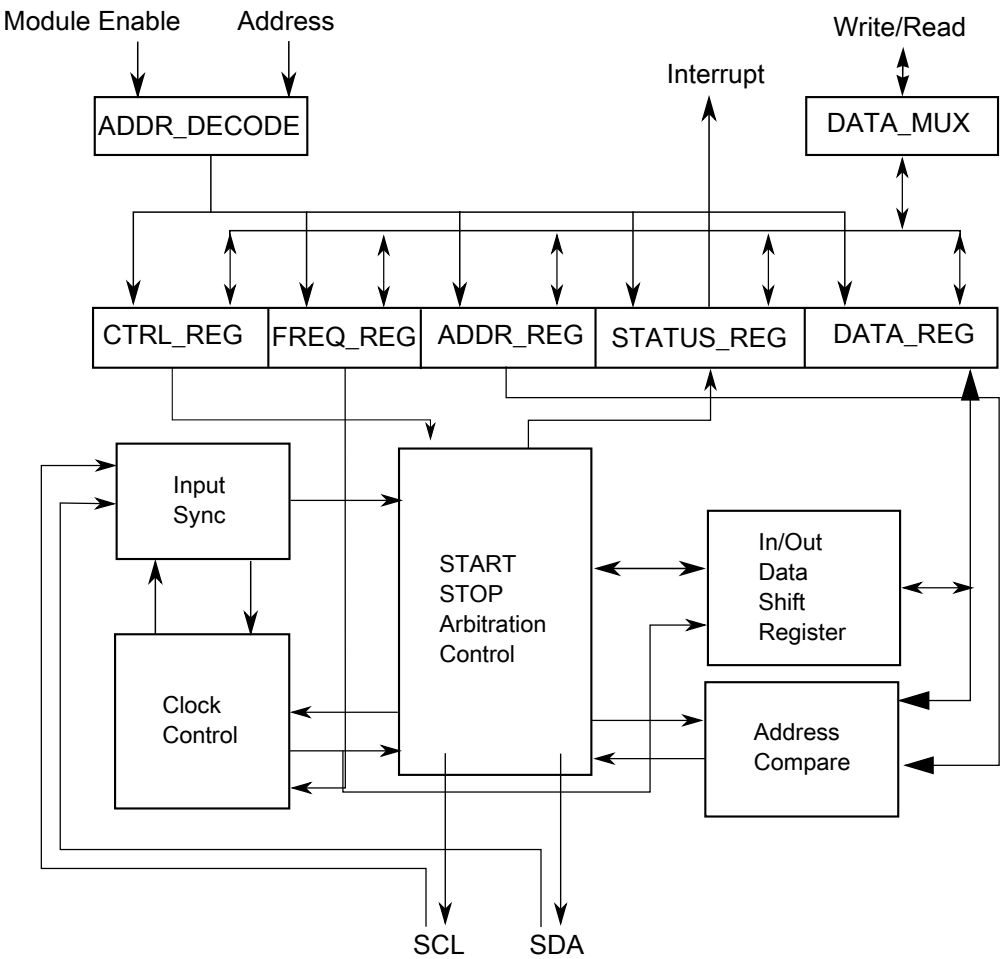


Figure 20-1. I2C Functional block diagram

20.3 I²C signal descriptions

The signal properties of I²C are shown in the table found here.

Table 20-2. I²C signal descriptions

Signal	Description	I/O
SCL	Bidirectional serial clock line of the I²C system.	I/O
SDA	Bidirectional serial data line of the I²C system.	I/O

20.4 Memory map/register definition

This section describes in detail all I2C registers accessible to the end user.

I2C memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3070	I2C Address Register 1 (I2C_A1)	8	R/W	00h	20.4.1/316
3071	I2C Frequency Divider register (I2C_F)	8	R/W	00h	20.4.2/317
3072	I2C Control Register 1 (I2C_C1)	8	R/W	00h	20.4.3/318
3073	I2C Status register (I2C_S)	8	R/W	80h	20.4.4/319
3074	I2C Data I/O register (I2C_D)	8	R/W	00h	20.4.5/321
3075	I2C Control Register 2 (I2C_C2)	8	R/W	00h	20.4.6/322
3076	I2C Programmable Input Glitch Filter Register (I2C_FLT)	8	R/W	00h	20.4.7/323
3077	I2C Range Address register (I2C_RA)	8	R/W	00h	20.4.8/324
3078	I2C SMBus Control and Status register (I2C_SMB)	8	R/W	00h	20.4.9/325
3079	I2C Address Register 2 (I2C_A2)	8	R/W	C2h	20.4.10/326
307A	I2C SCL Low Timeout Register High (I2C_SLTH)	8	R/W	00h	20.4.11/327
307B	I2C SCL Low Timeout Register Low (I2C_SLTL)	8	R/W	00h	20.4.12/327

20.4.1 I2C Address Register 1 (I2C_A1)

This register contains the slave address to be used by the I2C module.

Address: 3070h base + 0h offset = 3070h

Bit	7	6	5	4	3	2	1	0
Read Write	AD[7:1]							0
Reset	0	0	0	0	0	0	0	0

I2C_A1 field descriptions

Field	Description
7–1 AD[7:1]	Address Contains the primary slave address used by the I2C module when it is addressed as a slave. This field is used in the 7-bit address scheme and the lower seven bits in the 10-bit address scheme.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

20.4.2 I2C Frequency Divider register (I2C_F)

Address: 3070h base + 1h offset = 3071h

Bit	7	6	5	4	3	2	1	0
Read Write	MULT		ICR					
Reset	0	0	0	0	0	0	0	0

I2C_F field descriptions

Field	Description
7–6 MULT	Multiplier Factor Defines the multiplier factor (mul). This factor is used along with the SCL divider to generate the I2C baud rate. 00 mul = 1 01 mul = 2 10 mul = 4 11 Reserved

ICR	ClockRate
	
	Prescales the I2C module clock for bit rate selection. This field and the MULT field determine the I2C baud rate, the SDA hold time, the SCL start hold time, and the SCL stop hold time. For a list of values corresponding to each ICR setting, see I2C divider and hold values.
	
	The SCL divider multiplied by multiplier factor (mul) determines the I2C baud rate.
	
	`I2C baud rate = I2C module clock speed (Hz)/(mul × SCL divider)`
	
	The SDA hold time is the delay from the falling edge of SCL (I2C clock) to the changing of SDA (I2C data).
	
	`SDA hold time = I2C module clock period (s) × mul × SDA hold value`
	
	The SCL start hold time is the delay from the falling edge of SDA (I2C data) while SCL is high (start condition) to the falling edge of SCL (I2C clock).
	
	`SCL start hold time = I2C module clock period (s) × mul × SCL start hold value`
	
	The SCL stop hold time is the delay from the rising edge of SCL (I2C clock) to the rising edge of SDA (I2C data) while SCL is high (stop condition).
	
	`SCL stop hold time = I2C module clock period (s) × mul × SCL stop hold value`
	
	For example, if the I2C module clock speed is 8 MHz, the following table shows the possible hold time values with different ICR and MULT selections to achieve an I^2C baud rate of 100 kbit/s.

MULT	ICR	Hold times (µs)		
		SDA	SCL Start	SCL Stop
2h	00h	3.500	3.000	5.500
1h	07h	2.500	4.000	5.250
1h	0Bh	2.250	4.000	5.250
0h	14h	2.125	4.250	5.125

Table continues on the next page...

I2C_F field descriptions (continued)

Field	Description				
	MULT	ICR	Hold times (µs)		
			SDA	SCL Start	SCL Stop
	0h	18h	1.125	4.750	5.125

20.4.3 I2C Control Register 1 (I2C_C1)

Address: 3070h base + 2h offset = 3072h

Bit	7	6	5	4	3	2	1	0
Read	IICEN	IICIE	MST	TX	TXAK	0	WUEN	0
Write						RSTA		
Reset	0	0	0	0	0	0	0	0

I2C_C1 field descriptions

Field	Description
7 IICEN	I2C Enable Enables I2C module operation. 0 Disabled 1 Enabled
6 IICIE	I2C Interrupt Enable Enables I2C interrupt requests. 0 Disabled 1 Enabled
5 MST	Master Mode Select When MST is changed from 0 to 1, a START signal is generated on the bus and master mode is selected. When this bit changes from 1 to 0, a STOP signal is generated and the mode of operation changes from master to slave. 0 Slave mode 1 Master mode
4 TX	Transmit Mode Select Selects the direction of master and slave transfers. In master mode this bit must be set according to the type of transfer required. Therefore, for address cycles, this bit is always set. When addressed as a slave this bit must be set by software according to the SRW bit in the status register. 0 Receive 1 Transmit

Table continues on the next page...

I2C_C1 field descriptions (continued)

Field	Description
3 TXAK	Transmit Acknowledge Enable Specifies the value driven onto the SDA during data acknowledge cycles for both master and slave receivers. The value of SMB[FACK] affects NACK/ACK generation. **NOTE:** SCL is held low until TXAK is written. 0 An acknowledge signal is sent to the bus on the following receiving byte (if FACK is cleared) or the current receiving byte (if FACK is set). 1 No acknowledge signal is sent to the bus on the following receiving data byte (if FACK is cleared) or the current receiving data byte (if FACK is set).
2 RSTA	Repeat START Writing 1 to this bit generates a repeated START condition provided it is the current master. This bit will always be read as 0. Attempting a repeat at the wrong time results in loss of arbitration.
1 WUEN	Wakeup Enable The I2C module can wake the MCU from low power mode with no peripheral bus running when slave address matching occurs. 0 Normal operation. No interrupt generated when address matching in low power mode. 1 Enables the wakeup function in low power mode.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

20.4.4 I2C Status register (I2C_S)

Address: 3070h base + 3h offset = 3073h

Bit	7	6	5	4	3	2	1	0
Read	TCF	IAAS	BUSY	ARBL	RAM	SRW	IICIF	RXAK
Write				w1c			w1c	
Reset	1	0	0	0	0	0	0	0

I2C_S field descriptions

Field	Description
7 TCF	Transfer Complete Flag Acknowledges a byte transfer; TCF is set on the completion of a byte transfer. This bit is valid only during or immediately following a transfer to or from the I2C module. TCF is cleared by reading the I2C data register in receive mode or by writing to the I2C data register in transmit mode. 0 Transfer in progress 1 Transfer complete
6 IAAS	Addressed As A Slave This bit is set by one of the following conditions:

Table continues on the next page...

I2C_S field descriptions (continued)

Field	Description
	• The calling address matches the programmed primary slave address in the A1 register, or matches the range address in the RA register (which must be set to a nonzero value and under the condition I2C_C2[RMEN] = 1). • C2[GCAEN] is set and a general call is received. • SMB[SIICAEN] is set and the calling address matches the second programmed slave address. • ALERTEN is set and an SMBus alert response address is received • RMEN is set and an address is received that is within the range between the values of the A1 and RA registers. IAAS sets before the ACK bit. The CPU must check the SRW bit and set TX/RX accordingly. Writing the C1 register with any value clears this bit. 0 Not addressed 1 Addressed as a slave
5 BUSY	Bus Busy Indicates the status of the bus regardless of slave or master mode. This bit is set when a START signal is detected and cleared when a STOP signal is detected. 0 Bus is idle 1 Bus is busy
4 ARBL	Arbitration Lost This bit is set by hardware when the arbitration procedure is lost. The ARBL bit must be cleared by software, by writing 1 to it. 0 Standard bus operation. 1 Loss of arbitration.
3 RAM	Range Address Match This bit is set to 1 by any of the following conditions, if I2C_C2[RMEN] = 1: • Any nonzero calling address is received that matches the address in the RA register. • The calling address is within the range of values of the A1 and RA registers. Writing the C1 register with any value clears this bit to 0. 0 Not addressed 1 Addressed as a slave
2 SRW	Slave Read/Write When addressed as a slave, SRW indicates the value of the R/$\overline{W}$ command bit of the calling address sent to the master. 0 Slave receive, master writing to slave 1 Slave transmit, master reading from slave
1 IICIF	Interrupt Flag This bit sets when an interrupt is pending. This bit must be cleared by software by writing 1 to it, such as in the interrupt routine. One of the following events can set this bit: • One byte transfer, including ACK/NACK bit, completes if FACK is 0. An ACK or NACK is sent on the bus by writing 0 or 1 to TXAK after this bit is set in receive mode. • One byte transfer, excluding ACK/NACK bit, completes if FACK is 1.

Table continues on the next page...

I2C_S field descriptions (continued)

Field	Description
	• Match of slave address to calling address including primary slave address, range slave address, alert response address, second slave address, or general call address. • Arbitration lost • In SMBus mode, any timeouts except SCL and SDA high timeouts • I2C bus stop or start detection if the SSIE bit in the Input Glitch Filter register is 1 **NOTE:** To clear the I2C bus stop or start detection interrupt: In the interrupt service routine, first clear the STOPF or STARTF bit in the Input Glitch Filter register by writing 1 to it, and then clear the IICIF bit. If this sequence is reversed, the IICIF bit is asserted again. 0 No interrupt pending 1 Interrupt pending
0 RXAK	Receive Acknowledge 0 Acknowledge signal was received after the completion of one byte of data transmission on the bus 1 No acknowledge signal detected

20.4.5 I2C Data I/O register (I2C_D)

Address: 3070h base + 4h offset = 3074h

Bit	7	6	5	4	3	2	1	0
Read Write	DATA							
Reset	0	0	0	0	0	0	0	0

I2C_D field descriptions

Field	Description
DATA	Data In master transmit mode, when data is written to this register, a data transfer is initiated. The most significant bit is sent first. In master receive mode, reading this register initiates receiving of the next byte of data. **NOTE:** When making the transition out of master receive mode, switch the I2C mode before reading the Data register to prevent an inadvertent initiation of a master receive data transfer. In slave mode, the same functions are available after an address match occurs. The C1[TX] bit must correctly reflect the desired direction of transfer in master and slave modes for the transmission to begin. For example, if the I2C module is configured for master transmit but a master receive is desired, reading the Data register does not initiate the receive. Reading the Data register returns the last byte received while the I2C module is configured in master receive or slave receive mode. The Data register does not reflect every byte that is transmitted on the I2C bus, and neither can software verify that a byte has been written to the Data register correctly by reading it back. In master transmit mode, the first byte of data written to the Data register following assertion of MST (start bit) or assertion of RSTA (repeated start bit) is used for the address transfer and must consist of the calling address (in bits 7-1) concatenated with the required R/$\overline{W}$ bit (in position bit 0).

20.4.6 I2C Control Register 2 (I2C_C2)

Address: 3070h base + 5h offset = 3075h

Bit	7	6	5	4	3	2	1	0
Read Write	GCAEN	ADEXT	0	SBRC	RMEN	AD[10:8]		
Reset	0	0	0	0	0	0	0	0

I2C_C2 field descriptions

Field	Description
7 GCAEN	General Call Address Enable Enables general call address. 0 Disabled 1 Enabled
6 ADEXT	Address Extension Controls the number of bits used for the slave address. 0 7-bit address scheme 1 10-bit address scheme
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 SBRC	Slave Baud Rate Control Enables independent slave mode baud rate at maximum frequency, which forces clock stretching on SCL in very fast I2C modes. To a slave, an example of a "very fast" mode is when the master transfers at 40 kbit/s but the slave can capture the master's data at only 10 kbit/s. 0 The slave baud rate follows the master baud rate and clock stretching may occur 1 Slave baud rate is independent of the master baud rate
3 RMEN	Range Address Matching Enable This bit controls the slave address matching for addresses between the values of the A1 and RA registers. When this bit is set, a slave address matching occurs for any address greater than the value of the A1 register and less than or equal to the value of the RA register. 0 Range mode disabled. No address matching occurs for an address within the range of values of the A1 and RA registers. 1 Range mode enabled. Address matching occurs when a slave receives an address within the range of values of the A1 and RA registers.
AD[10:8]	Slave Address Contains the upper three bits of the slave address in the 10-bit address scheme. This field is valid only while the ADEXT bit is set.

20.4.7 I2C Programmable Input Glitch Filter Register (I2C_FLT)

Address: 3070h base + 6h offset = 3076h

Bit	7	6	5	4	3	2	1	0
Read	SHEN	STOPF	SSIE	STARTF	FLT			
Write		w1c		w1c				
Reset	0	0	0	0	0	0	0	0

I2C_FLT field descriptions

Field	Description
7 SHEN	Stop Hold Enable Set this bit to hold off entry to stop mode when any data transmission or reception is occurring. The following scenario explains the holdoff functionality: 1. The I2C module is configured for a basic transfer, and the SHEN bit is set to 1. 2. A transfer begins. 3. The MCU signals the I2C module to enter stop mode. 4. The byte currently being transferred, including both address and data, completes its transfer. 5. The I2C slave or master acknowledges that the in-transfer byte completed its transfer and acknowledges the request to enter stop mode. 6. After receiving the I2C module's acknowledgment of the request to enter stop mode, the MCU determines whether to shut off the I2C module's clock. If the SHEN bit is set to 1 and the I2C module is in an idle or disabled state when the MCU signals to enter stop mode, the module immediately acknowledges the request to enter stop mode. If SHEN is cleared to 0 and the overall data transmission or reception that was suspended by stop mode entry was incomplete: To resume the overall transmission or reception after the MCU exits stop mode, software must reinitialize the transfer by resending the address of the slave. If the I2C Control Register 1's IICIE bit was set to 1 before the MCU entered stop mode, system software will receive the interrupt triggered by the I2C Status Register's TCF bit after the MCU wakes from the stop mode. 0 Stop holdoff is disabled. The MCU's entry to stop mode is not gated. 1 Stop holdoff is enabled.
6 STOPF	I2C Bus Stop Detect Flag Hardware sets this bit when the I2C bus's stop status is detected. The STOPF bit must be cleared by writing 1 to it. **NOTE:** The stop flag is only for the matched slave devices, therefore the master will not respond for it. 0 No stop happens on I2C bus 1 Stop detected on I2C bus
5 SSIE	I2C Bus Stop or Start Interrupt Enable This bit enables the interrupt for I2C bus stop or start detection. **NOTE:** To clear the I2C bus stop or start detection interrupt: In the interrupt service routine, first clear the STOPF or STARTF bit by writing 1 to it, and then clear the IICIF bit in the status register. If this sequence is reversed, the IICIF bit is asserted again.

Table continues on the next page...

I2C_FLT field descriptions (continued)

Field	Description
	0 Stop or start detection interrupt is disabled 1 Stop or start detection interrupt is enabled
4 STARTF	I2C Bus Start Detect Flag Hardware sets this bit when the I2C bus's start status is detected. The STARTF bit must be cleared by writing 1 to it. 0 No start happens on I2C bus 1 Start detected on I2C bus
FLT	I2C Programmable Filter Factor Controls the width of the glitch, in terms of I2C module clock cycles, that the filter must absorb. For any glitch whose size is less than or equal to this width setting, the filter does not allow the glitch to pass. 0h No filter/bypass 1-Fh Filter glitches up to width of *n* I2C module clock cycles, where *n*=1-15d

20.4.8 I2C Range Address register (I2C_RA)

Address: 3070h base + 7h offset = 3077h

Bit	7	6	5	4	3	2	1	0
Read	RAD							0
Write								
Reset	0	0	0	0	0	0	0	0

I2C_RA field descriptions

Field	Description
7–1 RAD	Range Slave Address This field contains the slave address to be used by the I2C module. The field is used in the 7-bit address scheme. If I2C_C2[RMEN] is set to 1, any nonzero value write enables this register. This register value can be considered as a maximum boundary in the range matching mode.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

20.4.9 I2C SMBus Control and Status register (I2C_SMB)

NOTE

When the SCL and SDA signals are held high for a length of time greater than the high timeout period, the SHTF1 flag sets. Before reaching this threshold, while the system is detecting how long these signals are being held high, a master assumes that the bus is free. However, the SHTF1 bit is set to 1 in the bus transmission process with the idle bus state.

NOTE

When the TCKSEL bit is set, there is no need to monitor the SHTF1 bit because the bus speed is too high to match the protocol of SMBus.

Address: 3070h base + 8h offset = 3078h

Bit	7	6	5	4	3	2	1	0
Read	FACK	ALERTEN	SIICAEN	TCKSEL	SLTF	SHTF1	SHTF2	SHTF2IE
Write					w1c		w1c	
Reset	0	0	0	0	0	0	0	0

I2C_SMB field descriptions

Field	Description
7 FACK	Fast NACK/ACK Enable For SMBus packet error checking, the CPU must be able to issue an ACK or NACK according to the result of receiving data byte. 0 An ACK or NACK is sent on the following receiving data byte 1 Writing 0 to TXAK after receiving a data byte generates an ACK. Writing 1 to TXAK after receiving a data byte generates a NACK.
6 ALERTEN	SMBus Alert Response Address Enable Enables or disables SMBus alert response address matching. **NOTE:** After the host responds to a device that used the alert response address, you must use software to put the device's address on the bus. The alert protocol is described in the SMBus specification. 0 SMBus alert response address matching is disabled 1 SMBus alert response address matching is enabled
5 SIICAEN	Second I2C Address Enable Enables or disables SMBus device default address. 0 I2C address register 2 matching is disabled 1 I2C address register 2 matching is enabled

Table continues on the next page...

I2C_SMB field descriptions (continued)

Field	Description
4 TCKSEL	Timeout Counter Clock Select Selects the clock source of the timeout counter. 0 Timeout counter counts at the frequency of the I2C module clock / 64 1 Timeout counter counts at the frequency of the I2C module clock
3 SLTF	SCL Low Timeout Flag This bit is set when the SLT register (consisting of the SLTH and SLTL registers) is loaded with a non-zero value (LoValue) and an SCL low timeout occurs. Software clears this bit by writing a logic 1 to it. **NOTE:** The low timeout function is disabled when the SLT register's value is 0. 0 No low timeout occurs 1 Low timeout occurs
2 SHTF1	SCL High Timeout Flag 1 This read-only bit sets when SCL and SDA are held high more than clock × LoValue / 512, which indicates the bus is free. This bit is cleared automatically. 0 No SCL high and SDA high timeout occurs 1 SCL high and SDA high timeout occurs
1 SHTF2	SCL High Timeout Flag 2 This bit sets when SCL is held high and SDA is held low more than clock × LoValue / 512. Software clears this bit by writing 1 to it. 0 No SCL high and SDA low timeout occurs 1 SCL high and SDA low timeout occurs
0 SHTF2IE	SHTF2 Interrupt Enable Enables SCL high and SDA low timeout interrupt. 0 SHTF2 interrupt is disabled 1 SHTF2 interrupt is enabled

20.4.10 I2C Address Register 2 (I2C_A2)

Address: 3070h base + 9h offset = 3079h

Bit	7	6	5	4	3	2	1	0
Read	SAD							0
Write								
Reset	1	1	0	0	0	0	1	0

I2C_A2 field descriptions

Field	Description
7–1 SAD	SMBus Address

Table continues on the next page...

I2C_A2 field descriptions (continued)

Field	Description
	Contains the slave address used by the SMBus. This field is used on the device default address or other related addresses.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

20.4.11 I2C SCL Low Timeout Register High (I2C_SLTH)

Address: 3070h base + Ah offset = 307Ah

Bit	7	6	5	4	3	2	1	0
Read Write	SSLT[15:8]							
Reset	0	0	0	0	0	0	0	0

I2C_SLTH field descriptions

Field	Description
SSLT[15:8]	SSLT[15:8] Most significant byte of SCL low timeout value that determines the timeout period of SCL low.

20.4.12 I2C SCL Low Timeout Register Low (I2C_SLTL)

Address: 3070h base + Bh offset = 307Bh

Bit	7	6	5	4	3	2	1	0
Read Write	SSLT[7:0]							
Reset	0	0	0	0	0	0	0	0

I2C_SLTL field descriptions

Field	Description
SSLT[7:0]	SSLT[7:0] Least significant byte of SCL low timeout value that determines the timeout period of SCL low.

20.5 Functional description

This section provides a comprehensive functional description of the I2C module.

20.5.1 I2C protocol

The I2C bus system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers.

All devices connected to it must have open drain or open collector outputs. A logic AND function is exercised on both lines with external pull-up resistors. The value of these resistors depends on the system.

Normally, a standard instance of communication is composed of four parts:

1. START signal
2. Slave address transmission
3. Data transfer
4. STOP signal

The STOP signal should not be confused with the CPU STOP instruction. The following figure illustrates I2C bus system communication.

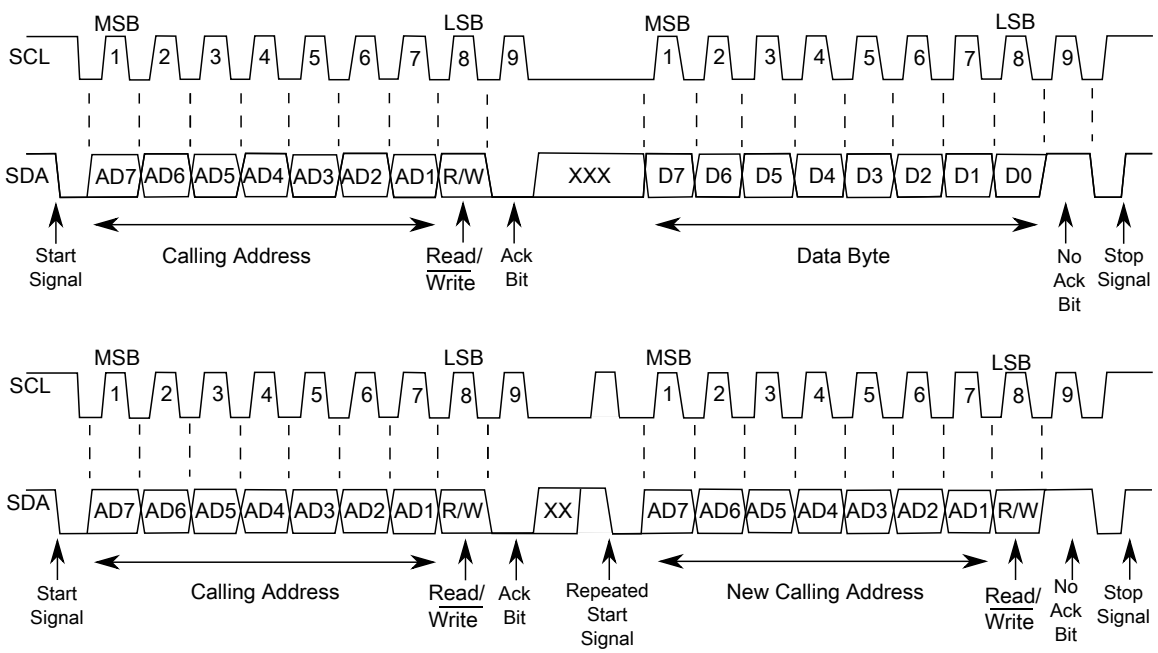


Figure 20-2. I2C bus transmission signals

20.5.1.1 START signal

The bus is free when no master device is engaging the bus (both SCL and SDA are high). When the bus is free, a master may initiate communication by sending a START signal. A START signal is defined as a high-to-low transition of SDA while SCL is high. This signal denotes the beginning of a new data transfer—each data transfer might contain several bytes of data—and brings all slaves out of their idle states.

20.5.1.2 Slave address transmission

Immediately after the START signal, the first byte of a data transfer is the slave address transmitted by the master. This address is a 7-bit calling address followed by an R/$\overline{W}$ bit. The R/$\overline{W}$ bit tells the slave the desired direction of data transfer.

- 1 = Read transfer: The slave transmits data to the master
- 0 = Write transfer: The master transmits data to the slave

Only the slave with a calling address that matches the one transmitted by the master responds by sending an acknowledge bit. The slave sends the acknowledge bit by pulling SDA low at the ninth clock.

No two slaves in the system can have the same address. If the I2C module is the master, it must not transmit an address that is equal to its own slave address. The I2C module cannot be master and slave at the same time. However, if arbitration is lost during an address cycle, the I2C module reverts to slave mode and operates correctly even if it is being addressed by another master.

20.5.1.3 Data transfers

When successful slave addressing is achieved, data transfer can proceed on a byte-by-byte basis in the direction specified by the R/$\overline{W}$ bit sent by the calling master.

All transfers that follow an address cycle are referred to as data transfers, even if they carry subaddress information for the slave device.

Each data byte is 8 bits long. Data may be changed only while SCL is low. Data must be held stable while SCL is high. There is one clock pulse on SCL for each data bit, and the MSB is transferred first. Each data byte is followed by a ninth (acknowledge) bit, which is signaled from the receiving device by pulling SDA low at the ninth clock. In summary, one complete data transfer needs nine clock pulses.

If the slave receiver does not acknowledge the master in the ninth bit, the slave must leave SDA high. The master interprets the failed acknowledgement as an unsuccessful data transfer.

If the master receiver does not acknowledge the slave transmitter after a data byte transmission, the slave interprets it as an end to data transfer and releases the SDA line.

In the case of a failed acknowledgement by either the slave or master, the data transfer is aborted and the master does one of two things:

- Relinquishes the bus by generating a STOP signal.
- Commences a new call by generating a repeated START signal.

20.5.1.4 STOP signal

The master can terminate the communication by generating a STOP signal to free the bus. A STOP signal is defined as a low-to-high transition of SDA while SCL is asserted.

The master can generate a STOP signal even if the slave has generated an acknowledgement, at which point the slave must release the bus.

20.5.1.5 Repeated START signal

The master may generate a START signal followed by a calling command without generating a STOP signal first. This action is called a repeated START. The master uses a repeated START to communicate with another slave or with the same slave in a different mode (transmit/receive mode) without releasing the bus.

20.5.1.6 Arbitration procedure

The I2C bus is a true multimaster bus that allows more than one master to be connected on it.

If two or more masters try to control the bus at the same time, a clock synchronization procedure determines the bus clock. The bus clock's low period is equal to the longest clock low period, and the high period is equal to the shortest one among the masters.

The relative priority of the contending masters is determined by a data arbitration procedure. A bus master loses arbitration if it transmits logic level 1 while another master transmits logic level 0. The losing masters immediately switch to slave receive mode and

stop driving SDA output. In this case, the transition from master to slave mode does not generate a STOP condition. Meanwhile, hardware sets a status bit to indicate the loss of arbitration.

20.5.1.7 Clock synchronization

Because wire AND logic is performed on SCL, a high-to-low transition on SCL affects all devices connected on the bus. The devices start counting their low period and, after a device's clock has gone low, that device holds SCL low until the clock reaches its high state. However, the change of low to high in this device clock might not change the state of SCL if another device clock is still within its low period. Therefore, the synchronized clock SCL is held low by the device with the longest low period. Devices with shorter low periods enter a high wait state during this time; see the following diagram. When all applicable devices have counted off their low period, the synchronized clock SCL is released and pulled high. Afterward there is no difference between the device clocks and the state of SCL, and all devices start counting their high periods. The first device to complete its high period pulls SCL low again.

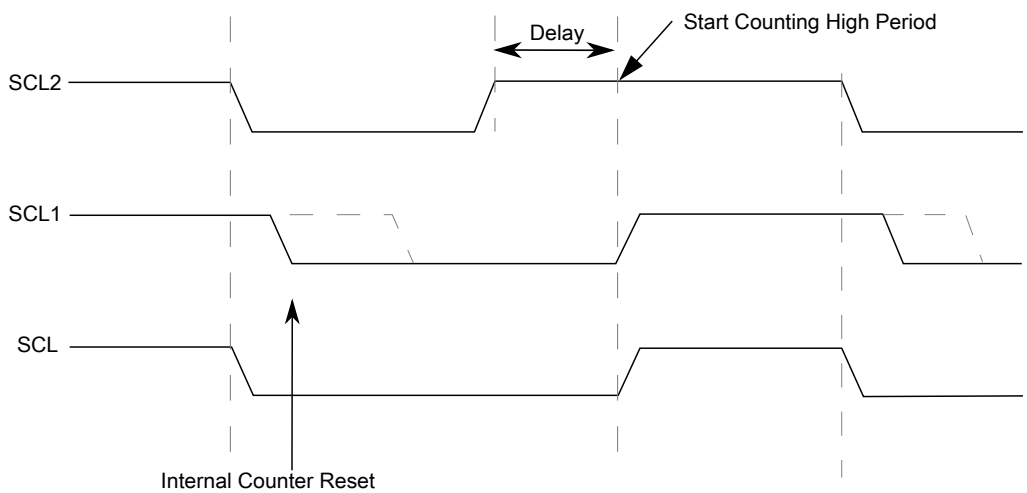


Figure 20-3. I2C clock synchronization

20.5.1.8 Handshaking

The clock synchronization mechanism can be used as a handshake in data transfers. A slave device may hold SCL low after completing a single byte transfer (9 bits). In this case, it halts the bus clock and forces the master clock into wait states until the slave releases SCL.

20.5.1.9 Clock stretching

The clock synchronization mechanism can be used by slaves to slow down the bit rate of a transfer. After the master drives SCL low, a slave can drive SCL low for the required period and then release it. If the slave's SCL low period is greater than the master's SCL low period, the resulting SCL bus signal's low period is stretched. In other words, the SCL bus signal's low period is increased to be the same length as the slave's SCL low period.

20.5.1.10 I2C divider and hold values

NOTE

For some cases on some devices, the SCL divider value may vary by ±2 or ±4 when ICR's value ranges from 00h to 0Fh. These potentially varying SCL divider values are highlighted in the following table.

Table 20-3. I2C divider and hold values

ICR (hex)	SCL divider	SDA hold value	SCL hold (start) value	SCL hold (stop) value	ICR (hex)	SCL divider (clocks)	SDA hold (clocks)	SCL hold (start) value	SCL hold (stop) value
00	20	7	6	11	20	160	17	78	81
01	22	7	7	12	21	192	17	94	97
02	24	8	8	13	22	224	33	110	113
03	26	8	9	14	23	256	33	126	129
04	28	9	10	15	24	288	49	142	145
05	30	9	11	16	25	320	49	158	161
06	34	10	13	18	26	384	65	190	193
07	40	10	16	21	27	480	65	238	241
08	28	7	10	15	28	320	33	158	161
09	32	7	12	17	29	384	33	190	193
0A	36	9	14	19	2A	448	65	222	225
0B	40	9	16	21	2B	512	65	254	257
0C	44	11	18	23	2C	576	97	286	289
0D	48	11	20	25	2D	640	97	318	321
0E	56	13	24	29	2E	768	129	382	385
0F	68	13	30	35	2F	960	129	478	481
10	48	9	18	25	30	640	65	318	321
11	56	9	22	29	31	768	65	382	385
12	64	13	26	33	32	896	129	446	449
13	72	13	30	37	33	1024	129	510	513
14	80	17	34	41	34	1152	193	574	577

Table continues on the next page...

Table 20-3. I2C divider and hold values (continued)

ICR (hex)	SCL divider	SDA hold value	SCL hold (start) value	SCL hold (stop) value	ICR (hex)	SCL divider (clocks)	SDA hold (clocks)	SCL hold (start) value	SCL hold (stop) value
15	88	17	38	45	35	1280	193	638	641
16	104	21	46	53	36	1536	257	766	769
17	128	21	58	65	37	1920	257	958	961
18	80	9	38	41	38	1280	129	638	641
19	96	9	46	49	39	1536	129	766	769
1A	112	17	54	57	3A	1792	257	894	897
1B	128	17	62	65	3B	2048	257	1022	1025
1C	144	25	70	73	3C	2304	385	1150	1153
1D	160	25	78	81	3D	2560	385	1278	1281
1E	192	33	94	97	3E	3072	513	1534	1537
1F	240	33	118	121	3F	3840	513	1918	1921

20.5.2 10-bit address

For 10-bit addressing, 0x11110 is used for the first 5 bits of the first address byte. Various combinations of read/write formats are possible within a transfer that includes 10-bit addressing.

20.5.2.1 Master-transmitter addresses a slave-receiver

The transfer direction is not changed. When a 10-bit address follows a START condition, each slave compares the first 7 bits of the first byte of the slave address (11110XX) with its own address and tests whether the eighth bit (R/$\overline{W}$ direction bit) is 0. It is possible that more than one device finds a match and generates an acknowledge (A1). Each slave that finds a match compares the 8 bits of the second byte of the slave address with its own address, but only one slave finds a match and generates an acknowledge (A2). The matching slave remains addressed by the master until it receives a STOP condition (P) or a repeated START condition (Sr) followed by a different slave address.

Table 20-4. Master-transmitter addresses slave-receiver with a 10-bit address

S	Slave address first 7 bits 11110 + AD10 + AD9	R/$\overline{W}$ 0	A1	Slave address second byte AD[8:1]	A2	Data	A	...	Data	A/A	P

After the master-transmitter has sent the first byte of the 10-bit address, the slave-receiver sees an I2C interrupt. User software must ensure that for this interrupt, the contents of the Data register are ignored and not treated as valid data.

20.5.2.2 Master-receiver addresses a slave-transmitter

The transfer direction is changed after the second R/$\overline{W}$ bit. Up to and including acknowledge bit A2, the procedure is the same as that described for a master-transmitter addressing a slave-receiver. After the repeated START condition (Sr), a matching slave remembers that it was addressed before. This slave then checks whether the first seven bits of the first byte of the slave address following Sr are the same as they were after the START condition (S), and it tests whether the eighth (R/$\overline{W}$) bit is 1. If there is a match, the slave considers that it has been addressed as a transmitter and generates acknowledge A3. The slave-transmitter remains addressed until it receives a STOP condition (P) or a repeated START condition (Sr) followed by a different slave address.

After a repeated START condition (Sr), all other slave devices also compare the first seven bits of the first byte of the slave address with their own addresses and test the eighth (R/$\overline{W}$) bit. However, none of them are addressed because R/$\overline{W}$ = 1 (for 10-bit devices), or the 11110XX slave address (for 7-bit devices) does not match.

Table 20-5. Master-receiver addresses a slave-transmitter with a 10-bit address

S	Slave address first 7 bits 11110 + AD10 + AD9	R/$\overline{W}$ 0	A1	Slave address second byte AD[8:1]	A2	Sr	Slave address first 7 bits 11110 + AD10 + AD9	R/$\overline{W}$ 1	A3	Data	A	...	Data	A	P

After the master-receiver has sent the first byte of the 10-bit address, the slave-transmitter sees an I2C interrupt. User software must ensure that for this interrupt, the contents of the Data register are ignored and not treated as valid data.

20.5.3 Address matching

All received addresses can be requested in 7-bit or 10-bit address format.

- AD[7:1] in Address Register 1, which contains the I2C primary slave address, always participates in the address matching process. It provides a 7-bit address.
- If the ADEXT bit is set, AD[10:8] in Control Register 2 participates in the address matching process. It extends the I2C primary slave address to a 10-bit address.

Additional conditions that affect address matching include:

- If the GCAEN bit is set, general call participates the address matching process.
- If the ALERTEN bit is set, alert response participates the address matching process.
- If the SIICAEN bit is set, Address Register 2 participates in the address matching process.
- If the RMEN bit is set, when the Range Address register is programmed to a nonzero value, any address within the range of values of Address Register 1 (excluded) and the Range Address register (included) participates in the address matching process. The Range Address register must be programmed to a value greater than the value of Address Register 1.

When the I2C module responds to one of these addresses, it acts as a slave-receiver and the IAAS bit is set after the address cycle. Software must read the Data register after the first byte transfer to determine that the address is matched.

20.5.4 System management bus specification

SMBus provides a control bus for system and power management related tasks. A system can use SMBus to pass messages to and from devices instead of tripping individual control lines.

Removing the individual control lines reduces pin count. Accepting messages ensures future expandability. With the system management bus, a device can provide manufacturer information, tell the system what its model/part number is, save its state for a suspend event, report different types of errors, accept control parameters, and return its status.

20.5.4.1 Timeouts

The $T_{TIMEOUT,MIN}$ parameter allows a master or slave to conclude that a defective device is holding the clock low indefinitely or a master is intentionally trying to drive devices off the bus. The slave device must release the bus (stop driving the bus and let SCL and SDA float high) when it detects any single clock held low longer than $T_{TIMEOUT,MIN}$. Devices that have detected this condition must reset their communication and be able to receive a new START condition within the timeframe of $T_{TIMEOUT,MAX}$.

SMBus defines a clock low timeout, $T_{TIMEOUT}$, of 35 ms, specifies $T_{LOW:SEXT}$ as the cumulative clock low extend time for a slave device, and specifies $T_{LOW:MEXT}$ as the cumulative clock low extend time for a master device.

20.5.4.1.1 SCL low timeout

If the SCL line is held low by a slave device on the bus, no further communication is possible. Furthermore, the master cannot force the SCL line high to correct the error condition. To solve this problem, the SMBus protocol specifies that devices participating in a transfer must detect any clock cycle held low longer than a timeout value condition. Devices that have detected the timeout condition must reset the communication. When the I2C module is an active master, if it detects that SMBCLK low has exceeded the value of $T_{TIMEOUT,MIN}$, it must generate a stop condition within or after the current data byte in the transfer process. When the I2C module is a slave, if it detects the $T_{TIMEOUT,MIN}$ condition, it resets its communication and is then able to receive a new START condition.

20.5.4.1.2 SCL high timeout

When the I2C module has determined that the SMBCLK and SMBDAT signals have been high for at least $T_{HIGH:MAX}$, it assumes that the bus is idle.

A HIGH timeout occurs after a START condition appears on the bus but before a STOP condition appears on the bus. Any master detecting this scenario can assume the bus is free when either of the following occurs:

- SHTF1 rises.
- The BUSY bit is high and SHTF1 is high.

When the SMBDAT signal is low and the SMBCLK signal is high for a period of time, another kind of timeout occurs. The time period must be defined in software. SHTF2 is used as the flag when the time limit is reached. This flag is also an interrupt resource, so it triggers IICIF.

20.5.4.1.3 CSMBCLK TIMEOUT MEXT and CSMBCLK TIMEOUT SEXT

The following figure illustrates the definition of the timeout intervals $T_{LOW:SEXT}$ and $T_{LOW:MEXT}$. When in master mode, the I2C module must not cumulatively extend its clock cycles for a period greater than $T_{LOW:MEXT}$ within a byte, where each byte is defined as START-to-ACK, ACK-to-ACK, or ACK-to-STOP. When CSMBCLK TIMEOUT MEXT occurs, SMBus MEXT rises and also triggers the SLTF.

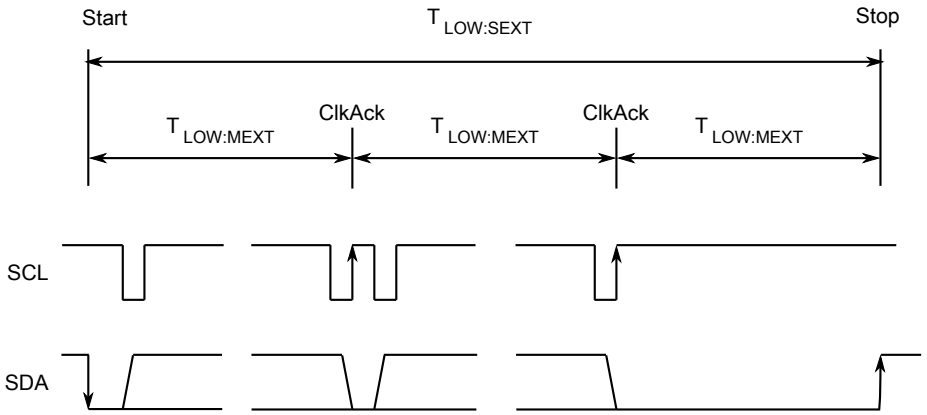


Figure 20-4. Timeout measurement intervals

A master is allowed to abort the transaction in progress to any slave that violates the $T_{LOW:SEXT}$ or $T_{TIMEOUT,MIN}$ specifications. To abort the transaction, the master issues a STOP condition at the conclusion of the byte transfer in progress. When a slave, the I2C module must not cumulatively extend its clock cycles for a period greater than $T_{LOW:SEXT}$ during any message from the initial START to the STOP. When CSMBCLK TIMEOUT SEXT occurs, SEXT rises and also triggers SLTF.

NOTE

CSMBCLK TIMEOUT SEXT and CSMBCLK TIMEOUT MEXT are optional functions that are implemented in the second step.

20.5.4.2 FAST ACK and NACK

To improve reliability and communication robustness, implementation of packet error checking (PEC) by SMBus devices is optional for SMBus devices but required for devices participating in and only during the address resolution protocol (ARP) process. The PEC is a CRC-8 error checking byte, calculated on all the message bytes. The PEC is appended to the message by the device that supplied the last data byte. If the PEC is present but not correct, a NACK is issued by the receiver. Otherwise an ACK is issued. To calculate the CRC-8 by software, this module can hold the SCL line low after receiving the eighth SCL (8th bit) if this byte is a data byte. So software can determine whether an ACK or NACK should be sent to the bus by setting or clearing the TXAK bit if the FACK (fast ACK/NACK enable) bit is enabled.

SMBus requires a device always to acknowledge its own address, as a mechanism to detect the presence of a removable device (such as a battery or docking station) on the bus. In addition to indicating a slave device busy condition, SMBus uses the NACK mechanism to indicate the reception of an invalid command or invalid data. Because such a condition may occur on the last byte of the transfer, SMBus devices are required to

have the ability to generate the not acknowledge after the transfer of each byte and before the completion of the transaction. This requirement is important because SMBus does not provide any other resend signaling. This difference in the use of the NACK signaling has implications on the specific implementation of the SMBus port, especially in devices that handle critical system data such as the SMBus host and the SBS components.

NOTE

In the last byte of master receive slave transmit mode, the master must send a NACK to the bus, so FACK must be switched off before the last byte transmits.

20.5.5 Resets

The I2C module is disabled after a reset. The I2C module cannot cause a core reset.

20.5.6 Interrupts

The I2C module generates an interrupt when any of the events in the table found here occur, provided that the IICIE bit is set.

The interrupt is driven by the IICIF bit (of the I2C Status Register) and masked with the IICIE bit (of the I2C Control Register 1). The IICIF bit must be cleared (by software) by writing 1 to it in the interrupt routine. The SMBus timeouts interrupt is driven by SLTF and masked with the IICIE bit. The SLTF bit must be cleared by software by writing 1 to it in the interrupt routine. You can determine the interrupt type by reading the Status Register.

NOTE

In master receive mode, the FACK bit must be set to zero before the last byte transfer.

Table 20-6. Interrupt summary

Interrupt source	Status	Flag	Local enable
Complete 1-byte transfer	TCF	IICIF	IICIE
Match of received calling address	IAAS	IICIF	IICIE
Arbitration lost	ARBL	IICIF	IICIE
I^2C bus stop detection	STOPF	IICIF	IICIE & SSIE
I^2C bus start detection	STARTF	IICIF	IICIE & SSIE
SMBus SCL low timeout	SLTF	IICIF	IICIE
SMBus SCL high SDA low timeout	SHTF2	IICIF	IICIE & SHTF2IE
Wakeup from stop3 or wait mode	IAAS	IICIF	IICIE & WUEN

20.5.6.1 Byte transfer interrupt

The Transfer Complete Flag (TCF) bit is set at the falling edge of the ninth clock to indicate the completion of a byte and acknowledgement transfer. When FACK is enabled, TCF is then set at the falling edge of eighth clock to indicate the completion of byte.

20.5.6.2 Address detect interrupt

When the calling address matches the programmed slave address (I2C Address Register) or when the GCAEN bit is set and a general call is received, the IAAS bit in the Status Register is set. The CPU is interrupted, provided the IICIE bit is set. The CPU must check the SRW bit and set its Tx mode accordingly.

20.5.6.3 Stop Detect Interrupt

When the stop status is detected on the I^2C bus, the STOPF bit is set to 1. The CPU is interrupted, provided the IICIE and SSIE bits are both set to 1.

20.5.6.4 Exit from low-power/stop modes

The slave receive input detect circuit and address matching feature are still active on low power modes (wait and stop). An asynchronous input matching slave address or general call address brings the CPU out of low power/stop mode if the interrupt is not masked. Therefore, TCF and IAAS both can trigger this interrupt.

20.5.6.5 Arbitration lost interrupt

The I2C is a true multimaster bus that allows more than one master to be connected on it. If two or more masters try to control the bus at the same time, the relative priority of the contending masters is determined by a data arbitration procedure. The I2C module asserts the arbitration-lost interrupt when it loses the data arbitration process and the ARBL bit in the Status Register is set.

Arbitration is lost in the following circumstances:

1. SDA is sampled as low when the master drives high during an address or data transmit cycle.

2. SDA is sampled as low when the master drives high during the acknowledge bit of a data receive cycle.
3. A START cycle is attempted when the bus is busy.
4. A repeated START cycle is requested in slave mode.
5. A STOP condition is detected when the master did not request it.

The ARBL bit must be cleared (by software) by writing 1 to it.

20.5.6.6 Timeout interrupt in SMBus

When the IICIE bit is set, the I2C module asserts a timeout interrupt (outputs SLTF and SHTF2) upon detection of any of the mentioned timeout conditions, with one exception. The SCL high and SDA high TIMEOUT mechanism must not be used to influence the timeout interrupt output, because this timeout indicates an idle condition on the bus. SHTF1 rises when it matches the SCL high and SDA high TIMEOUT and falls automatically just to indicate the bus status. The SHTF2's timeout period is the same as that of SHTF1, which is short compared to that of SLTF, so another control bit, SHTF2IE, is added to enable or disable it.

20.5.7 Programmable input glitch filter

An I2C glitch filter has been added outside legacy I2C modules but within the I2C package. This filter can absorb glitches on the I2C clock and data lines for the I2C module.

The width of the glitch to absorb can be specified in terms of the number of (half) I2C module clock cycles. A single Programmable Input Glitch Filter control register is provided. Effectively, any down-up-down or up-down-up transition on the data line that occurs within the number of clock cycles programmed in this register is ignored by the I2C module. The programmer must specify the size of the glitch (in terms of I2C module clock cycles) for the filter to absorb and not pass.

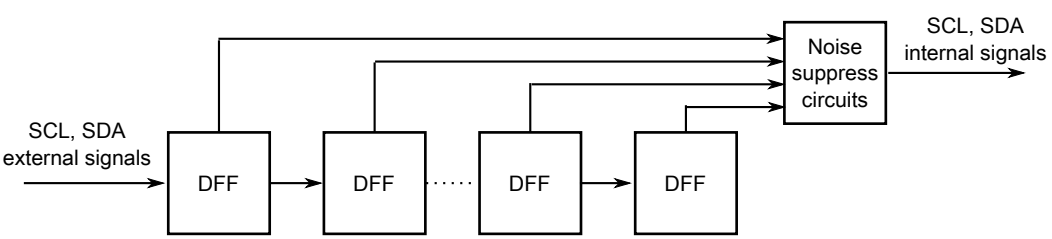


Figure 20-5. Programmable input glitch filter diagram

20.5.8 Address matching wake-up

When a primary, range, or general call address match occurs when the I2C module is in slave receive mode, the MCU wakes from a low power mode where no peripheral bus is running.

Data sent on the bus that is the same as a target device address might also wake the target MCU.

After the address matching IAAS bit is set, an interrupt is sent at the end of address matching to wake the core. The IAAS bit must be cleared after the clock recovery.

NOTE

After the system recovers and is in Run mode, restart the I2C module if it is needed to transfer packets. To avoid I2C transfer problems resulting from the situation, firmware should prevent the MCU execution of a STOP instruction when the I2C module is in the middle of a transfer unless the Stop mode holdoff feature is used during this period (set FLT[SHEN] to 1).

20.6 Initialization/application information

Module Initialization (Slave)

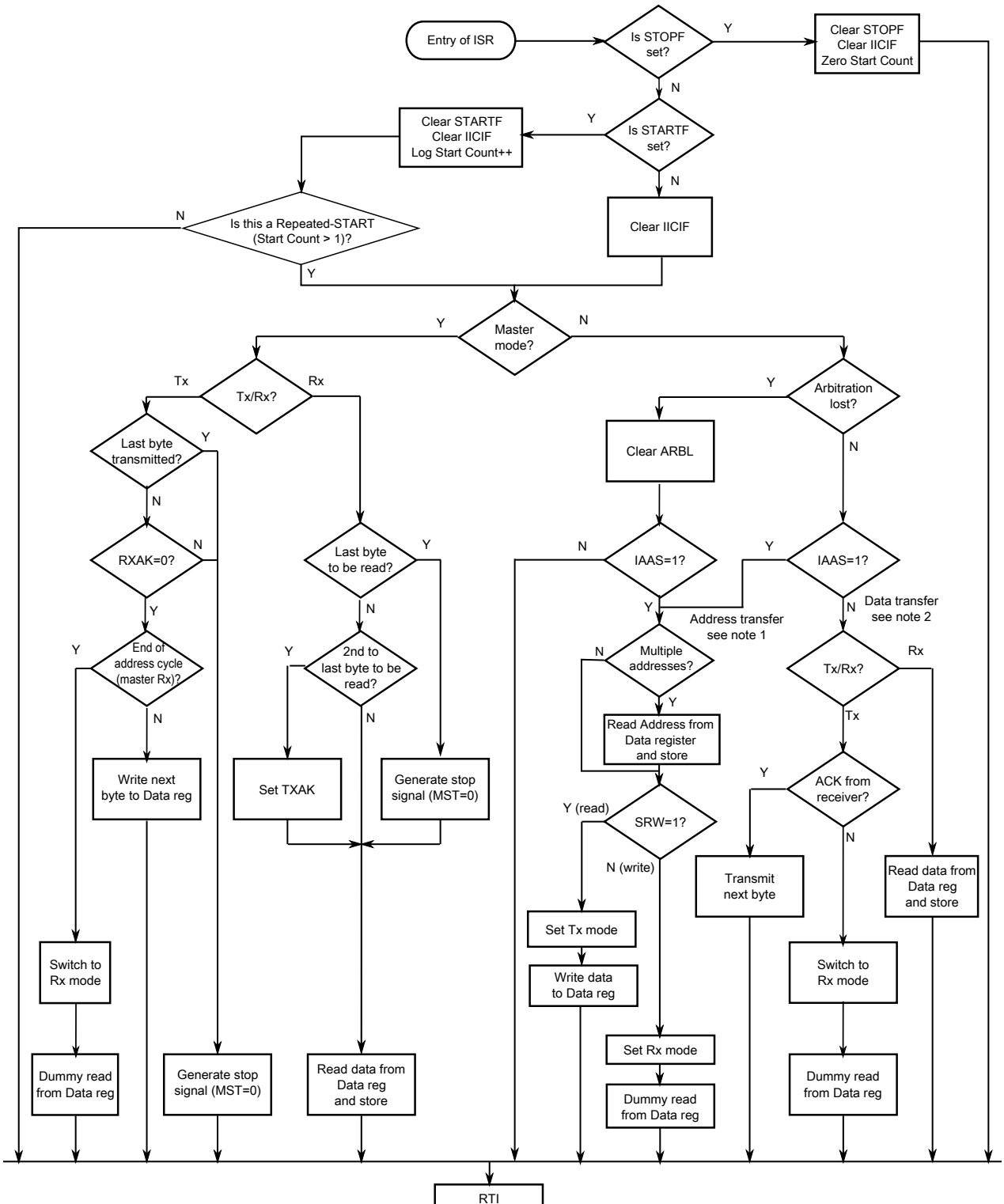
1. Write: Control Register 2
   - to enable or disable general call
   - to select 10-bit or 7-bit addressing mode
2. Write: Address Register 1 to set the slave address
3. Write: Control Register 1 to enable the I2C module and interrupts
4. Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data
5. Initialize RAM variables used to achieve the routine shown in the following figure

Module Initialization (Master)

1. Write: Frequency Divider register to set the I2C baud rate (see example in description of ICR)
2. Write: Control Register 1 to enable the I2C module and interrupts
3. Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data
4. Initialize RAM variables used to achieve the routine shown in the following figure
5. Write: Control Register 1 to enable TX

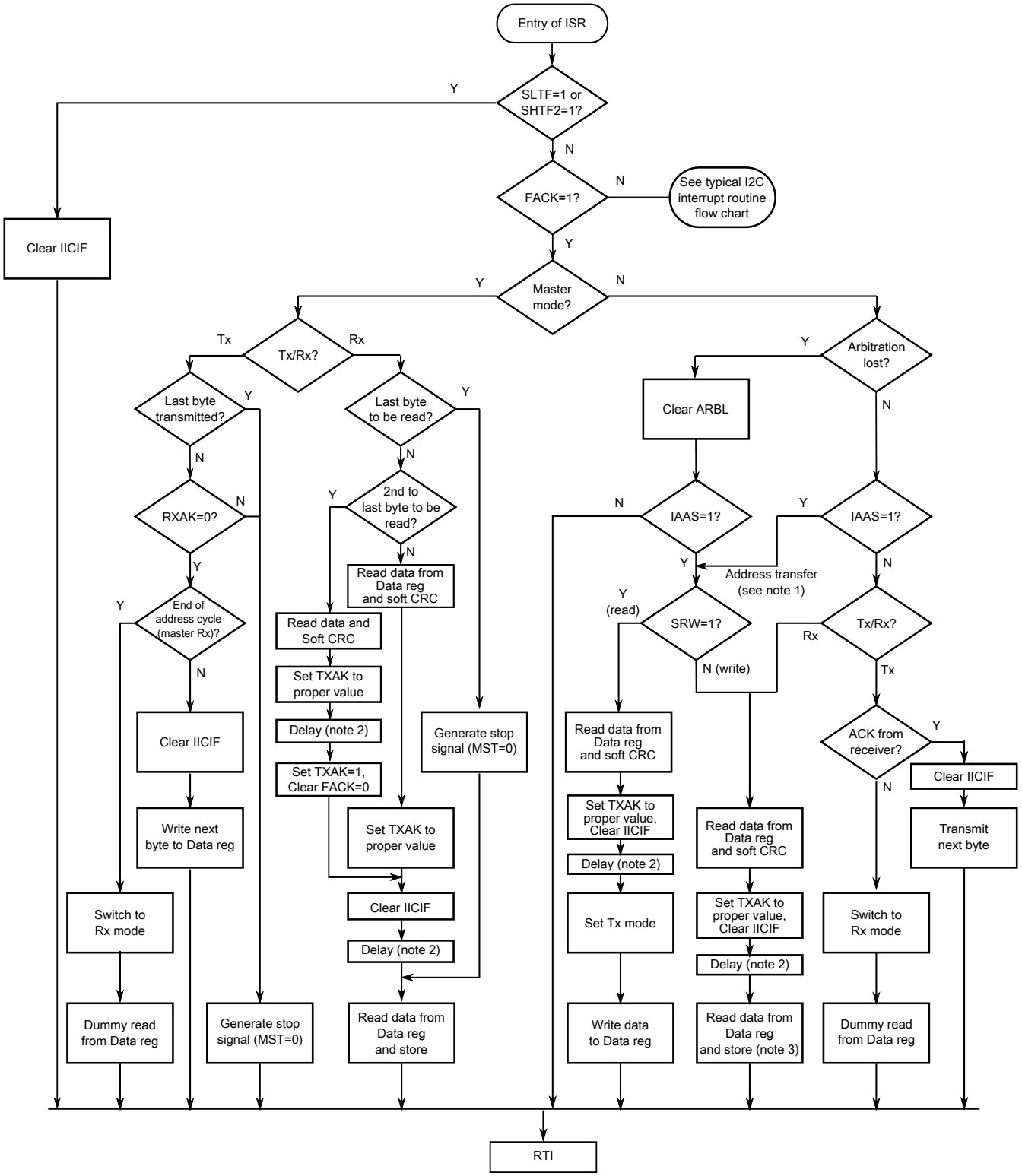
6. Write: Control Register 1 to enable MST (master mode)
7. Write: Data register with the address of the target slave (the LSB of this byte determines whether the communication is master receive or transmit)

The routine shown in the following figure encompasses both master and slave I2C operations. For slave operation, an incoming I2C message that contains the proper address begins I2C communication. For master operation, communication must be initiated by writing the Data register. An example of an I2C driver which implements many of the steps described here is available in AN4342: Using the Inter-Integrated Circuit on ColdFire+ and Kinetis .



Notes:
1. If general call is enabled, check to determine if the received address is a general call address (0x00).
   If the received address is a general call address, the general call must be handled by user software.
2. When 10-bit addressing addresses a slave, the slave sees an interrupt following the first byte of the extended address.
   Ensure that for this interrupt, the contents of the Data register are ignored and not treated as a valid data transfer.

Figure 20-6. Typical I2C interrupt routine



Notes:
1. If general call or SIICAEN is enabled, check to determine if the received address is a general call address (0x00) or an SMBus device default address. In either case, they must be handled by user software.
2. In receive mode, one bit time delay may be needed before the first and second data reading, to wait for the possible longest time period (in worst case) of the 9th SCL cycle.
3. This read is a dummy read in order to reset the SMBus receiver state machine.

Figure 20-7. Typical I2C SMBus interrupt routine

Chapter 21
Analog-to-digital converter (ADC)

21.1 Chip specific ADC information

This device contains one 12-bit analog-to-digital converter (ADC).

21.1.1 Channel assignments

The ADC channel assignments are shown in following table. Reserved channels convert to an unknown value.

Table 21-1. ADC channel assignments

ADCH	Channel	Input
00000	AD0	PTA0/ADP0
00001	AD1	PTA1/ADP1
00010	AD2	PTA2/ADP2
00011	AD3	PTA3/ADP3
00100	AD4	PTB0/ADP4
00101	AD5	PTB1/ADP5
00110	AD6	PTB2/ADP6
00111	AD7	PTB3/ADP7
01000	AD8	PTC0/ADP8
01001	AD9	PTC1/ADP9
01010	AD10	PTC2/ADP10
01011	AD11	PTC3/ADP11
01100	AD12	OPAMP
01101	AD13	VSS
01110	AD14	VSS
01111	AD15	VSS
10000	AD16	VSS
10001	AD17	VSS

Table continues on the next page...

Table 21-1. ADC channel assignments (continued)

ADCH	Channel	Input
10010	AD18	VSS
10011	AD19	VSS
10100	AD20	Reserved
10101	AD21	Reserved
10110	AD22	Temperature Sensor
10111	AD23	Bandgap
11000	AD24	Reserved
11001	AD25	Reserved
11010	AD26	Reserved
11011	AD27	Reserved
11100	AD28	Reserved
11101	AD29	VREFH(VDD)
11110	AD30	VREFL(VSS)
11111	Module Disabled	None

21.1.2 Alternate clock

The ADC module is capable of performing conversions using the MCU bus clock, the bus clock divided by two, the local asynchronous clock (ADACK) within the module, or the alternate clock, ALTCLK. The alternate clock for this device is the external oscillator output (OSCOUT).

The selected clock source must run at a frequency, so that the ADC conversion clock (ADCK) runs at a frequency within its specified range (f_{ADCK}) after being divided down from the ALTCLK input as determined by the ADIV bits.

ALTCLK is active while the MCU is in wait mode provided the conditions described above are met. This allows ALTCLK to be used as the conversion clock source for the ADC while the MCU is in wait mode.

ALTCLK cannot be used as the ADC conversion clock source while the MCU is in stop3 mode.

21.1.3 Hardware trigger

The ADC hardware trigger, ADHWT, is selectable from RTC overflow, MTIM0 overflow, ACMP0 output, FTM0 Channel 0/1 or FTM2 Channel 0/1 with configurable edge. The hardware trigger can be configured to cause a hardware trigger in MCU run, wait, and stop3 modes. Refer to Figure 7-1.

21.1.4 Temperature sensor

The ADC module integrates an on-chip temperature sensor. Following actions must be performed to use this temperature sensor.

- Configure ADC for long sample with a maximum of 1 MHz clock
- Convert the bandgap voltage reference channel (AD23)
  - By converting the digital value of the bandgap voltage reference channel using the value of VBG the user can determine V_{DD}.
- Convert the temperature sensor channel (AD22)
  - By using the calculated value of VDD, convert the digital value of AD22 into a voltage, V_{TEMP}

Following equation provides an approximate transfer function of the on-chip temperature sensor for VDD = 5.0V, Temp =25°C, using the ADC at f_{ADCK} = 1.0 MHz and configured for long sample.

Temp = 25 - ((V_{TEMP}-V_{TEMP25})/m)

where:

- V_{TEMP} is the voltage of the temperature sensor channel at the ambient temperature
- V_{TEMP25} is the voltage of the temperature sensor channel at 25°C
- m is the hot or cold voltage versus temperature slope in V/°C

For temperature calculations, use the VTEMP25 and m values in the datasheet.

In application code, the user reads the temperature sensor channel, calculates V_{TEMP}, and compares it to V_{TEMP25}. If V_{TEMP} is greater than VTEMP25 the cold slope value is applied in above equation. If V_{TEMP} is less than V_{TEMP25} the hot slope value is applied in above equation.

21.2 Introduction

The 12-bit analog-to-digital converter (ADC) is a successive approximation ADC designed for operation within an integrated microcontroller system-on-chip.

21.2.1 Features

Features of the ADC module include:

- Linear Successive Approximation algorithm with 8-, 10-, or 12-bit resolution
- Up to 12 external analog inputs, external pin inputs, and 5 internal analog inputs including internal bandgap, temperature sensor, and references
- Output formatted in 8-, 10-, or 12-bit right-justified unsigned format
- Single or Continuous Conversion (automatic return to idle after single conversion)
- Support up to eight result FIFO with selectable FIFO depth
- Configurable sample time and conversion speed/power
- Conversion complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in Wait or Stop modes for lower noise operation
- Asynchronous clock source for lower noise operation
- Selectable asynchronous hardware conversion trigger
- Automatic compare with interrupt for less-than, or greater-than or equal-to, programmable value

21.2.2 Block Diagram

This figure provides a block diagram of the ADC module.

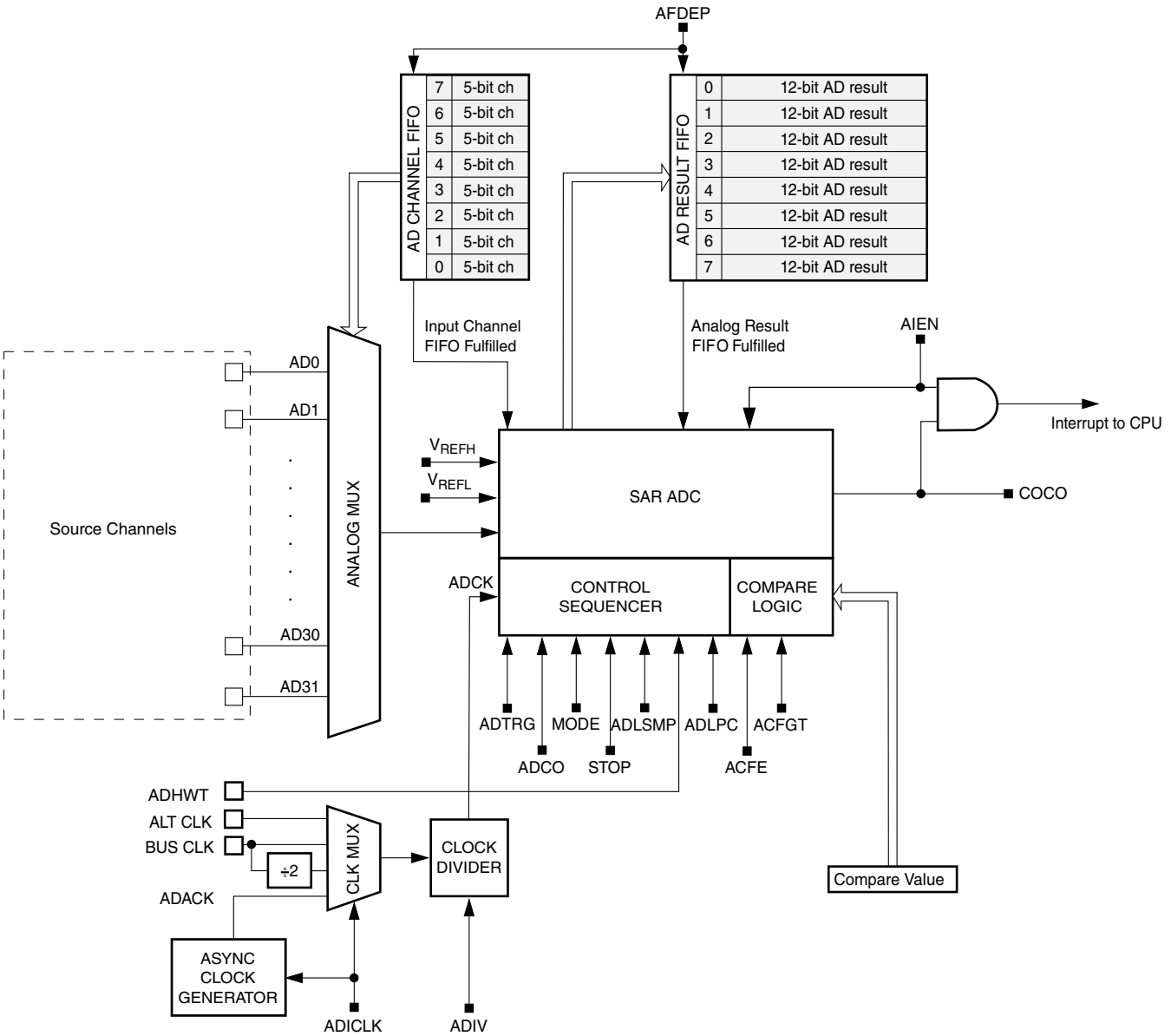


Figure 21-1. ADC Block Diagram

See chip specific sections for the channel assignments.

21.3 External Signal Description

The ADC module supports up to 12 separate analog inputs. It also requires four supply/ reference/ground connections.

Table 21-2. Signal Properties

Name	Function
AD11–AD0	Analog Channel inputs

Table continues on the next page...

Table 21-2. Signal Properties (continued)

Name	Function
V_{REFH}	High reference voltage
V_{REFL}	Low reference voltage
V_{DDA}	Analog power supply
V_{SSA}	Analog ground

21.3.1 Analog Power (V_{DDA})

The ADC analog portion uses V_{DDA} as its power connection. In some packages, V_{DDA} is connected internally to V_{DDX}. If externally available, connect the V_{DDA} pin to the same voltage potential as V_{DDX}. External filtering may be necessary to ensure clean V_{DDA} for good results.

21.3.2 Analog Ground (V_{SSA})

The ADC analog portion uses V_{SSA} as its ground connection. In some packages, V_{SSA} is connected internally to V_{SS}. If externally available, connect the V_{SSA} pin to the same voltage potential as V_{SS}.

21.3.3 Voltage Reference High (V_{REFH})

V_{REFH} is the high reference voltage for the converter. In some packages, V_{REFH} is connected internally to V_{DDA}. If externally available, V_{REFH} may be connected to the same potential as V_{DDA} or may be driven by an external source between the minimum V_{DDA} specified in the data sheet and the V_{DDA} potential (V_{REFH} must never exceed V_{DDA}).

21.3.4 Voltage Reference Low (V_{REFL})

V_{REFL} is the low-reference voltage for the converter. In some packages, V_{REFL} is connected internally to V_{SSA}. If externally available, connect the V_{REFL} pin to the same voltage potential as V_{SSA}.

21.3.5 Analog Channel Inputs (ADx)

The ADC module supports up to 24 separate analog inputs. An input is selected for conversion through the ADCH channel select bits.

21.4 ADC Control Registers

ADC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
10	Status and Control Register 1 (ADC_SC1)	8	R/W	1Fh	21.4.1/351
11	Status and Control Register 2 (ADC_SC2)	8	R/W	08h	21.4.2/352
12	Status and Control Register 3 (ADC_SC3)	8	R/W	00h	21.4.3/354
13	Status and Control Register 4 (ADC_SC4)	8	R/W	00h	21.4.4/355
14	Conversion Result High Register (ADC_RH)	8	R	00h	21.4.5/356
15	Conversion Result Low Register (ADC_RL)	8	R	00h	21.4.6/357
16	Compare Value High Register (ADC_CVH)	8	R/W	00h	21.4.7/357
17	Compare Value Low Register (ADC_CVL)	8	R/W	00h	21.4.8/358
30AC	Pin Control 1 Register (ADC_APCTL1)	8	R/W	00h	21.4.9/358
30AD	Pin Control 2 Register (ADC_APCTL2)	8	R/W	00h	21.4.10/360

21.4.1 Status and Control Register 1 (ADC_SC1)

This section describes the function of the ADC status and control register (ADC_SC1). Writing ADC_SC1 aborts the current conversion and initiates a new conversion (if the ADCH bits are equal to a value other than all 1s).

When FIFO is enabled, the analog input channel FIFO is written via ADCH. The analog input channel queue must be written to ADCH continuously. The resulting FIFO follows the order in which the analog input channel is written. The ADC will start conversion when the input channel FIFO is fulfilled at the depth indicated by the ADC_SC4[AFDEP]. Any write 0x1F to these bits will reset the FIFO and stop the conversion if it is active.

Address: 10h base + 0h offset = 10h

Bit	7	6	5	4	3	2	1	0
Read	COCO	AIEN	ADCO	ADCH				
Write								
Reset	0	0	0	1	1	1	1	1

ADC_SC1 field descriptions

Field	Description
7 COCO	Conversion Complete Flag Conversion Complete Flag. The COCO flag is a read-only bit set each time a conversion is completed when the compare function is disabled (ADC_SC2[ACFE] = 0). When the compare function is enabled (ADC_SC2[ACFE] = 1), the COCO flag is set upon completion of a conversion only if the compare result is true. When the FIFO function is enabled (ADC_SC4[AFDEP] > 0), the COCO flag is set upon completion of the set of FIFO conversion. This bit is cleared when ADC_SC1 is written or when ADC_RL is read. 0 Conversion not completed. 1 Conversion completed.
6 AIEN	Interrupt Enable AIEN enables conversion complete interrupts. When COCO becomes set while AIEN is high, an interrupt is asserted. 0 Conversion complete interrupt disabled. 1 Conversion complete interrupt enabled.
5 ADCO	Continuous Conversion Enable ADCO enables continuous conversions. 0 One conversion following a write to the ADC_SC1 when software triggered operation is selected, or one conversion following assertion of ADHWT when hardware triggered operation is selected. When the FIFO function is enabled (AFDEP > 0), a set of conversions are triggered. 1 Continuous conversions are initiated following a write to ADC_SC1 when software triggered operation is selected. Continuous conversions are initiated by an ADHWT event when hardware triggered operation is selected. When the FIFO function is enabled (AFDEP > 0), a set of conversions are loop triggered.
ADCH	Input Channel Select The ADCH bits form a 5-bit field that selects one of the input channels. See chip specific section for the ADCH configurations.

21.4.2 Status and Control Register 2 (ADC_SC2)

The ADC_SC2 register controls the compare function, conversion trigger, and conversion active of the ADC module.

Address: 10h base + 1h offset = 11h

Bit	7	6	5	4	3	2	1	0
Read	ADACT	ADTRG	ACFE	ACFGT	FEMPTY	FFULL	REFSEL	
Write								
Reset	0	0	0	0	1	0	0	0

ADC_SC2 field descriptions

Field	Description
7 ADACT	Conversion Active Indicates that a conversion is in progress. ADACT is set when a conversion is initiated and cleared when a conversion is completed or aborted. 0 Conversion not in progress. 1 Conversion in progress.
6 ADTRG	Conversion Trigger Select Selects the type of trigger used for initiating a conversion. Two types of trigger are selectable: software trigger and hardware trigger. When software trigger is selected, a conversion is initiated following a write to ADC_SC1. When hardware trigger is selected, a conversion is initiated following the assertion of the ADHWT input. 0 Software trigger selected. 1 Hardware trigger selected.
5 ACFE	Compare Function Enable Enables the compare function. 0 Compare function disabled. 1 Compare function enabled.
4 ACFGT	Compare Function Greater Than Enable Configures the compare function to trigger when the result of the conversion of the input being monitored is greater than or equal to the compare value. The compare function defaults to triggering when the result of the compare of the input being monitored is less than the compare value. 0 Compare triggers when input is less than compare level. 1 Compare triggers when input is greater than or equal to compare level.
3 FEMPTY	Result FIFO empty 0 Indicates that ADC result FIFO have at least one valid new data. 1 Indicates that ADC result FIFO have no valid new data.
2 FFULL	Result FIFO full 0 Indicates that ADC result FIFO is not full and next conversion data still can be stored into FIFO. 1 Indicates that ADC result FIFO is full and next conversion will override old data in case of no read action.
REFSEL	Voltage Reference Selection Selects the voltage reference source used for conversions. 00 Reserved. 01 Analog supply pin pair (V_{DDA}/V_{SSA}). 10 Reserved. 11 Reserved.

21.4.3 Status and Control Register 3 (ADC_SC3)

ADC_SC3 selects the mode of operation, clock source, clock divide, and configure for low power or long sample time.

Address: 10h base + 2h offset = 12h

Bit	7	6	5	4	3	2	1	0
Read Write	ADLPC	ADIV		ADLSMP	MODE		ADICLK	
Reset	0	0	0	0	0	0	0	0

ADC_SC3 field descriptions

Field	Description
7 ADLPC	Low-Power Configuration ADLPC controls the speed and power configuration of the successive approximation converter. This optimizes power consumption when higher sample rates are not required. 0 High speed configuration. 1 Low power configuration:The power is reduced at the expense of maximum clock speed.
6–5 ADIV	Clock Divide Select ADIV selects the divide ratio used by the ADC to generate the internal clock ADCK. 00 Divide ration = 1, and clock rate = Input clock. 01 Divide ration = 2, and clock rate = Input clock ÷ 2. 10 Divide ration = 3, and clock rate = Input clock ÷ 4. 11 Divide ration = 4, and clock rate = Input clock ÷ 8.
4 ADLSMP	Long Sample Time Configuration ADLSMP selects between long and short sample time. This adjusts the sample period to allow higher impedance inputs to be accurately sampled or to maximize conversion speed for lower impedance inputs. Longer sample times can also be used to lower overall power consumption when continuous conversions are enabled if high conversion rates are not required. 0 Short sample time. 1 Long sample time.
3–2 MODE	Conversion Mode Selection MODE bits are used to select between 12-, 10-, or 8-bit operation. 00 8-bit conversion (N=8) 01 10-bit conversion (N=10) 10 12-bit conversion (N=12) 11 Reserved
ADICLK	Input Clock Select ADICLK bits select the input clock source to generate the internal clock ADCK. 00 Bus clock 01 Bus clock divided by 2

Table continues on the next page...

ADC_SC3 field descriptions (continued)

Field	Description
	10 Alternate clock (ALTCLK) 11 Asynchronous clock (ADACK)

21.4.4 Status and Control Register 4 (ADC_SC4)

This register controls the FIFO scan mode, FIFO compare function and FIFO depth selection of the ADC module.

Address: 10h base + 3h offset = 13h

Bit	7	6	5	4	3	2	1	0
Read	0	ASCANE	ACFSEL	0		AFDEP		
Write								
Reset	0	0	0	0	0	0	0	0

ADC_SC4 field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 ASCANE	FIFO Scan Mode Enable The FIFO always use the first dummied FIFO channels when it is enabled. When this bit is set and FIFO function is enabled, ADC will repeat using the first FIFO channel as the conversion channel until the result FIFO is fulfilled. In continuous mode (ADCO = 1), ADC will start next conversion with the same channel when COCO is set. 0 FIFO scan mode disabled. 1 FIFO scan mode enabled.
5 ACFSEL	Compare function select OR/AND when the FIFO function is enabled (AFDEP > 0). When this field is cleared, ADC will OR all of compare triggers and set COCO after at least one of compare trigger occurs. When this field is set, ADC will AND all of compare triggers and set COCO after all of compare triggers occur. 0 OR all of compare trigger. 1 AND all of compare trigger.
4–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
AFDEP	FIFO Depth enables the FIFO function and sets the depth of FIFO. When AFDEP is cleared, the FIFO is disabled. When AFDEP is set to nonzero, the FIFO function is enabled and the depth is indicated by the AFDEP bits. The ADCH in ADC_SC1 and ADC_RH:ADC_RL must be accessed by FIFO mode when FIFO function is enabled. ADC starts conversion when the analog channel FIFO is upon the level indicated by AFDEP bits. The COCO bit is set when the set of conversions are completed and the result FIFO is upon the level indicated by AFDEP bits. **NOTE:** The bus clock frequency must be at least double the ADC clock when FIFO mode is enabled. It means, if ICS FBE mode is used, the ADC clock can not be ADACK.

Table continues on the next page...

ADC_SC4 field descriptions (continued)

Field	Description
	000 FIFO is disabled. 001 2-level FIFO is enabled. 010 3-level FIFO is enabled.. 011 4-level FIFO is enabled. 100 5-level FIFO is enabled. 101 6-level FIFO is enabled. 110 7-level FIFO is enabled. 111 8-level FIFO is enabled.

21.4.5 Conversion Result High Register (ADC_RH)

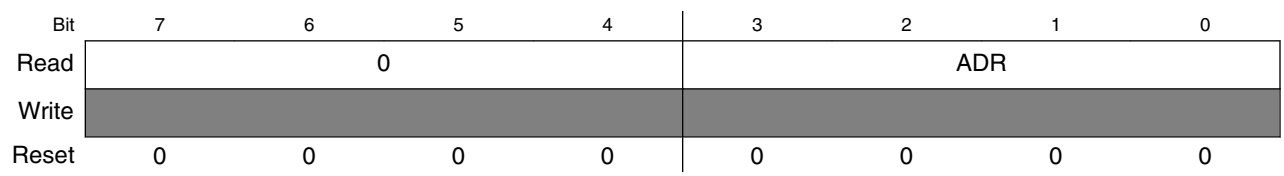
In 12-bit operation, ADC_RH contains the upper four bits of the result of a 12-bit conversion.

ADC_RH is updated each time a conversion completes except when automatic compare is enabled and the compare condition is not met. Reading ADC_RH prevents the ADC from transferring subsequent conversion results into the result registers until ADC_RL is read. If ADC_RL is not read until after the next conversion is completed, the intermediate conversion result is lost. In 8-bit mode, there is no interlocking with ADC_RL.

When FIFO is enabled, the result FIFO is read via ADC_RH:ADC_RL. The ADC conversion completes when the input channel FIFO is fulfilled at the depth indicated by the AFDEP. The AD result FIFO can be read via ADC_RH:ADC_RL continuously by the order set in analog input channel ADCH.

If the MODE bits are changed, any data in ADC_RH becomes invalid.

Address: 10h base + 4h offset = 14h



ADC_RH field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
ADR	Conversion Result[11:8]

21.4.6 Conversion Result Low Register (ADC_RL)

ADC_RL contains the lower eight bits of the result of a 12-bit conversion. This register is updated each time a conversion completes except when automatic compare is enabled and the compare condition is not met. In 12-bit mode, reading ADC_RH prevents the ADC from transferring subsequent conversion results into the result registers until ADC_RL is read. If ADC_RL is not read until the next conversion is completed, the intermediate conversion results are lost. In 8-bit mode, there is no interlocking with ADC_RH. If the MODE bits are changed, any data in ADC_RL becomes invalid.

When FIFO is enabled, the result FIFO is read via ADC_RH:ADC_RL. The ADC conversion completes when the input channel FIFO is fulfilled at the depth indicated by the AFDEP. The AD result FIFO can be read via ADC_RH:ADC_RL continuously by the order set in analog input channel FIFO.

Address: 10h base + 5h offset = 15h

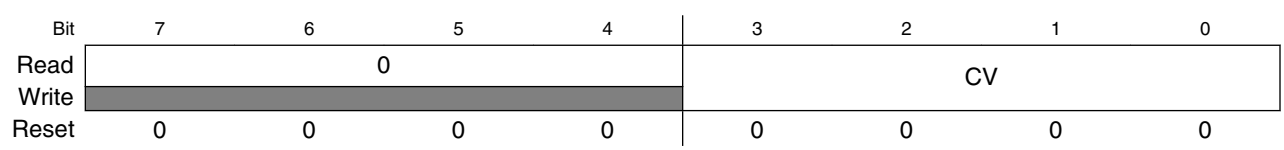
ADC_RL field descriptions

Field	Description
ADR	Conversion Result[7:0]

21.4.7 Compare Value High Register (ADC_CVH)

In 12-bit mode, this register holds the upper four bits of the 12-bit compare value. These bits are compared to the upper four bits of the result following a conversion in 12-bit mode when the compare function is enabled.

Address: 10h base + 6h offset = 16h



ADC_CVH field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CV	Conversion Result[11:8]

21.4.8 Compare Value Low Register (ADC_CVL)

This register holds the lower 8 bits of the 12-bit compare value. Bits CV7:CV0 are compared to the lower 8 bits of the result following a conversion in 12-bit mode.

Address: 10h base + 7h offset = 17h

Bit	7	6	5	4	3	2	1	0
Read Write	CV							
Reset	0	0	0	0	0	0	0	0

ADC_CVL field descriptions

Field	Description
CV	Conversion Result[7:0]

21.4.9 Pin Control 1 Register (ADC_APCTL1)

The pin control registers disable the I/O port control of MCU pins used as analog inputs. APCTL1 is used to control the pins associated with channels 0-7 of the ADC module.

Address: 10h base + 309Ch offset = 30ACh

Bit	7	6	5	4	3	2	1	0
Read Write	ADPC7	ADPC6	ADPC5	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0
Reset	0	0	0	0	0	0	0	0

ADC_APCTL1 field descriptions

Field	Description
7 ADPC7	ADC Pin Control 7 ADPC7 controls the pin associated with channel AD7. 0 AD7 pin I/O control enabled. 1 AD7 pin I/O control disabled.

Table continues on the next page...

ADC_APCTL1 field descriptions (continued)

Field	Description
6 ADPC6	ADC Pin Control 6 ADPC6 controls the pin associated with channel AD6. 0 AD6 pin I/O control enabled. 1 AD6 pin I/O control disabled.
5 ADPC5	ADC Pin Control 5 ADPC5 controls the pin associated with channel AD5. 0 AD5 pin I/O control enabled. 1 AD5 pin I/O control disabled.
4 ADPC4	ADC Pin Control 4 ADPC4 controls the pin associated with channel AD4. 0 AD4 pin I/O control enabled. 1 AD4 pin I/O control disabled.
3 ADPC3	ADC Pin Control 3 ADPC3 controls the pin associated with channel AD3. 0 AD3 pin I/O control enabled. 1 AD3 pin I/O control disabled.
2 ADPC2	ADC Pin Control 2 ADPC2 controls the pin associated with channel AD2. 0 AD2 pin I/O control enabled. 1 AD2 pin I/O control disabled.
1 ADPC1	ADC Pin Control 1 ADPC1 controls the pin associated with channel AD1. 0 AD1 pin I/O control enabled. 1 AD1 pin I/O control disabled.
0 ADPC0	ADC Pin Control 0 ADPC0 controls the pin associated with channel AD0. 0 AD0 pin I/O control enabled. 1 AD0 pin I/O control disabled.

21.4.10 Pin Control 2 Register (ADC_APCTL2)

APCTL2 controls channels 8-15 of the ADC module.

Address: 10h base + 309Dh offset = 30ADh

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved				ADPC11	ADPC10	ADPC9	ADPC8
Reset	0	0	0	0	0	0	0	0

ADC_APCTL2 field descriptions

Field	Description
7–4 Reserved	This field is reserved.
3 ADPC11	ADC Pin Control 11 ADPC11 controls the pin associated with channel AD11. 0 AD11 pin I/O control enabled. 1 AD11 pin I/O control disabled.
2 ADPC10	ADC Pin Control 10 ADPC10 controls the pin associated with channel AD10. 0 AD10 pin I/O control enabled. 1 AD10 pin I/O control disabled.
1 ADPC9	ADC Pin Control 9 ADPC9 controls the pin associated with channel AD1. 0 AD9 pin I/O control enabled. 1 AD9 pin I/O control disabled.
0 ADPC8	ADC Pin Control 8 ADPC8 controls the pin associated with channel AD8. 0 AD8 pin I/O control enabled. 1 AD8 pin I/O control disabled.

21.5 Functional description

The ADC module is disabled during reset or when the ADC_SC1[ADCH] bits are all high. The module is idle when a conversion has completed and another conversion has not been initiated. When idle, the module is in its lowest power state.

The ADC can perform an analog-to-digital conversion on any of the software selectable channels. In 12-bit mode, the selected channel voltage is converted by a successive approximation algorithm into a 12-bit digital result. In 10-bit mode, the selected channel voltage is converted by a successive approximation algorithm into a 10-bit digital result. In 8-bit mode, the selected channel voltage is converted by a successive approximation algorithm into a 8-bit digital result.

When the conversion is completed, the result is placed in the data registers (ADC_RH and ADC_RL). In 10-bit mode, the result is rounded to 10 bits and placed in the data registers (ADC_RH and ADC_RL). In 8-bit mode, the result is rounded to 8 bits and placed in ADC_RL. The conversion complete flag (ADC_SC1[COCO]) is then set and an interrupt is generated if the conversion complete interrupt has been enabled (ADC_SC1[AIEN] = 1).

The ADC module has the capability of automatically comparing the result of a conversion with the contents of its compare registers. The compare function is enabled by setting the ADC_SC2[ACFE] bit and operates with any of the conversion modes and configurations.

21.5.1 Clock select and divide control

One of four clock sources can be selected as the clock source for the ADC module. This clock source is then divided by a configurable value to generate the input clock to the converter (ADCK). The clock is selected from one of the following sources by means of the ADC_SC3[ADICLK] bits.

- The bus clock, which is equal to the frequency at which software is executed. This is the default selection following reset.
- The bus clock divided by 2: For higher bus clock rates, this allows a maximum divide by 16 of the bus clock.
- ALTCLK, that is, alternate clock which is OSCOUT
- The asynchronous clock (ADACK): This clock is generated from a clock source within the ADC module. When selected as the clock source, this clock remains active while the MCU is in Wait or Stop mode and allows conversions in these modes for lower noise operation.

Whichever clock is selected, its frequency must fall within the specified frequency range for ADCK. If the available clocks are too slow, the ADC does not perform according to specifications. If the available clocks are too fast, the clock must be divided to the appropriate frequency. This divider is specified by the ADC_SC3[ADIV] bits and can be divide-by 1, 2, 4, or 8.

21.5.2 Input select and pin control

The Pin Control registers (ADC_APCTL2 and ADC_APCTL1) disables the I/O port control of the pins used as analog inputs. When a pin control register bit is set, the following conditions are forced for the associated MCU pin:

- The output buffer is forced to its high impedance state.
- The input buffer is disabled. A read of the I/O port returns a zero for any pin with its input buffer disabled.
- The pullup is disabled.

21.5.3 Hardware trigger

The ADC module has a selectable asynchronous hardware conversion trigger, ADHWT, that is enabled when the ADC_SC2[ADTRG] bit is set. This source is not available on all MCUs. See the module introduction for information on the ADHWT source specific to this MCU.

When ADHWT source is available and hardware trigger is enabled (ADC_SC2[ADTRG] = 1), a conversion is initiated on the rising edge of ADHWT. If a conversion is in progress when a rising edge occurs, the rising edge is ignored. In continuous convert configuration, only the initial rising edge to launch continuous conversions is observed. The hardware trigger function operates in conjunction with any of the conversion modes and configurations.

21.5.4 Conversion control

Conversions can be performed in 12-bit mode, 10-bit mode, or 8-bit mode as determined by the ADC_SC3[MODE] bits. Conversions can be initiated by a software or hardware trigger. In addition, the ADC module can be configured for low power operation, long sample time, continuous conversion, and an automatic compare of the conversion result to a software determined compare value.

21.5.4.1 Initiating conversions

A conversion initiates under the following conditions:

- A write to ADC_SC1 or a set of write to ADC_SC1 in FIFO mode (with ADCH bits not all 1s) if software triggered operation is selected.
- A hardware trigger (ADHWT) event if hardware triggered operation is selected.
- The transfer of the result to the data registers when continuous conversion is enabled.

If continuous conversions are enabled, a new conversion is automatically initiated after the completion of the current conversion. In software triggered operation, continuous conversions begin after ADC_SC1 is written and continue until aborted. In hardware triggered operation, continuous conversions begin after a hardware trigger event and continue until aborted.

21.5.4.2 Completing conversions

A conversion is completed when the result of the conversion is transferred into the data result registers, ADC_RH and ADC_RL. This is indicated by the setting of ADC_SC1[COCO]. An interrupt is generated if ADC_SC1[AIEN] is high at the time that ADC_SC1[COCO] is set.

A blocking mechanism prevents a new result from overwriting previous data in ADC_RH and ADC_RL if the previous data is in the process of being read while in 12-bit or 10-bit MODE (the ADC_RH register has been read but the ADC_RL register has not). When blocking is active, the data transfer is blocked, ADC_SC1[COCO] is not set, and the new result is lost. In the case of single conversions with the compare function enabled and the compare condition false, blocking has no effect and ADC operation is terminated. In all other cases of operation, when a data transfer is blocked, another conversion is initiated regardless of the state of ADC_SC1[ADCO] whether single or continuous conversions are enabled.

If single conversions are enabled, the blocking mechanism could result in several discarded conversions and excess power consumption. To avoid this issue, the data registers must not be read after initiating a single conversion until the conversion completes.

In fifo mode, a blocking mechanism will keep current channel conversion and no channel fifo and result fifo switching until a block mechanism is released.

21.5.4.3 Aborting conversions

Any conversion in progress is aborted in the following cases:

- A write to ADC_SC1 occurs.
  - The current conversion will be aborted and a new conversion will be initiated, if ADC_SC1[ADCH] are not all 1s and ADC_SC4[AFDEP] are all 0s.
  - The current conversion and the rest of conversions will be aborted and no new conversion will be initialed, if ADC_SC4[AFDEP] are not all 0s.
  - A new conversion will be initiated when the FIFO is re-fulfilled upon the levels indicated by the ADC_SC4[AFDEP] bits).
- A write to ADC_SC2, ADC_SC3, ADC_SC4, ADC_CVH, or ADC_CVL occurs. This indicates a mode of operation change has occurred and the current and rest of conversions (when ADC_SC4[AFDEP] are not all 0s) are therefore invalid.
- The MCU is reset.
- The MCU enters Stop mode with ADACK not enabled.

When a conversion is aborted, the contents of the data registers, ADC_RH and ADC_RL, are not altered. However, they continue to be the values transferred after the completion of the last successful conversion. If the conversion was aborted by a reset, ADC_RH and ADC_RL return to their reset states.

21.5.4.4 Power control

The ADC module remains in its idle state until a conversion is initiated. If ADACK is selected as the conversion clock source, the ADACK clock generator is also enabled.

Power consumption when active can be reduced by setting ADC_SC3[ADLPC]. This results in a lower maximum value for f_{ADCK} (see the data sheet).

21.5.4.5 Sample time and total conversion time

The total conversion time depends on the sample time (as determined by ADC_SC3[ADLSMP]), the MCU bus frequency, the conversion mode (8-bit, 10-bit or 12-bit), and the frequency of the conversion clock (f_{ADCK}). After the module becomes active, sampling of the input begins.ADC_SC3[ADLSMP] selects between short (3.5 ADCK cycles) and long (23.5 ADCK cycles) sample times. When sampling is complete, the converter is isolated from the input channel and a successive approximation algorithm

is performed to determine the digital value of the analog signal. The result of the conversion is transferred to ADC_RH and ADC_RL upon completion of the conversion algorithm.

If the bus frequency is less than the f_{ADCK} frequency, precise sample time for continuous conversions cannot be guaranteed when short sample is enabled (ADC_SC3[ADLSMP] = 0). If the bus frequency is less than 1/11th of the f_{ADCK} frequency, precise sample time for continuous conversions cannot be guaranteed when long sample is enabled (ADC_SC3[ADLSMP] = 1).

The maximum total conversion time for different conditions is summarized in the table below.

Table 21-3. Total conversion time vs. control conditions

Conversion type	ADICLK	ADLSMP	Max total conversion time
Single or first continuous 8-bit	0x, 10	0	20 ADCK cycles + 5 bus clock cycles
Single or first continuous 10-bit or 12-bit	0x, 10	0	23 ADCK cycles + 5 bus clock cycles
Single or first continuous 8-bit	0x, 10	1	40 ADCK cycles + 5 bus clock cycles
Single or first continuous 10-bit or 12-bit	0x, 10	1	43 ADCK cycles + 5 bus clock cycles
Single or first continuous 8-bit	11	0	5 µs + 20 ADCK + 5 bus clock cycles
Single or first continuous 10-bit or 12-bit	11	0	5 µs + 23 ADCK + 5 bus clock cycles
Single or first continuous 8-bit	11	1	5 µs + 40 ADCK + 5 bus clock cycles
Single or first continuous 10-bit or 12-bit	11	1	5 µs + 43 ADCK + 5 bus clock cycles
Subsequent continuous 8-bit; $f_{BUS} > f_{ADCK}$	xx	0	17 ADCK cycles
Subsequent continuous 10-bit or 12-bit; $f_{BUS} > f_{ADCK}$	xx	0	20 ADCK cycles
Subsequent continuous 8-bit; $f_{BUS} > f_{ADCK}/11$	xx	1	37 ADCK cycles
Subsequent continuous 10-bit or 12-bit; $f_{BUS} > f_{ADCK}/11$	xx	1	40 ADCK cycles

The maximum total conversion time is determined by the selected clock source and the divide ratio. The clock source is selectable by the ADC_SC3[ADICLK] bits, and the divide ratio is specified by the ADC_SC3[ADIV] bits. For example, in 10-bit mode, with the bus clock selected as the input clock source, the input clock divide-by-1 ratio selected, and a bus frequency of 8 MHz, then the conversion time for a single conversion as given below:

$$\text{Conversion time} = \frac{23\,\text{ADCK Cyc}}{8\,\text{MHz}/1} + \frac{5\,\text{bus Cyc}}{8\,\text{MHz}} = 3.5\,\mu\text{s}$$

The number of bus cycles at 8 MHz is:

$$\text{Bus cycles} = 3.5\mu s \times 8MHz = 28$$

Note

The ADCK frequency must be between f_{ADCK} minimum and f_{ADCK} maximum to meet ADC specifications.

21.5.5 Automatic compare function

The compare function can be configured to check for an upper or lower limit. After the input is sampled and converted, the result is added to the two's complement of the compare value (ADC_CVH and ADC_CVL). When comparing to an upper limit (ADC_SC2[ACFGT] = 1), if the result is greater-than or equal-to the compare value, ADC_SC1[COCO] is set. When comparing to a lower limit (ADC_SC2[ACFGT] = 0), if the result is less than the compare value, ADC_SC1[COCO] is set. The value generated by the addition of the conversion result and the two's complement of the compare value is transferred to ADC_RH and ADC_RL.

On completion of a conversion while the compare function is enabled, if the compare condition is not true, ADC_SC1[COCO] is not set and no data is transferred to the result registers. An ADC interrupt is generated on the setting of ADC_SC1[COCO] if the ADC interrupt is enabled (ADC_SC1[AIEN] = 1).

On completion of all conversions while the compare function is enabled and FIFO enabled, if none of the compare conditions are true when ADC_SC4[ACFSEL] is low or if not all of compare conditions are true when ADC_SC4[ACFSEL] is high, ADC_SC1[COCO] is not set. The compare data are transferred to the result registers regardless of compare condition true or false when FIFO enabled.

Note

The compare function can monitor the voltage on a channel while the MCU is in Wait or Stop mode. The ADC interrupt wakes the MCU when the compare condition is met.

Note

The compare function can not work in continuous conversion mode when FIFO enabled.

21.5.6 FIFO operation

The ADC module supports FIFO operation to minimize the interrupts to CPU in order to reduce CPU loading in ADC interrupt service routines. This module contains two FIFOs to buffer analog input channels and analog results respectively.

The FIFO function is enabled when the ADC_SC4[AFDEP] bits are set non-zero. The FIFO depth is indicated by these bits. The FIFO supports up to eight level buffer.

The analog input channel FIFO is accessed by ADC_SC1[ADCH] bits, when FIFO function is enabled. The analog channel must be written to this FIFO in order. The ADC will not start the conversion if the channel FIFO is fulfilled below the level indicated by the ADC_SC4[AFDEP] bits, no matter whether software or hardware trigger is set. Read ADC_SC1[ADCH] will read the current active channel value. Write to ADC_SC1[ADCH] will re-fill channel FIFO to initial new conversion. It will abort current conversion and any other conversions that did not start. Write to the ADC_SC1 after all the conversions are completed or ADC is in idle state.

The result of the FIFO is accessed by ADC_RH:ADC_RL registers, when FIFO function is enabled. The result must be read via these two registers by the same order of analog input channel FIFO to get the proper results. Don't read ADC_RH:ADC_RL until all of the conversions are completed in FIFO mode. The ADC_SC1[COCO] bit will be set only when all conversions indicated by the analog input channel FIFO complete whatever software or hardware trigger is set. An interrupt request will be submitted to CPU if the ADC_SC1[AIEN] is set when the FIFO conversion completes and the ADC_SC1[COCO] bit is set.

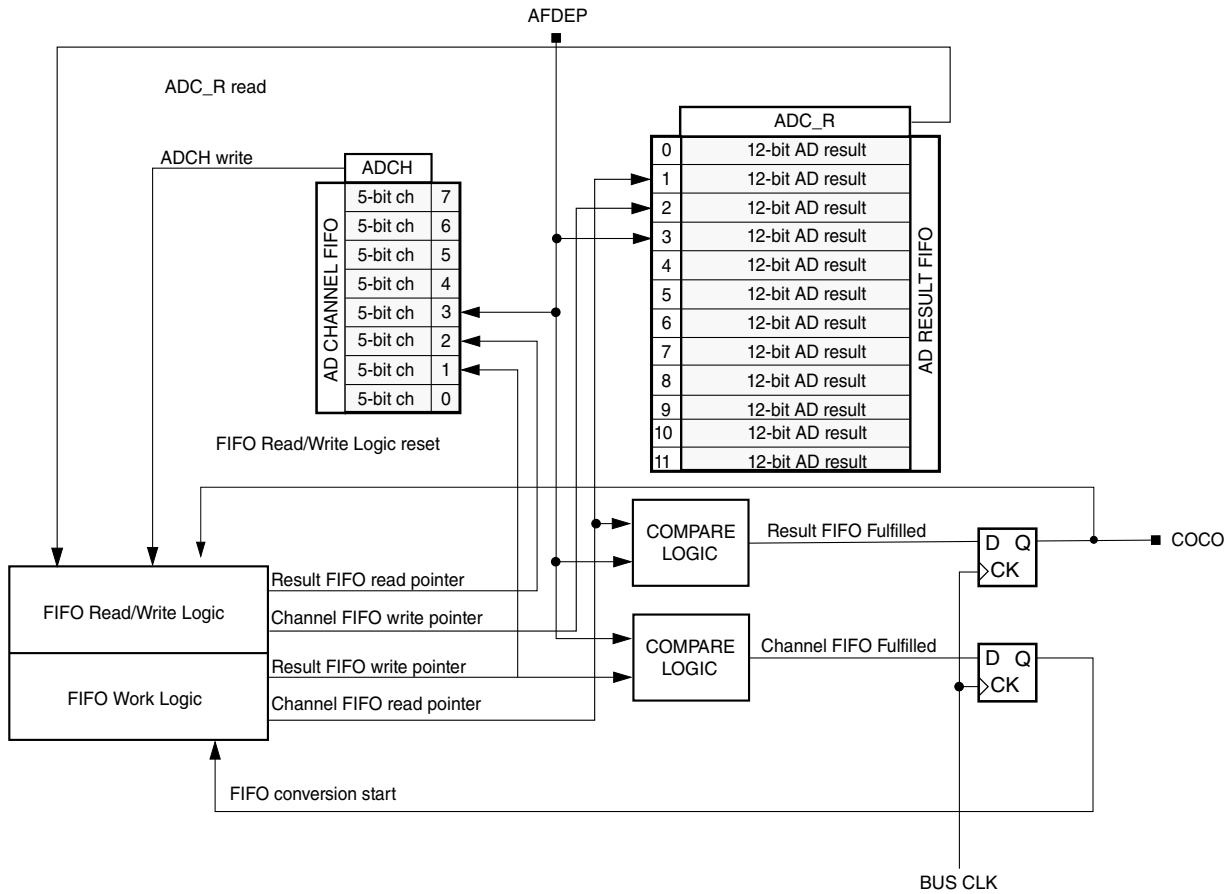


Figure 21-2. FADC FIFO structure

If software trigger is enabled, the next analog channel is fetched from analog input channel FIFO as soon as a conversion completes and its result is stored in the result FIFO. When all conversions set in the analog input channel FIFO completes, the ADC_SC1[COCO] bit is set and an interrupt request will be submitted to CPU if the ADC_SC1[AIEN] bit is set.

If hardware trigger mode is enabled, the next analog is fetched from analog input channel FIFO only when this conversion completes, its result is stored in the result FIFO, and the next hardware trigger is fed to ADC module. When all conversions set in the analog input channel FIFO completes, the ADC_SC1[COCO] bit is set and an interrupt request will be submitted to CPU if the ADC_SC1[AIEN] bit is set.

In single conversion in which ADC_SC1[ADCO] bit is clear, the ADC stops conversions when ADC_SC1[COCO] bit is set until the channel FIFO is fulfilled again or new hardware trigger occur.

The FIFO also provides scan mode to simplify the dummy work of input channel FIFO. When the ADC_SC4[ASCANE] bit is set in FIFO mode, the FIFO will always use the first dummied channel in spite of the value in the input channel FIFO. The ADC conversion start to work in FIFO mode as soon as the first channel is dummied. The

following write operation to the input channel FIFO will cover the first channel element in this FIFO. In scan FIFO mode, the ADC_SC1[COCO] bit is set when the result FIFO is fulfilled according to the depth indicated by the ADC_SC4[AFDEP] bits.

In continuous conversion in which the ADC_SC1[ADCO] bit is set, the ADC starts next conversion immediately when all conversions are completed. ADC module will fetch the analog input channel from the beginning of analog input channel FIFO.

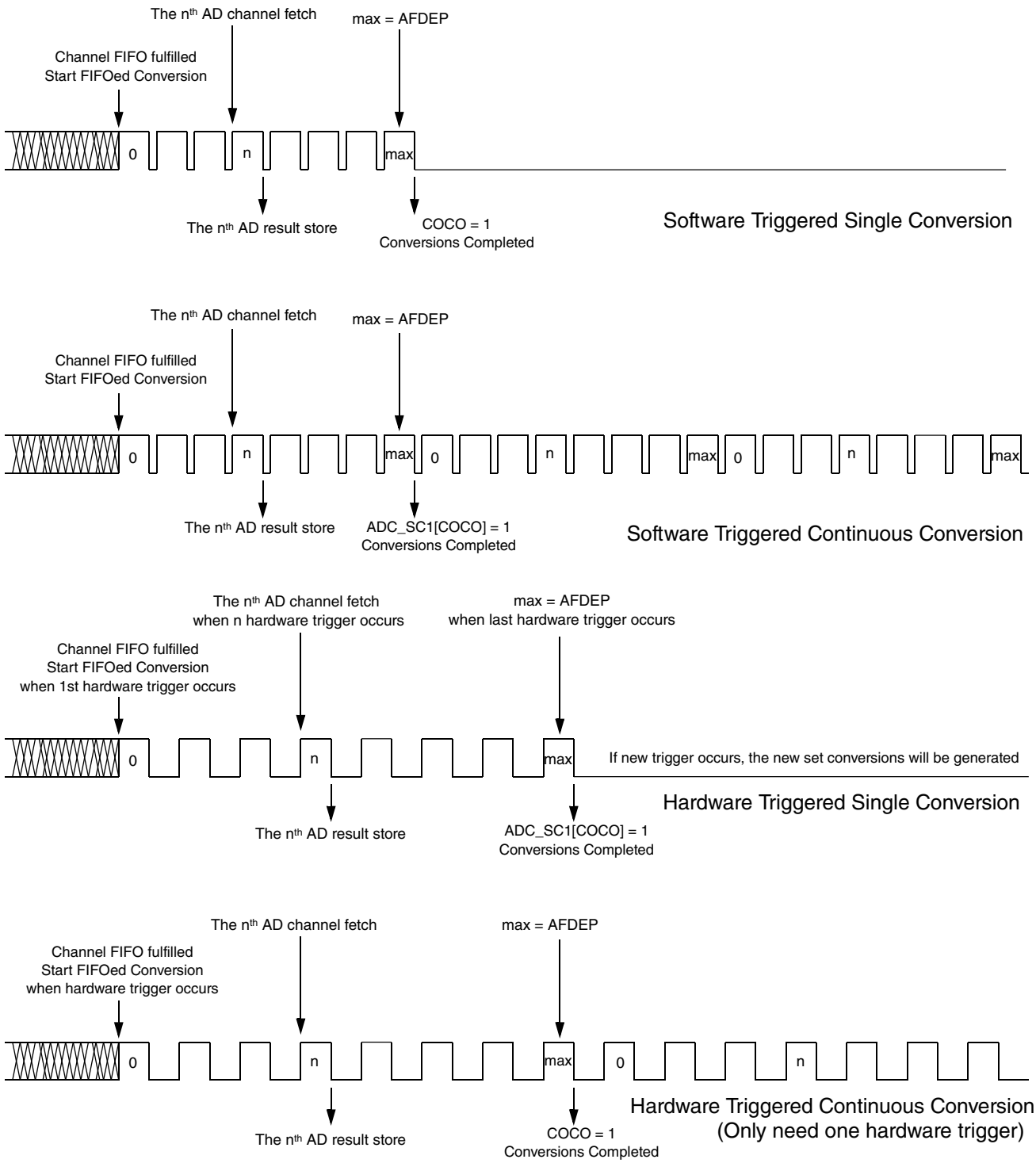


Figure 21-3. ADC FIFO conversion sequence

21.5.7 MCU wait mode operation

Wait mode is a low-power consumption standby mode from which recovery is fast because the clock sources remain active. If a conversion is in progress when the MCU enters wait mode, it continues until completion. Conversions can be initiated while the MCU is in wait mode by means of the hardware trigger or if continuous conversions are enabled.

The bus clock, bus clock divided by two, ALTCLK and ADACK are available as conversion clock sources while in wait mode.

ADC_SC1[COCO] is set by a conversion complete event that generates an ADC interrupt to wake the MCU from wait mode if the ADC interrupt is enabled (ADC_SC1[AIEN] = 1).

21.5.8 MCU Stop mode operation

Stop mode is a low-power consumption standby mode during which most or all clock sources on the MCU are disabled.

21.5.8.1 Stop mode with ADACK disabled

If the asynchronous clock, ADACK, is not selected as the conversion clock, executing a STOP instruction aborts the current conversion and places the ADC in its idle state. The contents of ADC_RH and ADC_RL are unaffected by Stop mode. After exiting from Stop mode, a software or hardware trigger is required to resume conversions.

21.5.8.2 Stop mode with ADACK enabled

If ADACK is selected as the conversion clock, the ADC continues operation during Stop mode. For guaranteed ADC operation, the MCU's voltage regulator must remain active during Stop mode. See the module introduction for configuration information for this MCU.

If a conversion is in progress when the MCU enters Stop mode, it continues until completion. Conversions can be initiated while the MCU is in Stop mode by means of the hardware trigger or if continuous conversions are enabled.

A conversion complete event sets the ADC_SC1[COCO] and generates an ADC interrupt to wake the MCU from Stop mode if the ADC interrupt is enabled (ADC_SC1[AIEN] = 1). In fifo mode, ADC cannot complete the conversion operation fully or wake the MCU from Stop mode.

Note

The ADC module can wake the system from low-power stop and cause the MCU to begin consuming run-level currents without generating a system level interrupt. To prevent this scenario, the data transfer blocking mechanism must be cleared when entering Stop and continuing ADC conversions.

21.6 Initialization information

This section gives an example that provides some basic direction on how to initialize and configure the ADC module. You can configure the module for 8-, 10-, or 12-bit resolution, single or continuous conversion, and a polled or interrupt approach, among many other options. Refer to ADC_SC3 register for information used in this example.

Note

Hexadecimal values prefixed by a 0x, binary values prefixed by a %, and decimal values have no preceding character.

21.6.1 ADC module initialization example

Before the ADC module can be used to complete conversions, it must be initialized. Given below is a method to initialize ADC module.

21.6.1.1 Initialization sequence

A typical initialization sequence is as follows:

1. Update the configuration register (ADC_SC3) to select the input clock source and the divide ratio used to generate the internal clock, ADCK. This register is also used for selecting sample time and low-power configuration.
2. Update status and control register 2 (ADC_SC2) to select the hardware or software conversion trigger and compare function options, if enabled.

3. Update status and control register 1 (ADC_SC1) to select whether conversions will be continuous or completed only once, and to enable or disable conversion complete interrupts. The input channel on which conversions will be performed is also selected here.

21.6.1.2 Pseudo-code example

In this example, the ADC module is set up with interrupts enabled to perform a single 10-bit conversion at low power with a long sample time on input channel 1, where the internal ADCK clock is derived from the bus clock divided by 1.

Example: 21.6.1.2.1 General ADC initialization routine

```
void ADC_init(void)
{
      /* The following code segment demonstrates how to initialize ADC by low-power mode,
long
      sample time, bus frequency, software triggered from AD1 external pin without FIFO
enabled
      */
 ADC_APCTL1 = ADC_APCTL1_ADPC1_MASK;
      ADC_SC3 = ADC_SC3_ADLPC_MASK | ADC_SC3_ADLSMP_MASK | ADC_SC3_MODE0_MASK;
      ADC_SC2 = 0x00;
      ADC_SC1 = ADC_SC1_AIEN_MASK | ADC_SC1_ADCH0_MASK;
}
```

21.6.2 ADC FIFO module initialization example

Before the ADC module can be used to start FIFOed conversions, an initialization procedure must be performed. A typical sequence is as follows:

1. Update the configuration register (ADC_SC3) to select the input clock source and the divide ratio used to generate the internal clock, ADCK. This register is also used to select sample time and low-power configuration.
2. Update the configuration register (ADC_SC4) to select the FIFO scan mode, FIFO compare function selection (OR or AND function) and FIFO depth.
3. Update status and control register 2 (ADC_SC2) to select the hardware or software conversion trigger, compare function options if enabled.
4. Update status and control register 1 (ADC_SC1) to select whether conversions will be continuous or completed only once, and to enable or disable conversion complete interrupts. The input channel on which conversions will be performed is also selected here.

21.6.2.1 Pseudo-code example

In this example, the ADC module is set up with interrupts enabled to perform a single hardware triggered 10-bit 4-level-FIFO conversion at low power with a long sample time on input channels of 1, 3, 5, and 7. Here the internal ADCK clock is derived from the bus clock divided by 1.

Example: 21.6.2.1.1 FIFO ADC initialization routine

```
void ADC_init(void)
{
/* The following code segment demonstrates how to initialize ADC by low-power mode, long
sample time, bus frequency, hardware triggered from AD1, AD3, AD5, and AD7 external pins
with 4-level FIFO enabled */

ADC_APCTL1 = ADC_APCTL1_ADPC6_MASK | ADC_APCTL1_ADPC5_MASK | ADC_APCTL1_ADPC3_MASK |
ADC_APCTL1_ADPC1_MASK; ADC_SC3 = ADC_SC3_ADLPC_MASK | ADC_SC3_ADLSMP_MASK |
ADC_SC3_MODE1_MASK;


// setting hardware trigger
ADC_SC2 = ADC_SC2_ADTRG_MASK ;

//4-Level FIFO
ADC_SC4 = ADC_SC4_AFDEP1_MASK | ADC_SC4_AFDEP0_MASK;

// dummy the 1st channel
ADC_SC1 = ADC_SC1_ADCH0_MASK;

// dummy the 2nd channel
ADC_SC1 = ADC_SC1_ADCH1_MASK | ADC_SC1_ADCH0_MASK;

// dummy the 3rd channel
ADC_SC1 = ADC_SC1_ADCH2_MASK | ADC_SC1_ADCH0_MASK;

// dummy the 4th channel and ADC starts conversion
ADC_SC1 = ADC_SC1_AIEN_MASK | ADC_SC1_ADCH2_MASK | ADC_SC1_ADCH1_MASK | ADC_SC1_ADCH0_MASK;

}
```

Example: 21.6.2.1.2 FIFO ADC interrupt service routine

```
unsigned short buffer[4];
interrupt VectorNumber_Vadc void ADC_isr(void)
{
      /* The following code segment demonstrates read AD result FIFO */
      // read conversion result of channel 1 and COCO bit is cleared
      buffer[0] = ADC_R;
      // read conversion result of channel 3
      buffer[1] = ADC_R;
      // read conversion result of channel 5
      buffer[2] = ADC_R;
      // read conversion result of channel 7
      buffer[3] = ADC_R;
}
```

NOTE

ADC_R is 16-bit ADC result register, combined from ADC_RH and ADC_RL

21.7 Application information

This section contains information for using the ADC module in applications. The ADC has been designed to be integrated into a microcontroller for use in embedded control applications requiring an A/D converter.

21.7.1 External pins and routing

The following sections discuss the external pins associated with the ADC module and how they are used for best results.

21.7.1.1 Analog supply pins

The ADC module has analog power and ground supplies (V_{DDA} and V_{SSA}) available as separate pins on some devices. V_{SSA} is shared on the same pin as the MCU digital V_{SS} on some devices. On other devices, V_{SSA} and V_{DDA} are shared with the MCU digital supply pins. In these cases, there are separate pads for the analog supplies bonded to the same pin as the corresponding digital supply so that some degree of isolation between the supplies is maintained.

When available on a separate pin, both V_{DDA} and V_{SSA} must be connected to the same voltage potential as their corresponding MCU digital supply (V_{DD} and V_{SS}) and must be routed carefully for maximum noise immunity and bypass capacitors placed as near as possible to the package.

If separate power supplies are used for analog and digital power, the ground connection between these supplies must be at the V_{SSA} pin. This should be the only ground connection between these supplies if possible. The V_{SSA} pin makes a good single point ground location.

21.7.1.2 Analog reference pins

In addition to the analog supplies, the ADC module has connections for two reference voltage inputs. The high reference is V_{REFH}, which may be shared on the same pin as V_{DDA} on some devices. The low reference is V_{REFL}, which may be shared on the same pin as V_{SSA} on some devices.

When available on a separate pin, V_{REFH} may be connected to the same potential as V_{DDA}, or may be driven by an external source between the minimum V_{DDA} spec and the V_{DDA} potential (V_{REFH} must never exceed V_{DDA}). When available on a separate pin, V_{REFL} must be connected to the same voltage potential as V_{SSA}. V_{REFH} and V_{REFL} must be routed carefully for maximum noise immunity and bypass capacitors placed as near as possible to the package.

AC current in the form of current spikes required to supply charge to the capacitor array at each successive approximation step is drawn through the V_{REFH} and V_{REFL} loop. The best external component to meet this current demand is a 0.1 μF capacitor with good high frequency characteristics. This capacitor is connected between V_{REFH} and V_{REFL} and must be placed as near as possible to the package pins. Resistance in the path is not recommended because the current causes a voltage drop that could result in conversion errors. Inductance in this path must be minimum (parasitic only).

21.7.1.3 Analog input pins

The external analog inputs are typically shared with digital I/O pins on MCU devices. The pin I/O control is disabled by setting the appropriate control bit in one of the pin control registers. Conversions can be performed on inputs without the associated pin control register bit set. It is recommended that the pin control register bit always be set when using a pin as an analog input. This avoids problems with contention because the output buffer is in its high impedance state and the pullup is disabled. Also, the input buffer draws DC current when its input is not at V_{DD} or V_{SS}. Setting the pin control register bits for all pins used as analog inputs should be done to achieve lowest operating current.

Empirical data shows that capacitors on the analog inputs improve performance in the presence of noise or when the source impedance is high. Use of 0.01 μF capacitors with good high-frequency characteristics is sufficient. These capacitors are not necessary in all cases, but when used they must be placed as near as possible to the package pins and be referenced to V_{SSA}.

For proper conversion, the input voltage must fall between V_{REFH} and V_{REFL}. If the input is equal to or exceeds V_{REFH}, the converter circuit converts the signal to 0xFFF (full scale 12-bit representation), 0x3FF (full scale 10-bit representation) or 0xFF (full scale 8-bit

representation). If the input is equal to or less than V_{REFL}, the converter circuit converts it to 0x000. Input voltages between V_{REFH} and V_{REFL} are straight-line linear conversions. There is a brief current associated with V_{REFL} when the sampling capacitor is charging. The input is sampled for 3.5 cycles of the ADCK source when ADC_SC3[ADLSMP] is low, or 23.5 cycles when ADC_SC3[ADLSMP] is high.

For minimal loss of accuracy due to current injection, pins adjacent to the analog input pins should not be transitioning during conversions.

21.7.2 Sources of error

Several sources of error exist for A/D conversions. These are discussed in the following sections.

21.7.2.1 Sampling error

For proper conversions, the input must be sampled long enough to achieve the proper accuracy. Given the maximum input resistance of approximately 7 kΩ and input capacitance of approximately 5.5 pF, sampling to within 1/4 LSB (at 12-bit resolution) can be achieved within the minimum sample window (3.5 cycles at 8 MHz maximum ADCK frequency) provided the resistance of the external analog source (R_{AS}) is kept below 2 kΩ.

Higher source resistances or higher-accuracy sampling is possible by setting ADC_SC3[ADLSMP] (to increase the sample window to 23.5 cycles) or decreasing ADCK frequency to increase sample time.

21.7.2.2 Pin leakage error

Leakage on the I/O pins can cause conversion error if the external analog source resistance (R_{AS}) is high. If this error cannot be tolerated by the application, keep R_{AS} lower than $V_{DDA} / (2^N * I_{LEAK})$ for less than 1/4 LSB leakage error (N = 8 in 8-bit, 10 in 10-bit or 12 in 12-bit mode).

21.7.2.3 Noise-induced errors

System noise that occurs during the sample or conversion process can affect the accuracy of the conversion. The ADC accuracy numbers are guaranteed as specified only if the following conditions are met:

- There is a 0.1 μF low-ESR capacitor from V_{REFH} to V_{REFL}.
- There is a 0.1 μF low-ESR capacitor from V_{DDA} to V_{SSA}.
- If inductive isolation is used from the primary supply, an additional 1 μF capacitor is placed from V_{DDA} to V_{SSA}.
- V_{SSA} (and V_{REFL}, if connected) is connected to V_{SS} at a quiet point in the ground plane.
- Operate the MCU in wait or Stop mode before initiating (hardware triggered conversions) or immediately after initiating (hardware or software triggered conversions) the ADC conversion.
  - For software triggered conversions, immediately follow the write to ADC_SC1 with a wait instruction or stop instruction.
  - For Stop mode operation, select ADACK as the clock source. Operation in Stop reduces V_{DD} noise but increases effective conversion time due to stop recovery.
- There is no I/O switching, input or output, on the MCU during the conversion.

There are some situations where external system activity causes radiated or conducted noise emissions or excessive V_{DD} noise is coupled into the ADC. In these situations, or when the MCU cannot be placed in wait or Stop or I/O activity cannot be halted, these recommended actions may reduce the effect of noise on the accuracy:

- Place a 0.01 μF capacitor (C_{AS}) on the selected input channel to V_{REFL} or V_{SSA} (this improves noise issues, but affects the sample rate based on the external analog source resistance).
- Average the result by converting the analog input many times in succession and dividing the sum of the results. Four samples are required to eliminate the effect of a 1LSB, one-time error.
- Reduce the effect of synchronous noise by operating off the asynchronous clock (ADACK) and averaging. Noise that is synchronous to ADCK cannot be averaged out.

21.7.2.4 Code width and quantization error

The ADC quantizes the ideal straight-line transfer function into 4096 steps (in 12-bit mode). Each step ideally has the same height (1 code) and width. The width is defined as the delta between the transition points to one code and the next. The ideal code width for an N bit converter (in this case N can be 8, 10 or 12), defined as 1LSB, is:

$$1\,\text{lsb} = \left(V_{\text{REFH}} - V_{\text{REFL}}\right) / \ 2^N$$

There is an inherent quantization error due to the digitization of the result. For 8-bit or 10-bit conversions the code transitions when the voltage is at the midpoint between the points where the straight line transfer function is exactly represented by the actual transfer function. Therefore, the quantization error will be ± 1/2 lsb in 8- or 10-bit mode. As a consequence, however, the code width of the first (0x000) conversion is only 1/2 lsb and the code width of the last (0xFF or 0x3FF) is 1.5 lsb.

For 12-bit conversions the code transitions only after the full code width is present, so the quantization error is -1 lsb to 0 lsb and the code width of each step is 1 lsb.

21.7.2.5 Linearity errors

The ADC may also exhibit non-linearity of several forms. Every effort has been made to reduce these errors but the system must be aware of them because they affect overall accuracy. These errors are:

- Zero-scale error (E_{ZS}) (sometimes called offset) — This error is defined as the difference between the actual code width of the first conversion and the ideal code width (1/2 lsb in 8-bit or 10-bit modes and 1 lsb in 12-bit mode). If the first conversion is 0x001, the difference between the actual 0x001 code width and its ideal (1 lsb) is used.
- Full-scale error (E_{FS}) — This error is defined as the difference between the actual code width of the last conversion and the ideal code width (1.5 lsb in 8-bit or 10-bit modes and 1LSB in 12-bit mode). If the last conversion is 0x3FE, the difference between the actual 0x3FE code width and its ideal (1 lsb) is used.
- Differential non-linearity (DNL) — This error is defined as the worst-case difference between the actual code width and the ideal code width for all conversions.
- Integral non-linearity (INL) — This error is defined as the highest-value that the absolute value of the running sum of DNL achieves. More simply, this is the worst-case difference of the actual transition voltage to a given code and its corresponding ideal transition voltage, for all codes.
- Total unadjusted error (TUE) — This error is defined as the difference between the actual transfer function and the ideal straight-line transfer function and includes all forms of error.

21.7.2.6 Code jitter, non-monotonicity, and missing codes

Analog-to-digital converters are susceptible to three special forms of error. These are code jitter, non-monotonicity, and missing codes.

Code jitter occurs when, at certain points, a given input voltage converts to one of two values when sampled repeatedly. Ideally, when the input voltage is infinitesimally smaller than the transition voltage, the converter yields the lower code (and vice-versa). However, even small amounts of system noise can cause the converter to be indeterminate, between two codes, for a range of input voltages around the transition voltage. This range is normally around ±1/2 lsb in 8-bit or 10-bit mode, or around 2 lsb in 12-bit mode, and increases with noise.

This error may be reduced by repeatedly sampling the input and averaging the result. Additionally the techniques discussed in Noise-induced errors reduces this error.

Non-monotonicity is defined when, except for code jitter, the converter converts to a lower code for a higher input voltage. Missing codes are those values that are never converted for any input value.

In 8-bit or 10-bit mode, the ADC is guaranteed to be monotonic and have no missing codes.

Chapter 22
Analog comparator (ACMP)

22.1 Chip specific ACMP information

This device includes two analog comparator modules. The following table summarizes the external signals of ACMP modules

Table 22-1. ACMP modules external signals

ACMP	Channel	Connection
ACMP0	0	PTA0/ACMP0IN0
	1	PTA1/ACMP0IN1
	2	Reserved
	3	DAC output
	Output	PTA4/ACMP0O
ACMP1	0	PTA3/ACMP1IN0/OPAMP+
	1	PTB1/ACMP1IN1
	2	OPAMP output
	3	DAC output

22.1.1 ACMP configuration information

Each ACMP contains one 6-bit DAC. Besides internal DAC reference, ACMP supports choosing external reference. When using the bandgap reference voltage as the reference voltage to the built-in DAC, the user must enable the bandgap buffer by setting SPMSC1[BGBE] = 1.

22.1.2 ACMP in Stop3 mode

This module continues to operate in stop3 mode if enabled. The MCU is brought out of stop when a compare event occurs and ACIE is enabled; ACF flag sets accordingly.

22.1.3 ACMP0 for SCI0 RXD Filter

SCI0 RxD input can be filtered by ACMP0 module. Refer to Figure 7-1.

22.1.4 ACMP0 output as FTM2CH0 input capture

ACMP0 output can be FTM2CH0 input capture source. Refer to Figure 7-1.

22.1.5 ACMP0 for PWT input

ACMP0 output can be PWT input 2. Refer to Figure 7-1.

22.1.6 ACMP0 for ADC trigger

ACMP0 output can be ADC trigger source. Refer to Figure 7-1.

22.1.7 ACMP1 for FDS fault

ACMP1 output is the fault input signal for FDS. The ACMP1 also supports interrupt. Refer to Figure 7-2.

22.1.8 ACMP1 for PWT input

ACMP1 output can be PWT input 3. The ACMP1 also supports interrupt. Refer to Figure 7-1.

22.2 Introduction

The analog comparator module (ACMP) provides a circuit for comparing two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage (rail-to-rail operation).

The analog mux provides a circuit for selecting an analog input signal from eight channels. One signal provided by the 6-bit DAC. The mux circuit is designed to operate across the full range of the supply voltage. The 6-bit DAC is 64-tap resistor ladder

network which provides a selectable voltage reference for applications where voltage reference is needed. The 64-tap resistor ladder network divides the supply reference V_{in} into 64 voltage level. A 6-bit digital signal input selects output voltage level, which varies from V_{in} to $V_{in}/64$. V_{in} can be selected from two voltage sources.

22.2.1 Features

ACMP features include:

- Operational over the whole supply range of 2.7 V to 5.5 V
- On-chip 6-bit resolution DAC with selectable reference voltage from V_{DD} or internal bandgap
- Configurable hysteresis
- Selectable interrupt on rising edge, falling edge, or both rising or falling edges of comparator output
- Selectable inversion on comparator output
- Up to four selectable comparator inputs
- Operational in Stop mode

22.2.2 Modes of operation

This section defines the ACMP operation in Wait, Stop, and Background Debug modes.

22.2.2.1 Operation in Wait mode

The ACMP continues to operate in Wait mode, if enabled. The interrupt can wake the MCU if enabled.

22.2.2.2 Operation in Stop mode

The ACMP (including DAC and CMP) continues to operate in Stop mode if enabled. If ACMP_CS[ACIE] is set, a ACMP interrupt can be generated to wake the MCU up from Stop mode.

If the Stop is exited by an interrupt, the ACMP setting remains before entering the Stop mode. If Stop is exited with a reset, the ACMP goes into its reset.

The user must turn off the DAC if the output is not used as a reference input of ACMP to save power, because the DAC consumes additional power.

22.2.2.3 Operation in Debug mode

When the MCU is in Debug mode, the ACMP continues operating normally.

22.2.3 Block diagram

The block diagram of the ACMP module is shown in the following figure.

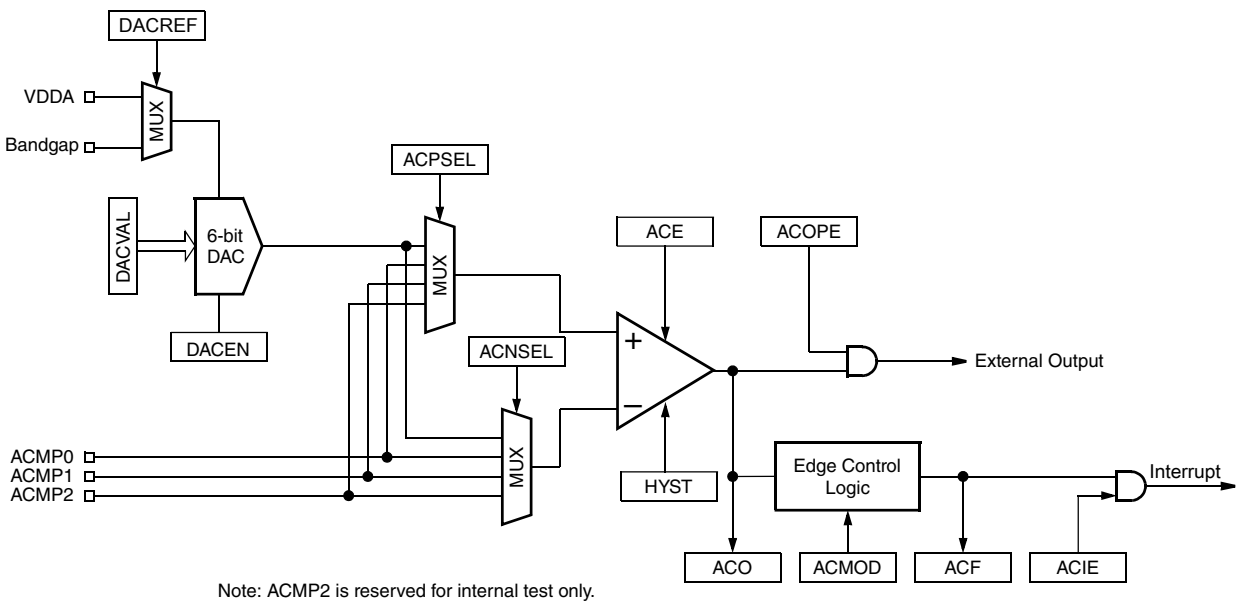


Figure 22-1. ACMP block diagram

22.3 External signal description

The output of ACMP can also be mapped to an external pin. When the output is mapped to an external pin, ACMP_CS[ACOPE] controls the pin to enable/disable the ACMP output function.

22.4 Memory map and register definition

ACMP memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
2C	ACMP Control and Status Register (ACMP0_CS)	8	R/W	00h	22.4.1/385
2D	ACMP Control Register 0 (ACMP0_C0)	8	R/W	00h	22.4.2/386
2E	ACMP Control Register 1 (ACMP0_C1)	8	R/W	00h	22.4.3/387
2F	ACMP Control Register 2 (ACMP0_C2)	8	R/W	00h	22.4.4/387
305C	ACMP Control and Status Register (ACMP1_CS)	8	R/W	00h	22.4.1/385
305D	ACMP Control Register 0 (ACMP1_C0)	8	R/W	00h	22.4.2/386
305E	ACMP Control Register 1 (ACMP1_C1)	8	R/W	00h	22.4.3/387
305F	ACMP Control Register 2 (ACMP1_C2)	8	R/W	00h	22.4.4/387

22.4.1 ACMP Control and Status Register (ACMPx_CS)

Address: Base address + 0h offset

Bit	7	6	5	4	3	2	1	0
Read	ACE	HYST	ACF	ACIE	ACO	ACOPE	ACMOD	
Write								
Reset	0	0	0	0	0	0	0	0

ACMPx_CS field descriptions

Field	Description
7 ACE	Analog Comparator Enable Enables the ACMP module. 0 The ACMP is disabled. 1 The ACMP is enabled.
6 HYST	Analog Comparator Hysterisis Selection Selects ACMP hysterisis. 0 20 mV. 1 30 mV.
5 ACF	ACMP Interrupt Flag Bit Synchronously set by hardware when ACMP output has a valid edge defined by ACMOD. The setting of this bit lags the ACMPO to bus clocks. Clear ACF bit by writing a 0 to this bit. Writing a 1 to this bit has no effect.
4 ACIE	ACMP Interrupt Enable Enables an ACMP CPU interrupt. 0 Disable the ACMP Interrupt. 1 Enable the ACMP Interrupt.

Table continues on the next page...

ACMPx_CS field descriptions (continued)

Field	Description
3 ACO	ACMP Output Reading ACO will return the current value of the analog comparator output. ACO is reset to a 0 and will read as a 0 when the ACMP is disabled (ACE = 0)
2 ACOPE	ACMP Output Pin Enable ACOPE enables the pad logic so that the output can be placed onto an external pin. 0 ACMP output cannot be placed onto external pin. 1 ACMP output can be placed onto external pin.
ACMOD	ACMP MOD Determines the sensitivity modes of the interrupt trigger. 00 ACMP interrupt on output falling edge. 01 ACMP interrupt on output rising edge. 10 ACMP interrupt on output falling edge. 11 ACMP interrupt on output falling or rising edge.

22.4.2 ACMP Control Register 0 (ACMPx_C0)

Address: Base address + 1h offset

Bit	7	6	5	4	3	2	1	0
Read	0		ACPSEL		0		ACNSEL	
Write								
Reset	0	0	0	0	0	0	0	0

ACMPx_C0 field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5–4 ACPSEL	ACMP Positive Input Select 00 External reference 0 01 External reference 1 10 External reference 2 11 DAC output
3–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
ACNSEL	ACMP Negative Input Select 00 External reference 0 01 External reference 1 10 External reference 2 11 DAC output

22.4.3 ACMP Control Register 1 (ACMPx_C1)

Address: Base address + 2h offset

Bit	7	6	5	4	3	2	1	0
Read Write	DACEN	DACREF	DACVAL					
Reset	0	0	0	0	0	0	0	0

ACMPx_C1 field descriptions

Field	Description
7 DACEN	DAC Enable Enables the output of 6-bit DAC. 0 The DAC is disabled. 1 The DAC is enabled.
6 DACREF	DAC Reference Select 0 The DAC selects Bandgap as the reference. 1 The DAC selects V_{DDA} as the reference.
DACVAL	DAC Output Level Selection Selects the output voltage using the given formula: V_{output}= (V_{in}/64)x(DACVAL[5:0]+1) The V_{output} range is from V_{in}/64 to V_{in}, the step is V_{in}/64

22.4.4 ACMP Control Register 2 (ACMPx_C2)

Address: Base address + 3h offset

Bit	7	6	5	4	3	2	1	0
Read	0					0	ACIPE	
Write								
Reset	0	0	0	0	0	0	0	0

ACMPx_C2 field descriptions

Field	Description
7–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
ACIPE	ACMP Input Pin Enable This 3-bit field controls if the corresponding ACMP external pin can be driven by an analog input. 0 The corresponding external analog input is not allowed. 1 The corresponding external analog input is allowed.

22.5 Functional description

The ACMP module is functionally composed of two parts: digital-to-analog (DAC) and comparator (CMP).

The DAC includes a 64-level DAC (digital to analog converter) and relevant control logic. DAC can select one of two reference inputs, V_{DD} or on-chip bandgap, as the DAC input V_{in} by setting ACMP_C1[DACREF]. After the DAC is enabled, it converts the data set in ACMP_C1[DACVAL] to a stepped analog output, which is fed into ACMP as an internal reference input. This stepped analog output is also mapped out of the module. The output voltage range is from $V_{in}/64$ to V_{in}. The step size is $V_{in}/64$.

The ACMP can achieve the analog comparison between positive input and negative input, and then give out a digital output and relevant interrupt. Both the positive and negative input of ACMP can be selected from the four common inputs: three external reference inputs and one internal reference input from the DAC output. The positive input of ACMP is selected by ACMP_C0[ACPSEL] and the negative input is selected by ACMP_C0[ACNSEL]. Any pair of the eight inputs can be compared by configuring the ACMPC0 with the appropriate value.

After the ACMP is enabled by setting ACMP_CS[ACE], the comparison result appears as a digital output. Whenever a valid edge defined in ACMP_CS[ACMOD] occurs, ACMP_CS[ACF] is asserted. If ACMP_CS[ACIE] is set, a ACMP CPU interrupt occurs. The valid edge is defined by ACMP_CS[ACMOD]. When ACMP_CS[ACMOD] = 00b or 10b, only the falling-edge on ACMP output is valid. When ACMP_CS[ACMOD] = 01b, only rising-edge on ACMP output is valid. When ACMP_CS[ACMOD] = 11b, both the rising-edge and falling-edge on the ACMP output are valid.

The ACMP output is synchronized by the bus clock to generate ACMP_CS[ACO] so that the CPU can read the comparison. In stop3 mode, if the output of ACMP is changed, ACMPO cannot be updated in time. The output can be synchronized and ACMP_CS[ACO] can be updated upon the waking up of the CPU because of the availability of the bus clock. ACMP_CS[ACO] changes following the comparison result, so it can serve as a tracking flag that continuously indicates the voltage delta on the inputs.

If a reference input external to the chip is selected as an input of ACMP, the corresponding ACMP_C2[ACIPE] bit must be set to enable the input from pad interface. If the output of the ACMP needs to be put onto the external pin, the ACMP_CS[ACOPE] bit must enable the ACMP pin function of pad logic.

22.6 Setup and operation of ACMP

The two parts of ACMP (DAC and CMP) can be set up and operated independently. But if the DAC works as an input of the CMP, the DAC must be configured before the ACMP is enabled.

Because the input-switching can cause problems on the ACMP inputs, the user should complete the input selection before enabling the ACMP and must not change the input selection setting when the ACMP is enabled to avoid unexpected output. Similarly, because the DAC experiences a setup delay after ACMP_C1[DACVAL] is changed, the user should complete the setting of ACMP_C1[DACVAL] before DAC is enabled.

22.7 Resets

During a reset the ACMP is configured in the default mode. Both CMP and DAC are disabled.

22.8 Interrupts

If the bus clock is available when a valid edge defined in ACMP_CS[ACMOD] occurs, the ACMP_CS[ACF] is asserted. If ACMP_CS[ACIE] is set, a ACMP interrupt event occurs. The ACMP_CS[ACF] bit remains asserted until the ACMP interrupt is cleared by software. When in stop3 mode, a valid edge on ACMP output generates an asynchronous interrupt that can wake the MCU from stop3. The interrupt can be cleared by writing a 0 to the ACMP_CS[ACF] bit.

Chapter 23
Operational Amplifier (OPAMP)

23.1 Chip specific OPAMP information

This device has one on-chip fixed gain, single-ended input operational amplifier (OPAMP) module.

23.1.1 Analog supply connections

The VDDA and VSSA power inputs for OPAMP are supplied by VDD and VSS pins respectively on this device.

23.1.2 Default reference voltage

The default OPAMP reference voltage is 1/2 VDDA on this device.

23.1.3 OPAMP inputs

The OPAMP on this device is a single end input amplifier (negative input OPAMP- is tied to GND on chip). The OPAMP+ is available on: PTA3/KBI0P3/TXD0/SCL/ ACMP1IN0/OPAMP+/ADP3

23.1.4 OPAMP outputs

The OPAMP analog output connects internally to ACMP1 or ADC input channel AD12. The OPAMP analog output is not available on an external pin.

23.1.5 OPAMP registers

The OPAMP is controlled by SYS_SOPT6 register.

23.2 Introduction

This chapter introduces the fixed gain operational amplifier (OPAMP) module, which is commonly used as current sense amplifier to sense the current flowing through the external resistor shunt as a voltage across the resistor.

23.3 Features

The OPAMP has the following features:

- x 20 default gain
- 0-100 mV input range
- single-ended or differential input
- gain adjustable with external resistor (only feasible for differential input)

23.4 Block diagram

The following figure show the block diagram of the OPAMP and the interconnections with other modules..

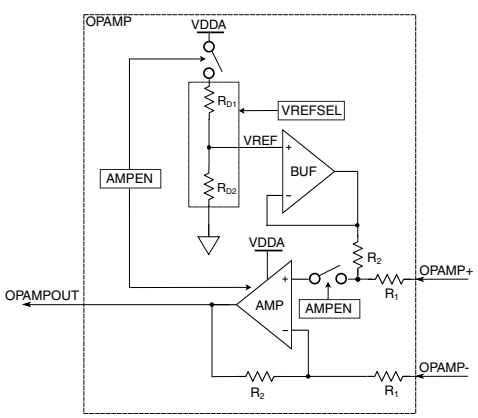


Figure 23-1. OPAMP block diagram

23.5 External signal description

The OPAMP module supports differential input. On some chips, the negative input is internally tied to the ground, thus only single-end positive input OPAMP+ is available. It also requires two supply/ground power pairs connections. The analog power is also used as the OPAMP reference voltage source.

Table 23-1. OPAMP external signal properties

Name	Function
OPAMP+	OPAMP positive input
OPAMP-	OPAMP negative input
OPAMPOUT	OPAMP analog output
VDDA	OPAMP analog power
VSSA	OPAMP analog ground

23.6 Functional description

The operational amplifier normally is used as current sense amplifier to sense the current flowing through the external resistor shunt as a voltage across the resistor. The gain is internally set to 20.

23.6.1 OPAMP Startup

There is a delay ($T_{Start-up}$) from the time the OPAMP is first enabled to when it is available for conversions. The SYS_SOPT6[AMPEN] bit controls the enable or disable of the OPAMP.

23.6.2 OPAMP Reference Voltage

In order to measure both positive and negative currents, an internal reference voltage must be used. This reference voltage VREF is selected from 1/2 VDDA, 1/4 VDDA or 1/8 VDDA and added to positive input of amplifier. The VREF options can be selected by the SYS_SOPT6[VREFSEL].

23.6.3 OPAMP gain adjustment

Although the OPAMP gain is internally set to 20, the gain can be reduced by adding/ cascading external series resistors (R0) on its plus and minus input. To keep the OPAMP output without saturation distortion, the selected R0 must meet the following equation:

OPAMP output=VREF+((R2)/(R1+R0))×V_{shunt}

V_{shunt} is the OPAMP single end input voltage.

The OPAMP gain adjustment only applies for differential input.

Chapter 24
Cyclic redundancy check (CRC)

24.1 Introduction

Cyclic redundancy check (CRC) generates 16/32-bit CRC code for error detection. The CRC can be configured to work as a standard CRC. It provides the user with programmable polynomial, SEED and other parameters required to implement a 16-bit or 32-bit CRC standard. These parameters are detailed in further sections.

24.2 Features

Features of the CRC module are:

- Hardware 16/32-bit CRC generator
- Programmable initial seed value
- Programmable 16/32-bit polynomial
- Optional feature to reverse input and output data by bit
- Optional final complement output of result
- High-speed CRC calculation

24.3 Block diagram

The following figure is the CRC block diagram.

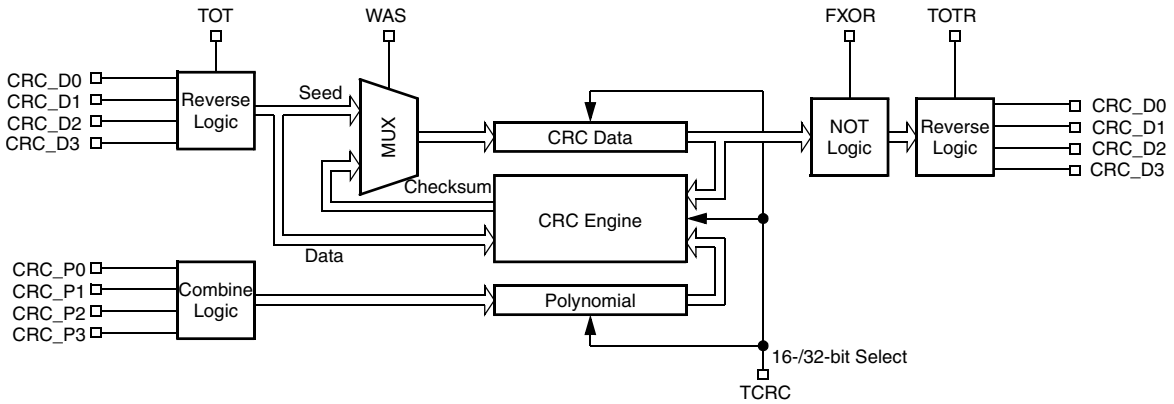


Figure 24-1. Cyclic redundancy check (S08CRC) block diagram

24.4 Modes of operation

This section defines the CRC operation in run, wait, and stop modes.

- Run mode - This is the basic mode of operation in which CRC is full functional.
- Wait mode - The CRC module is optional functional
- Stop3 mode - The CRC module is not functional in this low-power standby state. CRC calculations in progress stop and will resume after the CPU goes into run mode.

24.5 Register definition

CRC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3060	CRC Data 0 Register (CRC_D0)	8	R/W	FFh	24.5.1/397
3061	CRC Data 1 Register (CRC_D1)	8	R/W	FFh	24.5.2/397
3062	CRC Data 2 Register (CRC_D2)	8	R/W	FFh	24.5.3/398
3063	CRC Data 3 Register (CRC_D3)	8	R/W	FFh	24.5.4/399
3064	CRC Polynomial 0 Register (CRC_P0)	8	R/W	00h	24.5.5/399
3065	CRC Polynomial 1 Register (CRC_P1)	8	R/W	00h	24.5.6/400
3066	CRC Polynomial 2 Register (CRC_P2)	8	R/W	10h	24.5.7/400
3067	CRC Polynomial 3 Register (CRC_P3)	8	R/W	21h	24.5.8/401
3068	CRC Control Register (CRC_CTRL)	8	R/W	00h	24.5.9/401

24.5.1 CRC Data 0 Register (CRC_D0)

D0 is one of the CRC data registers (D0:D3). The set of CRC data registers contains the value of seed, data, and checksum. When CRC_CTRL[WAS] bit is set, any write to the data registers is regarded as seed for CRC module. When CRC_CTRL[WAS] bit is clear, any write to the data registers is regarded as data for general CRC computation, in which D0:D2 does not accept any data and D3 accept 8-bit write upon the polynomial configuration. When final data are written, the final result can be read from the data register. The registers of D0:D1 contain the MSB 16-bit of CRC data, which is used only in CRC 32-bit mode. Only D3 is used to dummy data to CRC. Writing D2 will be ignored when WAS = 0.

Address: 3060h base + 0h offset = 3060h

Bit	7	6	5	4	3	2	1	0
Read Write	DH0							
Reset	1	1	1	1	1	1	1	1

CRC_D0 field descriptions

Field	Description
DH0	CRC Data Bit 31:24

24.5.2 CRC Data 1 Register (CRC_D1)

D1 is one of the CRC data registers (D0:D3). The set of CRC data registers contains the value of seed, data, and checksum. When CRC_CTRL[WAS] bit is set, any write to the data registers is regarded as seed for CRC module. When CRC_CTRL[WAS] bit is clear, any write to the data registers is regarded as data for general CRC computation, in which D0:D2 does not accept any data and D3 accept 8-bit write upon the polynomial configuration. When final data are written, the final result can be read from the data register. The registers of D0:D1 contain the MSB 16-bit of CRC data, which is used only in CRC 32-bit mode. Only D3 is used to dummy data to CRC. Writing D2 will be ignored when WAS = 0.

Address: 3060h base + 1h offset = 3061h

Bit	7	6	5	4	3	2	1	0
Read Write	D1							
Reset	1	1	1	1	1	1	1	1

CRC_D1 field descriptions

Field	Description
D1	CRC Data Bit 23:16

24.5.3 CRC Data 2 Register (CRC_D2)

D2 is one of the CRC data registers (D0:D3). The set of CRC data registers contains the value of seed, data, and checksum. When CRC_CTRL[WAS] bit is set, any write to the data registers is regarded as seed for CRC module. When CRC_CTRL[WAS] bit is clear, any write to the data registers is regarded as data for general CRC computation, in which D0:D2 does not accept any data and D3 accept 8-bit write upon the polynomial configuration. When final data are written, the final result can be read from the data register. The registers of D0:D1 contain the MSB 16-bit of CRC data, which is used only in CRC 32-bit mode. Only D3 is used to dummy data to CRC. Writing D2 will be ignored when WAS = 0.

Address: 3060h base + 2h offset = 3062h

Bit	7	6	5	4	3	2	1	0
Read Write	D2							
Reset	1	1	1	1	1	1	1	1

CRC_D2 field descriptions

Field	Description
D2	CRC Data Bit 15:8

24.5.4 CRC Data 3 Register (CRC_D3)

D3 is one of the CRC data registers (D0:D3). The set of CRC data registers contains the value of seed, data, and checksum. When CRC_CTRL[WAS] bit is set, any write to the data registers is regarded as seed for CRC module. When CRC_CTRL[WAS] bit is clear, any write to the data registers is regarded as data for general CRC computation, in which D0:D2 does not accept any data and D3 accept 8-bit write upon the polynomial configuration. When final data are written, the final result can be read from the data register. The registers of D0:D1 contain the MSB 16-bit of CRC data, which is used only in CRC 32-bit mode. Only D3 is used to dummy data to CRC. Writing D2 will be ignored when WAS = 0.

Address: 3060h base + 3h offset = 3063h

Bit	7	6	5	4	3	2	1	0
Read Write	D3							
Reset	1	1	1	1	1	1	1	1

CRC_D3 field descriptions

Field	Description
D3	CRC Data Bit 7:0

24.5.5 CRC Polynomial 0 Register (CRC_P0)

P0 is one of the CRC polynomial registers (P0:P3). The set of CRC polynominal registers contains the value of polynomial. The registers of P0:P1 contain the MSB 16-bit of CRC polynomial, which is used only in CRC 32-bit mode. The registers of P2:P3 contain the LSB 16-bit of CRC polynomial, which is used in both CRC 16- and 32-bit modes.

Address: 3060h base + 4h offset = 3064h

Bit	7	6	5	4	3	2	1	0
Read Write	P0							
Reset	0	0	0	0	0	0	0	0

CRC_P0 field descriptions

Field	Description
P0	CRC Polynominal Bit 31:24

24.5.6 CRC Polynomial 1 Register (CRC_P1)

P1 is one of the CRC polynomial registers (P0:P3). The set of CRC polynominal registers contains the value of polynomial. The registers of P0:P1 contain the MSB 16-bit of CRC polynomial, which is used only in CRC 32-bit mode. The registers of P2:P3 contain the LSB 16-bit of CRC polynomial, which is used in both CRC 16- and 32-bit modes.

Address: 3060h base + 5h offset = 3065h

Bit	7	6	5	4	3	2	1	0
Read Write	P1							
Reset	0	0	0	0	0	0	0	0

CRC_P1 field descriptions

Field	Description
P1	CRC Polynominal Bit 23:16

24.5.7 CRC Polynomial 2 Register (CRC_P2)

P2 is one of the CRC polynomial registers (P0:P3). The set of CRC polynominal registers contains the value of polynomial. The registers of P0:P1 contain the MSB 16-bit of CRC polynomial, which is used only in CRC 32-bit mode. The registers of P2:P3 contain the LSB 16-bit of CRC polynomial, which is used in both CRC 16- and 32-bit modes.

Address: 3060h base + 6h offset = 3066h

Bit	7	6	5	4	3	2	1	0
Read Write	P2							
Reset	0	0	0	1	0	0	0	0

CRC_P2 field descriptions

Field	Description
P2	CRC Polynominal Bit 15:8

24.5.8 CRC Polynomial 3 Register (CRC_P3)

P3 is one of the CRC polynomial registers (P0:P3). The set of CRC polynominal registers contains the value of polynomial. The registers of P0:P1 contain the MSB 16-bit of CRC polynomial, which is used only in CRC 32-bit mode. The registers of P2:P3 contain the LSB 16-bit of CRC polynomial, which is used in both CRC 16- and 32-bit modes.

Address: 3060h base + 7h offset = 3067h

Bit	7	6	5	4	3	2	1	0
Read Write	P3							
Reset	0	0	1	0	0	0	0	1

CRC_P3 field descriptions

Field	Description
P3	CRC Polynominal Bit 7:0

24.5.9 CRC Control Register (CRC_CTRL)

Address: 3060h base + 8h offset = 3068h

Bit	7	6	5	4	3	2	1	0
Read	TOT		TOTR		0	FXOR	WAS	TCRC
Write								
Reset	0	0	0	0	0	0	0	0

CRC_CTRL field descriptions

Field	Description
7–6 TOT	Reverse of Write These bits identify the reverse of the input data. 00 No reverse. 01 Bit is reversed in byte; No byte is reversed. 10 Reserved. 11 Reserved.
5–4 TOTR	Reverse of Read These bits identify the reverse of the output data. 00 No reverse. 01 Bit is reversed in byte; No byte is reversed. 10 Reserved. 11 Reserved.

Table continues on the next page...

CRC_CTRL field descriptions (continued)

Field	Description
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 FXOR	Complement of Read This bit allows CRC module to output the complement of the final CRC checksum. 0 Normal checksum output. 1 Complement of checksum output.
1 WAS	Write CRC data register as seed This bit indicates the data written to the CRC data register (D0:D3) is seed or data. 0 Data is written in data registers. 1 Seed is written in data registers.
0 TCRC	Width of Polynomial Generator This bit indicates the bit width of the polynomial generator. 0 16-bit CRC Polynomial Generator. 1 32-bit CRC Polynomial Generator.

24.6 Functional description

24.6.1 16-bit CRC calculation

The following steps show how to start a general 16-bit CRC calculation:

1. Clear CRC_CTRL[TCRC] bit to enable 16-bit CRC mode.
2. Optional to enable reverse and complement function. Please see Bit reverse and Result complement for details.
3. Write 16-bit polynomial to CRC_P2:CRC_P3.
4. Set CRC_CTRL[WAS] bit to allow CRC_D2:CRC_D3 to be written by seed.
5. Write 16-bit seed to CRC_D2:CRC_D3.
6. Clear CRC_CTRL[WAS] bit to start 16-bit CRC calculation.
7. Dummy CRC_D3 with 8-bit CRC raw data.
8. Get the checksum from CRC_D2:CRC_D3 when all CRC raw data dummied.

24.6.2 32-bit CRC calculation

The following steps show how to start a general 32-bit CRC calculation:

1. Set CRC_CTRL[TCRC] bit to enable 32-bit CRC mode.

2. Optional to enable reverse and complement function. Please see Bit reverse and Result complement for details.
3. Write 32-bit polynomial to CRC_P0:CRC_P3.
4. Set CRC_CTRL[WAS] bit to allow CRC_D0:CRC_D3 written by seed.
5. Write 32-bit seed to CRC_D0:CRC_D3.
6. Clear CRC_CTRL[WAS] bit to start 32-bit CRC calculation.
7. Dummy CRC_D3 with 8-bit CRC raw data.
8. Get the checksum from CRC_D0:CRC_D3 when all CRC raw data dummied.

24.6.3 Bit reverse

The bit reverse function allows the input and output data reversed by bit for different CRC standard and endian systems. The CRC_CTRL[TOT] bits control the reverse of input data and the CRC_CTRL[TOTR] bits control the reverse of output data. The following table shows how the CRC_CTRL[TOT] and CRC_CTRL[TOTR] bits work.

Table 24-1. TOT and TOTR bit and byte reverse function

TOT ROW	D0	D1	D2	D3
00	b31b30b29b28b27b26b25b24	b23b22b21b20b19b18b17b16	b15b14b13b12b11b10b9b8	b7b6b5b4b3b2b1b0
01	b24b25b26b27b28b29b30b31	b16b17b18b19b20b21b22b23	b8b9b10b11b12b13b14b15	b0b1b2b3b4b5b6b7

NOTE

00 is the default case that no bit is reversed.

24.6.4 Result complement

The result complement function allows to output the complement of the checksum in CRC data registers. When CRC_CTRL[FXOR] bit is set, the checksum is read by its complement. Otherwise, the raw checksum is accessed.

24.6.5 CCITT compliant CRC example

The following code segment shows CCITT CRC-16 compliant example.

Example: 24.6.5.1 CCITT CRC-16 compliant example

```
CRC_CTRL = CRC_CTRL_WAS_MASK; // 16-bit CRC, ready to dummy seed
CRC_P2P3 = 0x1021; // Standard CCITT polynomail of (x^16 + x^12 + x^5 + 1)
CRC_D2D3 = 0xFFFF; // Set seed by 0xFFFF
CRC_CTRL = 0x00;

for ( i = 0 ; i < 128 ; i++ )
{
CRC_D3 = 'A'; // Dummy 256 `A'
CRC_D3 = 'A';
}

// Get 0xea0b in CRC_D2:CRC_D3 here
```

Chapter 25
Fault Detection and Shutdown (FDS)

25.1 Chip specific FDS information

This device has the fault detect and shutdown (FDS) module provides a mechanism to immediately place port pins in a pre-defined state when a fault condition occurs. Table 25-1 and Table 25-2 is the input fault and output control configuration of FDS in this device.

Table 25-1. Input configuration

Input Fault Channel	Source	Description
FIN0	KBIINT	KBI interrupt output
FIN1	ACMP0INT	ACMP0 interrupt output
FIN2	ACMP1INT	ACMP1 interrupt output
FIN3	MTIM0INT	MTIM0 interrupt output
FIN4	MTIM1INT	MTIM1 interrupt output
FIN5	PWTRDY	PWT interrupt output
FIN6	FDSIN	FDS external fault input
FIN7	Active BDM	Active BDM mode

Table 25-2. Output configuration

Output Control Channel	Output Controlled Function
FDSOUT0	PTC0/FTM2CH0
FDSOUT1	PTC1/FTM2CH1
FDSOUT2	PTC2/FTM2CH2
FDSOUT3	PTC3/FTM2CH3
FDSOUT4	PTB4/FTM2CH4
FDSOUT5	PTB5/FTM2CH5
FDSOUT6	PTA0/KBI0P0/FTM0CH0
FDSOUT7	PTA1/KBI0P1/FTM0CH1

NOTE

FDS should take higher priority than FTM software controlled output.

25.2 Introduction

The fault detect and shutdown (FDS) module provides a mechanism to immediately place port pins in a pre-defined state when a fault condition occurs. The module is configurable with up to eight fault input sources and control of up to eight port pins.

25.2.1 Features

The FDS has the following features:

- Eight fault inputs
  - Hard configured to signals for each MCU
- Single bit software controlled fault input
- Control of up to eight outputs, upon fault event trigger 8 pins can be independently configured
  - High impedance
  - An output driven high
  - An output driven low
  - Ignore fault event
- Optional Interrupt request generated when fault occurs

25.2.2 Modes of operation

25.2.2.1 Run mode

When enabled, the FDS will monitor the eight input signals and place the associated port pins in a programmable determined state if an enabled fault source is active. The pin will remain under control of the FDS until the occurrence of one of the following three conditions: the fault is removed and the FDF bit is cleared; the FDS module is disabled; or the FPCE bit is cleared.

The default state of the module is disabled. In the disabled state, the module has no impact on port control and no interrupts are generated.

25.2.2.2 Wait mode

The FDS module remains active when the MCU is in wait mode, and functionality will be identical to when the MCU is in run mode.

25.2.2.3 Stop mode

In stop3 mode, the FDS module can't respond to any fault source and no interrupt can be generated. If the pin outputs are already under the control of FDS module when MCU enters stop3 mode, these pins will hold the states that they were before stop3 entry. After the waking up of MCU from stop3 mode by interrupt, the FDS module resumes the capability of responding to fault source with the setting before stop3 entry.

25.2.2.4 Active background mode

In order to protect external circuitry, the FDS remains active in active BDM and can be configured to force a fault upon the entry of active BDM.

25.2.3 Block diagram

The following figure show the block diagram of the FDS.

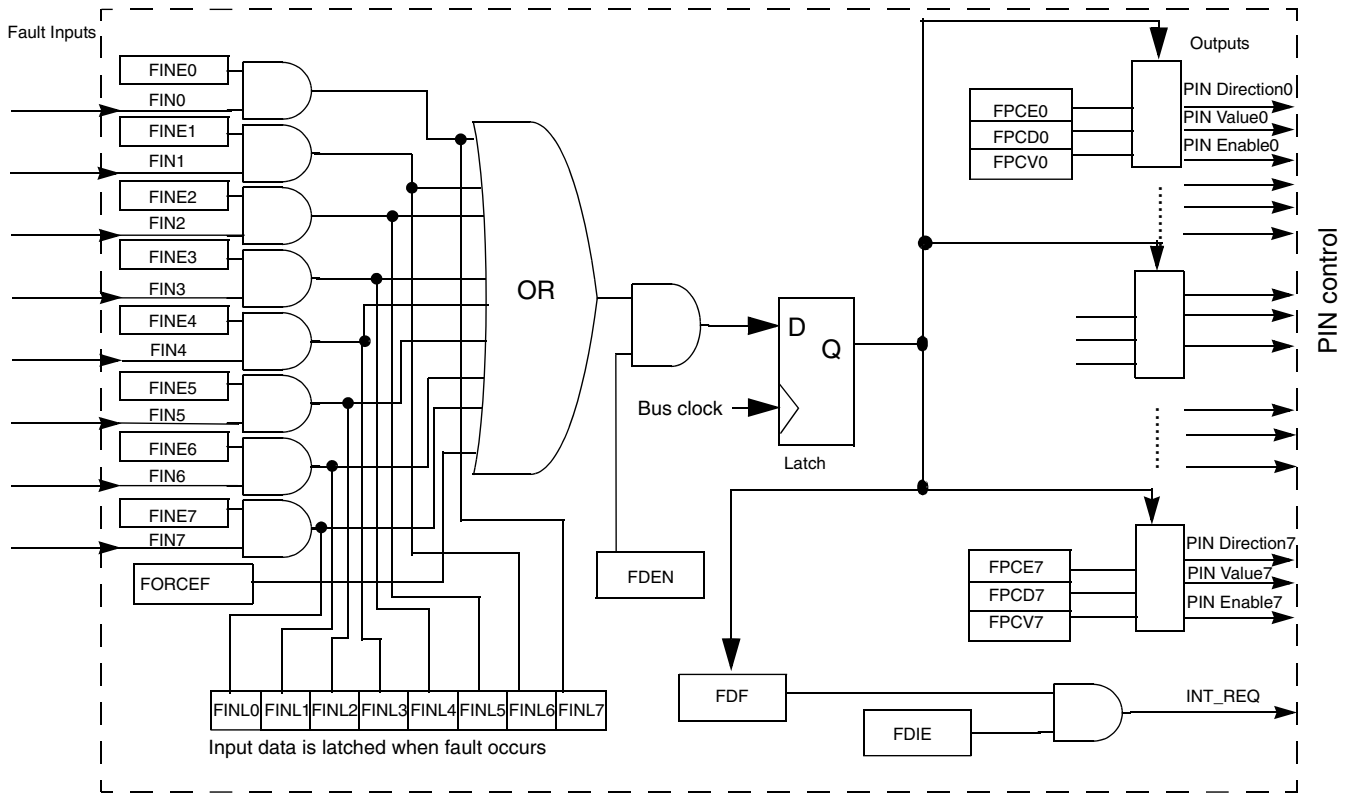


Figure 25-1. FDS block diagram

25.3 FDS Registers

FDS memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
30DD	FDS Control and Status Register (FDS_CS)	8	R/W	00h	25.3.1/409
30DE	FDS Input Enable Register (FDS_INE)	8	R/W	00h	25.3.2/410
30DF	FDS Pin Configuration Enable Register (FDS_PCE)	8	R/W	00h	25.3.3/411
30E0	FDS Pin Configuration Direction Register (FDS_PCD)	8	R/W	00h	25.3.4/412
30E1	FDS Pin Configuration Value Register (FDS_PCV)	8	R/W	00h	25.3.5/414
30E2	FDS Input Latched Register (FDS_INL)	8	R/W	00h	25.3.6/415

25.3.1 FDS Control and Status Register (FDS_CS)

This register contains the fault detect status flag and control bits which are used to configure the interrupt enable, enable the module, and force a fault.

Address: 30DDh base + 0h offset = 30DDh

Bit	7	6	5	4	3	2	1	0
Read	FDF	FDIE	FDEN	0	0			
Write				FORCEF				
Reset	0	0	0	0	0	0	0	0

FDS_CS field descriptions

Field	Description
7 FDF	FDS Flag This bit is set when the FDS receives an active fault input on an enabled channel. If FORCEF reset occurs, this bit is also asserted. Clear FDF by reading the FDS_CS register while FDF is set, then writing a 0 to FDF. Writing a 1 has no effect. 0 No enabled fault inputs are active. 1 An enabled fault input is active.
6 FDIE	FDS Interrupt Enable This read/write bit enables FDS interrupt. If FDIE is set, then an interrupt is generated when an active fault inputs on a channel that is enabled and FDF is set to 1. Reset clears FDIE. Do not set FDIE if FDF = 1. Clear FDF first, then set FDIE. 0 Fault detection interrupts are disabled. Use software polling. 1 Fault detection interrupts are enabled.
5 FDEN	FDS Enable This read/write bit enables the entire module. All other control bits should be configured prior to setting this bit. 0 Module is disabled. Pin control is not conditioned by the FDS module. 1 Module is enabled.
4 FORCEF	FDS Force Fault Writing a one to this bit forces a fault input and the module reacts as when an external fault input is detected. Writing 1 to FORCE also asserts FDF bit. Read this bit always returns a 0. 0 No fault forced on FDS. 1 FDS fault forced.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

25.3.2 FDS Input Enable Register (FDS_INE)

FDS_INE contains the bits to enable each of the 8 optional fault inputs.

Address: 30DDh base + 1h offset = 30DEh

Bit	7	6	5	4	3	2	1	0
Read Write	FINE7	FINE6	FINE5	FINE4	FINE3	FINE2	FINE1	FINE0
Reset	0	0	0	0	0	0	0	0

FDS_INE field descriptions

Field	Description
7 FINE7	FDS Input 7 Enable These bit provides independent and dynamic control for input fault source 7. 0 Fault input 7 is disabled. 1 Fault input 7 is enabled.
6 FINE6	FDS Input 6 Enable These bit provides independent and dynamic control for input fault source 6. 0 Fault input 6 is disabled. 1 Fault input 6 is enabled.
5 FINE5	FDS Input 5 Enable These bit provides independent and dynamic control for input fault source 5. 0 Fault input 5 is disabled. 1 Fault input 5 is enabled.
4 FINE4	FDS Input 4 Enable These bit provides independent and dynamic control for input fault source 4. 0 Fault input 4 is disabled. 1 Fault input 4 is enabled.
3 FINE3	FDS Input 3 Enable These bit provides independent and dynamic control for input fault source 3. 0 Fault input 3 is disabled. 1 Fault input 3 is enabled.
2 FINE2	FDS Input 2 Enable These bit provides independent and dynamic control for input fault source 2. 0 Fault input 2 is disabled. 1 Fault input 2 is enabled.
1 FINE1	FDS Input 1 Enable These bit provides independent and dynamic control for input fault source 1.

Table continues on the next page...

FDS_INE field descriptions (continued)

Field	Description
	0 Fault input 1 is disabled. 1 Fault input 1 is enabled.
0 FINE0	FDS Input 0 Enable These bit provides independent and dynamic control for input fault source 0. 0 Fault input 0 is disabled. 1 Fault input 0 is enabled.

25.3.3 FDS Pin Configuration Enable Register (FDS_PCE)

This register provides independent and dynamic control of all 8 output pins.

Address: 30DDh base + 2h offset = 30DFh

Bit	7	6	5	4	3	2	1	0
Read Write	FPCE7	FPCE6	FPCE5	FPCE4	FPCE3	FPCE2	FPCE1	FPCE0
Reset	0	0	0	0	0	0	0	0

FDS_PCE field descriptions

Field	Description
7 FPCE7	FDSOUT7 Pin Configuration Enable This field enables/disables FDSOUT7 function. Reset clears this bit. 0 The FDSOUT7 function is bypassed in the corresponding output pin. The output pin functions just as the module input. 1 The FDSOUT7 function is enabled in the corresponding output pin and the output pin can be configured as setting in FDS_PCD and FDS_PCV registers.
6 FPCE6	FDSOUT6 Pin Configuration Enable This field enables/disables FDSOUT6 function. Reset clears this bit. 0 The FDSOUT6 function is bypassed in the corresponding output pin. The output pin functions just as the module input. 1 The FDSOUT6 function is enabled in the corresponding output pin and the output pin can be configured as setting in FDS_PCD and FDS_PCV registers.
5 FPCE5	FDSOUT5 Pin Configuration Enable This field enables/disables FDSOUT5 function. Reset clears this bit. 0 The FDSOUT5 function is bypassed in the corresponding output pin. The output pin functions just as the module input. 1 The FDSOUT5 function is enabled in the corresponding output pin and the output pin can be configured as setting in FDS_PCD and FDS_PCV registers.
4 FPCE4	FDSOUT4 Pin Configuration Enable

Table continues on the next page...

FDS_PCE field descriptions (continued)

Field	Description
	This field enables/disables FDSOUT4 function. Reset clears this bit. 0 The FDSOUT4 function is bypassed in the corresponding output pin. The output pin functions just as the module input. 1 The FDSOUT4 function is enabled in the corresponding output pin and the output pin can be configured as setting in FDS_PCD and FDS_PCV registers.
3 FPCE3	FDSOUT3 Pin Configuration Enable This field enables/disables FDSOUT3 function. Reset clears this bit. 0 The FDSOUT3 function is bypassed in the corresponding output pin. The output pin functions just as the module input. 1 The FDSOUT3 function is enabled in the corresponding output pin and the output pin can be configured as setting in FDS_PCD and FDS_PCV registers.
2 FPCE2	FDSOUT2 Pin Configuration Enable This field enables/disables FDSOUT2 function. Reset clears this bit. 0 The FDSOUT2 function is bypassed in the corresponding output pin. The output pin functions just as the module input. 1 The FDSOUT2 function is enabled in the corresponding output pin and the output pin can be configured as setting in FDS_PCD and FDS_PCV registers.
1 FPCE1	FDSOUT1 Pin Configuration Enable This field enables/disables FDSOUT1 function. Reset clears this bit. 0 The FDSOUT1 function is bypassed in the corresponding output pin. The output pin functions just as the module input. 1 The FDSOUT1 function is enabled in the corresponding output pin and the output pin can be configured as setting in FDS_PCD and FDS_PCV registers.
0 FPCE0	FDSOUT0 Pin Configuration Enable This field enables/disables FDSOUT0 function. Reset clears this bit. 0 The FDSOUT0 function is bypassed in the corresponding output pin. The output pin functions just as the module input. 1 The FDSOUT0 function is enabled in the corresponding output pin and the output pin can be configured as setting in FDS_PCD and FDS_PCV registers.

25.3.4 FDS Pin Configuration Direction Register (FDS_PCD)

PCD provides independent and dynamic control of all 8 output pins. This register can be read or write.

Address: 30DDh base + 3h offset = 30E0h

Bit	7	6	5	4	3	2	1	0
Read Write	FPCD7	FPCD6	FPCD5	FPCD4	FPCD3	FPCD2	FPCD1	FPCD0
Reset	0	0	0	0	0	0	0	0

FDS_PCD field descriptions

Field	Description
7 FPCD7	FDSOUT7 Pin Configuration Direction This field controls the direction of output pin FDSOUT7 when corresponding FPCE bit is set. Reset clears this bit. 0 Output pin FDSOUT7 set as high impedance. 1 Output pin FDSOUT7 set as output.
6 FPCD6	FDSOUT6 Pin Configuration Direction This field controls the direction of output pin FDSOUT6 when corresponding FPCE bit is set. Reset clears this bit. 0 Output pin FDSOUT6 set as high impedance. 1 Output pin FDSOUT6 set as output.
5 FPCD5	FDSOUT5 Pin Configuration Direction This field controls the direction of output pin FDSOUT5 when corresponding FPCE bit is set. Reset clears this bit. 0 Output pin FDSOUT5 set as high impedance. 1 Output pin FDSOUT5 set as output.
4 FPCD4	FDSOUT4 Pin Configuration Direction This field controls the direction of output pin FDSOUT4 when corresponding FPCE bit is set. Reset clears this bit. 0 Output pin FDSOUT4 set as high impedance. 1 Output pin FDSOUT4 set as output.
3 FPCD3	FDSOUT3 Pin Configuration Direction This field controls the direction of output pin FDSOUT3 when corresponding FPCE bit is set. Reset clears this bit. 0 Output pin FDSOUT3 set as high impedance. 1 Output pin FDSOUT3 set as output.
2 FPCD2	FDSOUT2 Pin Configuration Direction This field controls the direction of output pin FDSOUT2 when corresponding FPCE bit is set. Reset clears this bit. 0 Output pin FDSOUT2 set as high impedance. 1 Output pin FDSOUT2 set as output.
1 FPCD1	FDSOUT1 Pin Configuration Direction This field controls the direction of output pin FDSOUT1 when corresponding FPCE bit is set. Reset clears this bit. 0 Output pin FDSOUT1 set as high impedance. 1 Output pin FDSOUT1 set as output.
0 FPCD0	FDSOUT0 Pin Configuration Direction

Table continues on the next page...

FDS_PCD field descriptions (continued)

Field	Description
	This field controls the direction of output pin FDSOUT0 when corresponding FPCE bit is set. Reset clears this bit. 0 Output pin FDSOUT0 set as high impedance. 1 Output pin FDSOUT0 set as output.

25.3.5 FDS Pin Configuration Value Register (FDS_PCV)

PCV provides independent and dynamic drive state control to all enabled and configured as output pins.

Address: 30DDh base + 4h offset = 30E1h

Bit	7	6	5	4	3	2	1	0
Read Write	FPCV7	FPCV6	FPCV5	FPCV4	FPCV3	FPCV2	FPCV1	FPCV0
Reset	0	0	0	0	0	0	0	0

FDS_PCV field descriptions

Field	Description
7 FPCV7	FDSOUT7 Pin Configuration Direction This field gives the output value of FDSOUT7 when the output pin configuration is enabled and the pin is configured as output. 0 Output pin FDSOUT7 is driven a 0. 1 Output pin FDSOUT7 is driven a 1.
6 FPCV6	FDSOUT6 Pin Configuration Direction This field gives the output value of FDSOUT6 when the output pin configuration is enabled and the pin is configured as output. 0 Output pin FDSOUT6 is driven a 0. 1 Output pin FDSOUT6 is driven a 1.
5 FPCV5	FDSOUT5 Pin Configuration Direction This field gives the output value of FDSOUT5 when the output pin configuration is enabled and the pin is configured as output. 0 Output pin FDSOUT5 is driven a 0. 1 Output pin FDSOUT5 is driven a 1.
4 FPCV4	FDSOUT4 Pin Configuration Direction This field gives the output value of FDSOUT4 when the output pin configuration is enabled and the pin is configured as output. 0 Output pin FDSOUT4 is driven a 0. 1 Output pin FDSOUT4 is driven a 1.

Table continues on the next page...

FDS_PCV field descriptions (continued)

Field	Description
3 FPCV3	FDSOUT3 Pin Configuration Direction This field gives the output value of FDSOUT3 when the output pin configuration is enabled and the pin is configured as output. 0 Output pin FDSOUT3 is driven a 0. 1 Output pin FDSOUT3 is driven a 1.
2 FPCV2	FDSOUT2 Pin Configuration Direction This field gives the output value of FDSOUT2 when the output pin configuration is enabled and the pin is configured as output. 0 Output pin FDSOUT2 is driven a 0. 1 Output pin FDSOUT2 is driven a 1.
1 FPCV1	FDSOUT1 Pin Configuration Direction This field gives the output value of FDSOUT1 when the output pin configuration is enabled and the pin is configured as output. 0 Output pin FDSOUT1 is driven a 0. 1 Output pin FDSOUT1 is driven a 1.
0 FPCV0	FDSOUT0 Pin Configuration Direction This field gives the output value of FDSOUT0 when the output pin configuration is enabled and the pin is configured as output. 0 Output pin FDSOUT0 is driven a 0. 1 Output pin FDSOUT0 is driven a 1.

25.3.6 FDS Input Latched Register (FDS_INL)

Address: 30DDh base + 5h offset = 30E2h

Bit	7	6	5	4	3	2	1	0
Read Write	FINL7	FINL6	FINL5	FINL4	FINL3	FINL2	FINL1	FINL0
Reset	0	0	0	0	0	0	0	0

FDS_INL field descriptions

Field	Description
7 FINL7	FIN7 latched input data This field latches the status of the fault input line 7 when a fault occurs. Whenever a fault occurs in the FIN7, it will be latched into the FINL7 bit until this bit is cleared. If several faults occur before the reading of FDS_INL, the read value of FDS_INL will reflect all the fault sources. This register is cleared by chip reset or by reading followed by writing 0. Writing 1 has not effect. 0 FIN7 pin was low at time of last fault trigger. 1 FIN7 pin was high at time of last fault trigger.

Table continues on the next page...

FDS_INL field descriptions (continued)

Field	Description
6 FINL6	FIN6 latched input data This field latches the status of the fault input line 6 when a fault occurs. Whenever a fault occurs in the FIN6, it will be latched into the FINL6 bit until this bit is cleared. If several faults occur before the reading of FDS_INL, the read value of FDS_INL will reflect all the fault sources. This register is cleared by chip reset or by reading followed by writing 0. Writing 1 has not effect. 0 FIN6 pin was low at time of last fault trigger. 1 FIN6 pin was high at time of last fault trigger.
5 FINL5	FIN5 latched input data This field latches the status of the fault input line 5 when a fault occurs. Whenever a fault occurs in the FIN5, it will be latched into the FINL5 bit until this bit is cleared. If several faults occur before the reading of FDS_INL, the read value of FDS_INL will reflect all the fault sources. This register is cleared by chip reset or by reading followed by writing 0. Writing 1 has not effect. 0 FIN5 pin was low at time of last fault trigger. 1 FIN5 pin was high at time of last fault trigger.
4 FINL4	FIN4 latched input data This field latches the status of the fault input line 4 when a fault occurs. Whenever a fault occurs in the FIN4, it will be latched into the FINL4 bit until this bit is cleared. If several faults occur before the reading of FDS_INL, the read value of FDS_INL will reflect all the fault sources. This register is cleared by chip reset or by reading followed by writing 0. Writing 1 has not effect. 0 FIN4 pin was low at time of last fault trigger. 1 FIN4 pin was high at time of last fault trigger.
3 FINL3	FIN3 latched input data This field latches the status of the fault input line 3 when a fault occurs. Whenever a fault occurs in the FIN3, it will be latched into the FINL3 bit until this bit is cleared. If several faults occur before the reading of FDS_INL, the read value of FDS_INL will reflect all the fault sources. This register is cleared by chip reset or by reading followed by writing 0. Writing 1 has not effect. 0 FIN3 pin was low at time of last fault trigger. 1 FIN3 pin was high at time of last fault trigger.
2 FINL2	FIN2 latched input data This field latches the status of the fault input line 2 when a fault occurs. Whenever a fault occurs in the FIN2, it will be latched into the FINL2 bit until this bit is cleared. If several faults occur before the reading of FDS_INL, the read value of FDS_INL will reflect all the fault sources. This register is cleared by chip reset or by reading followed by writing 0. Writing 1 has not effect. 0 FIN2 pin was low at time of last fault trigger. 1 FIN2 pin was high at time of last fault trigger.
1 FINL1	FIN1 latched input data This field latches the status of the fault input line 1 when a fault occurs. Whenever a fault occurs in the FIN1, it will be latched into the FINL1 bit until this bit is cleared. If several faults occur before the reading of FDS_INL, the read value of FDS_INL will reflect all the fault sources. This register is cleared by chip reset or by reading followed by writing 0. Writing 1 has not effect.

Table continues on the next page...

FDS_INL field descriptions (continued)

Field	Description
	0 FIN1 pin was low at time of last fault trigger. 1 FIN1 pin was high at time of last fault trigger.
0 FINL0	FIN0 latched input data This field latches the status of the fault input line 0 when a fault occurs. Whenever a fault occurs in the FIN0, it will be latched into the FINL0 bit until this bit is cleared. If several faults occur before the reading of FDS_INL, the read value of FDS_INL will reflect all the fault sources. This register is cleared by chip reset or by reading followed by writing 0. Writing 1 has not effect. 0 FIN0 pin was low at time of last fault trigger. 1 FIN0 pin was high at time of last fault trigger.

25.4 Functional description

The FDS provides rapid shutdown for up to 8 pins when a fault input activated. Due to the synchronous design of the FDS module, there is up to 1 bus clock of delay from the fault occurrence to the shut down of the output pin.

The module can be broken down into three pieces: input enable configuration, action taken upon fault and output control.

25.4.1 Input enable configuration

Each input signal can be enabled independently. All the inputs are synchronous signals. The fault inputs are latched into the FDSINL register.

25.4.2 Action taken upon fault

When a fault is detected, it is latched as FDF (fault detection flag) by bus clock if the corresponding fault input is enabled. At the same time, the output pins are shut down and driven to the states based on the setting in FDS_PCE, FDS_PCD and FDS_PCV. An interrupt is generated if it is enabled. Until the FDF is cleared, the pins keep shutting down state.

25.4.3 Output control

The output pin of FDS can be configured as output 1, output 0, high impedance and bypass based on the setting in PCE, PCD and PCV. When the FDS module is disabled, all the output pins are in bypass mode. The FDS module is independent with any other modules. That is to say, if a FDS output is used to shut down a PWM channel, the FDS output pin can be set to any intended value(1, 0 or high impedance) upon a fault detection even the PWM channel is not active. When the fault source is removed and the FDF is cleared, the FDS module will release the control on corresponding pin for PWM or other functions. Table 25-3 lists the output control configuration and Figure 25-2 illustrates the output control realization.

Table 25-3. Output control configuration

FDEN	FPCE	FPCD	FPCV	The pin state
1	0	x	x	The FDS control is bypassed, the output comes from pin other functions
1	1	1	0	Pin outputs a 0 during shutdown
1	1	1	1	Pin outputs a 1 during shutdown
1	1	0	x	High impedance during shutdown
0	x	x	x	The FDS control is bypassed, the output comes from pin other functions

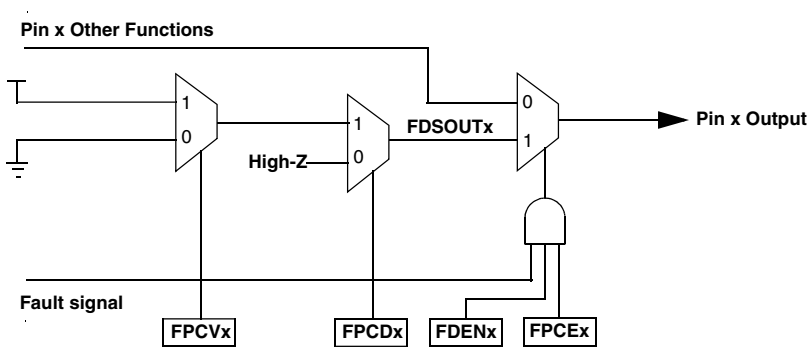


Figure 25-2. FDS output realization

25.5 FDS interrupt operation

If the FDS interrupt is enabled, any fault occurrence can cause an interrupt if the interrupt is enabled. The interrupt can be cleared by reading FDSCS followed by clearing FDF. If a new fault occurs after the FDF is read but before it is cleared, the FDF will not be cleared.

25.6 FDS operation example

This section shows an example of the FDS operation in a hypothetical system example.

25.6.1 Example system configuration

Table 25-4. Input configuration example

	FINEx Content	Source	Notes
0	1	KBI interrupt output	KBI interrupt is used to external shutdown control
1	1	ACMP0 interrupt output	ACMP0 is used to sense overcurrent in load
2	0	ACMP1 interrupt output	ACMP1 is used to sense open circuit on one of the symmetric loads (Not used for this particular system)
3	0	MTIM0 interrupt output	Not used for this particular system configuration
4	1	MTIM1 interrupt output	MTIM1 is used as a software watchdog
5	1	PWT interrupt output	PWT is used to catch external pulses.
6	0	FDS external fault input	Not used for this particular chip
7	1	Active BDM mode	When debugging the system with breakpoints, a fault will be generated when program execution halts for debugging.

Table 25-5. Output configuration

	FDEN	FPCE	FPCD	FPCV	Output	Notes
0	1	1	1	1	FDSOUT0	The channel is shut down and

Table continues on the next page...

Table 25-5. Output configuration (continued)

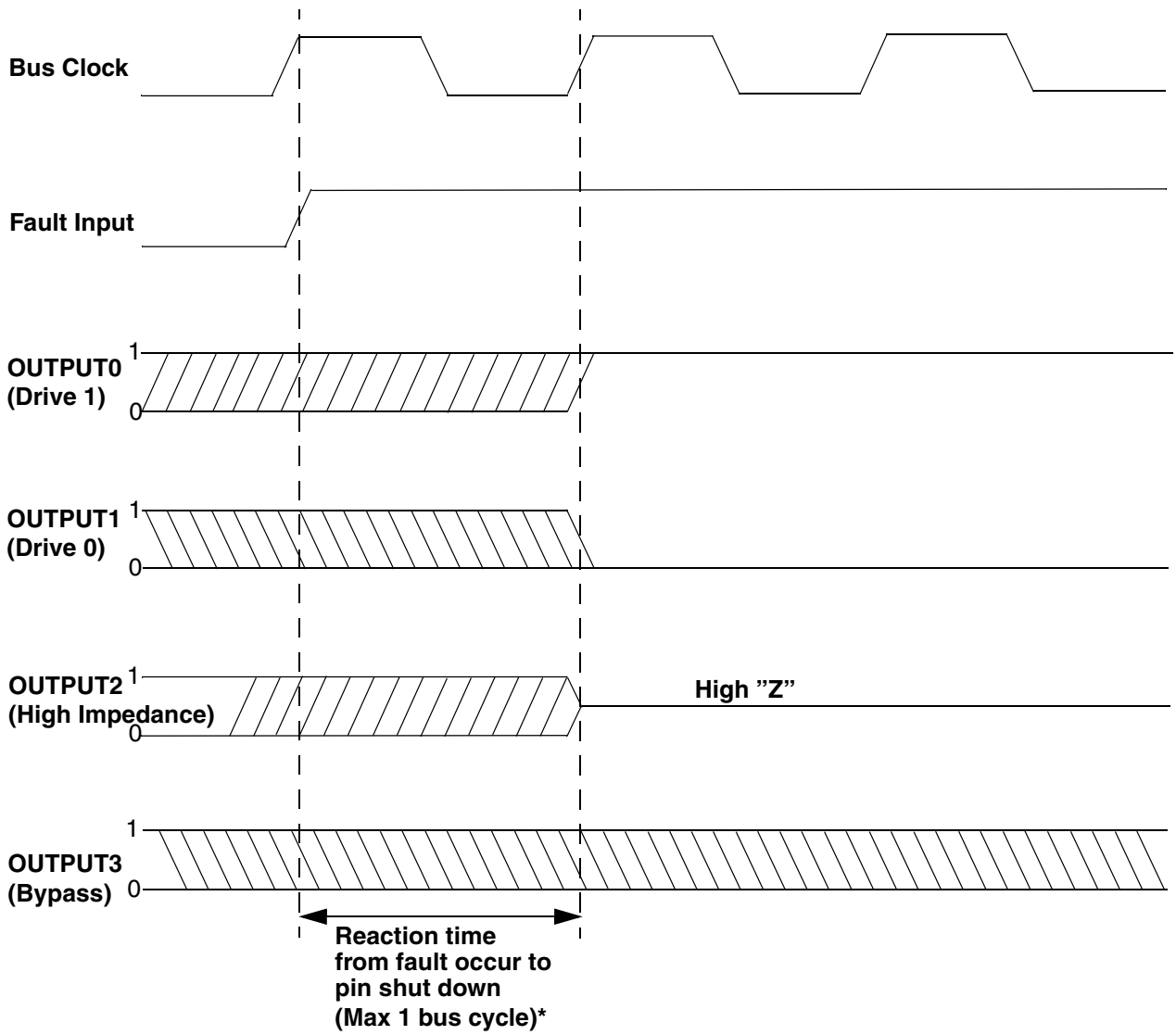
	FDEN	FPCE	FPCD	FPCV	Output	Notes
						the pin is output and driven 1
1	1	1	1	0	FDSOUT1	The channel is shut down and the pin is output and driven 0
2	1	1	0	1	FDSOUT2	The channel is shut down and the pin is high impedance
3	0	1	0	1	FDSOUT3	The channel is bypassed and the pin outputs other functions
4	0	1	1	0	FDSOUT4	The channel is bypassed and the pin outputs other functions
5	1	0	1	1	FDSOUT5	The channel is bypassed and the pin outputs other functions
6	1	1	0	0	FDSOUT6	The channel is shut down and the pin is high impedance
7	1	0	0	0	Not connected	This channel has no meaning in this particular chip

Table 25-6. Status and control

Bit Position	Bit Name	Content	Bit Meaning	Notes
0	FDF	1	Status Flag	Indicates the detection of a fault, a interrupt can be generated if the interrupt is enabled
1	FDIE	0	Interrupts enabled	Enable FDS to generate a interrupt upon the fault detection
2	FDEN	1	Module enabled	Enable FDS module function, the outputs are bypassed
3	FORCEF	Writing 1	Force Fault	Generate a forced fault pulse, FDF is set when this bit is written 1.

25.6.2 Example fault detection and shutdown Cases

The following figure illustrates reactions of four FDS outputs with different output configurations separately when a fault (enabled for shutdown) occurs.



**** Note: The reaction time here doesn't include the fault source delay and the port delay.***

Figure 25-3. Fault detection and shutdown Cases

Chapter 26
Windowed COP (WCOP)

26.1 Chip specific WCOP information

This device includes one windowed COP (WCOP) which has four clock options:

Table 26-1. WCOP clock options

WCOP Module Clock Interface	Chip Specific Clock Source
Bus clock (BUSCLK)	BUSCLK
Internal LPO clock (LPOCLK)	LPOCLK (1 kHz)
Internal RC oscillator clock (IRCLK)	ICSIRCLK (up to the 32 kHz)
External clock (EXTCLK)	OSCOUT

The WCOP control and status registers are implemented in SYS_SOPT5.

26.2 Introduction

The Windowed COP (WCOP) module is an independent timer that is available for system use. It provides a safety feature to ensure that software is executing as planned and the CPU is not stuck in an infinite loop or executing unintended code. If the WCOP counter is not reset (refreshed) within a certain period, it resets the MCU.

26.3 Features

The WCOP has the following features:

- Configurable clock source inputs independent from the:
  - Bus clock (BUSCLK)
  - Internal LPO clock (LPOCLK)

  - Internal RC oscillator clock (IRCLK)
  - External clock (EXTCLK)
- Programmable timeout period based on different clock source:
  - 2^5, 2^8 or 2^{10} cycles (LPOCLK or IRCLK)
  - 2^{13}, 2^{16} or 2^{18} cycles (BUSCLK or EXTCLK)
- Robust write sequence for counter refresh
  - Refresh sequence of writing 0x55 and then 0xAA to the address of SRS during the selected timeout period
- Window mode option for the refresh mechanism
  - Provides robust check that program flow is faster than expected
  - Early refresh attempts trigger a reset
- Optional timeout interrupt to allow post-processing diagnostics
  - Interrupt request to CPU with interrupt vector for an interrupt service routine (ISR)
- Configuration bits are write-once-after-reset to ensure watchdog configuration cannot be mistakenly altered

26.4 Functional description

The Windowed Computer operating properly (WCOP) watchdog is used to force a system reset when the application software fails to execute as expected. To prevent a system reset from the WCOP timer (when it is enabled), application software must reset (refresh) the WCOP counter periodically. If the application program gets lost and fails to reset the WCOP counter before it times out, a system reset is generated to force the system back to an known starting point. After any reset, the WCOP watchdog is enabled (see SYS_SOPT5 for additional information). If the WCOP watchdog is not used in an application, it can be disabled by clearing SYS_SOPT5[COPT].

26.4.1 Watchdog refresh mechanism

The WCOP counter is reset (refreshed) by writing 0x55 and 0xAA (in this order) to the address of SRS during the selected timeout period. Writes do not affect the data in the read-only SRS. As soon as the write sequence is done, the WCOP timeout period is restarted. If the program fails to do this during the time-out period, the MCU will reset. Also, if any value other than 0x55 or 0xAA is written to SRS, the MCU is immediately reset.

This will prevent accidental changes if the application program gets lost. The write to SRS that services (refreshed) the WCOP counter must not be placed in an interrupt service routine (ISR) because the ISR could continue to be executed periodically even if the main application program fails.

26.4.2 Window mode

When the bus clock source is selected, windowed COP operation is available by setting SYS_SOPT5[COPW]. In this mode, writes to the SRS register to clear the WCOP timer must occur in the last 25% of the selected timeout period. A premature write immediately resets the MCU. When the LPO, IRCLK, or EXTCLK clock source is selected, windowed COP operation is not available.

26.5 Configuring the WCOP

All watchdog control bits are write-once after reset. This means that after a write has occurred they cannot be changed unless a reset occurs. This provides a robust mechanism to configure the watchdog and ensure that a runaway condition cannot mistakenly disable or modify the watchdog configuration after configured.

The WCOP counter is initialized by the first writes to the SYS_SOPT5[COPCLKS] and after any system reset. Subsequent writes to SYS_SOPT5 have no effect on COP operation. Even if the application will use the reset default settings of SYS_SOPT5[COPT], SYS_SOPT5[COPCLKS], and SYS_SOPT5[COPW] bits, the user must write to the write-once SYS_SOPT5 register during reset initialization to lock in the settings.

26.6 Clock source

The SYS_SOPT5[COPCLKS] selects the clock source used for the WCOP timer. The clock source options are:

- Bus clock (BUSCLK)
- Internal LPO clock (LPOCLK)
- Internal RC oscillator clock (IRCLK)
- External clock (EXTCLK)

With each clock source, there are three associated time-outs controlled by SYS_SOPT5[COPT]. The following table summarizes the control functions of the SYS_SOPT5[COPCLKS] and SYS_SOPT5[COPT] bits. The WCOP watchdog defaults to operation from the LPO clock source and the longest time-out (2^{10} cycles)

Table 26-2. Configuration option

Control bits		Clock source	WCOP window opens[1]	WCOP timeout period
SYS_SOPT5[COPCLKS]	SYS_SOPT5[COPT]			
N/A	00	N/A	N/A	WCOP is disabled
00/10	01	LPOCLK/IRCLK	N/A	2^5 cycles
00/10	10	LPOCLK/IRCLK	N/A	2^8 cycles
00/10	11	LPOCLK/IRCLK	N/A	2^{10} cycles
01	01	BUSCLK	6,144 cycles	2^{13} cycles
01	10	BUSCLK	49,152 cycles	2^{16} cycles
01	11	BUSCLK	196,608 cycles	2^{18} cycles
11	01	EXTCLK	N/A	2^{13} cycles
11	10	EXTCLK	N/A	2^{16} cycles
11	11	EXTCLK	N/A	2^{18} cycles

1. Windowed COP operation requires the user to clear the WCOP timer in the last 25% of the selected timeout period. This column displays the minimum number of clock counts required before the WCOP timer can be reset when in windowed COP mode (SYS_SOPT5[COPW] = 1).

26.7 Functionality in debug and low-power modes

If the bus clock source is selected, the WCOP counter does not increment while the MCU is in background debug mode or while the system is in stop mode. The WCOP counter resumes when the MCU exits background debug mode or stop mode.

If the LPO, IRCLK, or EXTCLK clock source is selected, the WCOP counter is re-initialized to zero upon entry to either background debug mode or stop mode and begins from zero upon exit from background debug mode or stop mode.

Chapter 27
Development support

27.1 Introduction

This chapter describes the single-wire background debug mode (BDM), which uses the on-chip background debug controller (BDC) module, and the independent on-chip real-time in-circuit emulation (ICE) system, which uses the on-chip debug (DBG) module.

27.1.1 Forcing active background

The method for forcing active background mode depends on the specific HCS08 derivative. For the 9S08xxxx, you can force active background after a power-on reset by holding the BKGD pin low as the device exits the reset condition. You can also force active background by driving BKGD low immediately after a serial background command that writes a one to the BDFR bit in the SBDFR register. Other causes of reset including an external pin reset or an internally generated error reset ignore the state of the BKGD pin and reset into normal user mode. If no debug pod is connected to the BKGD pin, the MCU will always reset into normal operating mode.

27.1.2 Features

Features of the BDC module include:

- Single pin for mode selection and background communications
- BDC registers are not located in the memory map
- SYNC command to determine target communications rate
- Non-intrusive commands for memory access
- Active background mode commands for CPU register access
- GO and TRACE1 commands
- BACKGROUND command can wake CPU from stop or wait modes
- One hardware address breakpoint built into BDC

- BDC clock runs in stop mode, if BDC enabled
- Watchdog disabled by default while in active background mode. It can also be enabled by proper configuration

Features of the ICE system include:

- Two trigger comparators: Two address + read/write (R/W) or one full address + data + R/W
- Flexible 8-word by 16-bit FIFO (first-in, first-out) buffer for capture information:
  - Change-of-flow addresses or
  - Event-only data
- Two types of breakpoints:
  - Tag breakpoints for instruction opcodes
  - Force breakpoints for any address access
- Nine trigger modes:
  - Basic: A-only, A OR B
  - Sequence: A then B
  - Full: A AND B data, A AND NOT B data
  - Event (store data): Event-only B, A then event-only B
  - Range: Inside range (A ≤ address ≤ B), outside range (address < A or address > B)

27.2 Background debug controller (BDC)

All MCUs in the HCS08 Family contain a single-wire background debug interface that supports in-circuit programming of on-chip nonvolatile memory and sophisticated non-intrusive debug capabilities. Unlike debug interfaces on earlier 8-bit MCUs, this system does not interfere with normal application resources. It does not use any user memory or locations in the memory map and does not share any on-chip peripherals.

BDC commands are divided into two groups:

- Active background mode commands require that the target MCU is in active background mode (the user program is not running). Active background mode commands allow the CPU registers to be read or written, and allow the user to trace one user instruction at a time, or GO to the user program from active background mode.
- Non-intrusive commands can be executed at any time even while the user's program is running. Non-intrusive commands allow a user to read or write MCU memory locations or access status and control registers within the background debug controller.

Typically, a relatively simple interface pod is used to translate commands from a host computer into commands for the custom serial interface to the single-wire background debug system. Depending on the development tool vendor, this interface pod may use a standard RS-232 serial port, a parallel printer port, or some other type of communications such as a universal serial bus (USB) to communicate between the host PC and the pod. The pod typically connects to the target system with ground, the BKGD pin, RESET, and sometimes V_{DD}. An open-drain connection to reset allows the host to force a target system reset, which is useful to regain control of a lost target system or to control startup of a target system before the on-chip nonvolatile memory has been programmed. Sometimes V_{DD} can be used to allow the pod to use power from the target system to avoid the need for a separate power supply. However, if the pod is powered separately, it can be connected to a running target system without forcing a target system reset or otherwise disturbing the running application program.

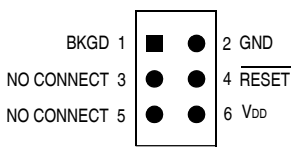


Figure 27-1. BDM tool connector

27.2.1 BKGD pin description

BKGD is the single-wire background debug interface pin. The primary function of this pin is for bidirectional serial communication of active background mode commands and data. During reset, this pin is used to select between starting in active background mode or starting the user's application program. This pin is also used to request a timed sync response pulse to allow a host development tool to determine the correct clock frequency for background debug serial communications.

BDC serial communications use a custom serial protocol first introduced on the M68HC12 Family of microcontrollers. This protocol assumes the host knows the communication clock rate that is determined by the target BDC clock rate. All communication is initiated and controlled by the host that drives a high-to-low edge to signal the beginning of each bit time. Commands and data are sent most significant bit first (MSB first). For a detailed description of the communications protocol, refer to Communication details.

If a host is attempting to communicate with a target MCU that has an unknown BDC clock rate, a SYNC command may be sent to the target MCU to request a timed sync response signal from which the host can determine the correct communication speed.

BKGD is a pseudo-open-drain pin and there is an on-chip pullup so no external pullup resistor is required. Unlike typical open-drain pins, the external RC time constant on this pin, which is influenced by external capacitance, plays almost no role in signal rise time. The custom protocol provides for brief, actively driven speedup pulses to force rapid rise times on this pin without risking harmful drive level conflicts. Refer to Communication details for more detail.

When no debugger pod is connected to the 6-pin BDM interface connector, the internal pullup on BKGD chooses normal operating mode. When a debug pod is connected to BKGD it is possible to force the MCU into active background mode after reset. The specific conditions for forcing active background depend upon the HCS08 derivative (refer to the introduction to this Development Support section). It is not necessary to reset the target MCU to communicate with it through the background debug interface.

27.2.2 Communication details

The BDC serial interface requires the external controller to generate a falling edge on the BKGD pin to indicate the start of each bit time. The external controller provides this falling edge whether data is transmitted or received.

BKGD is a pseudo-open-drain pin that can be driven either by an external controller or by the MCU. Data is transferred MSB first at 16 BDC clock cycles per bit (nominal speed). The interface times out if 512 BDC clock cycles occur between falling edges from the host. Any BDC command that was in progress when this timeout occurs is aborted without affecting the memory or operating mode of the target MCU system.

The custom serial protocol requires the debug pod to know the target BDC communication clock speed.

The clock switch (CLKSW) control bit in the BDC status and control register allows the user to select the BDC clock source. The BDC clock source can either be the MSTRCLK or the alternate BDC clock source.

The BKGD pin can receive a high or low level or transmit a high or low level. The following diagrams show timing for each of these cases. Interface timing is synchronous to clocks in the target BDC, but asynchronous to the external host. The internal BDC clock signal is shown for reference in counting cycles.

The following figure shows an external host transmitting a logic 1 or 0 to the BKGD pin of a target HCS08 MCU. The host is asynchronous to the target so there is a 0-to-1 cycle delay from the host-generated falling edge to where the target perceives the beginning of the bit time. Ten target BDC clock cycles later, the target senses the bit level on the BKGD pin. Typically, the host actively drives the pseudo-open-drain BKGD pin during

host-to-target transmissions to speed up rising edges. Because the target does not drive the BKGD pin during the host-to-target transmission period, there is no need to treat the line as an open-drain signal during this period.

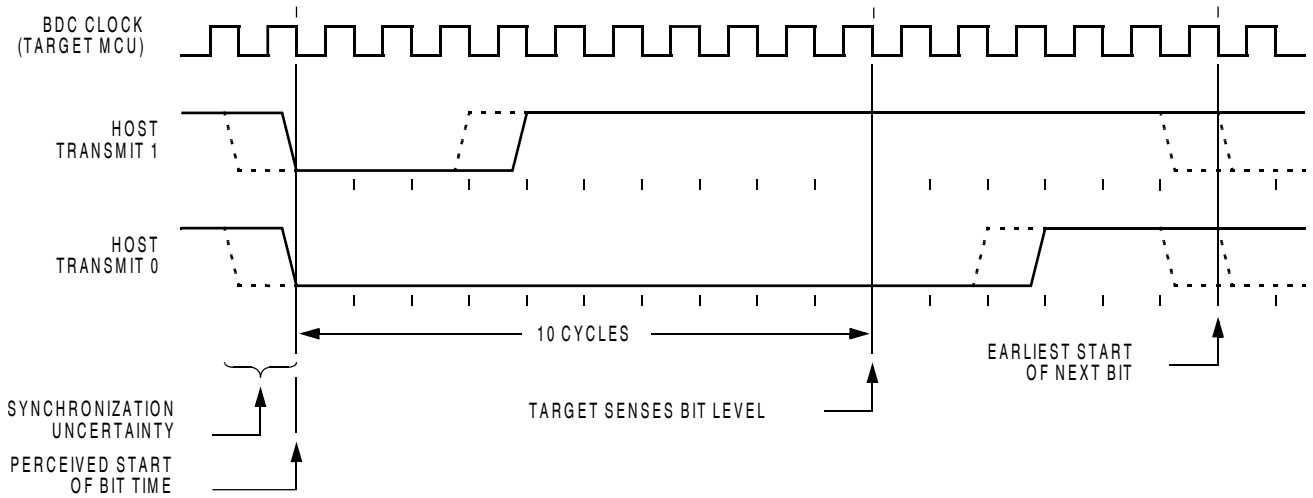


Figure 27-2. BDC host-to-target serial bit timing

The next figure shows the host receiving a logic 1 from the target HCS08 MCU. Because the host is asynchronous to the target MCU, there is a 0-to-1 cycle delay from the host-generated falling edge on BKGD to the perceived start of the bit time in the target MCU. The host holds the BKGD pin low long enough for the target to recognize it (at least two target BDC cycles). The host must release the low drive before the target MCU drives a brief active-high speedup pulse seven cycles after the perceived start of the bit time. The host should sample the bit level about 10 cycles after it started the bit time.

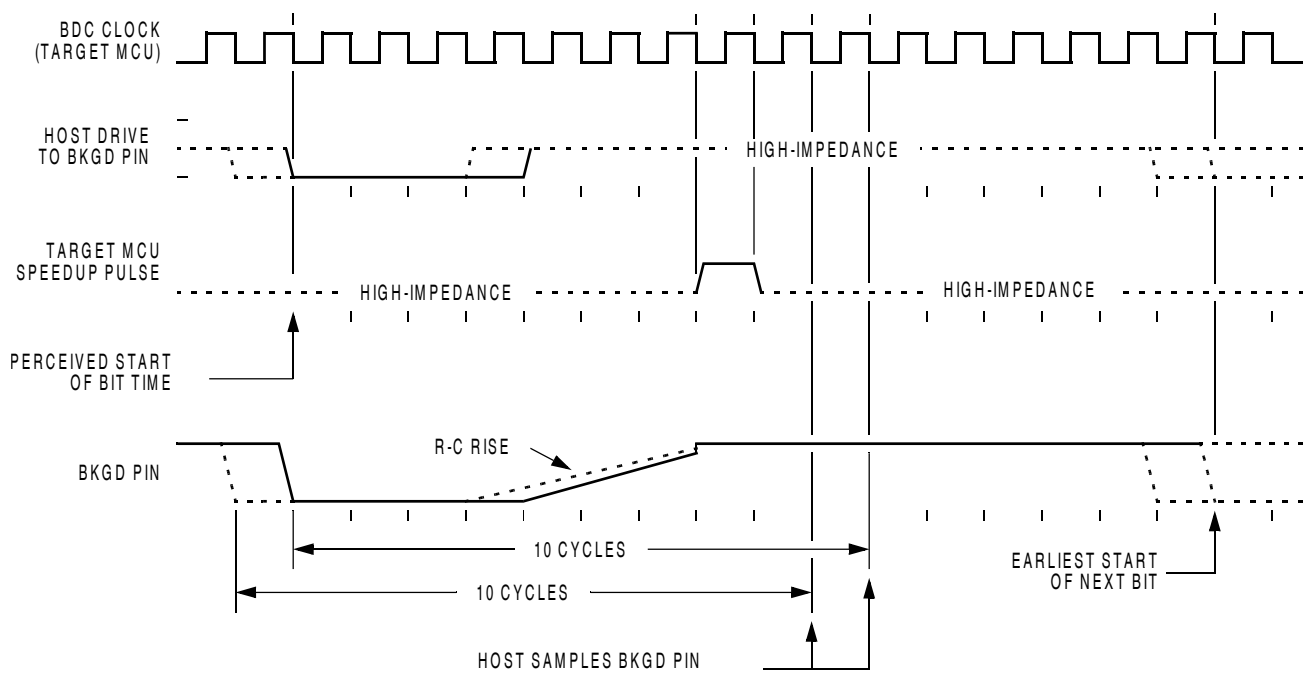


Figure 27-3. BDC target-to-host serial bit timing (logic 1)

The following figure shows the host receiving a logic 0 from the target HCS08 MCU. Because the host is asynchronous to the target MCU, there is a 0-to-1 cycle delay from the host-generated falling edge on BKGD to the start of the bit time as perceived by the target MCU. The host initiates the bit time but the target HCS08 finishes it. Because the target wants the host to receive a logic 0, it drives the BKGD pin low for 13 BDC clock cycles, then briefly drives it high to speed up the rising edge. The host samples the bit level about 10 cycles after starting the bit time.

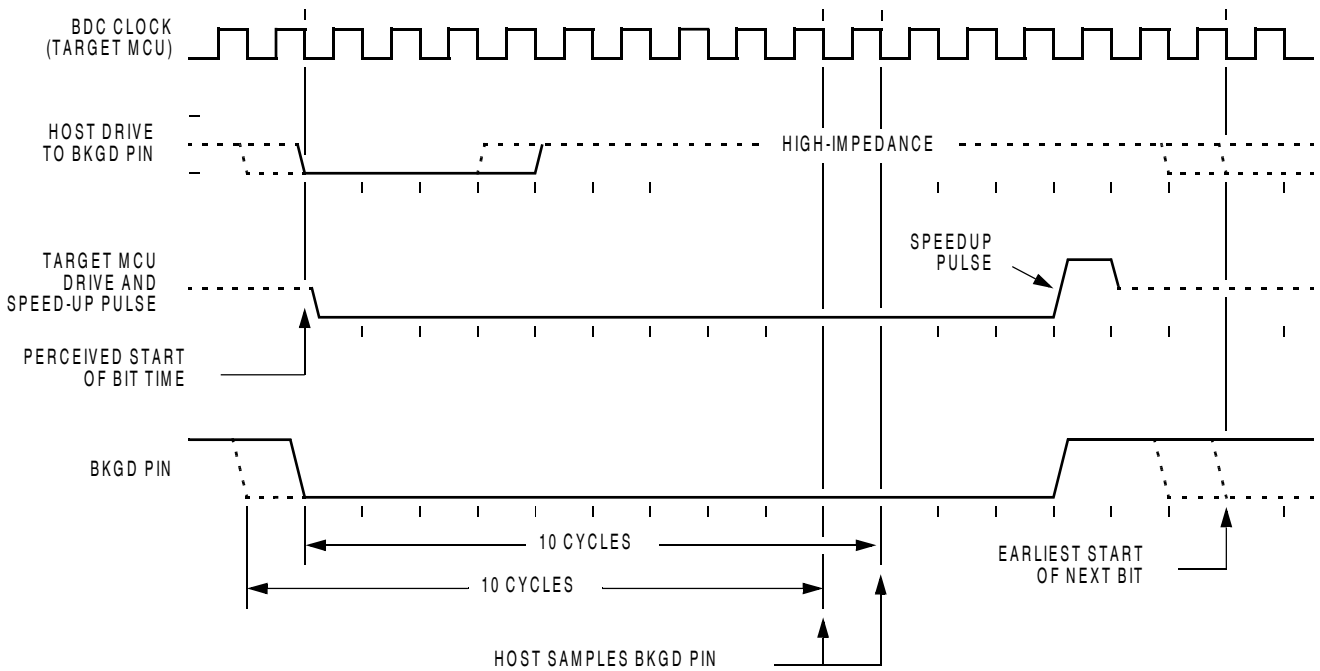


Figure 27-4. BDM target-to-host serial bit timing (logic 0)

27.2.3 BDC commands

BDC commands are sent serially from a host computer to the BKGD pin of the target HCS08 MCU. All commands and data are sent MSB-first using a custom BDC communications protocol. Active background mode commands require that the target MCU is currently in the active background mode while non-intrusive commands may be issued at any time whether the target MCU is in active background mode or running a user application program.

The following table shows all HCS08 BDC commands, a shorthand description of their coding structure, and the meaning of each command.

Coding Structure Nomenclature

This nomenclature is used in the following table to describe the coding structure of the BDC commands.

```
Commands begin with an 8-bit hexadecimal command code in the host-to-target direction (most
significant bit first)
/ =separates parts of the command
d=delay 16 target BDC clock cycles
AAAA = a 16-bit address in the host-to-target direction
RD   = 8 bits of read data in the target-to-host direction
WD   = 8 bits of write data in the host-to-target direction
RD16 = 16 bits of read data in the target-to-host direction
WD16 = 16 bits of write data in the host-to-target direction
SS   = the contents of BDCSCR in the target-to-host direction (STATUS)
CC   = 8 bits of write data for BDCSCR in the host-to-target direction (CONTROL)
RBKP = 16 bits of read data in the target-to-host direction (from BDCBKPT breakpoint
register)
WBKP = 16 bits of write data in the host-to-target direction (for BDCBKPT breakpoint
register)
```

Table 27-1. BDC command summary

Command mnemonic	Active BDM/ non-intrusive	Coding structure	Description
SYNC	Non-intrusive	N/A[1]	Request a timed reference pulse to determine target BDC communication speed
ACK_ENABLE	Non-intrusive	D5/d	Enable acknowledge protocol. Refer to NXP document order no. HCS08RMv1/D.
ACK_DISABLE	Non-intrusive	D6/d	Disable acknowledge protocol. Refer to NXP document order no. HCS08RMv1/D.
BACKGROUND	Non-intrusive	90/d	Enter active background mode if enabled (ignore if ENBDM bit equals 0)
READ_STATUS	Non-intrusive	E4/SS	Read BDC status from BDCSCR
WRITE_CONTROL	Non-intrusive	C4/CC	Write BDC controls in BDCSCR
READ_BYTE	Non-intrusive	E0/AAAA/d/RD	Read a byte from target memory
READ_BYTE_WS	Non-intrusive	E1/AAAA/d/SS/RD	Read a byte and report status
READ_LAST	Non-intrusive	E8/SS/RD	Re-read byte from address just read and report status
WRITE_BYTE	Non-intrusive	C0/AAAA/WD/d	Write a byte to target memory
WRITE_BYTE_WS	Non-intrusive	C1/AAAA/WD/d/SS	Write a byte and report status
READ_BKPT	Non-intrusive	E2/RBKP	Read BDCBKPT breakpoint register
WRITE_BKPT	Non-intrusive	C2/WBKP	Write BDCBKPT breakpoint register
GO	Active BDM	08/d	Go to execute the user application program starting at the address currently in the PC
TRACE1	Active BDM	10/d	Trace 1 user instruction at the address in the PC, then return to active background mode

Table continues on the next page...

Table 27-1. BDC command summary (continued)

Command mnemonic	Active BDM/ non-intrusive	Coding structure	Description
TAGGO	Active BDM	18/d	Same as GO but enable external tagging (HCS08 devices have no external tagging pin)
READ_A	Active BDM	68/d/RD	Read accumulator (A)
READ_CCR	Active BDM	69/d/RD	Read condition code register (CCR)
READ_PC	Active BDM	6B/d/RD16	Read program counter (PC)
READ_HX	Active BDM	6C/d/RD16	Read H and X register pair (H:X)
READ_SP	Active BDM	6F/d/RD16	Read stack pointer (SP)
READ_NEXT	Active BDM	70/d/RD	Increment H:X by one then read memory byte located at H:X
READ_NEXT_WS	Active BDM	71/d/SS/RD	Increment H:X by one then read memory byte located at H:X. Report status and data.
WRITE_A	Active BDM	48/WD/d	Write accumulator (A)
WRITE_CCR	Active BDM	49/WD/d	Write condition code register (CCR)
WRITE_PC	Active BDM	4B/WD16/d	Write program counter (PC)
WRITE_HX	Active BDM	4C/WD16/d	Write H and X register pair (H:X)
WRITE_SP	Active BDM	4F/WD16/d	Write stack pointer (SP)
WRITE_NEXT	Active BDM	50/WD/d	Increment H:X by one, then write memory byte located at H:X
WRITE_NEXT_WS	Active BDM	51/WD/d/SS	Increment H:X by one, then write memory byte located at H:X. Also report status.

1. The SYNC command is a special operation that does not have a command code.

The SYNC command is unlike other BDC commands because the host does not necessarily know the correct communications speed to use for BDC communications until after it has analyzed the response to the SYNC command.

To issue a SYNC command, the host:

- Drives the BKGD pin low for at least 128 cycles of the slowest possible BDC clock (The slowest clock is normally the reference oscillator/64 or the self-clocked rate/ 64.)
- Drives BKGD high for a brief speedup pulse to get a fast rise time (This speedup pulse is typically one cycle of the fastest clock in the system.)
- Removes all drive to the BKGD pin so it reverts to high impedance
- Monitors the BKGD pin for the sync response pulse

The target, upon detecting the SYNC request from the host (which is a much longer low time than would ever occur during normal BDC communications):

- Waits for BKGD to return to a logic high
- Delays 16 cycles to allow the host to stop driving the high speedup pulse
- Drives BKGD low for 128 BDC clock cycles
- Drives a 1-cycle high speedup pulse to force a fast rise time on BKGD
- Removes all drive to the BKGD pin so it reverts to high impedance

The host measures the low time of this 128-cycle sync response pulse and determines the correct speed for subsequent BDC communications. Typically, the host can determine the correct communication speed within a few percent of the actual target speed and the communication protocol can easily tolerate speed errors of several percent.

27.2.4 BDC hardware breakpoint

The BDC includes one relatively simple hardware breakpoint that compares the CPU address bus to a 16-bit match value in the BDCBKPT register. This breakpoint can generate a forced breakpoint or a tagged breakpoint. A forced breakpoint causes the CPU to enter active background mode at the first instruction boundary following any access to the breakpoint address. The tagged breakpoint causes the instruction opcode at the breakpoint address to be tagged so that the CPU will enter active background mode rather than executing that instruction if and when it reaches the end of the instruction queue. This implies that tagged breakpoints can be placed only at the address of an instruction opcode while forced breakpoints can be set at any address.

The breakpoint enable (BKPTEN) control bit in the BDC status and control register (BDCSCR) is used to enable the breakpoint logic (BKPTEN = 1). When BKPTEN = 0, its default value after reset, the breakpoint logic is disabled and no BDC breakpoints are requested regardless of the values in other BDC breakpoint registers and control bits. The force/tag select (FTS) control bit in BDCSCR is used to select forced (FTS = 1) or tagged (FTS = 0) type breakpoints.

The on-chip debug module (DBG) includes circuitry for two additional hardware breakpoints that are more flexible than the simple breakpoint in the BDC module.

27.3 On-chip debug system (DBG)

Because HCS08 devices do not have external address and data buses, the most important functions of an in-circuit emulator have been built onto the chip with the MCU. The debug system consists of an 8-stage FIFO that can store address or data bus information,

and a flexible trigger system to decide when to capture bus information and what information to capture. The system relies on the single-wire background debug system to access debug control registers and to read results out of the eight stage FIFO.

The debug module includes control and status registers that are accessible in the user's memory map. These registers are located in the high register space to avoid using valuable direct page memory space.

Most of the debug module's functions are used during development, and user programs rarely access any of the control and status registers for the debug module. The one exception is that the debug system can provide the means to implement a form of ROM patching. This topic is discussed in greater detail in Hardware breakpoints.

27.3.1 Comparators A and B

Two 16-bit comparators (A and B) can optionally be qualified with the R/W signal and an opcode tracking circuit. Separate control bits allow you to ignore R/W for each comparator. The opcode tracking circuitry optionally allows you to specify that a trigger will occur only if the opcode at the specified address is actually executed as opposed to only being read from memory into the instruction queue. The comparators are also capable of magnitude comparisons to support the inside range and outside range trigger modes. Comparators are disabled temporarily during all BDC accesses.

The A comparator is always associated with the 16-bit CPU address. The B comparator compares to the CPU address or the 8-bit CPU data bus, depending on the trigger mode selected. Because the CPU data bus is separated into a read data bus and a write data bus, the RWAEN and RWA control bits have an additional purpose, in full address plus data comparisons they are used to decide which of these buses to use in the comparator B data bus comparisons. If RWAEN = 1 (enabled) and RWA = 0 (write), the CPU's write data bus is used. Otherwise, the CPU's read data bus is used.

The currently selected trigger mode determines what the debugger logic does when a comparator detects a qualified match condition. A match can cause:

- Generation of a breakpoint to the CPU
- Storage of data bus values into the FIFO
- Starting to store change-of-flow addresses into the FIFO (begin type trace)
- Stopping the storage of change-of-flow addresses into the FIFO (end type trace)

27.3.2 Bus capture information and FIFO operation

The usual way to use the FIFO is to setup the trigger mode and other control options, then arm the debugger. When the FIFO has filled or the debugger has stopped storing data into the FIFO, you would read the information out of it in the order it was stored into the FIFO. Status bits indicate the number of words of valid information that are in the FIFO as data is stored into it. If a trace run is manually halted by writing 0 to ARM before the FIFO is full (CNT = 1:0:0:0), the information is shifted by one position and the host must perform ((8 - CNT) - 1) dummy reads of the FIFO to advance it to the first significant entry in the FIFO.

In most trigger modes, the information stored in the FIFO consists of 16-bit change-of-flow addresses. In these cases, read DBGFH then DBGFL to get one coherent word of information out of the FIFO. Reading DBGFL (the low-order byte of the FIFO data port) causes the FIFO to shift so the next word of information is available at the FIFO data port. In the event-only trigger modes (see Trigger modes), 8-bit data information is stored into the FIFO. In these cases, the high-order half of the FIFO (DBGFH) is not used and data is read out of the FIFO by simply reading DBGFL. Each time DBGFL is read, the FIFO is shifted so the next data value is available through the FIFO data port at DBGFL.

In trigger modes where the FIFO is storing change-of-flow addresses, there is a delay between CPU addresses and the input side of the FIFO. Because of this delay, if the trigger event itself is a change-of-flow address or a change-of-flow address appears during the next two bus cycles after a trigger event starts the FIFO, it will not be saved into the FIFO. In the case of an end-trace, if the trigger event is a change-of-flow, it will be saved as the last change-of-flow entry for that debug run.

The FIFO can also be used to generate a profile of executed instruction addresses when the debugger is not armed. When ARM = 0, reading DBGFL causes the address of the most-recently fetched opcode to be saved in the FIFO. To use the profiling feature, a host debugger would read addresses out of the FIFO by reading DBGFH then DBGFL at regular periodic intervals. The first eight values would be discarded because they correspond to the eight DBGFL reads needed to initially fill the FIFO. Additional periodic reads of DBGFH and DBGFL return delayed information about executed instructions so the host debugger can develop a profile of executed instruction addresses.

27.3.3 Change-of-flow information

To minimize the amount of information stored in the FIFO, only information related to instructions that cause a change to the normal sequential execution of instructions is stored. With knowledge of the source and object code program stored in the target system, an external debugger system can reconstruct the path of execution through many instructions from the change-of-flow information stored in the FIFO.

For conditional branch instructions where the branch is taken (branch condition was true), the source address is stored (the address of the conditional branch opcode). Because BRA and BRN instructions are not conditional, these events do not cause change-of-flow information to be stored in the FIFO.

Indirect JMP and JSR instructions use the current contents of the H:X index register pair to determine the destination address, so the debug system stores the run-time destination address for any indirect JMP or JSR. For interrupts, RTI, or RTS, the destination address is stored in the FIFO as change-of-flow information.

27.3.4 Tag vs. force breakpoints and triggers

Tagging is a term that refers to identifying an instruction opcode as it is fetched into the instruction queue, but not taking any other action until and unless that instruction is actually executed by the CPU. This distinction is important because any change-of-flow from a jump, branch, subroutine call, or interrupt causes some instructions that have been fetched into the instruction queue to be thrown away without being executed.

A force-type breakpoint waits for the current instruction to finish and then acts upon the breakpoint request. The usual action in response to a breakpoint is to go to active background mode rather than continuing to the next instruction in the user application program.

The tag vs. force terminology is used in two contexts within the debug module. The first context refers to breakpoint requests from the debug module to the CPU. The second refers to match signals from the comparators to the debugger control logic. When a tag-type break request is sent to the CPU, a signal is entered into the instruction queue along with the opcode so that if/when this opcode ever executes, the CPU will effectively replace the tagged opcode with a BGND opcode so the CPU goes to active background mode rather than executing the tagged instruction. When the TRGSEL control bit in the DBGT register is set to select tag-type operation, the output from comparator A or B is qualified by a block of logic in the debug module that tracks opcodes and produces only a trigger to the debugger if the opcode at the compare address is actually executed. There is separate opcode tracking logic for each comparator so more than one compare event can be tracked through the instruction queue at a time.

27.3.5 Trigger modes

The trigger mode controls the overall behavior of a debug run. The 4-bit TRG field in the DBGT register selects one of nine trigger modes. When TRGSEL = 1 in the DBGT register, the output of the comparator must propagate through an opcode tracking circuit before triggering FIFO actions. The BEGIN bit in DBGT chooses whether the FIFO begins storing data when the qualified trigger is detected (begin trace), or the FIFO stores data in a circular fashion from the time it is armed until the qualified trigger is detected (end trigger).

A debug run is started by writing a 1 to the ARM bit in the DBGC register, which sets the ARMF flag and clears the AF and BF flags and the CNT bits in DBGS. A begin-trace debug run ends when the FIFO gets full. An end-trace run ends when the selected trigger event occurs. Any debug run can be stopped manually by writing a 0 to ARM or DBGEN in DBGC.

In all trigger modes except event-only modes, the FIFO stores change-of-flow addresses. In event-only trigger modes, the FIFO stores data in the low-order eight bits of the FIFO.

The BEGIN control bit is ignored in event-only trigger modes and all such debug runs are begin type traces. When TRGSEL = 1 to select opcode fetch triggers, it is not necessary to use R/W in comparisons because opcode tags would apply only to opcode fetches that are always read cycles. It would also be unusual to specify TRGSEL = 1 while using a full mode trigger because the opcode value is normally known at a particular address.

The following trigger mode descriptions state only the primary comparator conditions that lead to a trigger. Either comparator can usually be further qualified with R/W by setting RWAEN (RWBEN) and the corresponding RWA (RWB) value to be matched against R/W. The signal from the comparator with optional R/W qualification is used to request a CPU breakpoint if BRKEN = 1 and TAG determines whether the CPU request will be a tag request or a force request.

A-Only – Trigger when the address matches the value in comparator A

A OR B – Trigger when the address matches either the value in comparator A or the value in comparator B

A Then B – Trigger when the address matches the value in comparator B but only after the address for another cycle matched the value in comparator A. There can be any number of cycles after the A match and before the B match.

A AND B Data (Full Mode)— This is called a full mode because address, data, and R/W (optionally) must match within the same bus cycle to cause a trigger event. Comparator A checks address, the low byte of comparator B checks data, and R/W is checked against RWA if RWAEN = 1. The high-order half of comparator B is not used.

In full trigger modes it is not useful to specify a tag-type CPU breakpoint (BRKEN = TAG = 1), but if you do, the comparator B data match is ignored for the purpose of issuing the tag request to the CPU and the CPU breakpoint is issued when the comparator A address matches.

A AND NOT B Data (Full Mode)— Address must match comparator A, data must not match the low half of comparator B, and R/W must match RWA if RWAEN = 1. All three conditions must be met within the same bus cycle to cause a trigger.

In full trigger modes it is not useful to specify a tag-type CPU breakpoint (BRKEN = TAG = 1), but if you do, the comparator B data match is ignored for the purpose of issuing the tag request to the CPU and the CPU breakpoint is issued when the comparator A address matches.

Event-Only B (Store Data)— Trigger events occur each time the address matches the value in comparator B. Trigger events cause the data to be captured into the FIFO. The debug run ends when the FIFO becomes full.

A Then Event-Only B (Store Data)— After the address has matched the value in comparator A, a trigger event occurs each time the address matches the value in comparator B. Trigger events cause the data to be captured into the FIFO. The debug run ends when the FIFO becomes full.

Inside Range (A ≤ Address ≤ B)— A trigger occurs when the address is greater than or equal to the value in comparator A and less than or equal to the value in comparator B at the same time.

Outside Range (Address < A or Address > B)— A trigger occurs when the address is either less than the value in comparator A or greater than the value in comparator B.

27.3.6 Hardware breakpoints

The BRKEN control bit in the DBGC register may be set to 1 to allow any of the trigger conditions described in Trigger modes to be used to generate a hardware breakpoint request to the CPU. TAG in DBGC controls whether the breakpoint request will be treated as a tag-type breakpoint or a force-type breakpoint. A tag breakpoint causes the current opcode to be marked as it enters the instruction queue. If a tagged opcode reaches

the end of the pipe, the CPU executes a BGND instruction to go to active background mode rather than executing the tagged opcode. A force-type breakpoint causes the CPU to finish the current instruction and then go to active background mode.

If the background mode has not been enabled (ENBDM = 1) by a serial WRITE_CONTROL command through the BKGD pin, the CPU will execute an SWI instruction instead of going to active background mode.

27.4 Memory map and register description

This section contains the descriptions of the BDCand DBG registers and control bits. Refer to the high-page register summary in the device overview chapter of this data sheet for the absolute address assignments for all DBG registers. This section refers to registers and control bits only by their names. An NXP-provided equate or header file is used to translate these names into the appropriate absolute addresses.

BDC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	BDC Status and Control Register (BDC_SCR)	8	R/W	00h	27.4.1/441
1	BDC Breakpoint Match Register: High (BDC_BKPTH)	8	R/W	00h	27.4.2/443
2	BDC Breakpoint Register: Low (BDC_BKPTL)	8	R/W	00h	27.4.3/444
3	System Background Debug Force Reset Register (BDC_SBDFR)	8	W (always reads 0)	00h	27.4.4/444

27.4.1 BDC Status and Control Register (BDC_SCR)

This register can be read or written by serial BDC commands (READ_STATUS and WRITE_CONTROL) but is not accessible to user programs because it is not located in the normal memory map of the MCU.

NOTE

The reset values shown in the register figure are those in the normal reset conditions. If the MCU is reset in BDM, ENBDM, BDMACT, CLKSW will be reset to 1 and others all be to 0.

Address: 0h base + 0h offset = 0h

Bit	7	6	5	4	3	2	1	0
Read	ENBDM	BDMACT	BKPTEN	FTS	CLKSW	WS	WSF	DVF
Write								
Reset	0	0	0	0	0	0	0	0

BDC_SCR field descriptions

Field	Description
7 ENBDM	Enable BDM (Permit Active Background Mode) Typically, this bit is written to 1 by the debug host shortly after the beginning of a debug session or whenever the debug host resets the target and remains 1 until a normal reset clears it. 0 BDM cannot be made active (non-intrusive commands still allowed). 1 BDM can be made active to allow active background mode commands.
6 BDMACT	Background Mode Active Status This is a read-only status bit. 0 BDM not active (user application program running). 1 BDM active and waiting for serial commands.
5 BKPTEN	BDC Breakpoint Enable If this bit is clear, the BDC breakpoint is disabled and the FTS (force tag select) control bit and BDCBKPT match register are ignored. 0 BDC breakpoint disabled. 1 BDC breakpoint enabled.
4 FTS	Force/Tag Select When FTS = 1, a breakpoint is requested whenever the CPU address bus matches the BDCBKPT match register. When FTS = 0, a match between the CPU address bus and the BDCBKPT register causes the fetched opcode to be tagged. If this tagged opcode ever reaches the end of the instruction queue, the CPU enters active background mode rather than executing the tagged opcode. 0 Tag opcode at breakpoint address and enter active background mode if CPU attempts to execute that instruction 1 Breakpoint match forces active background mode at next instruction boundary (address need not be an opcode)
3 CLKSW	Select Source for BDC Communications Clock CLKSW defaults to 0, which selects the alternate BDC clock source. 0 Alternate BDC clock source. 1 MCU MSTRCLK.
2 WS	Wait or Stop Status When the target CPU is in wait or stop mode, most BDC commands cannot function. However, the BACKGROUND command can be used to force the target CPU out of wait or stop and into active background mode where all BDC commands work. Whenever the host forces the target MCU into active background mode, the host should issue a READ_STATUS command to check that BDMACT = 1 before attempting other BDC commands.

Table continues on the next page...

BDC_SCR field descriptions (continued)

Field	Description
	0 Target CPU is running user application code or in active background mode (was not in wait or stop mode when background became active). 1 Target CPU is in wait or stop mode, or a BACKGROUND command was used to change from wait or stop to active background mode.
1 WSF	Wait or Stop Failure Status This status bit is set if a memory access command failed due to the target CPU executing a wait or stop instruction at or about the same time. The usual recovery strategy is to issue a BACKGROUND command to get out of wait or stop mode into active background mode, repeat the command that failed, then return to the user program. (Typically, the host would restore CPU registers and stack values and re-execute the wait or stop instruction.) 0 Memory access did not conflict with a wait or stop instruction. 1 Memory access command failed because the CPU entered wait or stop mode.
0 DVF	Data Valid Failure Status 0 Memory access did not conflict with a slow memory access 1 Memory access command failed because CPU was not finished with a slow memory access.

27.4.2 BDC Breakpoint Match Register: High (BDC_BKPTH)

This register, together with BDC_BKPTL, holds the address for the hardware breakpoint in the BDC. The BKPTEN and FTS control bits in BDCSCR are used to enable and configure the breakpoint logic. Dedicated serial BDC commands (READ_BKPT and WRITE_BKPT) are used to read and write the BDCBKPT register but is not accessible to user programs because it is not located in the normal memory map of the MCU. Breakpoints are normally set while the target MCU is in active background mode before running the user application program.

Address: 0h base + 1h offset = 1h

Bit	7	6	5	4	3	2	1	0
Read Write	A[15:8]							
Reset	0	0	0	0	0	0	0	0

BDC_BKPTH field descriptions

Field	Description
A[15:8]	High 8-bit of hardware breakpoint address.

27.4.3 BDC Breakpoint Register: Low (BDC_BKPTL)

BDC_BKPTH and BDC_BKPTL registers hold the address for the hardware breakpoint in the BDC. The BDC_SCR[FTS] and BDC_SCR[BKPTEN] bits are used to enable and configure the breakpoint logic. Dedicated serial BDC commands (READ_BKPT and WRITE_BKPT) are used to read and write the BDC_BKPTH and BDC_BKPTL register. Breakpoints are normally set while the target MCU is in background debug mode before running the user application program. However, since READ_BKPT and WRITE_BKPT are foreground commands, they could be executed even while the user program is running.

Address: 0h base + 2h offset = 2h

Bit	7	6	5	4	3	2	1	0
Read Write	A[7:0]							
Reset	0	0	0	0	0	0	0	0

BDC_BKPTL field descriptions

Field	Description
A[7:0]	Low 8-bit of hardware breakpoint address.

27.4.4 System Background Debug Force Reset Register (BDC_SBDFR)

This register contains a single write-only control bit. A serial background mode command such as WRITE_BYTE must be used to write to SBDFR. Attempts to write this register from a user program are ignored. Reads always return 0x00.

Address: 0h base + 3h offset = 3h

Bit	7	6	5	4	3	2	1	0
Read	0							0
Write								BDFR
Reset	0	0	0	0	0	0	0	0

BDC_SBDFR field descriptions

Field	Description
7–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 BDFR	Background Debug Force Reset

Table continues on the next page...

BDC_SBDFR field descriptions (continued)

Field	Description
	A serial active background mode command such as WRITE_BYTE allows an external debug host to force a target system reset. Writing 1 to this bit forces an MCU reset. This bit cannot be written from a user program.

Chapter 28
Debug module (DBG)

28.1 Introduction

The DBG module implements an on-chip ICE (in-circuit emulation) system and allows non-intrusive debug of application software by providing an on-chip trace buffer with flexible triggering capability. The trigger also can provide extended breakpoint capacity. The on-chip ICE system is optimized for the S08CPUV6 8-bit architecture and supports 2 M bytes of memory space.

28.1.1 Features

The on-chip ICE system includes these distinctive features:

- Three comparators (A, B, and C) with ability to match addresses in 64 KB space
  - Dual mode, Comparators A and B used to compare addresses
  - Full mode, Comparator A compares address and Comparator B compares data
  - Can be used as triggers and/or breakpoints
  - Comparator C can be used as a normal hardware breakpoint
  - Loop1 capture mode, Comparator C is used to track most recent COF event captured into FIFO
- Tag and Force type breakpoints
- Nine trigger modes
  - A
  - A Or B
  - A then B
  - A and B, where B is data (full mode)
  - A and not B, where B is data (full mode)
  - Event only B, store data
  - A then event only B, store data
  - Inside range, A ≤ address ≤ B
  - Outside range, address < A or address > B

- FIFO for storing change of flow information and event only data
  - Source address of conditional branches taken
  - Destination address of indirect JMP and JSR instruction
  - Destination address of interrupts, RTI, RTC, and RTS instruction
  - Data associated with Event B trigger modes
- Ability to End-trace until reset and begin-trace from reset

28.1.2 Modes of operation

The on-chip ICE system can be enabled in all MCU functional modes. The DBG module is disabled if the MCU is secure. The DBG module comparators are disabled when executing a Background Debug Mode (BDM) command.

28.1.3 Block diagram

The following figure shows the structure of the DBG module.

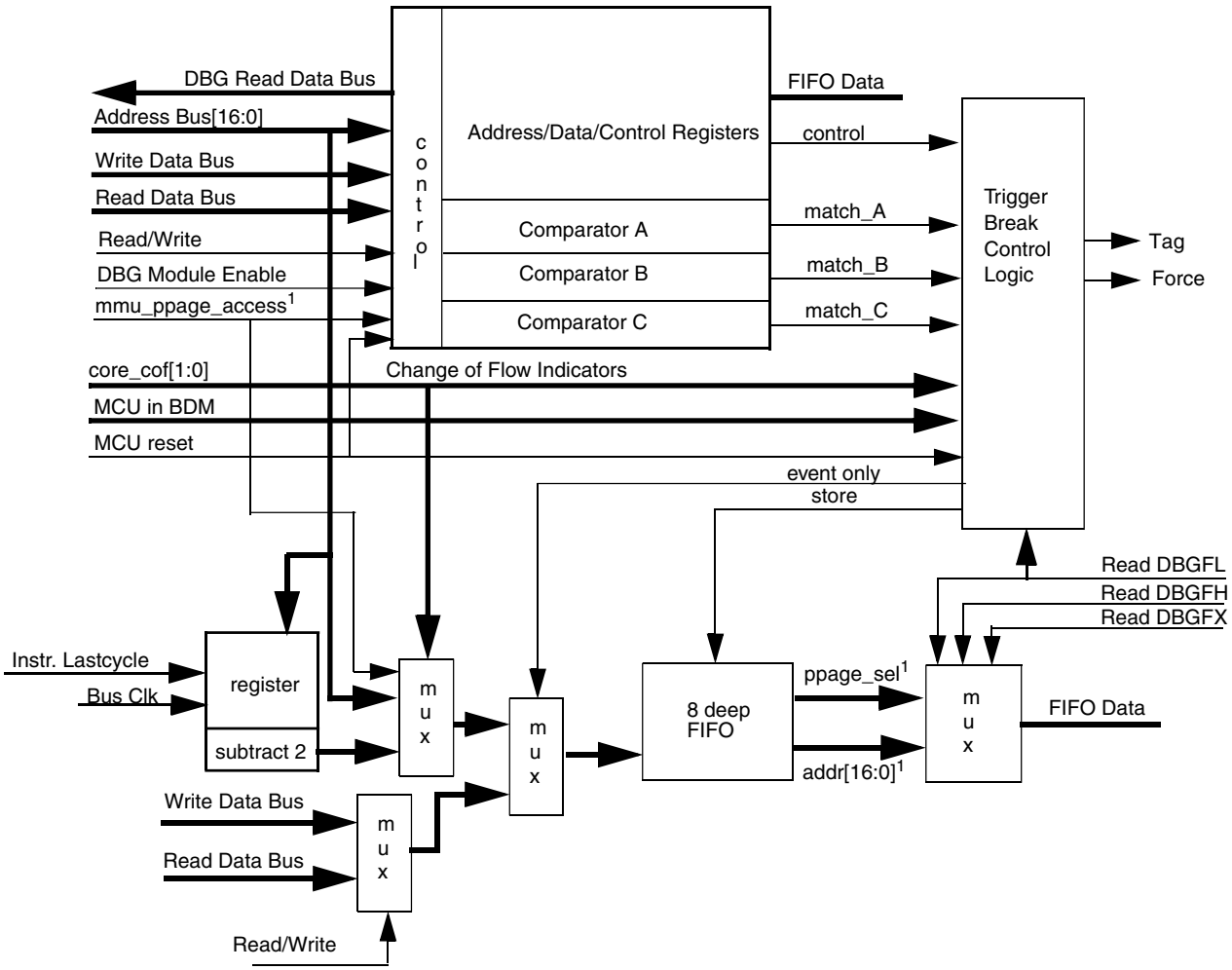


Figure 28-1. DBG block diagram

28.2 Signal description

The DBG module contains no external signals.

28.3 Memory map and registers

This section provides a detailed description of all DBG registers accessible to the end user.

DBG memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3010	Debug Comparator A High Register (DBG_CAH)	8	R/W	FFh	28.3.1/450
3011	Debug Comparator A Low Register (DBG_CAL)	8	R/W	FEh	28.3.2/451
3012	Debug Comparator B High Register (DBG_CBH)	8	R/W	00h	28.3.3/452
3013	Debug Comparator B Low Register (DBG_CBL)	8	R/W	00h	28.3.4/452
3014	Debug Comparator C High Register (DBG_CCH)	8	R/W	00h	28.3.5/453
3015	Debug Comparator C Low Register (DBG_CCL)	8	R/W	00h	28.3.6/454
3016	Debug FIFO High Register (DBG_FH)	8	R	00h	28.3.7/454
3017	Debug FIFO Low Register (DBG_FL)	8	R	00h	28.3.8/455
3018	Debug Comparator A Extension Register (DBG_CAX)	8	R/W	00h	28.3.9/456
3019	Debug Comparator B Extension Register (DBG_CBX)	8	R/W	00h	28.3.10/457
301A	Debug Comparator C Extension Register (DBG_CCX)	8	R/W	00h	28.3.11/458
301B	Debug FIFO Extended Information Register (DBG_FX)	8	R	00h	28.3.12/459
301C	Debug Control Register (DBG_C)	8	R/W	C0h	28.3.13/459
301D	Debug Trigger Register (DBG_T)	8	R/W	40h	28.3.14/460
301E	Debug Status Register (DBG_S)	8	R	01h	28.3.15/462
301F	Debug Count Status Register (DBG_CNT)	8	R	00h	28.3.16/463

28.3.1 Debug Comparator A High Register (DBG_CAH)

NOTE

All the bits in this register reset to 1 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 0h offset = 3010h

Bit	7	6	5	4	3	2	1	0
Read Write	CA[15:8]							
Reset	1	1	1	1	1	1	1	1

DBG_CAH field descriptions

Field	Description
CA[15:8]	Comparator A High Compare Bits The Comparator A High compare bits control whether Comparator A will compare the address bus bits [15:8] to a logic 1 or logic 0.

DBG_CAH field descriptions (continued)

Field	Description
	0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

28.3.2 Debug Comparator A Low Register (DBG_CAL)

NOTE

All the bits in this register reset to 1 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 1h offset = 3011h

Bit	7	6	5	4	3	2	1	0
Read Write	CA[7:0]							
Reset	1	1	1	1	1	1	1	0

DBG_CAL field descriptions

Field	Description
CA[7:0]	Comparator A Low The Comparator A Low compare bits control whether Comparator A will compare the address bus bits [7:0] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

28.3.3 Debug Comparator B High Register (DBG_CBH)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 2h offset = 3012h

Bit	7	6	5	4	3	2	1	0
Read Write	CB[15:8]							
Reset	0	0	0	0	0	0	0	0

DBG_CBH field descriptions

Field	Description
CB[15:8]	Comparator B High Compare Bits The Comparator B High compare bits control whether Comparator B will compare the address bus bits [15:8] to a logic 1 or logic 0.Not used in full mode. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

28.3.4 Debug Comparator B Low Register (DBG_CBL)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 3h offset = 3013h

Bit	7	6	5	4	3	2	1	0
Read Write	CB[7:0]							
Reset	0	0	0	0	0	0	0	0

DBG_CBL field descriptions

Field	Description
CB[7:0]	Comparator B Low The Comparator B Low compare bits control whether Comparator B will compare the address bus bits [7:0] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

28.3.5 Debug Comparator C High Register (DBG_CCH)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 4h offset = 3014h

Bit	7	6	5	4	3	2	1	0
Read Write	CC[15:8]							
Reset	0	0	0	0	0	0	0	0

DBG_CCH field descriptions

Field	Description
CC[15:8]	Comparator C High Compare Bits The Comparator C High compare bits control whether Comparator C will compare the address bus bits [15:8] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

28.3.6 Debug Comparator C Low Register (DBG_CCL)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 5h offset = 3015h

Bit	7	6	5	4	3	2	1	0
Read Write	CC[7:0]							
Reset	0	0	0	0	0	0	0	0

DBG_CCL field descriptions

Field	Description
CC[7:0]	Comparator C Low The Comparator C Low compare bits control whether Comparator C will compare the address bus bits [7:0] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

28.3.7 Debug FIFO High Register (DBG_FH)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 6h offset = 3016h

Bit	7	6	5	4	3	2	1	0
Read	F[15:8]							
Write								
Reset	0	0	0	0	0	0	0	0

DBG_FH field descriptions

Field	Description
F[15:8]	FIFO High Data Bits The FIFO High data bits provide access to bits [15:8] of data in the FIFO. This register is not used in event only modes and will read a $00 for valid FIFO words.

28.3.8 Debug FIFO Low Register (DBG_FL)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 7h offset = 3017h

Bit	7	6	5	4	3	2	1	0
Read	F[7:0]							
Write								
Reset	0	0	0	0	0	0	0	0

DBG_FL field descriptions

Field	Description
F[7:0]	FIFO Low Data Bits The FIFO Low data bits contain the least significant byte of data in the FIFO. When reading FIFO words, read DBGFX and DBGFH before reading DBGFL because reading DBGFL causes the FIFO pointers to advance to the next FIFO location. In event-only modes, there is no useful information in DBGFX and DBGFH so it is not necessary to read them before reading DBGFL.

28.3.9 Debug Comparator A Extension Register (DBG_CAX)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 8h offset = 3018h

Bit	7	6	5	4	3	2	1	0
Read	RWAEN	RWA	0					
Write								
Reset	0	0	0	0	0	0	0	0

DBG_CAX field descriptions

Field	Description
7 RWAEN	Read/Write Comparator A Enable Bit The RWAEN bit controls whether read or write comparison is enabled for Comparator A. 0 Read/Write is not used in comparison. 1 Read/Write is used in comparison.
6 RWA	Read/Write Comparator A Value Bit The RWA bit controls whether read or write is used in compare for Comparator A. The RWA bit is not used if RWAEN = 0. 0 Write cycle will be matched. 1 Read cycle will be matched.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

28.3.10 Debug Comparator B Extension Register (DBG_CBX)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 9h offset = 3019h

Bit	7	6	5	4	3	2	1	0
Read	RWBEN	RWB	0					
Write								
Reset	0	0	0	0	0	0	0	0

DBG_CBX field descriptions

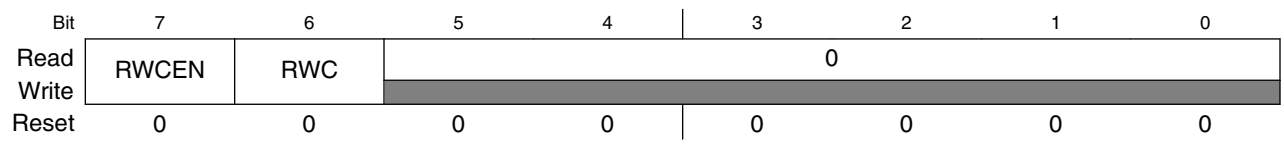
Field	Description
7 RWBEN	Read/Write Comparator B Enable Bit The RWBEN bit controls whether read or write comparison is enabled for Comparator B. In full modes, RWAEN and RWA are used to control comparison of R/W and RWBEN is ignored. 0 Read/Write is not used in comparison. 1 Read/Write is used in comparison.
6 RWB	Read/Write Comparator B Value Bit The RWB bit controls whether read or write is used in compare for Comparator B. The RWB bit is not used if RWBEN = 0.In full modes, RWAEN and RWA are used to control comparison of R/W and RWB is ignored. 0 Write cycle will be matched. 1 Read cycle will be matched.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

28.3.11 Debug Comparator C Extension Register (DBG_CCX)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + Ah offset = 301Ah



DBG_CCX field descriptions

Field	Description
7 RWCEN	Read/Write Comparator C Enable Bit The RWCEN bit controls whether read or write comparison is enabled for Comparator C. 0 Read/Write is not used in comparison. 1 Read/Write is used in comparison.
6 RWC	Read/Write Comparator C Value Bit The RWC bit controls whether read or write is used in compare for Comparator C. The RWC bit is not used if RWCEN = 0. 0 Write cycle will be matched. 1 Read cycle will be matched.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

28.3.12 Debug FIFO Extended Information Register (DBG_FX)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + Bh offset = 301Bh

Bit	7	6	5	4	3	2	1	0
Read	PPACC	0						Bit16
Write								
Reset	0	0	0	0	0	0	0	0

DBG_FX field descriptions

Field	Description
7 PPACC	PPAGE Access Indicator Bit This bit indicates whether the captured information in the current FIFO word is associated with an extended access through the PPAGE mechanism or not. This is indicated by the internal signal mmu_ppage_sel which is 1 when the access is through the PPAGE mechanism. 0 The information in the corresponding FIFO word is event-only data or an unpaged 17-bit CPU address with bit-16 = 0. 1 The information in the corresponding FIFO word is a 17-bit flash address with PPAGE[2:0] in the three most significant bits and CPU address[13:0] in the 14 least significant bits.
6–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 Bit16	Extended Address Bit 16 This bit is the most significant bit of the 17-bit core address.

28.3.13 Debug Control Register (DBG_C)

Address: 3010h base + Ch offset = 301Ch

Bit	7	6	5	4	3	2	1	0
Read	DBGEN	ARM	TAG	BRKEN	0			LOOP1
Write								
Reset	1	1	0	0	0	0	0	0

DBG_C field descriptions

Field	Description
7 DBGEN	DBG Module Enable Bit The DBGEN bit enables the DBG module. The DBGEN bit is forced to zero and cannot be set if the MCU is secure. 0 DBG not enabled. 1 DBG enabled.
6 ARM	Arm Bit The ARM bit controls whether the debugger is comparing and storing data in FIFO. 0 Debugger not armed. 1 Debugger armed.
5 TAG	Tag or Force Bit The TAG bit controls whether a debugger or comparator C breakpoint will be requested as a tag or force breakpoint to the CPU. The TAG bit is not used if BRKEN = 0. 0 Force request selected. 1 Tag request selected.
4 BRKEN	Break Enable Bit The BRKEN bit controls whether the debugger will request a breakpoint to the CPU at the end of a trace run, and whether comparator C will request a breakpoint to the CPU. 0 CPU break request not enabled. 1 CPU break request enabled.
3–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 LOOP1	Select LOOP1 Capture Mode This bit selects either normal capture mode or LOOP1 capture mode. LOOP1 is not used in event-only modes. 0 Normal operation - capture COF events into the capture buffer FIFO. 1 LOOP1 capture mode enabled. When the conditions are met to store a COF value into the FIFO, compare the current COF address with the address in comparator C. If these addresses match, override the FIFO capture and do not increment the FIFO count. If the address does not match comparator C, capture the COF address, including the PPACC indicator, into the FIFO and into comparator C..

28.3.14 Debug Trigger Register (DBG_T)

NOTE

The figure shows the values in POR or non-end-run reset. All the bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN=1 and BEGIN=0, the ARM and BRKEN bits are cleared but the remaining control bits in this register do not change after reset.

NOTE

The DBG trigger register (DBGT) can not be changed unless ARM=0.

Address: 3010h base + Dh offset = 301Dh

Bit	7	6	5	4	3	2	1	0
Read	TRGSEL	BEGIN	0		TRG			
Write								
Reset	0	1	0	0	0	0	0	0

DBG_T field descriptions

Field	Description
7 TRGSEL	Trigger Selection Bit The TRGSEL bit controls the triggering condition for the comparators. 0 Trigger on any compare address access. 1 Trigger if opcode at compare address is execute.
6 BEGIN	Begin/End Trigger Bit The BEGIN bit controls whether the trigger begins or ends storing of data in FIFO. 0 Trigger at end of stored data. 1 Trigger before storing data.
5–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
TRG	Trigger Mode Bits The TRG bits select the trigger mode of the DBG module. 0000 A only. 0001 A or B. 0010 A then B. 0011 Event only B. 0100 A then event only B. 0101 A and B (full mode). 0110 A and not B (full mode). 0111 Inside range. 1000 Outside range. 1001-1111 No trigger.

28.3.15 Debug Status Register (DBG_S)

NOTE

The figure shows the values in POR or non-end-run reset. The bits of AF, BF and CF are undefined and ARMF is reset to 0 in end-run reset. In the case of an end-trace to reset where DBGEN=1 and BEGIN=0, ARMF gets cleared by reset but AF, BF, and CF do not change after reset.

Address: 3010h base + Eh offset = 301Eh

Bit	7	6	5	4	3	2	1	0
Read	AF	BF	CF	0				ARMF
Write								
Reset	0	0	0	0	0	0	0	1

DBG_S field descriptions

Field	Description
7 AF	Trigger A Match Bit The AF bit indicates if Trigger A match condition was met since arming. 0 Comparator A did not match. 1 Comparator A match.
6 BF	Trigger B Match Bit The BF bit indicates if Trigger B match condition was met since arming. 0 Comparator B did not match. 1 Comparator B match.
5 CF	Trigger C Match Bit The CF bit indicates if Trigger C match condition was met since arming. 0 Comparator C did not match. 1 Comparator C match.
4–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 ARMF	Arm Flag Bit The ARMF bit indicates whether the debugger is waiting for trigger or waiting for the FIFO to fill. While DBGEN = 1, this status bit is a read-only image of the ARM bit in DBGC. 0 Debugger not armed. 1 Debugger armed.

28.3.16 Debug Count Status Register (DBG_CNT)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the CNT[3:0] bits do not change after reset.

Address: 3010h base + Fh offset = 301Fh

Bit	7	6	5	4	3	2	1	0
Read	0				CNT			
Write								
Reset	0	0	0	0	0	0	0	0

DBG_CNT field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CNT	FIFO Valid Count Bits The CNT bits indicate the amount of valid data stored in the FIFO. Table 1-20 shows the correlation between the CNT bits and the amount of valid data in FIFO. The CNT will stop after a count to eight even if more data is being stored in the FIFO. The CNT bits are cleared when the DBG module is armed, and the count is incremented each time a new word is captured into the FIFO. The host development system is responsible for checking the value in CNT[3:0] and reading the correct number of words from the FIFO because the count does not decrement as data is read out of the FIFO at the end of a trace run. 0000 No data valid. 0001 1 word valid. 0010 2 words valid. 0011 3 words valid. 0100 4 words valid. 0101 5 words valid. 0110 6 words valid. 0111 7 words valid. 1000 8 words valid.

28.4 Functional description

This section provides a complete functional description of the on-chip ICE system. The DBG module is enabled by setting the DBG_C[DBGEN] bit. Enabling the module allows the arming, triggering and storing of data in the FIFO. The DBG module is made up of three main blocks, the comparators, trigger break control logic and the FIFO.

28.4.1 Comparator

The DBG module contains three comparators, A, B, and C. Comparator A compares the core address bus with the address stored in the DBG_CAH and DBG_CAL registers. Comparator B compares the core address bus with the address stored in the DBG_CBH and DBG_CBL registers except in full mode, where it compares the data buses to the data stored in the DBG_CBL register. Comparator C compares the core address bus with the address stored in the DBG_CCH and DBG_CCL registers. Matches on comparators A, B, and C are signaled to the trigger break control (TBC) block.

28.4.1.1 RWA and RWAEN in full modes

In full modes ("A And B" and "A And Not B") DBG_CAX[RWAEN and DBG_CAX[RWA] are used to select read or write comparisons for both comparators A and B. To select write comparisons and the write data bus in Full Modes set DBG_CAX[RWAEN] = 1 and DBG_CAX[RWA] = 0, otherwise read comparisons and the read data bus will be selected. The DBG_CBX[RWBEN] and DBG_CBX[RWB] bits are not used and will be ignored in full modes.

28.4.1.2 Comparator C in loop1 capture mode

Normally comparator C is used as a third hardware breakpoint and is not involved in the trigger logic for the on-chip ICE system. In this mode, it compares the core address bus with the address stored in the DBG_CCX, DBG_CCH, and DBG_CCL registers. However, in loop1 capture mode, comparator C is managed by logic in the DBG module to track the address of the most recent change-of-flow event that was captured into the FIFO buffer. In loop1 capture mode, comparator C is not available for use as a normal hardware breakpoint.

When the DBG_C[ARM] and DBG_C[DBGEN] bits are set to one in loop1 capture mode, comparator C value registers are cleared to prevent the previous contents of these registers from interfering with the loop1 capture mode operation. When a COF event is detected, the address of the event is compared to the contents of the DBG_CCH and DBG_CCL registers to determine whether it is the same as the previous COF entry in the capture FIFO. If the values match, the capture is inhibited to prevent the FIFO from filling up with duplicate entries. If the values do not match, the COF event is captured into the FIFO and the DBG_CCH and DBG_CCL registers are updated to reflect the address of the captured COF event.

28.4.2 Breakpoints

A breakpoint request to the CPU at the end of a trace run can be created if the DBG_C[BRKEN] bit is set. The value of the DBG_T[BEGIN] bit determines when the breakpoint request to the CPU will occur. If the DBG_T[BEGIN] bit is set, begin-trigger is selected and the breakpoint request will not occur until the FIFO is filled with 8 words. If the DBG_T[BEGIN] bit is cleared, end-trigger is selected and the breakpoint request will occur immediately at the trigger cycle.

When traditional hardware breakpoints from comparators A or B are desired, set DBG_T[BEGIN] = 0 to select an end-trace run and set the trigger mode to either 0x0 (A-only) or 0x1 (A OR B) mode.

There are two types of breakpoint requests supported by the DBG module, tag-type and force-type. Tagged breakpoints are associated with opcode addresses and allow breaking just before a specific instruction executes. Force breakpoints are not associated with opcode addresses. The DBG_C[TAG] bit determines whether CPU breakpoint requests will be a tag-type or force-type breakpoints. When DBG_C[TAG] = 0, a force-type breakpoint is requested and it will take effect at the next instruction boundary after the request. When DBG_C[TAG] = 1, a tag-type breakpoint is registered into the instruction queue and the CPU will break if/when this tag reaches the head of the instruction queue and the tagged instruction is about to be executed.

28.4.2.1 Hardware breakpoints

Comparators A, B, and C can be used as three traditional hardware breakpoints whether the on-chip ICE real-time capture function is required or not. To use any breakpoint or trace run capture functions set DBG_C[DBGEN] = 1. DBG_C[BRKEN] and DBG_C[TAG] affect all three comparators. When DBG_C[BRKEN] = 0, no CPU breakpoints are enabled. When DBG_C[BRKEN] = 1, CPU breakpoints are enabled and the DBG_C[TAG] bit determines whether the breakpoints will be tag-type or force-type

breakpoints. To use comparators A and B as hardware breakpoints, set DBG_T = 0x81 for tag-type breakpoints and 0x01 for force-type breakpoints. This sets up an end-type trace with trigger mode "A OR B".

Comparator C is not involved in the trigger logic for the on-chip ICE system.

28.4.3 Trigger selection

The DBG_T[TRGSEL] bit is used to determine the triggering condition of the on-chip ICE system. DBG_T[TRGSEL] applies to both trigger A and B except in the event only trigger modes. By setting the DBG_T[TRGSEL] bit, the comparators will qualify a match with the output of opcode tracking logic. The opcode tracking logic is internal to each comparator and determines whether the CPU executed the opcode at the compare address. With the DBG_T[TRGSEL] bit cleared a comparator match is all that is necessary for a trigger condition to be met.

NOTE

If the DBG_T[TRGSEL] is set, the address stored in the comparator match address registers must be an opcode address for the trigger to occur.

28.4.4 Trigger break control (TBC)

The TBC is the main controller for the DBG module. Its function is to decide whether data should be stored in the FIFO based on the trigger mode and the match signals from the comparator. The TBC also determines whether a request to break the CPU should occur.

The DBG_C[TAG] bit controls whether CPU breakpoints are treated as tag-type or force-type breakpoints. The DBG_T[TRGSEL] bit controls whether a comparator A or B match is further qualified by opcode tracking logic. Each comparator has a separate circuit to track opcodes because the comparators could correspond to separate instructions that could be propagating through the instruction queue at the same time.

In end-type trace runs (DBG_T[BEGIN] = 0), when the comparator registers match, including the optional R/W match, this signal goes to the CPU break logic where DBG_C[BRKEN] determines whether a CPU break is requested and the DBG_C[TAG] control bit determines whether the CPU break will be a tag-type or force-type breakpoint. When DBG_T[TRGSEL] is set, the R/W qualified comparator match signal also passes through the opcode tracking logic. If/when it propagates through this logic, it will cause a

trigger to the ICE logic to begin or end capturing information into the FIFO. In the case of an end-type (DBG_T[BEGIN] = 0) trace run, the qualified comparator signal stops the FIFO from capturing any more information.

If a CPU breakpoint is also enabled, you would want DBG_C[TAG] and DBG_T[TRGSEL] to agree so that the CPU break occurs at the same place in the application program as the FIFO stopped capturing information. If DBG_T[TRGSEL] was 0 and DBG_C[TAG] was 1 in an end-type trace run, the FIFO would stop capturing as soon as the comparator address matched, but the CPU would continue running until a TAG signal could propagate through the CPUs instruction queue, which could take a long time in the case where changes of flow caused the instruction queue to be flushed. If DBG_T[TRGSEL] was one and DBG_C[TAG] was zero in an end-type trace run, the CPU would break before the comparator match signal could propagate through the opcode tracking logic to end the trace run.

In begin-type trace runs (DBG_T[BEGIN] = 1), the start of FIFO capturing is triggered by the qualified comparator signals, and the CPU breakpoint (if enabled by DBG_C[BRKEN]=1) is triggered when the FIFO becomes full. Since this FIFO full condition does not correspond to the execution of a tagged instruction, it would not make sense to use DBG_C[TAG] = 1 for a begin-type trace run.

28.4.4.1 Begin- and end-trigger

The definition of begin- and end-trigger as used in the DBG module are as follows:

- Begin-trigger: storage in FIFO occurs after the trigger and continues until 8 locations are filled.
- End-trigger: storage in FIFO occurs until the trigger with the least recent data falling out of the FIFO if more than 8 words are collected.

28.4.4.2 Arming the DBG module

Arming occurs by enabling the DBG module by setting the DBG_C[DBGEN] bit and by setting the DBG_C[ARM] bit. The DBG_C[ARM] and DBG_S[ARMF] bits are cleared when the trigger condition is met in end-trigger mode or when the FIFO is filled in begin-trigger mode. In the case of an end-trace where DBG_C[DBGEN] = 1 and DBG_T[BEGIN] = 0, DBG_C[ARM] and DBG_S[ARMF] are cleared by any reset to end the trace run that was in progress. The DBG_S[ARMF] bit is also cleared if DBG_C[ARM] is written to zero or when the DBG_C[DBGEN] bit is low. The TBC logic determines whether a trigger condition has been met based on the trigger mode and the trigger selection.

28.4.4.3 Trigger modes

The on-chip ICE system supports nine trigger modes. The trigger mode is used as a qualifier for either starting or ending the storing of data in the FIFO. When the match condition is met, the appropriate flag AF or BF is set in DBG_S register. Arming the DBG module clears the DBG_S[AF], DBG_S[BF], and DBG_S[CF] flags. In all trigger modes except for the event only modes change of flow addresses are stored in the FIFO. In the event only modes only the value on the data bus at the trigger event B comparator match address will be stored.

28.4.4.3.1 A only

In the A only trigger mode, if the match condition for A is met, the DBG_S[AF] flag is set.

28.4.4.3.2 A or B

In the A or B trigger mode, if the match condition for A or B is met, the corresponding flag(s) in the DBG_S register are set.

28.4.4.3.3 A then B

In the A then B trigger mode, the match condition for A must be met before the match condition for B is compared. When the match condition for A or B is met, the corresponding flag in the DBG_S register is set.

28.4.4.3.4 Event only B

In the event only B trigger mode, if the match condition for B is met, the DBG_S[BF] flag is set. The event only B trigger mode is considered a begin-trigger type and the DBG_T[BEGIN] bit is ignored.

28.4.4.3.5 A then event only B

In the A then event only B trigger mode, the match condition for A must be met before the match condition for B is compared. When the match condition for A or B is met, the corresponding flag in the DBG_S register is set. The A then event only B trigger mode is considered a begin-trigger type and the DBG_T[BEGIN] bit is ignored.

28.4.4.3.6 A and B (full mode)

In the A and B trigger mode, comparator A compares to the address bus and comparator B compares to the data bus. In the A and B trigger mode, if the match condition for A and B happen on the same bus cycle, both the DBG_S[AF] and DBG_S[BF] flags are set. If a match condition on only A or only B happens, no flags are set.

For breakpoint tagging operation with an end-trigger type trace, only matches from comparator A will be used to determine if the Breakpoint conditions are met and comparator B matches will be ignored.

28.4.4.3.7 A and not B (full mode)

In the A and not B trigger mode, comparator A compares to the address bus and comparator B compares to the data bus. In the A and not B trigger mode, if the match condition for A and not B happen on the same bus cycle, both the DBG_S[AF] and DBG_S[BF] flags are set. If a match condition on only A or only not B occur no flags are set.

For breakpoint tagging operation with an end-trigger type trace, only matches from comparator A will be used to determine if the breakpoint conditions are met and comparator B matches will be ignored.

28.4.4.3.8 Inside range, A ≤ address ≤ B

In the inside range trigger mode, if the match condition for A and B happen on the same bus cycle, both the DBG_S[AF] and DBG_S[BF] flags are set. If a match condition on only A or only B occur no flags are set.

28.4.4.3.9 Outside range, address < A or address > B

In the outside range trigger mode, if the match condition for A or B is met, the corresponding flag in the DBGS register is set.

The four control bits DBG_T[BEGIN] and DBG_T[TRGSEL], and DBG_C[BRKEN] and DBG_C[TAG], determine the basic type of debug run as shown in the following table. Some of the 16 possible combinations are not used (refer to the notes at the end of the table).

Table 28-1. Basic types of debug runs

BEGIN	TRGSEL	BRKEN	TAG	Type of debug run
0	0	0	x	Fill FIFO until trigger address (no CPU breakpoint - keep running)
0	0	1	0	Fill FIFO until trigger address, then force CPU breakpoint
0	0	1	1	Do not use
0	1	0	x	Fill FIFO until trigger opcode about to execute (no CPU breakpoint - keep running)
0	1	1	0	
0	1	1	1	Fill FIFO until trigger opcode about to execute (trigger causes CPU breakpoint)
1	0	0	x	Start FIFO at trigger address (No CPU breakpoint - keep running)
1	0	1	0	Start FIFO at trigger address, force CPU breakpoint when FIFO full
1	0	1	1	
1	1	0	x	Start FIFO at trigger opcode (No CPU breakpoint - keep running)
1	1	1	0	Start FIFO at trigger opcode, force CPU breakpoint when FIFO full
1	1	1	1	

28.4.5 FIFO

The FIFO is an eight word deep FIFO. In all trigger modes except for event only, the data stored in the FIFO will be change of flow addresses. In the event only trigger modes only the data bus value corresponding to the event is stored. In event only trigger modes, the high byte of the valid data from the FIFO will always read a 0x00.

28.4.5.1 Storing data in FIFO

In all trigger modes except for the event only modes, the address stored in the FIFO will be determined by the change of flow indicators from the core. The signal core_cof[1] indicates the current core address is the destination address of an indirect JSR or JMP instruction, or a RTS or RTI instruction or interrupt vector and the destination address should be stored. The signal core_cof[0] indicates that a conditional branch was taken and that the source address of the conditional branch should be stored.

28.4.5.2 Storing with begin-trigger

Storing with begin-trigger can be used in all trigger modes. Once the DBG module is enabled and armed in the begin-trigger mode, data is not stored in the FIFO until the trigger condition is met. Once the trigger condition is met the DBG module will remain armed until 8 words are stored in the FIFO. If the core_cof[1] signal becomes asserted, the current address is stored in the FIFO. If the core_cof[0] signal becomes asserted, the address registered during the previous last cycle is decremented by two and stored in the FIFO.

28.4.5.3 Storing with end-trigger

Storing with end-trigger cannot be used in event-only trigger modes. After the DBG module is enabled and armed in the end-trigger mode, data is stored in the FIFO until the trigger condition is met. If the core_cof[1] signal becomes asserted, the current address is stored in the FIFO. If the core_cof[0] signal becomes asserted, the address registered during the previous last cycle is decremented by two and stored in the FIFO. When the trigger condition is met, the DBG_C[ARM] and DBG_S[ARMF] will be cleared and no more data will be stored. In non-event only end-trigger modes, if the trigger is at a change of flow address the trigger event will be stored in the FIFO.

28.4.5.4 Reading data from FIFO

The data stored in the FIFO can be read using BDM commands provided the DBG module is enabled and not armed (DBG_C[DBGEN] = 1 and DBG_C[ARM] = 0). The FIFO data is read out first-in-first-out. By reading the DBG_CNT[CNT] bits at the end of a trace run, the number of valid words can be determined. The FIFO data is read by optionally reading the DBG_FH register followed by the DBG_FL register. Each time the DBG_FL register is read, the FIFO is shifted to allow reading of the next word, however, the count does not decrement. In event-only trigger modes where the FIFO will contain only the data bus values stored, to read the FIFO only DBG_FL needs to be accessed.

The FIFO is normally read only while DBG_C[ARM] = 0 and DBG_S[ARMF] = 0, however, reading the FIFO while the DBG module is armed will return the data value in the oldest location of the FIFO and the TBC will not allow the FIFO to shift. This action could cause a valid entry to be lost because the unexpected read blocked the FIFO advance.

If the DBG module is not armed and the DBG_FL register is read, the TBC will store the current opcode address. Through periodic reads of the DBG_FH and DBG_FL registers while the DBG module is not armed, host software can provide a histogram of program execution This is called profile mode.

28.4.6 Interrupt priority

When DBG_T[TRGSEL] is set and the DBG module is armed to trigger on begin- or end-trigger types, a trigger is not detected in the condition where a pending interrupt occurs at the same time that a target address reaches the top of the instruction pipe. In these conditions, the pending interrupt has higher priority and code execution switches to the interrupt service routine.

When DBG_T[TRGSEL] is clear and the DBG module is armed to trigger on end-trigger types, the trigger event is detected on a program fetch of the target address, even when an interrupt becomes pending on the same cycle. In these conditions, the pending interrupt has higher priority, the exception is processed by the core and the interrupt vector is fetched. Code execution is halted before the first instruction of the interrupt service routine is executed. In this scenario, the DBG module will have cleared DBG_C[ARM] without having recorded the change-of-flow that occurred as part of the interrupt exception. Note that the stack will hold the return addresses and can be used to reconstruct execution flow in this scenario.

When DBG_T[TRGSEL] is clear and the DBG module is armed to trigger on begin-trigger types, the trigger event is detected on a program fetch of the target address, even when an interrupt becomes pending on the same cycle. In this scenario, the FIFO captures

the change of flow event. Because the system is configured for begin-trigger, the DBG remains armed and does not break until the FIFO has been filled by subsequent change of flow events.

28.5 Resets

The DBG module cannot cause an MCU reset.

There are two different ways this module will respond to reset depending upon the conditions before the reset event. If the DBG module was setup for an end trace run with DBG_C[DBGEN] = 1 and DBG_T[BEGIN] = 0, DBG_C[ARM], DBG_S[ARMF], and DBG_C[BRKEN] are cleared but the reset function on most DBG control and status bits is overridden so a host development system can read out the results of the trace run after the MCU has been reset. In all other cases including POR, the DBG module controls are initialized to start a begin trace run starting from when the reset vector is fetched. The conditions for the default begin trace run are:

- DBG_CAX = 0x00, DBG_CAH=0xFF, DBG_CAL=0xFE so comparator A is set to match when the 16-bit CPU address 0xFFFE appears during the reset vector fetch
- DBG_C = 0xC0 to enable and arm the DBG module
- DBG_T = 0x40 to select a force-type trigger, a BEGIN trigger, and A-only trigger mode

Appendix A
Revision history

A.1 Revision history

The following table provides a revision history for this document.

Table A-1. Revision history

Rev. No.	Date	Substantial Changes
2	10/2019	Initial public release.

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