Jameco Part Number 1211897

FAIRCHILD SEMICONDUCTOR®

July 1999
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74LVTH273
Low Voltage Octal D-Type Flip-Flop with Clear

General Description

The LVTH273 is a high-speed, low-power positive-edge-triggered octal D-type flip-flop featuring separate D-type inputs for each flip-flop. A buffered Clock (CP) and Clear ($\overline{CLR}$) are common to all flip-flops.

The state of each D-type input, one setup time before the positive clock transition, is transferred to the corresponding flip-flop's output.

The LVTH273 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These octal flip-flops are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH273 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold on the data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Outputs source/sink −32 mA/+64 mA
- Functionally compatible with the 74 series 273
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V

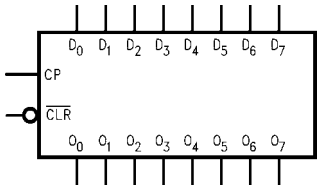
Ordering Code:

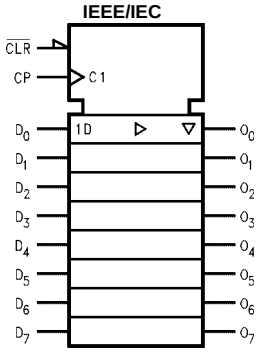
Order Number	Package Number	Package Description
74LVTH273WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVTH273SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVTH273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVTH273MTCX_NL (Note 1)	MTC20	Pb-Free 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

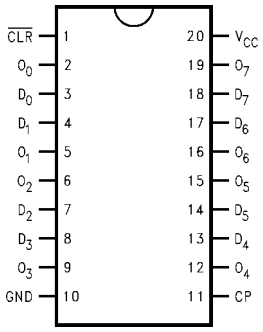
Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Logic Symbols





Connection Diagram



Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{CLR}$	Clear
O_0–O_7	Outputs

Truth Table

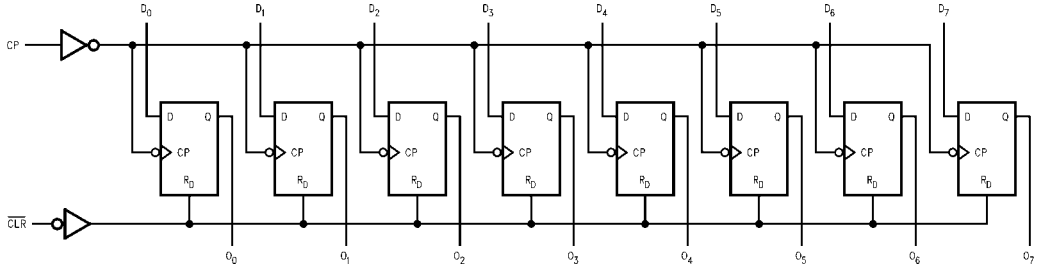
Inputs			Outputs
D_n	CP	$\overline{CLR}$	O_n
H	⌐	H	H
L	⌐	H	L
X	H or L	H	O_o
X	X	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition
O_o = Previous O_o before HIGH-to-LOW of CP

Functional Description

The LVTH273 consists of eight positive-edge-triggered flip-flops with individual D-type inputs. The buffered Clock and Clear are common to all flip-flops. The eight flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. When the Clock is either HIGH or LOW, the D-input signal has no effect at the output. When the Clear ($\overline{CLR}$) is LOW, all Outputs will be forced LOW.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in HIGH or LOW State (Note 3)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	V_O > V_{CC} Output at HIGH State	mA
		128	V_O > V_{CC} Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH Level Output Current		−32	mA
I_{OL}	LOW Level Output Current		64	mA
T_A	Free-Air Operating Temperature	−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note 2: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 3: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	T_A = −40°C to +85°C			Units	Conditions
				Min	Typ (Note 4)	Max		
V_{IK}	Input Clamp Diode Voltage		2.7			−1.2	V	I_I = −18 mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0			V	$V_O \le 0.1V$ or
V_{IL}	Input LOW Voltage		2.7–3.6			0.8	V	$V_O \ge V_{CC} - 0.1V$
V_{OH}	Output HIGH Voltage		2.7–3.6	V_{CC} − 0.2			V	I_{OH} = −100 μA
			2.7	2.4				I_{OH} = −8 mA
			3.0	2.0				I_{OH} = −32 mA
V_{OL}	Output LOW Voltage		2.7			0.2	V	I_{OL} = 100 μA
			2.7			0.5		I_{OL} = 24 mA
			3.0			0.4		I_{OL} = 16 mA
			3.0			0.5		I_{OL} = 32 mA
			3.0			0.55		I_{OL} = 64 mA
$I_{I(HOLD)}$	Bushold Input Minimum Drive		3.0	75			μA	V_I = 0.8V
				−75				V_I = 2.0V
$I_{I(OD)}$	Bushold Input Over-Drive		3.0	500			μA	(Note 5)
	Current to Change State			−500				(Note 6)
I_I	Input Current		3.6			10	μA	V_I = 5.5V
		Control Pins	3.6			±1	μA	V_I = 0V or V_{CC}
		Data Pins	3.6			−5	μA	V_I = 0V
						1	μA	V_I = V_{CC}
I_{OFF}	Power Off Leakage Current		0			±100	μA	0V ≤ V_I or V_O ≤ 5.5V
I_{CCH}	Power Supply Current		3.6			0.19	mA	Outputs HIGH
I_{CCL}	Power Supply Current		3.6			5	mA	Outputs LOW
ΔI_{CC}	Increase in Power Supply Current		3.6			0.2	mA	One Input at V_{CC} − 0.6V
	(Note 7)							Other Inputs at V_{CC} or GND

Note 4: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

DC Electrical Characteristics (Continued)

Note 5: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 6: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 8)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions
			Min	Typ	Max		$C_L = 50$ pF, $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$					Units
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
			Min	Typ (Note 10)	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		150			150		MHz
t_{PLH}	Propagation Delay		1.7		4.9	1.7	5.5	ns
t_{PHL}	CP to O_n		1.9		4.8	1.9	5.1	
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n		1.6		4.8	1.6	5.4	ns
t_W	Pulse Duration		3.3			3.3		ns
t_S	Setup Time	Data HIGH or LOW before CP	2.3			2.7		ns
		$\overline{CLR}$ HIGH before CP	2.3			2.7		
t_H	Hold Time	Data HIGH or LOW after CP	0			0		ns

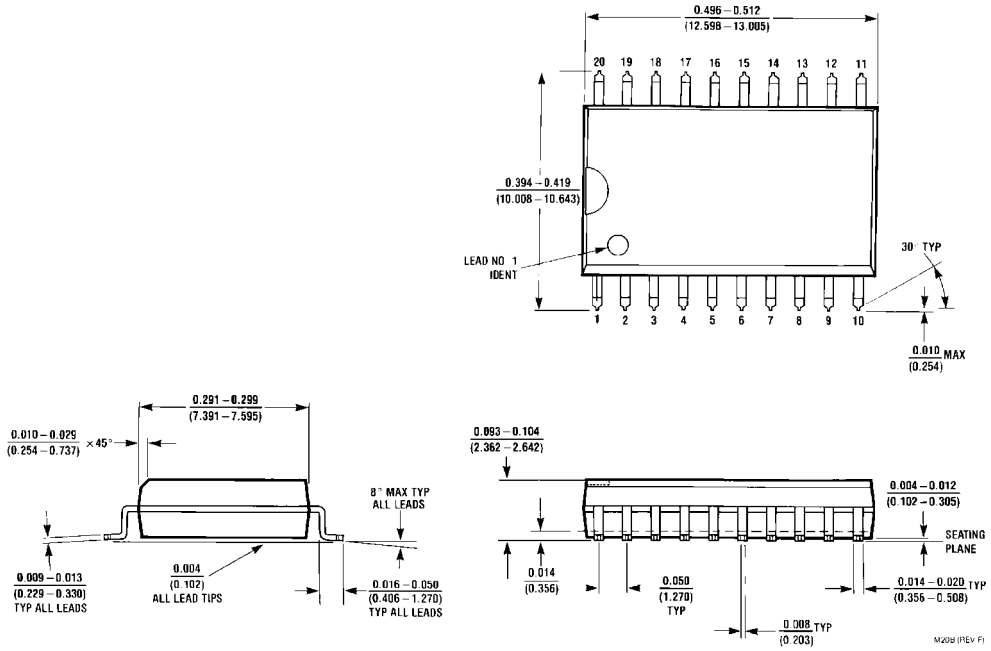
Note 10: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Capacitance (Note 11)

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}	3	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}	6	pF

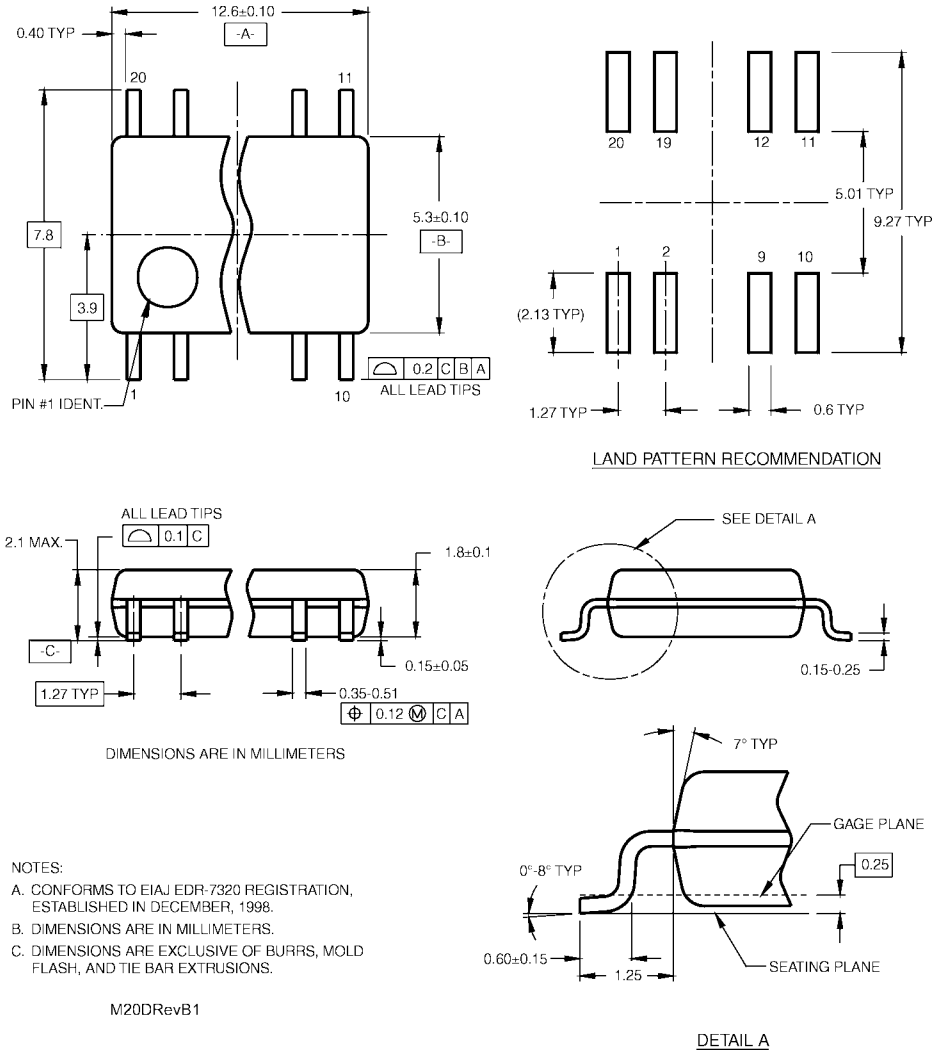
Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

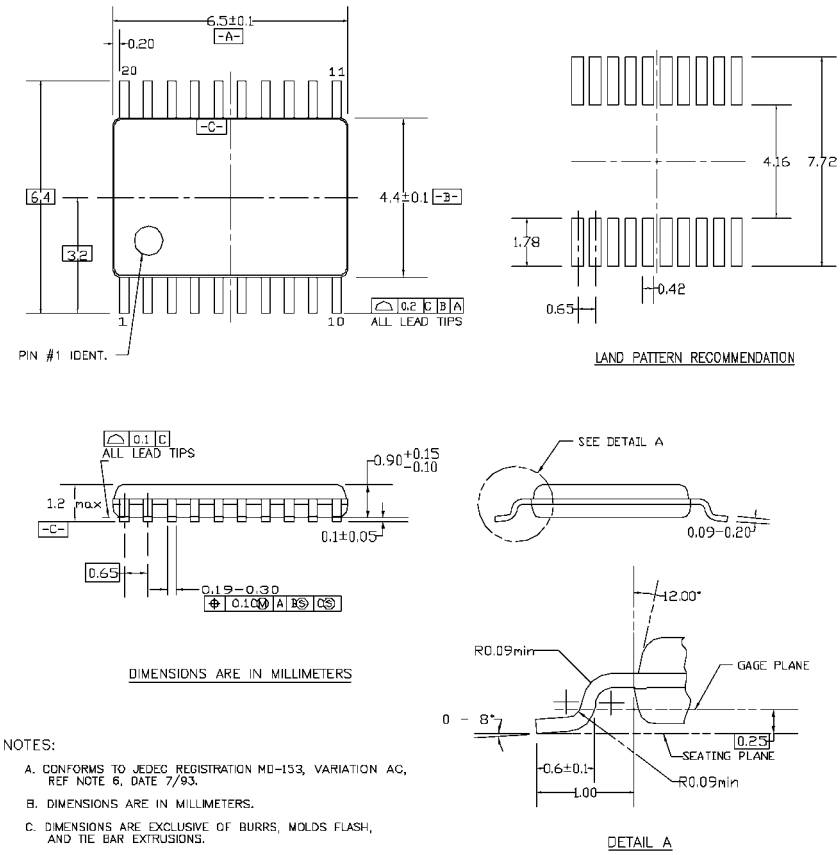
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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