# LC87F0N04A

**CMOS IC**
**4.5K-byte FROM and 128-byte RAM integrated**

# 8-bit 1-chip Microcontroller

**ON Semiconductor®**

http://onsemi.com

## Overview

The LC87F0N04A is an 8-bit microcomputer that, integrates on a single chip a number of hardware features such as 4.5K-byte flash ROM, 128-byte RAM, 16-bit timers/counters, a 16-bit timer, an asynchronous/synchronous SIO interface, motor control 10-bit PWM, two Analog Comparators, a 6-channel AD converter, a system clock frequency divider, an internal reset and an interrupt feature.

## Features

■Flash ROM
- 4608 × 8 bits (4096 + 512-byte)
- Capable of On-board programming
  with wide range (2.8 to 5.5V) of voltage source.
- Block-erasable in 128 byte units
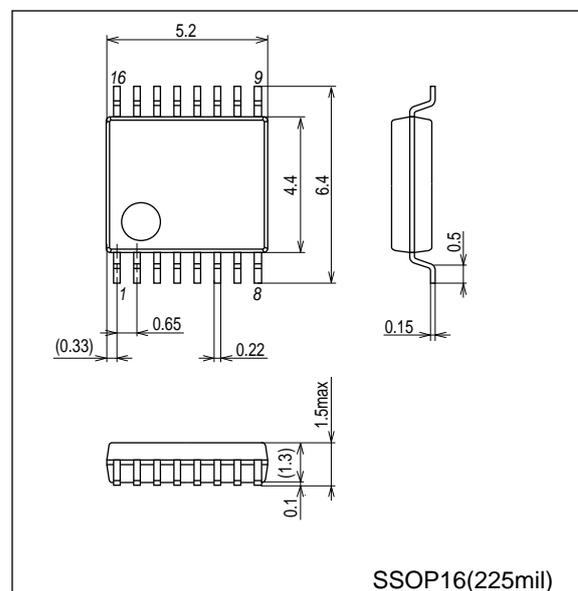- Writable in 2-byte units

■RAM
- 128 × 9 bits

■Package Form
- SSOP16 (225mil) : Lead-/Halogen-free type

## Package Dimensions

unit : mm (typ)
3178B



SSOP16(225mil)

■Minimum Bus Cycle
- 100.0ns (10MHz at $V_{DD}$=2.8V to 5.5V)

Note: The bus cycle time here refers to the ROM read speed.

■ Ports
- Normal withstand voltage I/O ports
  Ports I/O direction can be designated in 1 bit units     12(P00 to P03, P1n)
- Reset pin     1 ($\overline{RES}$)
- On-chip Debugger pin     1 (OWP0)
- Power pins     2 ($V_{SS}$, $V_{DD}$)

■Timers
- Timer 0: 16-bit timer/counter with a capture register.
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
  - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register)
    + 8-bit counter (with an 8-bit capture register)
  - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  - Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) × 2 channels
  - Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  - Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs)
    (toggle outputs also possible from the lower-order 8 bits)
  - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs)
    (The lower-order 8 bits can be used as PWM.)
- Base timer
  1) The clock is selectable from system clock, and timer 0 prescaler output.
  2) Interrupts are programmable in 5 different time schemes

■SIO
- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■AD Converter: 10 bits/8 bits × 6 channels
- 10/8 bits AD converter resolution selectable
- Auto start function (It links an interrupt factor of Motor control PWM)

■Remote Control Receiver Circuit (sharing pins with P11, INT3)
- Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)

■Clock Output Function
- Can generate clock outputs with a frequency of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of the source clock selected as the system clock.

■Analog Comparator × 2 channels
- Analog comparator Interrupt.
- Analog comparator reference selectable (External input / Programmable on-chip voltage reference).
  The voltage reference has 2 ranges with 16-level voltage levels in each range.
  Rang1: CMP1vref1= (CMP1vref-Register<3:0> + 1 )/16 × $V_{DD}$ × 0.64
         CMP2vref2= (CMP2vref-Register<3:0> + 1 )/16 × $V_{DD}$ × 0.64
  Rang2: CMP1vref1= (CMP1vref-Register<3:0> + 1 )/64 × $V_{DD}$ × 0.64
         CMP2vref2= (CMP2vref-Register<3:0> + 1 )/64 × $V_{DD}$ × 0.64

■MCPWM2: Motor control 10bits PWM with Full-Bridge
- Dead time is programmable.
- Forced stop is possible by the output of the analog comparator and the INT terminals.
- Edge-aligned / center-aligned selectable.

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■Watchdog Timer
- Can generate the internal reset signal on a timer overflow monitored by the WDT-dedicated low-speed RC oscillation clock (30kHz).
- Allows selection of continue, stop, or hold mode operation of the counter on entry into the HALT/HOLD mode.

■Interrupts
- 14 sources, 9 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

| No. | Vector Address | Level | Interrupt Source |
|-----|----------------|-------|------------------|
| 1 | 00003H | X or L | INT0 |
| 2 | 0000BH | X or L | INT1 |
| 3 | 00013H | H or L | INT2/T0L |
| 4 | 0001BH | H or L | INT3/base timer |
| 5 | 00023H | H or L | T0H |
| 6 | 0002BH | H or L | T1L/T1H |
| 7 | 00033H | H or L | - |
| 8 | 0003BH | H or L | SIO1/PWM |
| 9 | 00043H | H or L | ADC |
| 10 | 0004BH | H or L | CMP1/CMP2 |

- Priority levels $X > H > L$
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 64levels (The stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits      (5 tCYC execution time)
- 24 bits × 16 bits    (12 tCYC execution time)
- 16 bits ÷ 8 bits      (8 tCYC execution time)
- 24 bits ÷ 16 bits    (12 tCYC execution time)

■Oscillation Circuits
- Internal oscillation circuits
  Medium-speed RC oscillation circuit :   For system clock (1MHz)
  High-speed RC oscillation circuit :      For system clock (10MHz)
  Low-speed RC oscillation circuit :       For watch dog timer (30kHz)

■System Clock Divider Function
- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).

■Internal Reset Function
- Power-on reset (POR) function
  1) POR reset is generated only at power-on time.
  2) The POR release level can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) through option configuration.
- Low-voltage detection reset (LVD) function
  1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2) The use / disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, 4.28V).

■Standby Function
- ● HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  - 1) Oscillation is not halted automatically.
  - 2) There are three ways of resetting the HALT mode.
    - (1) Setting the reset pin to the low level
    - (2) System resetting by watchdog timer or low-voltage detection
    - (3) Occurrence of an interrupt
- ● HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  - 1) The RC oscillators automatically stop operation.
  - 2) There are four ways of resetting the HOLD mode.
    - (1) Setting the reset pin to the lower level.
    - (2) System resetting by watchdog timer or low-voltage detection
    - (3) Having an interrupt source established at either INT0, INT1, INT2
      - * INT0 and INT1 HOLD mode reset is available only when level detection is set.

■On-chip Debugger
- • Supports software debugging with the IC mounted on the target board.

■Data Security Function (flash versions only)
- • Protects the program data stored in flash memory from unauthorized read or copy.
  Note: This data security function does not necessarily provide absolute data security.

■Development Tools
- • On-chip-debugger : TCB87 TypeC + LC87F0N04A

■Programming Boards

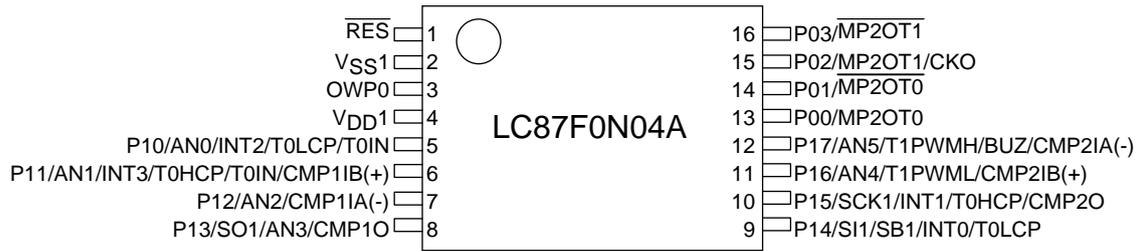| Package | Programming boards |
|---|---|
| SSOP16(225mil) | W87F0NS |

■Flash ROM Programmer

| Maker | | Model | Supported version | Device |
|---|---|---|---|---|
| Flash Support Group, Inc. (FSG) | Single Programmer | AF9709/AF9709B/AF9709C (Including Ando Electric Co., Ltd. models) | Rev 03.28 or later | 87F008SU (3B247) |
| | Gang Programmer | AF9723/AF9723B(Main body) (Including Ando Electric Co., Ltd. models) | - | - |
| | | AF9833(Unit) (Including Ando Electric Co., Ltd. models) | - | - |
| Sanyo | Single/Gang Programmer | SKK / SKK Type B (SanyoFWS) | Application Version 1.07 or later | LC87F0N04 |
| | Gang Programmer | SKK-4G (SanyoFWS) | Chip Data Version 2.40 or later | |
| | In-circuit/Gang Programmer | SKK-DBG Type C (SanyoFWS) | Application Version 1.07 or later Chip Data Version 2.40 or later | |

For information about AF-Series:
Flash Support Group, Inc.
TEL: +81-53-459-1050
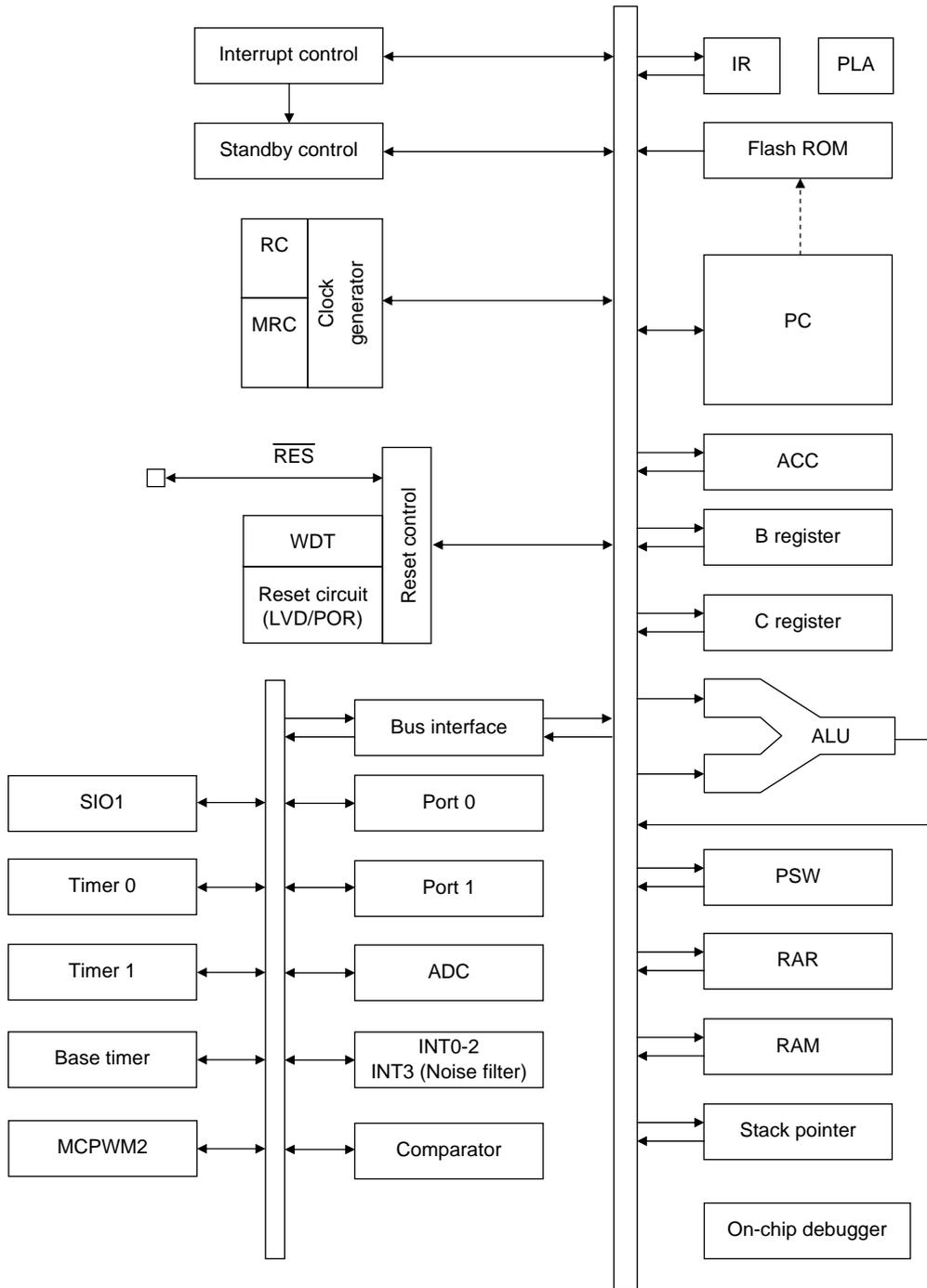E-mail: sales@j-fsg.co.jp

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## Pin Assignment



```
       ___
       RES ⊏ 1        ◯         16 ⊐ P03/MP2OT1
      VSS1 ⊏ 2                   15 ⊐ P02/MP2OT1/CKO
      OWP0 ⊏ 3                   14 ⊐ P01/MP2OT0
      VDD1 ⊏ 4     LC87F0N04A    13 ⊐ P00/MP2OT0
P10/AN0/INT2/T0LCP/T0IN ⊏ 5      12 ⊐ P17/AN5/T1PWMH/BUZ/CMP2IA(-)
P11/AN1/INT3/T0HCP/T0IN/CMP1IB(+) ⊏ 6  11 ⊐ P16/AN4/T1PWML/CMP2IB(+)
P12/AN2/CMP1IA(-) ⊏ 7            10 ⊐ P15/SCK1/INT1/T0HCP/CMP2O
P13/SO1/AN3/CMP1O ⊏ 8            9  ⊐ P14/SI1/SB1/INT0/T0LCP
```

Top view

SANYO: SSOP16(225mil) "Lead-/Halogen-free Type"

| SSOP16 | NAME |
|--------|------|
| 1 | $\overline{\text{RES}}$ |
| 2 | V$_{SS}$1 |
| 3 | OWP0 |
| 4 | V$_{DD}$1 |
| 5 | P10/AN0/INT2/T0LCP/T0IN |
| 6 | P11/AN1/INT3/T0HCP/T0IN/CMP1IB(+) |
| 7 | P12/AN2/CMP1IA(-) |
| 8 | P13/SO1/AN3/CMP1O |

| SSOP16 | NAME |
|--------|------|
| 9 | P14/SI1/SB1/INT0/T0LCP |
| 10 | P15/SCK1/INT1/T0HCP/CMP2O |
| 11 | P16/AN4/T1PWML/CMP2IB(+) |
| 12 | P17/AN5/T1PWMH/CMP2IA(-)/BUZ |
| 13 | P00/MP2OT0 |
| 14 | P01/$\overline{\text{MP2OT0}}$ |
| 15 | P02/MP2OT1/CKO |
| 16 | P03/$\overline{\text{MP2OT1}}$ |

## System Block Diagram

## Pin Description

| Pin Name | I/O | Description | Option |
|---|---|---|---|
| V$_{SS}$1 | - | - power supply pin | No |
| V$_{DD}$1 | - | + power supply pin | No |
| Port 0<br><br>P00 to P03 | I/O | • 4-bit I/O port<br>• I/O specifiable in 1 bit units<br>• Pull-up resistors can be turned on and off in 1 bit units.<br>• Pin functions<br>  P00: MP2OT0(PWM output)<br>  P01: $\overline{\text{MP2OT0}}$ (PWM output)<br>  P02: MP2OT1(PWM output) / System clock output<br>  P03: $\overline{\text{MP2OT1}}$ (PWM output) | Yes |
| Port 1<br><br>P10 to P17 | I/O | • 8-bit I/O port<br>• I/O specifiable in 1 bit units<br>• Pull-up resistors can be turned on and off in 1 bit units.<br>• Pin functions<br>  P10: AN0(AD converter input) / INT2 input / HOLD reset input /<br>       timer 0 event input / timer 0L capture input<br>  P11: AN1(AD converter input) / INT3 input (with noise filter) /<br>       timer 0 event input / timer 0H capture input / CMP1(+) input<br>  P12: AN2(AD converter input) / CMP1(-) input<br>  P13: SIO1 data output / AN3(AD converter input) / CMP1 output<br>  P14: SIO1 data input / bus I/O / INT0 input / HOLD reset input / timer 0L capture input<br>  P15: SIO1 clock I/O / INT1 input / HOLD reset input / timer 0H capture input / CMP2 output<br>  P16: Timer 1PWML output / CMP2(+) input / AN4(AD converter input)<br>  P17: Timer 1PWMH output / beeper output / CMP2(-) input / AN5(AD converter input)<br><br>Interrupt acknowledge type<br><br>{TABLE BELOW} | Yes |
| OWP0 | I/O | On-chip debugger (exclusive pin) | No |
| $\overline{\text{RES}}$ | I/O | External reset Input / internal reset output | No |

Interrupt acknowledge type

| | Rising | Falling | Rising & Falling | H level | L level |
|---|---|---|---|---|---|
| INT0 | enable | enable | disable | enable | enable |
| INT1 | enable | enable | disable | enable | enable |
| INT2 | enable | enable | enable | disable | disable |
| INT3 | enable | enable | enable | disable | disable |

## Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

| Port Name | Option selected in units of | Option type | Output type | Pull-up resistor |
|---|---|---|---|---|
| P00 to P03 | 1 bit | 1 | CMOS | Programmable |
| P10 to P17 | | 2 | Nch-open drain | Programmable |

## User Option Table

| Option Name | Option to be Applied on | Flash-ROM Version | Option Selected in Units of | Option Selection |
|---|---|---|---|---|
| Port output type | P00 to P03 | ○ | 1 bit | CMOS |
| | | | | Nch-open drain |
| | P10 to P17 | ○ | 1 bit | CMOS |
| | | | | Nch-open drain |
| Low-voltage detection reset function | Detect function | ○ | - | Enable:Use |
| | | | | Disable:Not Used |
| | Detect level | ○ | - | 7-level |
| Power-on reset function | Power-On reset level | ○ | - | 8-level |

## Recommended Unused Pin Connections

| Port Name | Recommended Unused Pin Connections | |
|---|---|---|
| | Board | Software |
| P00 to P03 | Open | Output low |
| P10 to P17 | Open | Output low |

## On-chip Debugger Pin Connection Requirements

Install and connect a limiting resistor ($100\Omega$) to the on-chip debugger dedicated pin (OWP0) on the user board and pull the pin down ($100k\Omega$). It is recommended to install a dedicated connector to accept the cable to the debugging tool (TCB87 Type C). The connector must accommodate three lines, i.e., $V_{SS}1$, OWP0, and $V_{DD}1$.
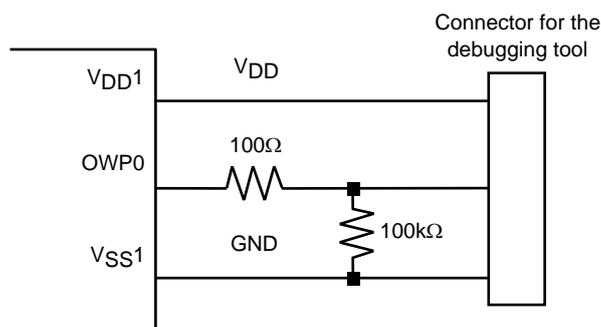
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**Absolute Maximum Ratings** at Ta = 25°C, $V_{SS}1 = 0V$

| Parameter | | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{DD}$[V] | min | typ | max | unit |
| Maximum supply voltage | | $V_{DD}$ max | $V_{DD}1$ | | | -0.3 | | +6.5 | V |
| Input voltage | | $V_I$ | $\overline{RES}$ | | | -0.3 | | $V_{DD}$+0.3 | |
| Input/output voltage | | $V_{IO}$ | Ports 0, 1 | | | -0.3 | | $V_{DD}$+0.3 | |
| High level output current | Peak output current | IOPH(1) | Ports 0, 1 | CMOS output select Per 1 applicable pin | | -10 | | | mA |
| | Mean output current (Note 1-1) | IOMH(1) | Ports 0, 1 | CMOS output select Per 1 applicable pin | | -7.5 | | | |
| | Total output current | ΣIOAH(1) | Ports 0 | Total of all applicable pins | | -25 | | | |
| | | ΣIOAH(2) | Ports 1 | Total of all applicable pins | | -25 | | | |
| Low level output current | Peak output current | IOPL(1) | Ports0, 1 | Per 1 applicable pin | | | | 20 | |
| | Mean output current (Note 1-1) | IOML(1) | Ports 0, 1 | Per 1 applicable pin | | | | 15 | |
| | Total output current | ΣIOAL(1) | Ports 0 | Total of all applicable pins | | | | 45 | |
| | | ΣIOAL(2) | Ports 1 | Total of all applicable pins | | | | 45 | |
| Power dissipation | | Pdmax | SSOP16 | Ta=-40 to +85°C Package with thermal resistance board (Note 1-2) | | | | 238 | mW |
| Operating ambient temperature | | Topr | | | | -40 | | +85 | °C |
| Storage ambient temperature | | Tstg | | | | -55 | | +125 | |

Note 1-1: The mean output current is a mean value measured over 100ms.
Note 1-2: SEMI standards thermal resistance board (size: 76.1×114.3×1.6tmm, glass epoxy) is used.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Allowable Operating Conditions** at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Operating supply voltage | $V_{DD}(1)$ | $V_{DD}1$ | $0.291\mu s \leq tCYC \leq 200\mu s$ | | 2.8 | | 5.5 | V |
| Memory sustaining supply voltage | $V_{HD}$ | $V_{DD}1$ | RAM and register contents sustained in HOLD mode. | | 2.0 | | | |
| High level input voltage | $V_{IH}(1)$ | Ports 1 | | 2.8 to 5.5 | $0.3V_{DD}+0.7$ | | $V_{DD}$ | |
| | $V_{IH}(2)$ | Ports 0 | | 2.8 to 5.5 | $0.3V_{DD}+0.7$ | | $V_{DD}$ | |
| | $V_{IH}(3)$ | $\overline{RES}$ | | 2.8 to 5.5 | $0.75V_{DD}$ | | $V_{DD}$ | |
| Low level input voltage | $V_{IL}(1)$ | Ports 1 | | 4.0 to 5.5 | $V_{SS}$ | | $0.1V_{DD}+0.4$ | |
| | | | | 2.8 to 4.0 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(2)$ | Ports 0 | | 4.0 to 5.5 | $V_{SS}$ | | $0.15V_{DD}+0.4$ | |
| | | | | 2.8 to 4.0 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(3)$ | $\overline{RES}$ | | 2.8 to 5.5 | $V_{SS}$ | | $0.25V_{DD}$ | |
| Instruction cycle time (Note 2-1) | tCYC | | | 2.8 to 5.5 | 0.291 | | 200 | μs |
| Oscillation frequency range | FmMRC(1) | | Internal High-speed RC oscillation. (Note 2-2) | 2.8 to 5.5 | 9.7 | 10.0 | 10.3 | MHz |
| | FmMRC(2) | | Internal High-speed RC oscillation. Ta=0°C to 85°C (Note 2-2) | 2.8 to 5.5 | 9.75 | 10.0 | 10.25 | MHz |
| | FmRC | | Internal Medium-speed RC oscillation | 2.8 to 5.5 | 0.5 | 1.0 | 2.0 | MHz |
| | FmSRC | | Internal Slow-speed RC oscillation for watchdog timer. | 2.8 to 5.5 | 15 | 30 | 60 | kHz |

Note 2-1: Relationship between tCYC and oscillation frequency is 3/FmMRC at a division ratio of 1/1 and 6/FmMRC at a division ratio of 1/2.

Note 2-2: When switching the system clock, allow an oscillation stabilization time of 100μs or longer after the High-speed RC oscillator circuit transmits from the "oscillation stopped" to "oscillation enabled" state.

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**Electrical Characteristics** at Ta = -40°C to +85°C, $V_{SS}1 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | $V_{DD}$[V] | Specification | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | min | typ | max | |
| High level input current | $I_{IH}(1)$ | Ports 0, 1 $\overline{RES}$ | Output disabled<br>Pull-up resistor off<br>$V_{IN}=V_{DD}$<br>(Including output Tr's off leakage current) | 2.8 to 5.5 | | | 1 | µA |
| Low level input current | $I_{IL}(1)$ | Ports 0, 1 $\overline{RES}$ | Output disabled<br>Pull-up resistor off<br>$V_{IN}=V_{SS}$<br>(Including output Tr's off leakage current) | 2.8 to 5.5 | -1 | | | |
| High level output voltage | $V_{OH}(1)$ | Ports 0, 1 | $I_{OH}$=-1mA | 4.5 to 5.5 | $V_{DD}$-1 | | | V |
| | $V_{OH}(2)$ | | $I_{OH}$=-0.35mA | 2.8 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(3)$ | Port0 | $I_{OH}$=-6mA | 4.5 to 5.5 | $V_{DD}$-1 | | | |
| | $V_{OH}(4)$ | (Note 3-1) | $I_{OH}$=-1.4mA | 2.8 to 5.5 | $V_{DD}$-0.4 | | | |
| Low level output voltage | $V_{OL}(1)$ | Ports 0, 1 | $I_{OL}$=10mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}(2)$ | | $I_{OL}$=1.4mA | 2.8 to 5.5 | | | 0.4 | |
| Pull-up resistance | Rpu(1) | Ports 0, 1 | $V_{OH}$=0.9$V_{DD}$ | 4.5 to 5.5 | 15 | 35 | 80 | kΩ |
| | Rpu(2) | | | 2.8 to 4.5 | 18 | 50 | 230 | |
| Hysteresis voltage | VHYS | P10(INT2), P11(INT3), P14,P15, $\overline{RES}$ | | 2.8 to 5.5 | | 0.1 $V_{DD}$ | | V |
| Pin capacitance | CP | All pins | For pins other than that under test:<br>$V_{IN}=V_{SS}$<br>f=1MHz<br>Ta=25°C | 2.8 to 5.5 | | 10 | | pF |

Note 3-1: When Ports0 selected MCPWM2.

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## SIO1 Serial I/O Characteristics at Ta = -40°C to +85°C, $V_{SS}1$ = 0V (Note 4)

| | | Parameter | Symbol | Pin/Remarks | Conditions | $V_{DD}$[V] | min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Serial clock | Input clock | Frequency | tSCK(3) | SCK1(P15) | • See Fig. 4. | 2.8 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(3) | | | | 1 | | | |
| | | High level pulse width | tSCKH(3) | | | | 1 | | | |
| | Output clock | Frequency | tSCK(4) | SCK1(P15) | • CMOS output selected<br>• See Fig. 4. | 2.8 to 5.5 | 2 | | | tSCK |
| | | Low level pulse width | tSCKL(4) | | | | 1/2 | | | |
| | | High level pulse width | tSCKH(4) | | | | 1/2 | | | |
| Serial input | | Data setup time | tsDI(2) | SB1(P14), SI1(P14) | • Must be specified with respect to rising edge of SIOCLK.<br>• See Fig. 4. | 2.8 to 5.5 | 0.05 | | | µs |
| | | Data hold time | thDI(2) | | | | 0.05 | | | |
| Serial output | | Output delay time | tdD0(4) | SO1(P13), SB1(P14) | • Must be specified with respect to falling edge of SIOCLK.<br>• Must be specified as the time to the beginning of output state change in open drain output mode.<br>• See Fig. 4. | 2.8 to 5.5 | | | (1/2)tCYC +0.08 | µs |

Note 4: These specifications are theoretical values. Add margin depending on its use.

## Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

| Parameter | Symbol | Pin/Remarks | Conditions | $V_{DD}$[V] | min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| High/low level pulse width | tPIH(1) tPIL(1) | INT0(P14), INT1(P15), INT2(P10) | • Interrupt source flag can be set.<br>• Event inputs for timer 0 or 1 are enabled. | 2.8 to 5.5 | 1 | | | tCYC |
| | tPIH(2) tPIL(2) | INT3(P11) when noise filter time constant is 1/1 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.8 to 5.5 | 2 | | | |
| | tPIH(3) tPIL(3) | INT3(P11) when noise filter time constant is 1/32 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.8 to 5.5 | 64 | | | |
| | tPIH(4) tPIL(4) | INT3(P11) when noise filter time constant is 1/128 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.8 to 5.5 | 256 | | | |
| | tPIL(5) | $\overline{RES}$ | • Resetting is enabled. | 2.8 to 5.5 | 200 | | | µs |

## AD Converter Characteristics at $V_{SS}1 = 0V$

<10bits AD Converter Mode/Ta = -40°C to +85°C >

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Resolution | N | AN0(P10) to AN3(P13) AN4(P16) AN5(P17) | | 2.8 to 5.5 | | 10 | | bit |
| Absolute accuracy | ET | | (Note 6-1) | 2.8 to 5.5 | | | ±4 | LSB |
| Conversion time | TCAD | | • See Conversion time calculation formulas. (Note 6-2) | 4.0 to 5.5 | 7.8 | | 65.6 | μs |
| | | | | 2.8 to 5.5 | 15 | | 65.6 | |
| Analog input voltage range | VAIN | | | 2.8 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Analog port input current | IAINH | | VAIN=$V_{DD}$ | 2.8 to 5.5 | | | 1 | μA |
| | IAINL | | VAIN=$V_{SS}$ | 2.8 to 5.5 | -1 | | | |

<8bits AD Converter Mode/Ta = -40°C to +85°C >

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Resolution | N | AN0(P10) to AN3(P13) AN4(P16) AN5(P17) | | 2.8 to 5.5 | | 8 | | bit |
| Absolute accuracy | ET | | (Note 6-1) | 2.8 to 5.5 | | | ±1.5 | LSB |
| Conversion time | TCAD | | • See Conversion time calculation formulas. (Note 6-2) | 4.0 to 5.5 | 2.85 | | 25.0 | μs |
| | | | | 2.8 to 5.5 | 5.5 | | 25.0 | |
| Analog input voltage range | VAIN | | | 2.8 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Analog port input current | IAINH | | VAIN=$V_{DD}$ | 2.8 to 5.5 | | | 1 | μA |
| | IAINL | | VAIN=$V_{SS}$ | 2.8 to 5.5 | -1 | | | |

Conversion time calculation formulas:

10bits AD Converter Mode: TCAD(Conversion time) = ((40/(AD division ratio))+2)×(1/3)×tCYC

8bits AD Converter Mode: TCAD(Conversion time) = ((28/(AD division ratio))+2)×(1/3)×tCYC

| External oscillation (FmMRC) | Operating supply voltage range ($V_{DD}$) | System division ratio (SYSDIV) | Cycle time (tCYC) | AD division ratio (ADDIV) | | AD conversion time (TCAD) | |
|---|---|---|---|---|---|---|---|
| | | | | 10bit AD | 8bit AD | 10bit AD | 8bit AD |
| 10MHz | 4.0V to 5.5V | 1/1 | 300ns | 1/2 | 1/1 | 8.5μs | 2.9μs |
| | 2.8V to 5.5V | 1/1 | 300ns | 1/4 | 1/2 | 17μs | 5.8μs |

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

• The first AD conversion is performed in the 10-bit AD conversion mode after a system reset.

• The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 10-bit conversion mode.

## Power-on Reset (POR) Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | Option selected voltage | min | typ | max | unit |
| POR release voltage | PORRL | | • Select from option. (Note 7-1) | 1.67V | 1.55 | 1.67 | 1.79 | V |
| | | | | 1.97V | 1.85 | 1.97 | 2.09 | |
| | | | | 2.07V | 1.95 | 2.07 | 2.19 | |
| | | | | 2.37V | 2.25 | 2.37 | 2.49 | |
| | | | | 2.57V | 2.45 | 2.57 | 2.69 | |
| | | | | 2.87V | 2.75 | 2.87 | 2.99 | |
| | | | | 3.86V | 3.73 | 3.86 | 3.99 | |
| | | | | 4.35V | 4.21 | 4.35 | 4.49 | |
| Detection voltage unknown state | POUKS | | • See Fig. 6. (Note 7-2) | | | 0.7 | 0.95 | |
| Power supply rise time | PORIS | | • Power supply rise time from 0V to 1.6V. | | | | 100 | ms |

Note7-1: The POR release level can be selected out of 8 levels only when the LVD reset function is disabled.

Note7-2: POR is in an unknown state before transistors start operation.

## Low Voltage Detection Reset (LVD) Characteristics at Ta = -40°C to +85°C, $V_{SS}1=0V$

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | Option selected voltage | min | typ | max | unit |
| LVD reset voltage (Note 8-2) | LVDET | | • Select from option. (Note 8-1) (Note 8-3) • See Fig. 7. | 1.91V | 1.81 | 1.91 | 2.01 | V |
| | | | | 2.01V | 1.91 | 2.01 | 2.11 | |
| | | | | 2.31V | 2.21 | 2.31 | 2.41 | |
| | | | | 2.51V | 2.41 | 2.51 | 2.61 | |
| | | | | 2.81V | 2.71 | 2.81 | 2.91 | |
| | | | | 3.79V | 3.69 | 3.79 | 3.89 | |
| | | | | 4.28V | 4.18 | 4.28 | 4.38 | |
| LVD hysteresys width | LVHYS | | | 1.91V | | 55 | | mV |
| | | | | 2.01V | | 55 | | |
| | | | | 2.31V | | 55 | | |
| | | | | 2.51V | | 55 | | |
| | | | | 2.81V | | 60 | | |
| | | | | 3.79V | | 65 | | |
| | | | | 4.28V | | 65 | | |
| Detection voltage unknown state | LVUKS | | • See Fig. 7. (Note 8-4) | | | 0.7 | 0.95 | V |
| Low voltage detection minimum width (Reply sensitivity) | TLVDW | | • LVDET-0.5V • See Fig. 8. | | 0.2 | | | ms |

Note8-1: The LVD reset level can be selected out of 7 levels only when the LVD reset function is enabled.

Note8-2: LVD reset voltage specification values do not include hysteresis voltage.

Note8-3: LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note8-4: LVD is in an unknown state before transistors start operation.

**Comparator Characteristics** at Ta = -40°C to +85°C, $V_{SS}1 = 0V$

| Parameter | Symbol | Pin/ Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Input common-mode voltage (Note9-1) | VCMIN | P12(CMP1IA), P11(CMP1IB), P17(CMP2IA), P16(CMP2IB) | | 2.8 to 5.5 | $V_{SS}$ | | $V_{DD}$ -1.5V | V |
| Offset voltage | VCPOFF(1) | P12(CMP1IA), P11(CMP1IB), P17(CMP2IA), P16(CMP2IB) | • Input common-mode voltage range<br>• CMP1 minus input = CMP1IA<br>• CMP2 minus input = CMP2IA | 2.8 to 5.5 | | | ±20 | mV |
| | VCPOFF(2) | P12(CMP1IA), P11(CMP1IB), P17(CMP2IA), P16(CMP2IB) | • Input common-mode voltage range<br>• CMP1 minus input = CMP1vref (Note9-2)<br>• CMP2 minus input = CMP2 vref (Note9-2) | 2.8 to 5.5 | | | ±40 | mV |
| CMP response speed | tCRT | P13(CMP1O), P15(CMP2O) | • Input common-mode voltage range<br>• Input amplitude=100mV, Over drive=50mV<br>• CMP1 minus input = CMP1IA<br>• CMP2 minus input = CMP2IA | 2.8 to 5.5 | | 200 | | ns |

Note9-1: When $V_{DD}$=5V, input voltage is effective from 0 to 3.5V.

Note9-2:

Rang1: CMP1vref1= (CMP1vref-Register<3:0> + 1)/16 × $V_{DD}$ × 0.64

CMP2vref2= (CMP2vref-Register<3:0> + 1)/16 × $V_{DD}$ × 0.64

Rang2: CMP1vref1= (CMP1vref-Register<3:0> + 1)/64 × $V_{DD}$ × 0.64

CMP2vref2= (CMP2vref-Register<3:0> + 1)/64 × $V_{DD}$ × 0.64

*: Range1/Range2 setting by a register is common to comparators 1 and 2.

**Consumption Current Characteristics** at Ta = -40°C to +85°C, $V_{SS}1 = 0V$

| Parameter | Symbol | Pin/ Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Normal mode consumption current (Note 10-1) (Note 10-2) | IDDOP(1) | $V_{DD}$1 | • Internal Medium speed RC oscillation stopped.<br>• System clock set to internal High speed RC oscillation(10MHz).<br>• 1/1 frequency division ratio | 2.8 to 5.5 | | 3.4 | 4.8 | mA |
| | IDDOP(2) | | • Internal High speed RC oscillation stopped.<br>• System clock set to internal Medium speed RC oscillation.<br>• 1/2 frequency division ratio | 2.8 to 5.5 | | 0.2 | 0.4 | |
| HALT mode consumption current (Note 10-1) (Note 10-2) | IDDHALT(1) | $V_{DD}$1 | • HALT mode<br>• Internal Medium speed RC oscillation stopped.<br>• System clock set to internal High speed RC oscillation(10MHz).<br>• 1/1 frequency division ratio | 2.8 to 5.5 | | 1.6 | 2.3 | mA |
| | IDDHALT(2) | $V_{DD}$1 | • HALT mode<br>• Internal High speed RC oscillation stopped.<br>• System clock set to internal Medium speed RC oscillation.<br>• 1/2 frequency division ratio | 2.8 to 5.5 | | 0.10 | 0.19 | |
| HOLD mode consumption current (Note 10-1) (Note 10-2) (Note 10-3) | IDDHOLD(1) | $V_{DD}$1 | HOLD mode | 2.8 to 5.5 | | 0.03 | 32 | μA |
| | IDDHOLD(2) | | HOLD mode<br>• LVD option selected | 2.8 to 5.5 | | 3 | 35 | |

Note10-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note10-2: The consumption current values do not include operational current of LVD function if not specified.

Note10-3: The amplifier / comparator circuit operates in the HOLD mode.

**F-ROM Programming Characteristics** at Ta = +10°C to +55°C, $V_{SS}1 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Onboard programming current | IDDFW(1) | $V_{DD}$1 | • Only current of the Flash block. | 2.8 to 5.5 | | 5 | 10 | mA |
| Programming time | tFW(1) | | • Erasing time | 2.8 to 5.5 | | 20 | 30 | ms |
| | tFW(2) | | • Programming time | | | 40 | 60 | μs |



$0.5V_{DD}$
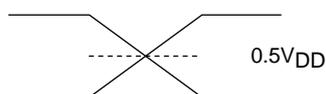
Figure 1 AC Timing Measurement Point
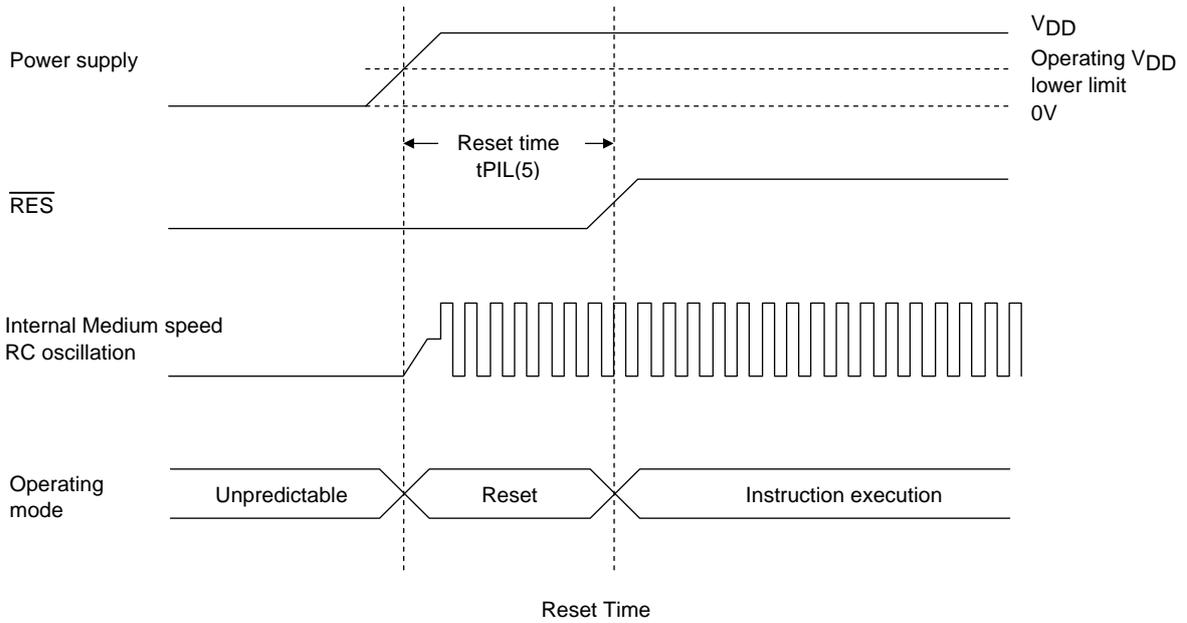
Reset Time

Figure 2 Reset Time
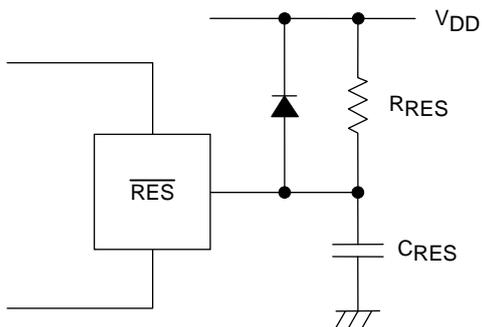


Note:
External circuits for reset may vary depending on the usage of POR and LVD. Please refer to the user's manual for more information.

Figure 3 Reset Circuit
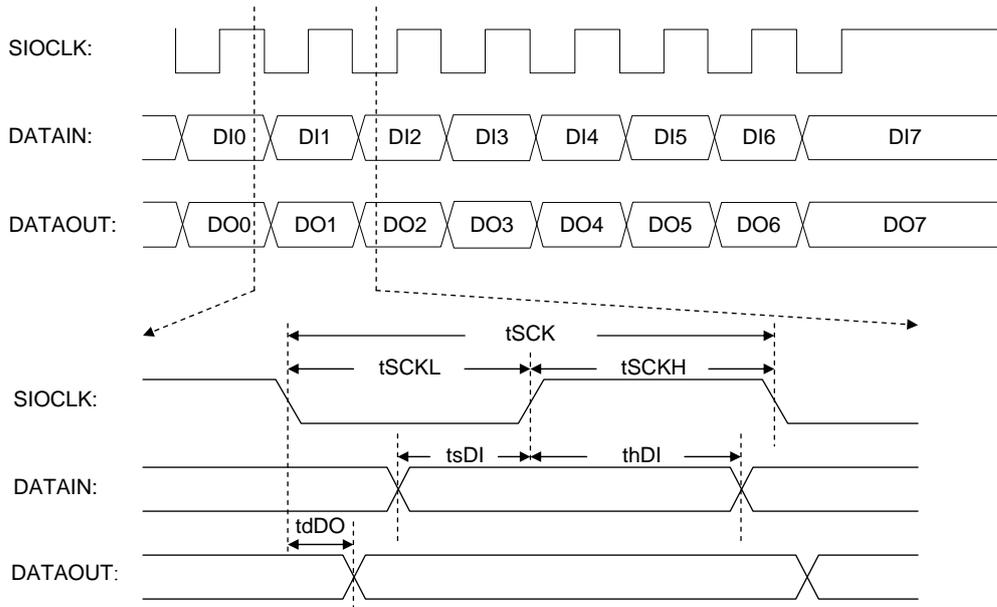
Figure 4 Serial I/O Output Waveforms
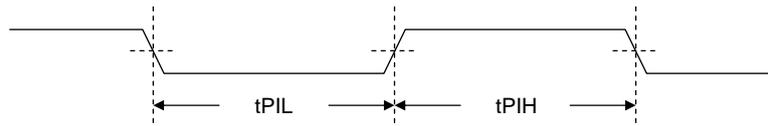
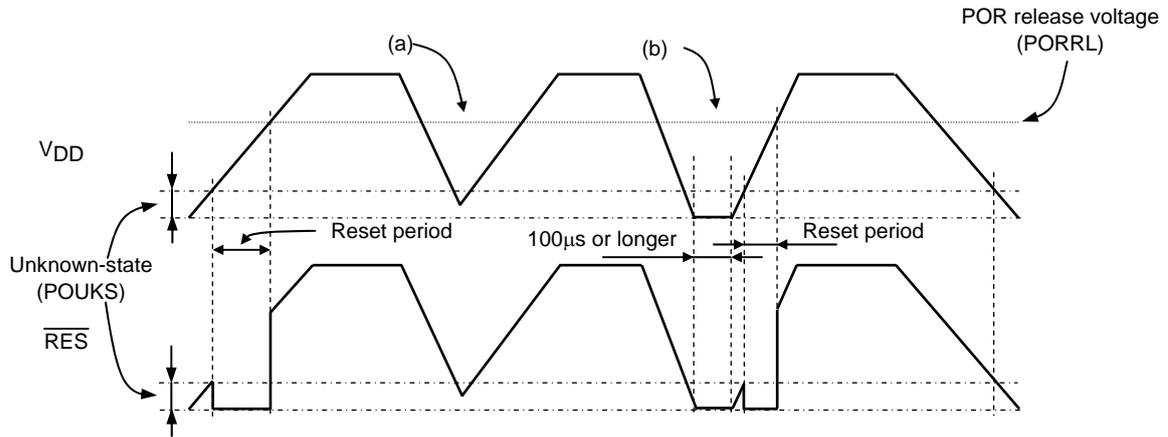Figure 5 Pulse Input Timing Signal Waveform

Figure 6 Waveform observed when only POR is used (LVD not used)
(RESET pin: Pull-up resistor R$_{RES}$ only)

- The POR function generates a reset only when power is turned on starting at the V$_{SS}$ level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V$_{SS}$ level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the V$_{SS}$ level as shown in (b) and power is turned on again after this condition continues for 100μs or longer.
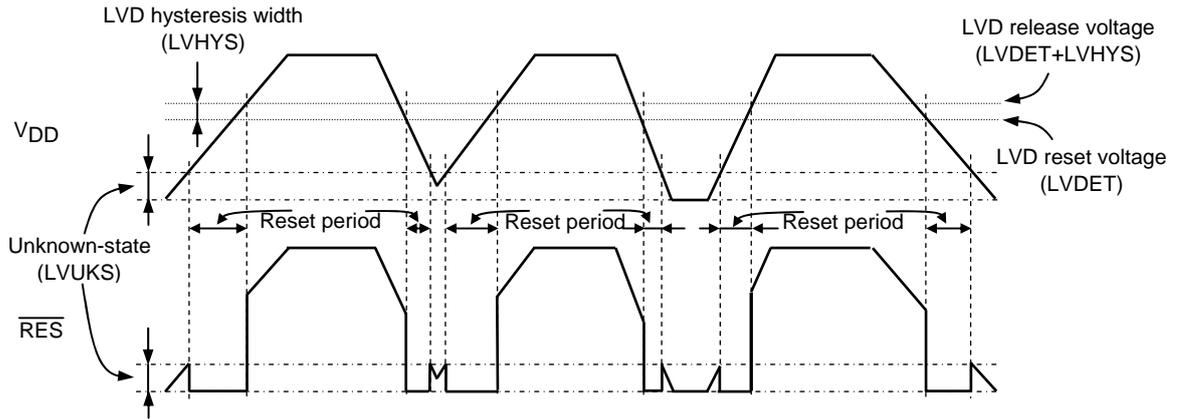
Figure 7 Waveform observed when both POR and LVD functions are used
(RESET pin: Pull-up resistor $R_{RES}$ only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.
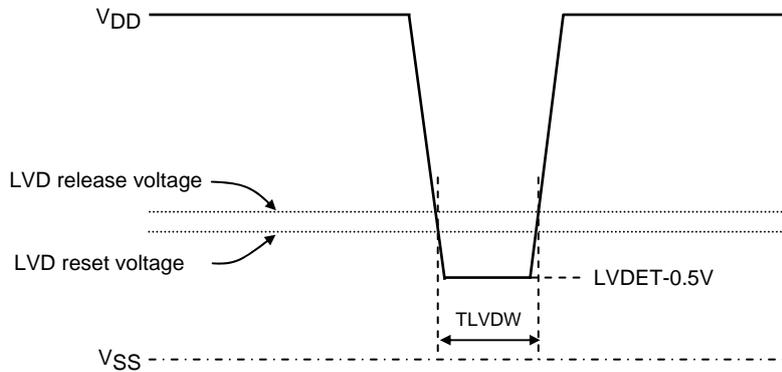


Figure 8 Low voltage detection minimum width
(Example of momentary power loss/Voltage variation waveform)