LV8811G, LV8813G

Advance Information

Motor Driver, 3-Phase, PWM, Full-Wave, BLDC

Overview

The LV8811G / LV8813G is a 3-phase BLDC motor driver which is controlled by single Hall sensor. A 180 degrees sinusoidal driving method is adopted and the IC can control motor with low vibration and the low noise. In addition, lead-angle adjustment is possible by an external pin. Lead-angle value and lead-angle slant can be adjusted independently. Thus, the device can be driven by high efficiency and low noise with various motors. The power element to drive a motor is built-in and contributes to high efficiency by low on resistance (0.5 Ω). The Hall sensor bias driver is equipped, and a Hall IC is supported as well. As a method of the rotary speed control of the motor, direct-PWM pulse input or DC-voltage input can be chosen.

Features

- 3-phase full wave (sinusoidal) drive
- Any practical combination of slot and pole can be handled. (e.g. 3S3P, 3S4P, 6S4P, 6S8P, 12S8P, 9S12P and so on)
- built-in power FETs (P-MOS/N-MOS)
- Speed control function by direct PWM or DC voltage input
- Minimum input PWM duty cycle can be configured by voltage input
- Soft start-up function and soft shutdown function
- Soft PWM duty cycle transitions
- Built-in current limit circuit and thermal protection circuit
- Regulated voltage output pin for Hall sensor bias
- Built-in locked rotor protection and auto recovery circuit
- FG signal output
- Dynamic lead angle adjustment with respect to rotational speed
- Lead-angle control parameters can be configured by voltage inputs.

Typical Applications

- Refrigerator
- PC
- Games

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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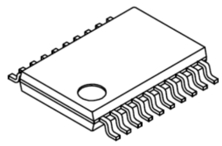
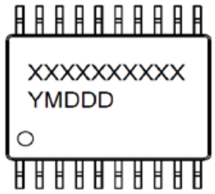


20-pin TSSOP with exposed pad
CASE 948AZ

MARKING DIAGRAM



XXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

ORDERING INFORMATION

Ordering Code:
LV8811G-AH
LV8813G-AH

Package
TSSOP20J
(Pb-Free / Halogen Free)

Shipping (Qty / packing)
2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

BLOCK DIAGRAM

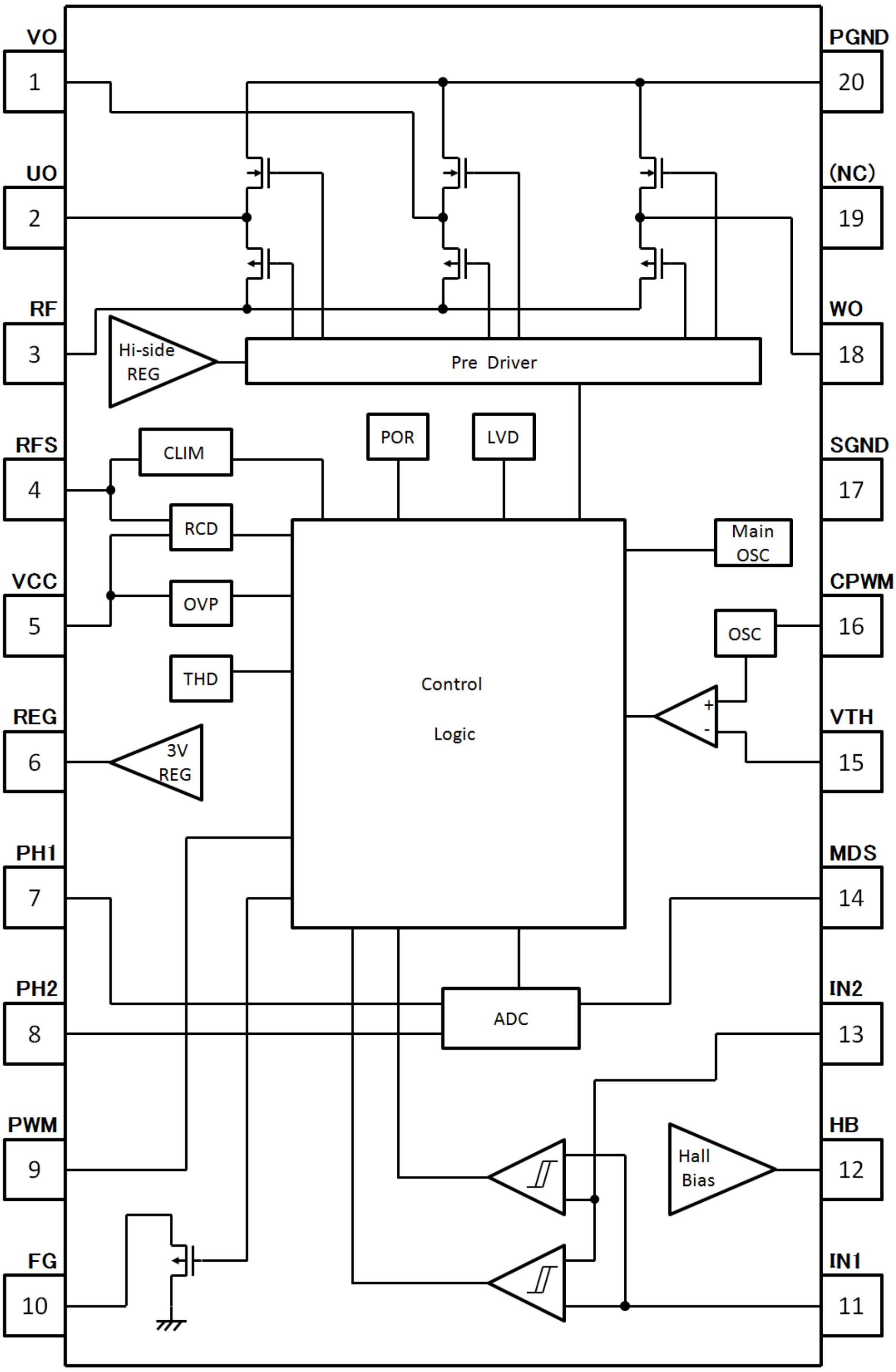


Figure 1: LV8811G/13G Block Diagram

APPLICATION CIRCUIT DIAGRAM

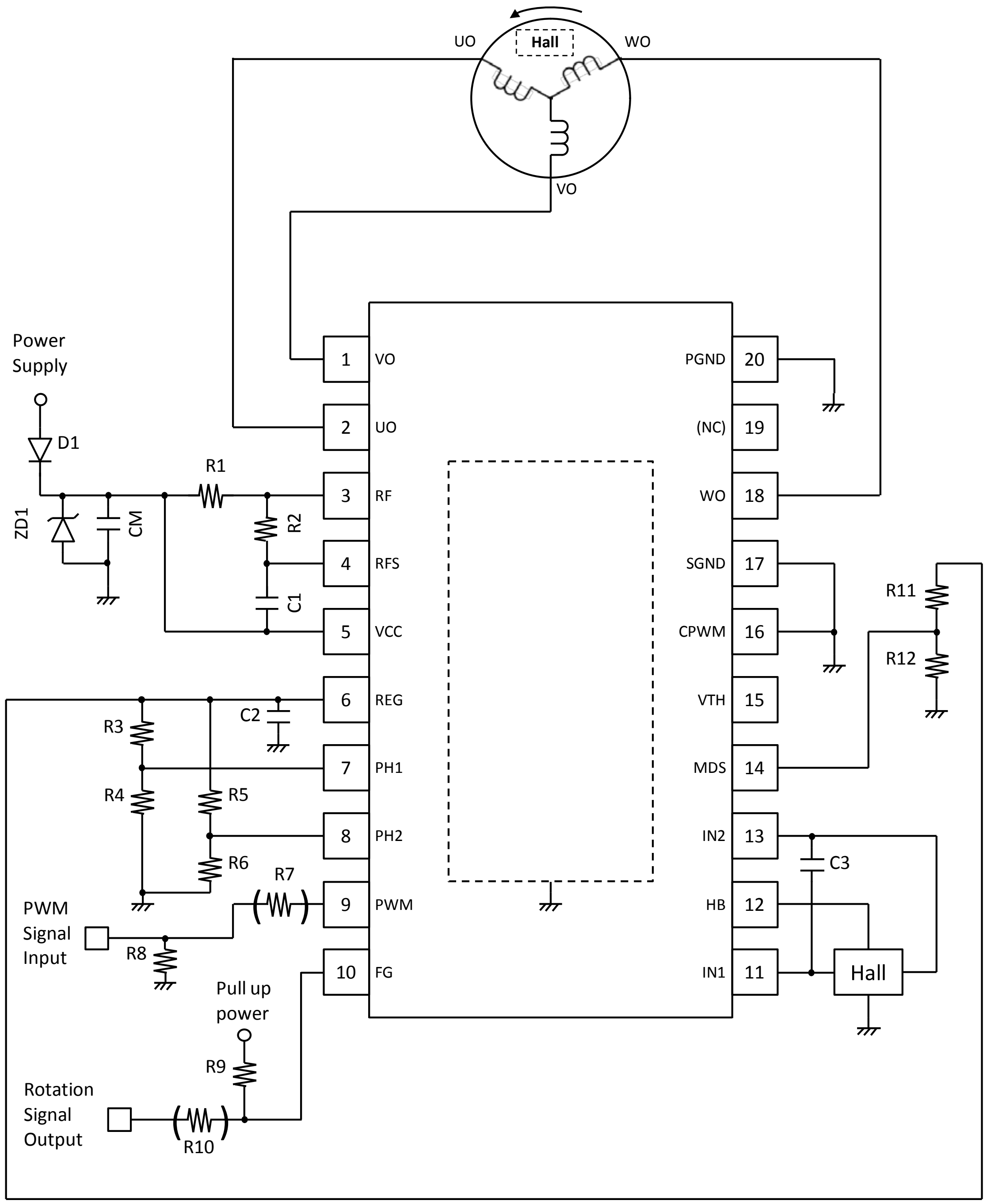


Figure 2: Three-phase BLDC Motor Drive with LV8811G/13G using One Hall Sensor

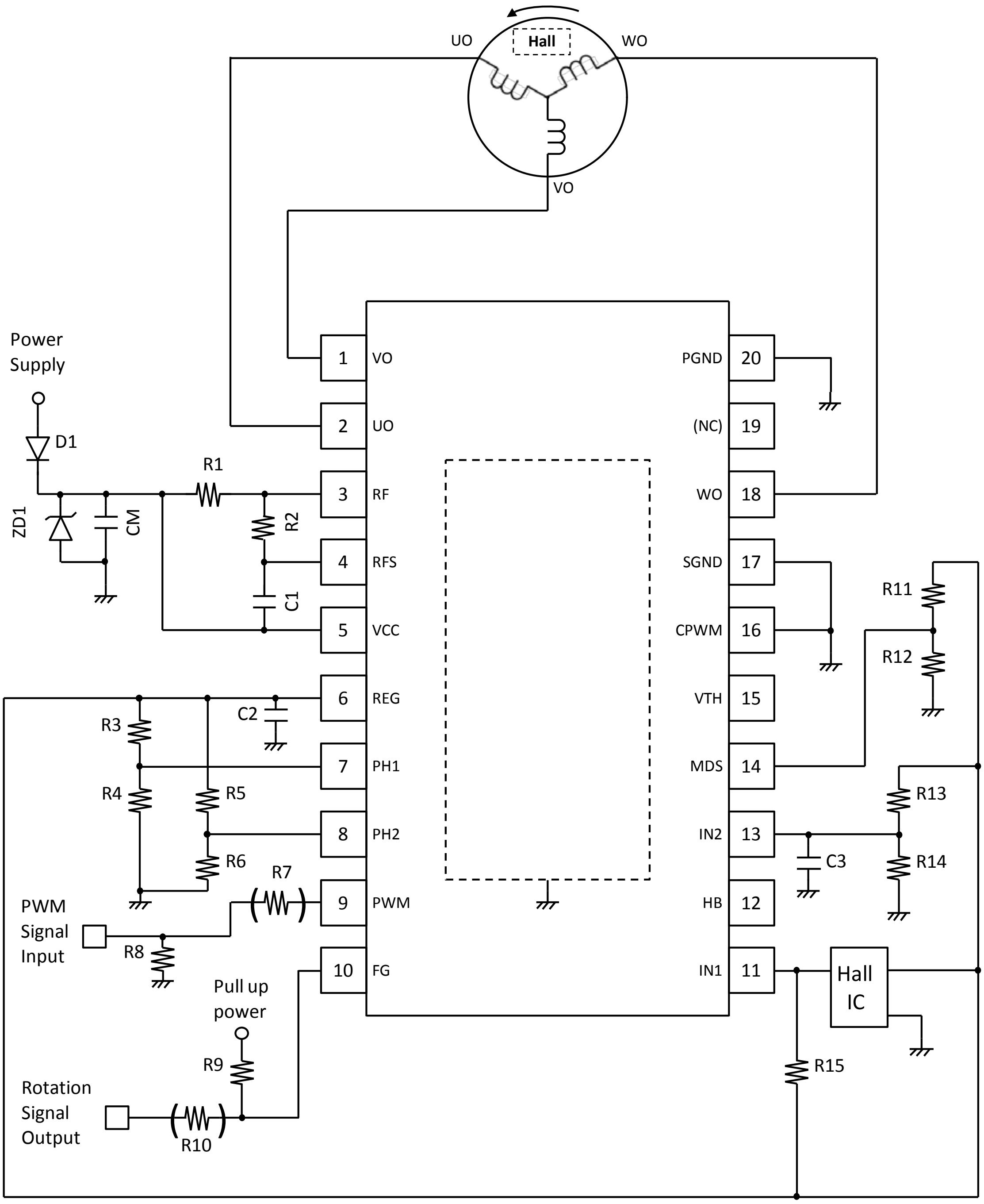


Figure 3: Three-phase BLDC Motor Drive with LV8811G/13G using One Hall IC

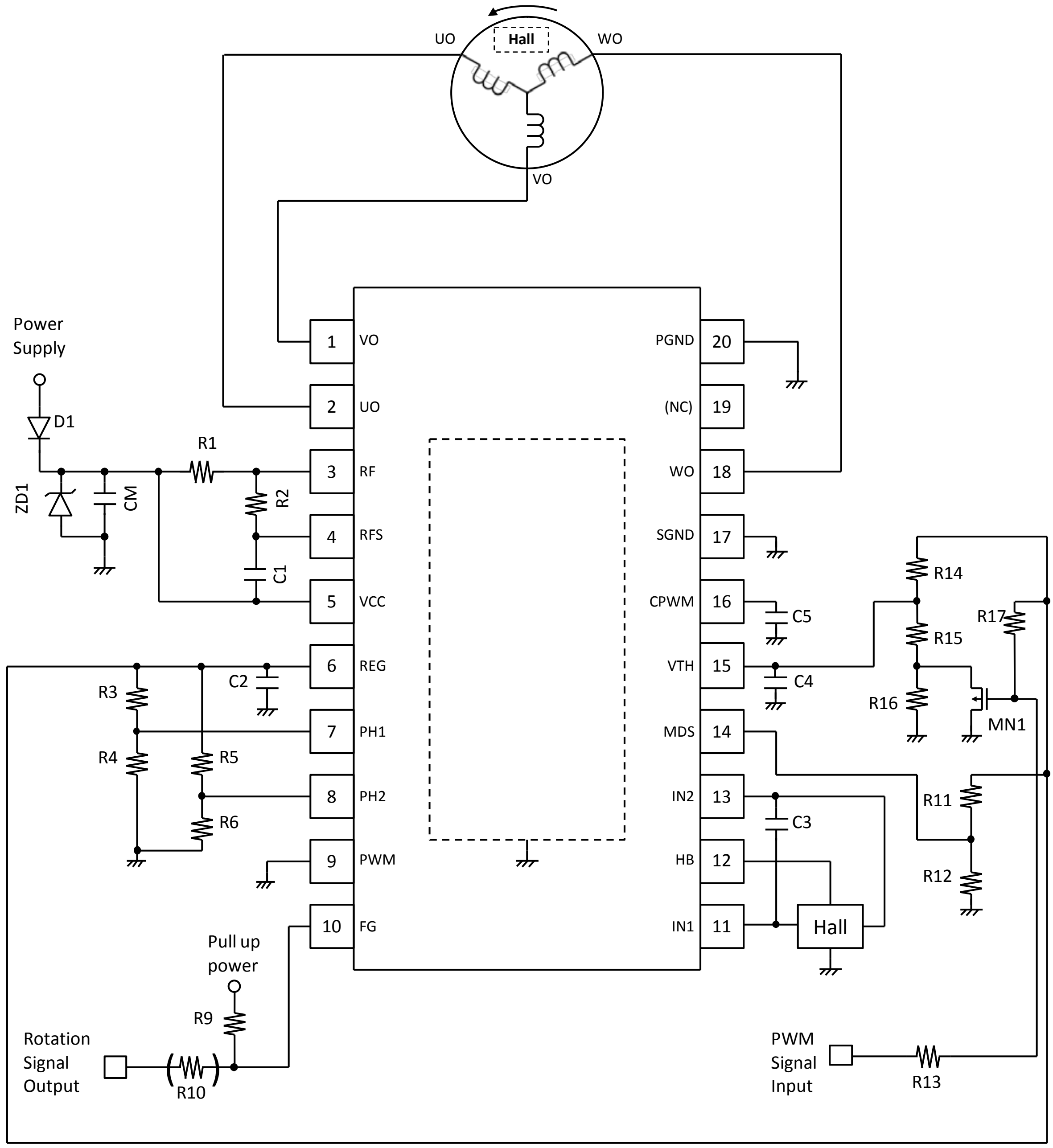


Figure 4: Three-phase BLDC Motor Drive with LV8811G/13G using input PWM to DC conversion for speed control

Example Component Value

Device	Value	Device	Value
D1	MBRA340T3G (ON semi)	R5	0 to 50kΩ
ZD1	MNSZ5247BT1G (ON semi)	R6	50 to 0kΩ
		R7	1kΩ
CM	4.7μF	R8	NC
C1	1500pF	R9	1 to 5kΩ
C2	1μF	R10	1kΩ
C3	0.1μF	R11	0 to 50kΩ
C4	1μF	R12	50 to 0kΩ
C5	390pF	R13	10kΩ
		R14	30kΩ
R1	0.22Ω // 0.22Ω (0.5W)	R15	7.5kΩ
R2	1kΩ	R16	62kΩ
R3	0 to 50kΩ	R17	68kΩ
R4	50 to 0kΩ		

PIN ASSIGNMENT

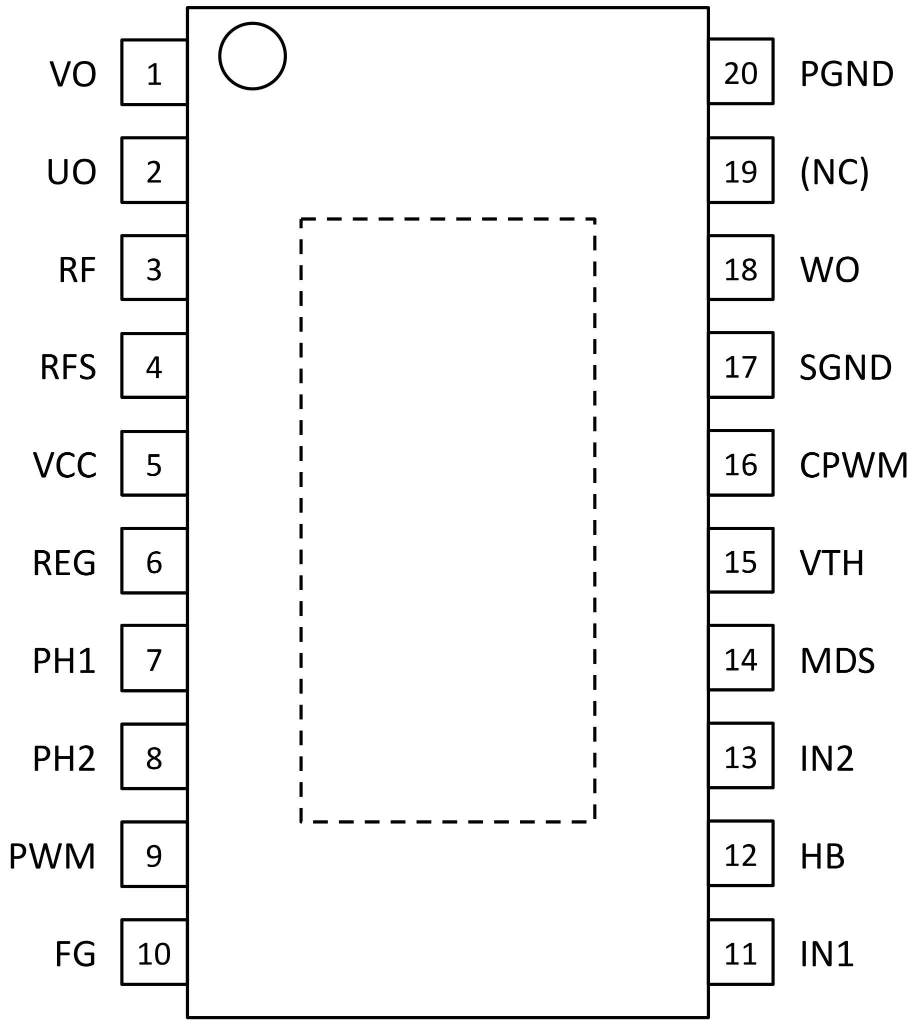


Figure 5: LV8811G/13G Pin Assignment

LV8811G VS LV8813G COMPARISION

Use application

-LV8811G : Wide operation supply voltage range. Suitable for small-size fans.
-LV8813G : Stable start-up even with a large load. Suitable for large-size fans.

Different Characteristics

	LV8811G	LV8813G	Comment	Reference
VCC/RF operating Supply voltage range	3.6V to 16V	6.0V to 16V	LV8811G has a wide operation voltage range. LV8813G has a different Vcc lower limit to support large-size fan.	Pg. 11
Alignment Duty	6%- >5%-> 20%->15%	50%->25%	LV8813G has stronger alignment to secure the start-up of large-size fans.	Pg. 20
Alignment time	0.8ms	1.0s	LV8813G has longer adjustment time to secure the start-up of large-size fans.	Pg.11, 23, 25
Lock detection time	0.33s	0.77s	LV8813G has longer detection time to prevent false Lock detection on large-size fans at the start-up.	Pg. 11, 23, 25
Lock-Stop Release Time	5.8s	5.4s	This characteristic is different due to a different Lock detection time.	Pg. 23, 25
Lock/Release time ratio	1:5	1:3		Pg. 23, 25

PIN FUNCTION DISCRIPTION

Pin No.	Pin Name	Description
1	VO	V-phase output pin
2	UO	U-phase output pin
3	RF	Inverter power supply and Motor current sense resistor pin
4	RFS	Motor Current Sense
5	VCC	Power supply pin
6	REG	Internal regulator output pin
7	PH1	Lead-angle adjustment pin 1
8	PH2	Lead-angle adjustment pin 2
9	PWM	Speed reference input PWM pin
10	FG	Motor speed feedback output pin
11	IN1	Hall sensor input pin 1
12	HB	Hall sensor bias output pin
13	IN2	Hall sensor input pin 2
14	MDS	Minimum output PWM duty cycle setting pin
15	VTH	Speed reference input DC voltage pin
16	CPWM	PWM clock frequency control pin
17	SGND	System ground pin
18	WO	W-phase output pin
19	NC	No connection
20	PGND	Power ground pin

MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Maximum supply voltage (Note2)	VCC_{MAX}	20	V
Maximum output voltage (Note3)	$VOUT_{MAX}$	20	V
Maximum output current (Note3, Note4)	$IOUT_{MAX}$	2.0	A
VREG pin maximum load current	$IREG_{MAX}$	20	mA
HB pin maximum load current	IHB_{MAX}	10	mA
PWM pin maximum input voltage	$VPWM_{MAX}$	6	V
FG pin maximum withstanding voltage	VFG_{MAX}	17	V
Input pins maximum withstanding voltage (Note5)	(Note 6)	3.6	V
Allowable Power Dissipation (Note7)	Pd_{MAX}	2.25	W
Storage Temperature	T_{stg}	−55 to 150	˚C
Junction Temperature	T_{JMAX}	150	ºC
Moisture Sensitivity Level (MSL) (Note8)	MSL	3	-
Lead Temperature Soldering Pb-Free Versions (30sec or less) (Note 9)	T_{SLD}	255	ºC

1. Stresses exceeding those listed in the Absolute Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. VCC supply pins are VCC(5pin), RF(3pin), and RFS(4pin).
3. Motor power supply pins are UO(2pin), VO(1pin), and WO(18pin).
4. $IOUT_{MAX}$ is the peak value of the motor supply current.
5. Input pins are PH1(7pin), PH2(8pin), IN1(11pin), IN2(13pin), MDS(14pin), VTH(15pin), and CPWM(16pin).
6. Pin : Symbol PH1:$VPH1_{MAX}$, PH2:$VPH2_{MAX}$, IN1:$VIN1_{MAX}$, IN2:$VIN2_{MAX}$, MDS:$VMDS_{MAX}$, VTH:$VVTH_{MAX}$, CPWM:$VCPWM_{MAX}$
7. Specified circuit board : 56.5mm×56.5mm×1.8mm, glass epoxy 2-layer board. It has 1 oz internal power and ground planes and 1/2 oz copper traces on top and bottom of the board. Please refer to Thermal Test Conditions of page 29.
8. Moisture Sensitivity Level (MSL): 3 per IPC/JEDEC standard: J-STD-020A
9. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D
http://www.onsemi.com/pub_link/Collateral/SOLDERRM-D.PDF

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient (Note7)	$R\theta JA$	45.2	ºC/W
Thermal Resistance, Junction-to-Case (Top) (Note7)	$R\Psi JT$	13.3	ºC/W

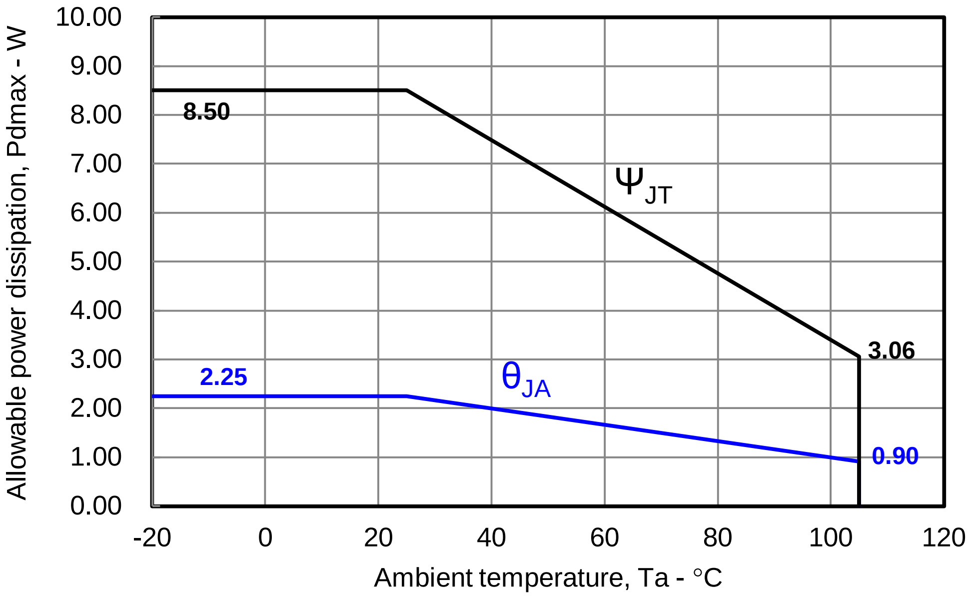


Figure6. Power Dissipation vs Ambient Temperature Characteristic

RECOMMENDED OPERATING RANGES (Note10)

Parameter	Symbol	Ratings	Unit
VCC supply voltage Range at LV8811G(Note2)	VCC_{OP}	3.6 to 16.0	V
VCC supply voltage Range at LV8813G(Note2)		6.0 to 16.0	V
PWM input frequency range	f_{PWM}	20 to 50	kHz
PWM input duty cycle range	D_{PWM}	0 to 100	%
PWM input voltage range	V_{PWM}	0 to 5	V
IN1 input voltage range	V_{IN1}	0 to VREG	V
IN2 input voltage range	V_{IN2}	0.3 to 1.8	V
Control input Voltage Range (Note11)	(Note 12)	0 to VREG	V
Ambient Temperature	T_A	–40 to 105	ºC

10. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
11. Control input pins are PH1, PH2, MDS, and VTH
12. Pin : Symbol PH1:V_{PH1}, PH2:V_{PH2}, MDS:V_{MDS}, VTH:V_{VTH}

ELECTRICAL CHARACTERISTICS

T_A=25ºC, VCC_{OP} = 12V unless otherwise noted. (Note 13)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Circuit Current						
Supply Current	ICC0	PWM = 3V, CPWM=0V, I_O=0A		4.5	7.0	mA
Protection (Note14)						
Over Current Detection Voltage	VTH_{OCP}	The voltage between VCC - RF	0.162	0.180	0.198	V
Over Voltage Detection Voltage	VTH_{OVP}	VCC pin, Guaranteed by design	20	21		V
Over Voltage Detection Hysteresis	ΔVTH_{OVP}	VCC pin, Guaranteed by design		3		V
Lock Detection Time	T_{LD}	Case of the LV8811G	0.26	0.33	0.40	S
		Case of the LV8813G	0.61	0.77	0.93	S
Lock-Stop Release Time	T_{LSR}	Case of the LV8811G	4.46	5.8	6.96	S
		Case of the LV8813G	4.32	5.4	6.48	S
Thermal Protection Detection Temperature	T_{THP}	Guaranteed by design	150	180		˚C
Thermal Protection Detection Hysteresis	ΔT_{THP}	Guaranteed by design		15		˚C
Regulator						
REG Pin Output Voltage	VREG		2.7	3.0	3.3	V
Output						
UO/VO/WO Output Resistance	$ROUT_{ON}$	I_O=0.8A, High-side + Low-side		0.5	0.65	Ω
FG Output (Note15)						
FG Pin Low Level Output Voltage	V_{FGL}	I_{FG}=5mA			0.3	V
FG Pin Leak Current	I_{FGLK}	V_{FG}=16V			1	μA
Hall Bias & Hall Signal Input						
HB Pin Output Voltage	V_{HB}	I_{HB}=5mA	1.06	1.18	1.30	V
IN1/IN2 Input Current	I_H				1	μA
Hall Signal Input Hysteresis	ΔV_H	Guaranteed by design		+/-10		mV

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PWM Input						
PWM Pin Low Level Input Voltage	V_{PWML}		0		0.6	V
PWM Pin High Level Input Voltage	V_{PWMH}		2.3		5.5	V
PWM On Time (Note16)	T_{PWMON}	Guaranteed by design	200			ns
PWM Off Time (Note16)	T_{PWMOFF}	Guaranteed by design	200			ns
CPWM Input						
CPWM Minimum Output Voltage	V_{CPWML}	$\text{CPWM Voltage} = \text{VREG} \times \text{Parcentage}$	16	18	20	%
CPWM Maximum Output Voltage	V_{CPWMH}	$\text{CPWM Voltage} = \text{VREG} \times \text{Parcentage}$	65	67	69	%
CPWM Source Current	I_{CPWMSO}	V_{CPWM}=1.3V	20	29	38	μA
CPWM Sink Current	I_{CPWMSI}	V_{CPWM}=1.3V	-38	-29	-20	μA

13. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
14. Refer to the protection circuit explanation in the function description
15. For FG output pin, it is recommended to connect pull-up resistor between the pin and power supply of the controller.
16. In case PWM frequency is 30kHz, the PWM duty cycle must be within a range between 0.6% and 100% except for 0%

TYPICAL CHARACTERISTICS

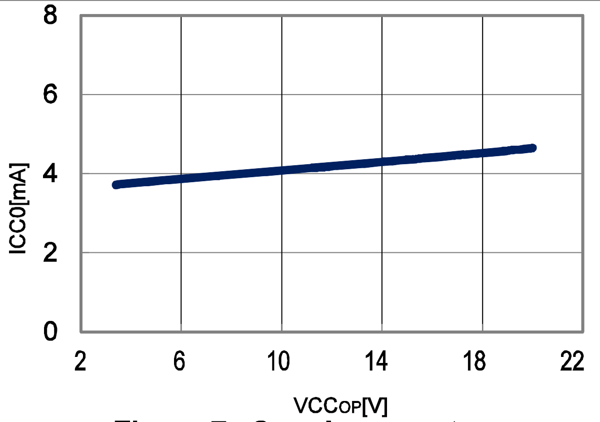


Figure 7. Supply current vs Vcc voltage

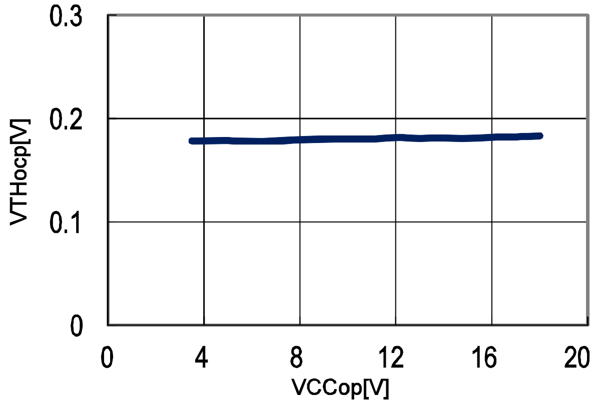


Figure8. Over Current Detection voltage vs Vcc voltage

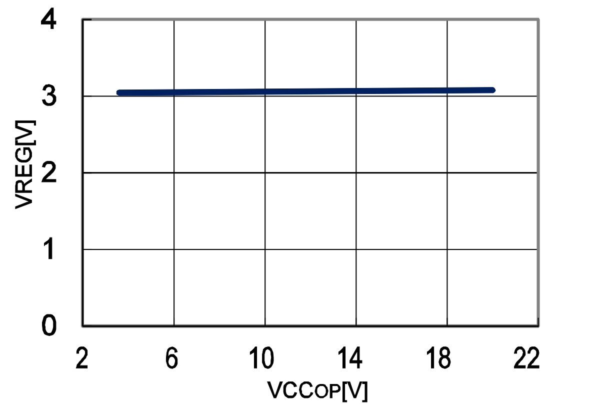


Figure9. VREG output voltage vs Vcc voltage

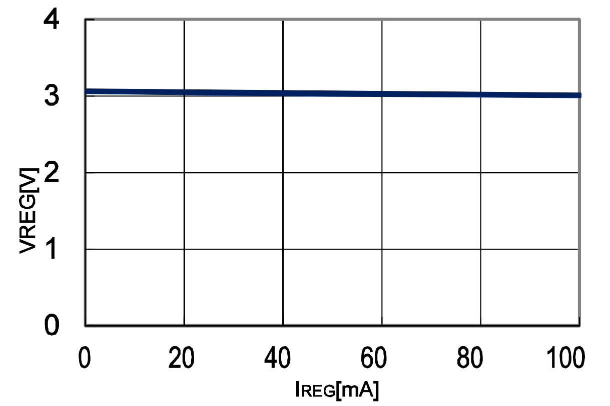


Figure10. VREG output voltage vs VREG load current

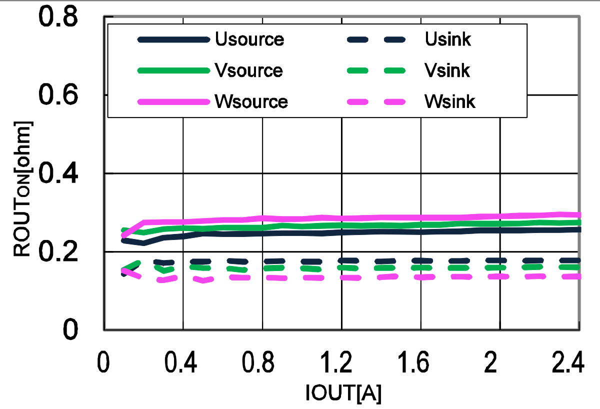


Figure11. Output ON resistance vs Output current

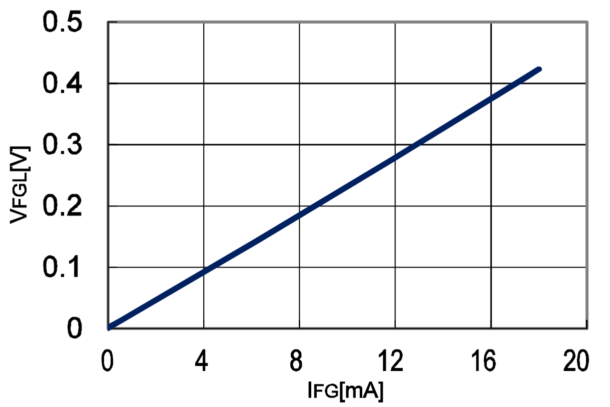


Figure12. FG output voltage vs FG input current

TYPICAL CHARACTERISTICS

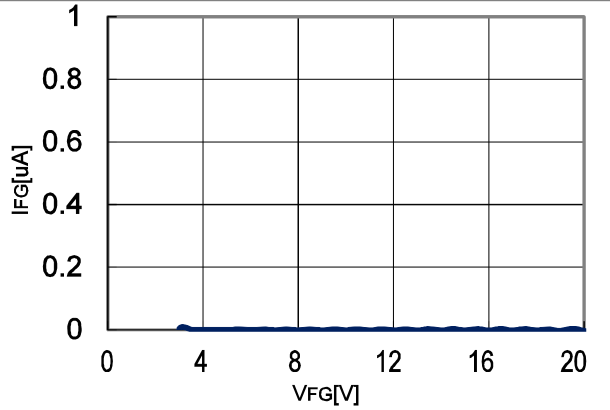


Figure13. FG leakage current vs FG input voltage

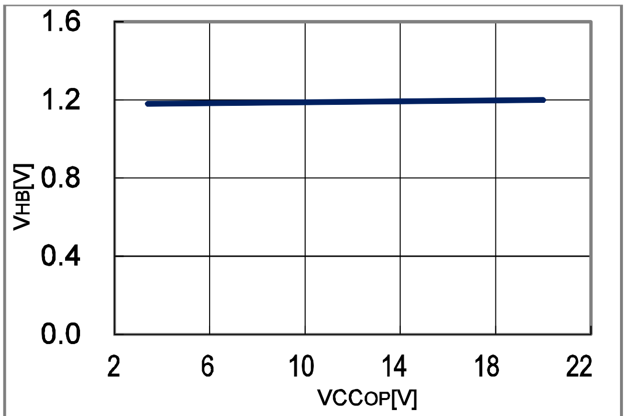


Figure14. VHB output voltage vs Vcc voltage

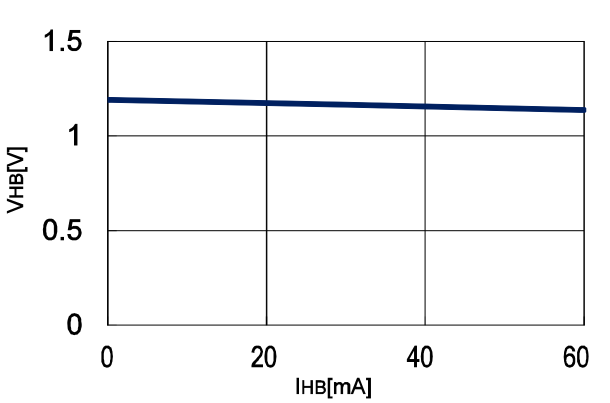


Figure15. VHB voltage vs VHB load current

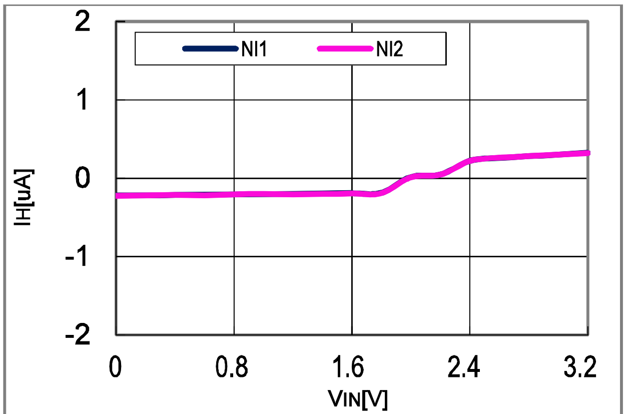


Figure16. IN1-2 input current vs IN1-2 Input voltage

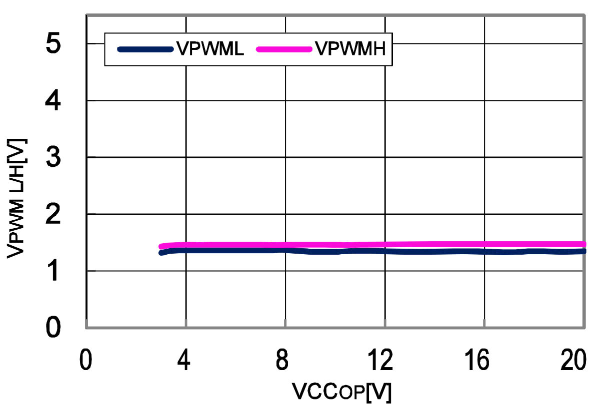


Figure17. PWM threshold voltage vs Vcc voltage

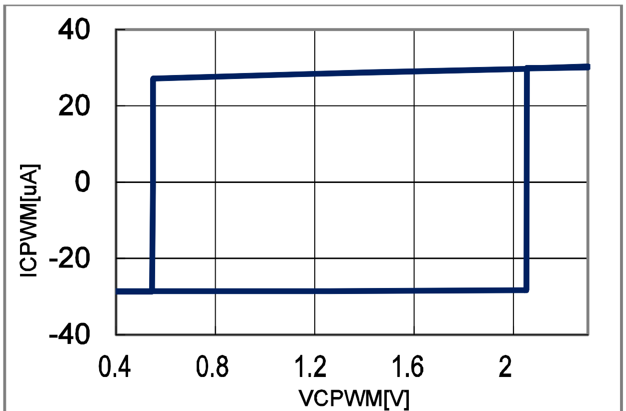


Figure18. CPWM charrge/discharge current

FUNCTIONAL DESCRIPTION

Power Supply Pins (VCC, RF)

VCC is a signal power supply whereas RF is output power supply. The RF pin supplies large current to built-in power MOS FTEs. (Figure22)
*Please refer to pg.16 "Resistor for Output Current Sense Pin (RF)" about the OCP sense resistance of RF terminal.

GND Pin (SGND, PGND)

SGND is a signal ground whereas PGND is a power ground. Since PGND has to tolerate surge of current, separate it from the SGND as far away as possible and connect it point-to-point to the ground side of the capacitor (CM) between power supply and ground.

Internal 3.0V Voltage Regulator Pin (REG)

An internal 3.0V voltage regulator acts a power source for internal logic, oscillator, and protection circuits.
When MDS and PH1 and PH2 are used, it is recommended that application circuits are made using this output. In addition, the application circuit of VTH is same, too. The maximum load current of VREG is 10mA. Warn not to exceed this. Place capacity of 1uF degree and the 0.1uF degree in the close this pin. (Figure19)

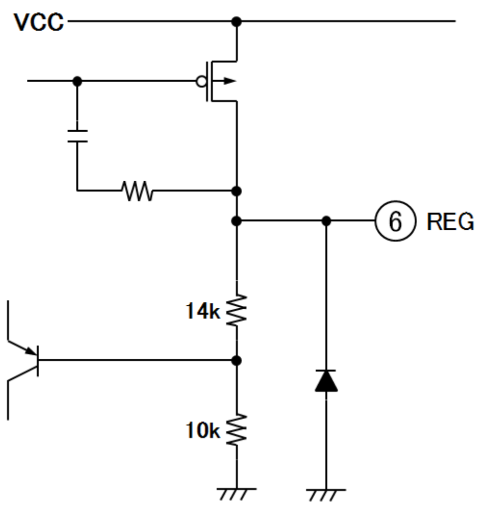


Figure19. Equivalent circuit of REG

Rotational Signal Pin (FG)

Frequency of the FG output represents the motor’s electrical rotational speed (the same rectangular waves as the UO). It is an open drain output. Recommended pull up resistor value is 100Ω – 1kΩ. Leave the pin open when not in use. (Figure20)

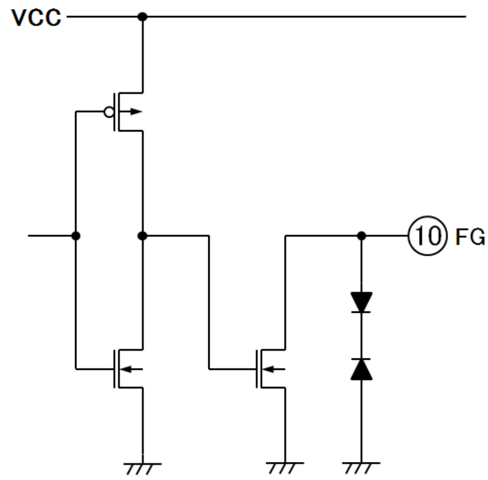


Figure20. Equivalent circuit of FG

Motor Drive Output Pins (UO, VO, WO)

These pins are output of built-in three-phase MOSFET based inverter that drives the motor. Each leg of the inverter is having high side P-MOSFET and low side N-MOSFET. (Figure21)

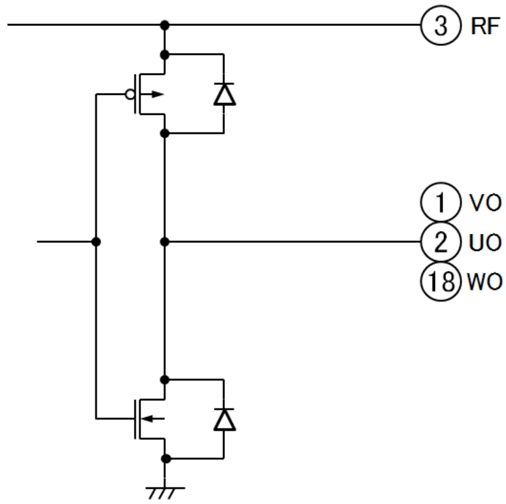


Figure21. Equivalent circuit of U/V/W

Hall-Sensor Bias Output Pin (HB)

The LV8811G/13G provides a bias regulator output (1.18V typ.) for a hall sensor. It is recommended that this output used only for hall sensor bias.

Hall-Sensor Input Pins (IN1, IN2)

Differential output signals of the hall sensor are to be interfaced at IN1 and IN2. It is recommended that 0.1uF capacitor is connected between both pins to filter system noise.
When a Hall IC is used, the output of the Hall IC must be connected to the pin IN1. And, the pin IN2 must be kept in the middle level of the Hall IC power supply voltage.
Regarding the polarity of a Hall sensor and IC, refer ‘*Rotation Direction*’ on page 17.

Motor Current Sense Resistor Pin (RF)

This is also the power supply pin for the built-in power inverter. Voltage across the sense resistor represents the motor current and is compared against the internal VTH_{OVC} (0.18Vtyp.) for setting the over-current protection (OCP) limit. (Figure22)

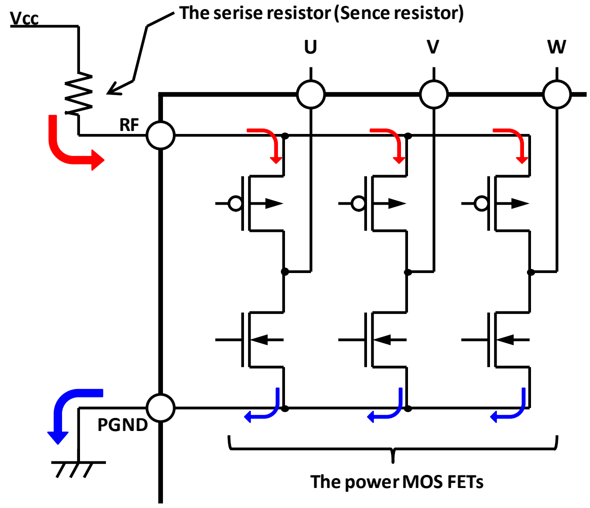


Figure22. Schematic view of power current route

The sense resistor value is calculated as follows.

$$\text{Sense Resistor}[\Omega] = \frac{VTH_{OCP}[V]}{OCP[A]}$$

For example, to set the OCP current threshold at 1.5A, the sense resistor value is

$$\text{Sense Resistor} = \frac{0.18(\text{typ})}{1.5}$$

$$\text{Res} = 0.12[\Omega]$$

Motor Current Sense Pin (RFS)

This pin reads voltage across the series sense resistor and compares with internal VTH_{OCP}. When the measured voltage exceeds VTH_{OCP}, OCP is triggered and when it falls below VTH_{OCP}, the LV8811G/13G exits from the OCP mode. A series RC filter is recommended to avoid OCP trigger due to switching noise. (Figure23)

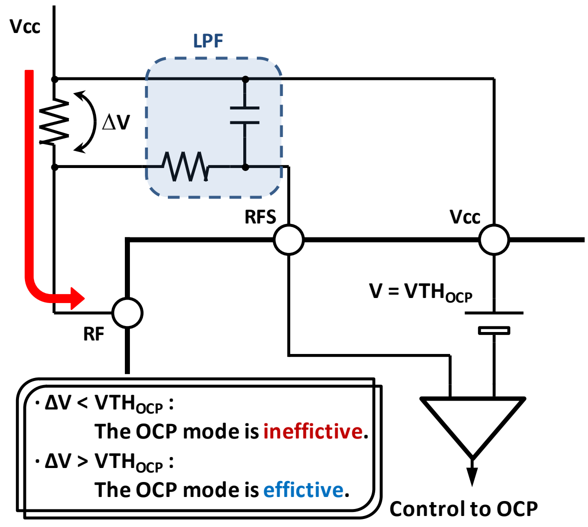


Figure23. Schematic view of the OCP circuit

Command Input (PWM)

This pin reads the duty-cycle of the PWM pulse and controls rotational speed. The PWM input signal levels can support both 3.3V and 5V. Confirm the standard level before using the pin. The combination with the rotational speed control by VTH, is impossible.
When the pin is not used, it should be connected to ground. The minimum pulse width is 200ns. (Figure24)

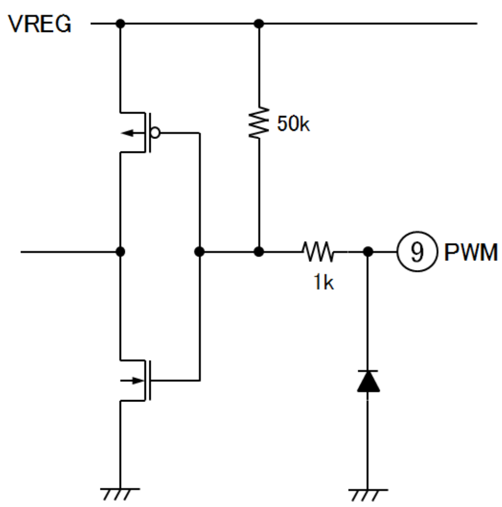


Figure24. Equivalent circuit of PWM

Minimum Duty Setting Pin (MDS)

The too small duty cycle of the input PWM can be blanked out. The threshold of the minimum duty cycle is configurable. The DC voltage level applied to this pin is converted to this threshold. The voltage is fetched right after the power-on-reset. Because the internal conversion circuit works inside VREG power rail, it is recommended that the MSD voltage is made from VREG. This pin is also used for setting of FG frequency. Refer '*Parameter Setting by Constant Voltage*' on page 24, and '*Setting Minimum PWM Duty Cycle*' on page 25.

Lead-angle Setting Pin (PH1, PH2)

LV8811G/13G provides the dynamic lead angle adjustment. To match the motor characteristics, the base angle and change ratio with respect to the rotation speed can be configured. The DC voltage levels applied to these pins are converted to the lead angle parameter. The voltages are fetched right after the power-on-reset. Because the internal conversion circuit works inside VREG power rail, it is recommended that the PH1 and PH2 voltages are made from VREG. Refer '*Parameter Setting by Constant Voltage*' on page 24, and '*Setting Lead Angle*' on page 26.

PWM Frequency Setting Pin (CPWM)

When rotational speed is controlled with the DC voltage, this pin is used. The frequency of the chopping wave which the pin generates at external capacity can be changed. The frequency of this chopping wave equals frequency of the PWM control that the output works. Thus, it is necessary to adjust within the range of 20k~50kHz.

The relations between the external capacitor and frequency are shown in the next formula.

PWM Frequency [Hz]

$$= \frac{I_{CPWMSI/O}[A]}{2 \times (V_{CPWMH} - V_{CPWML})VREG[V] \times C[pF]}$$

For example, the capacitance of CPWM, to make the PWM frequency 25k Hz, can be determined by the followings

$$25k = \frac{29u(typ)}{2.94(typ) \times C}$$

$$C \cong 390[pF]$$

The combination with the rotational speed control by PWM is impossible. When this pin is not used, it should be connected to GND. (Figure25)

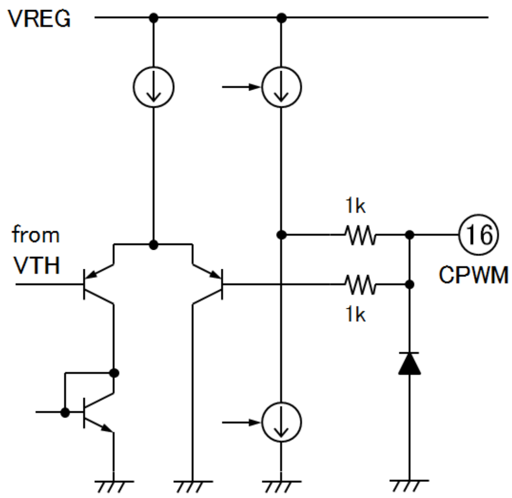


Figure25. Equivalent circuit of CPWM

Rotational Control Pin by DC voltage (VTH)

This pin reads the input DC voltage and controls rotational speed. The VTH voltage is compared with the CPWM chopping wave with an internal comparator and generates PWM pulse and controls rotational speed with frequency and duty-cycle of this pulse.

The CPWM amplitude is decided by VREF. Thus, VTH recommends that it is made from VREG. The combination with the rotational speed control by PWM is impossible. When the pin is not used, it should be OPEN. Refer 'PWM duty control by analog voltage' on page 23. (Figure26)

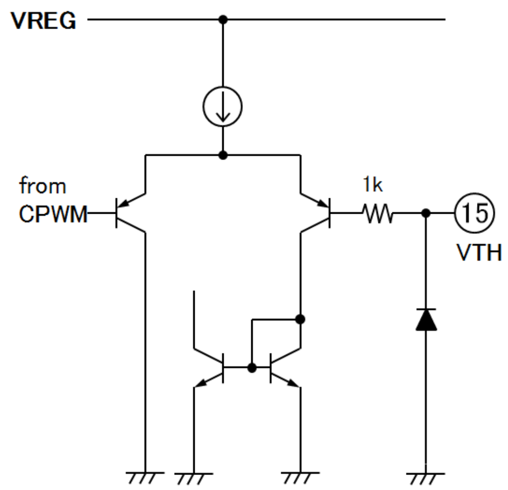


Figure26. Equivalent circuit of VTH

NC Pin (NC)

Do not connect any signal to the NC pin.

DETAILED DESCRIPTION As for all numerical value used in this description, the design value or the typical value is used.

Rotation Direction

The motor type can be categorized into two groups as 3S2P and 3S4P. (S: Slot, P: Pole). The 3S2P group contains 3S2P, 6S4P and 12S8P, for instance, and 3S4P groups contains 3S4P, 6S8P and 9S12P. The rotate direction of 3S2P group is CW, that of 3S4P group is CCW. The direction can be changed by exchanging connection between U and W, in the case where the hall sensor is between U coil and W coil. (Figure27)

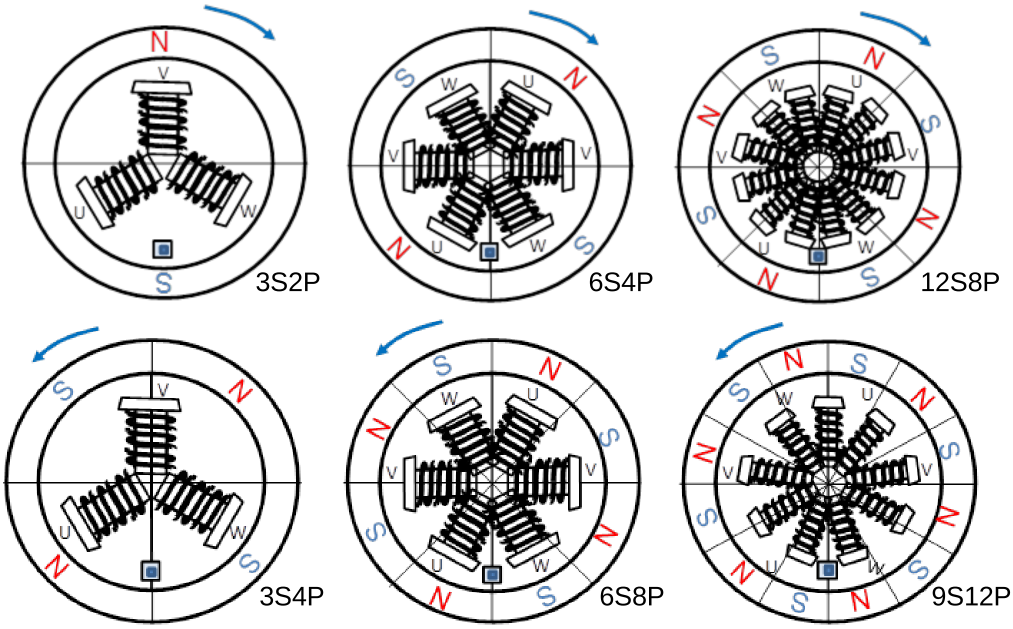


Figure27. Schematic diagram of motor

Hall output polarity also needs to be set with the type of SP motors. It is shown in Figure28, 29

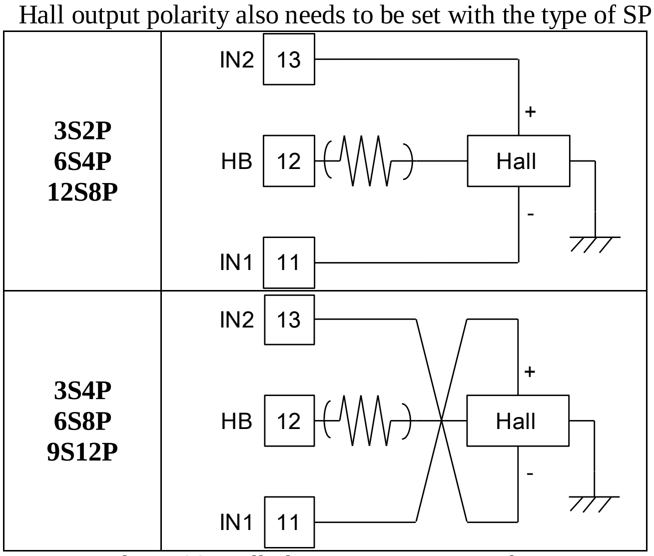


Figure28. Hall element use connection

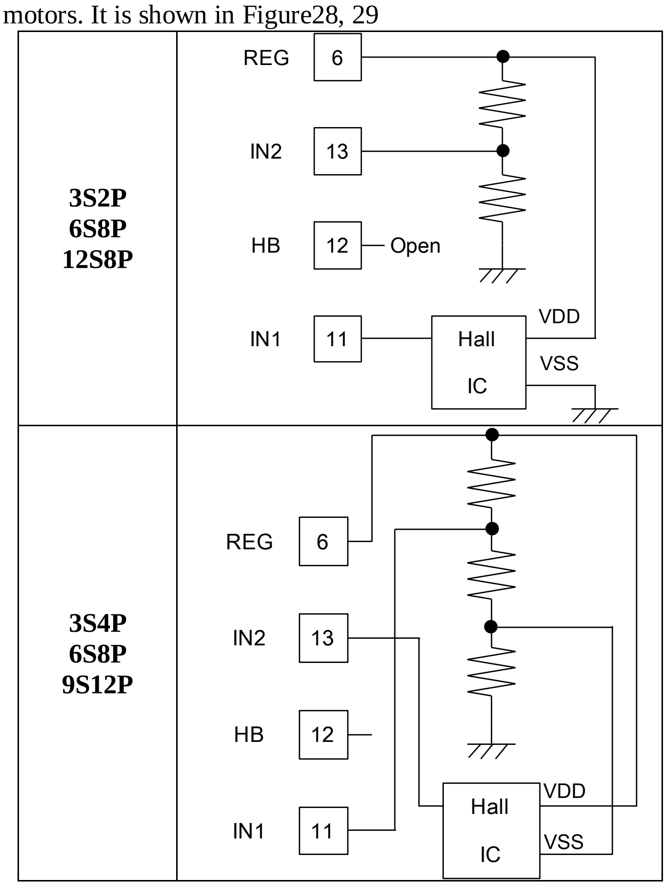


Figure29. Hall IC use connection

Device Start-up

The LV8811G/13G will start driving, when the PWM signal is input at the PWMIN pin after a power supply is turned on.

Commutation

The commutation timing is determined with respect to the one Hall sensor connected to the pin IN1, while conventional sensor-based BLDC motor drivers need three sensors.

Output Waveform

The output PWM duty cycle is modulated so that the phase-to-phase voltage waveform is sinusoidal. Two phases are driven with PWM, while the other phase sunk to ground.

It can handle the rotational speed up to the 250Hz of FG frequency (electrical cycle). However, for higher speed case, it depends on motor mechanical parameters.

A wave pattern example is shown in Figure30.

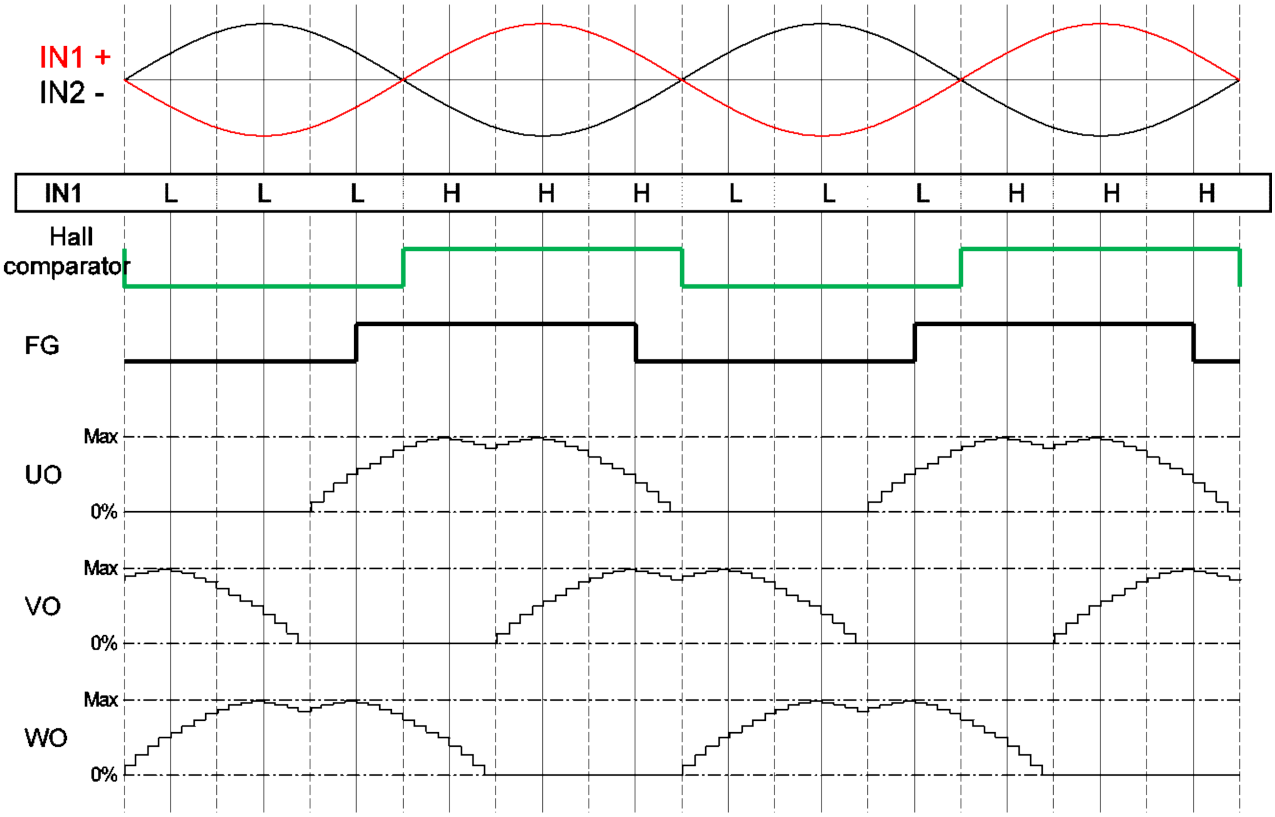
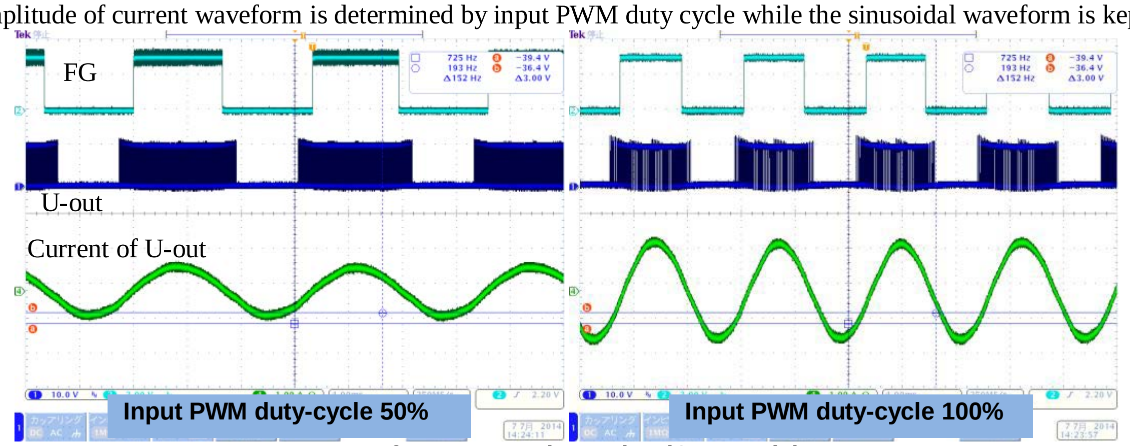


Figure30. Timing chart example: Normal Rotation

The amplitude of current waveform is determined by input PWM duty cycle while the sinusoidal waveform is kept.



Waveform1. Normal Rotation (Output pin)

Detail of the Rotor Start Position Alignment

After detecting input PWM, the motor is aligned to the start position.

[LV8811G]

The output PWM duty cycle sequence for the rotor alignment consists of the three steps.

Alignment duty 1st: 6%, 2nd: 5%, 3rd: 20%

[LV8813G]

The output PWM duty cycle sequence for the rotor alignment consists of the single step.

Alignment duty 50%

The start position alignment is independent on the input PWM duty cycle, and applies the preset duty cycle described above. (Figure31.)

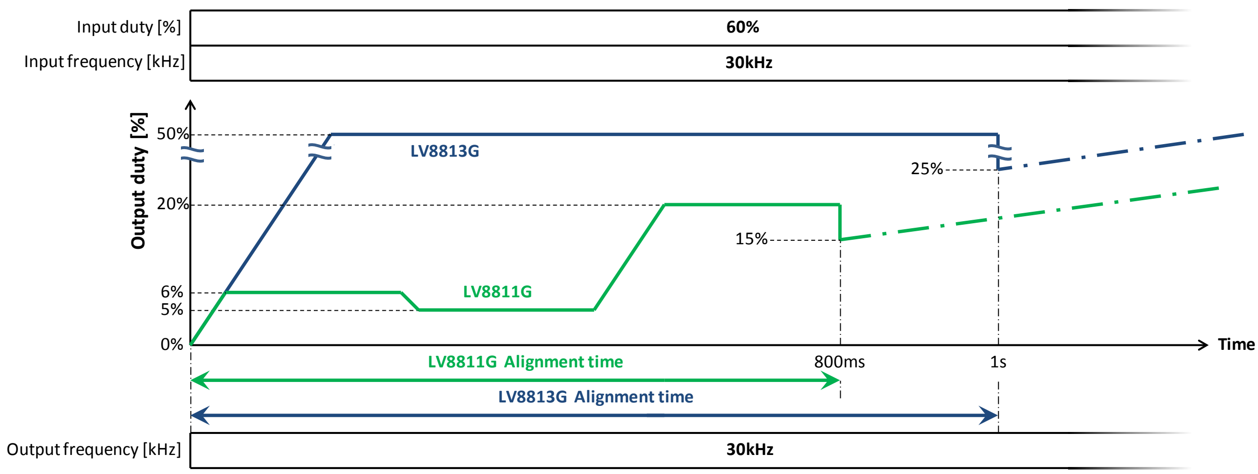


Figure31. Timing chart example: Alignment duty cycle

Rotation Start-up and Soft-start

After alignment at the start position, the motor starts to rotate in sinusoidal drives, increasing output duty-cycle (increment slope is 26%/s) till the output duty-cycle reaches the target duty-cycle. In case the input PWM duty-cycle is under 20%, the output duty-cycle decreases to the target duty-cycle after reaching 20%. After 32 FG pulses the lead angle increases to the target lead angle (tuned from PH1/PH2) by 1 degree steps at every FG edge. (Figure32)

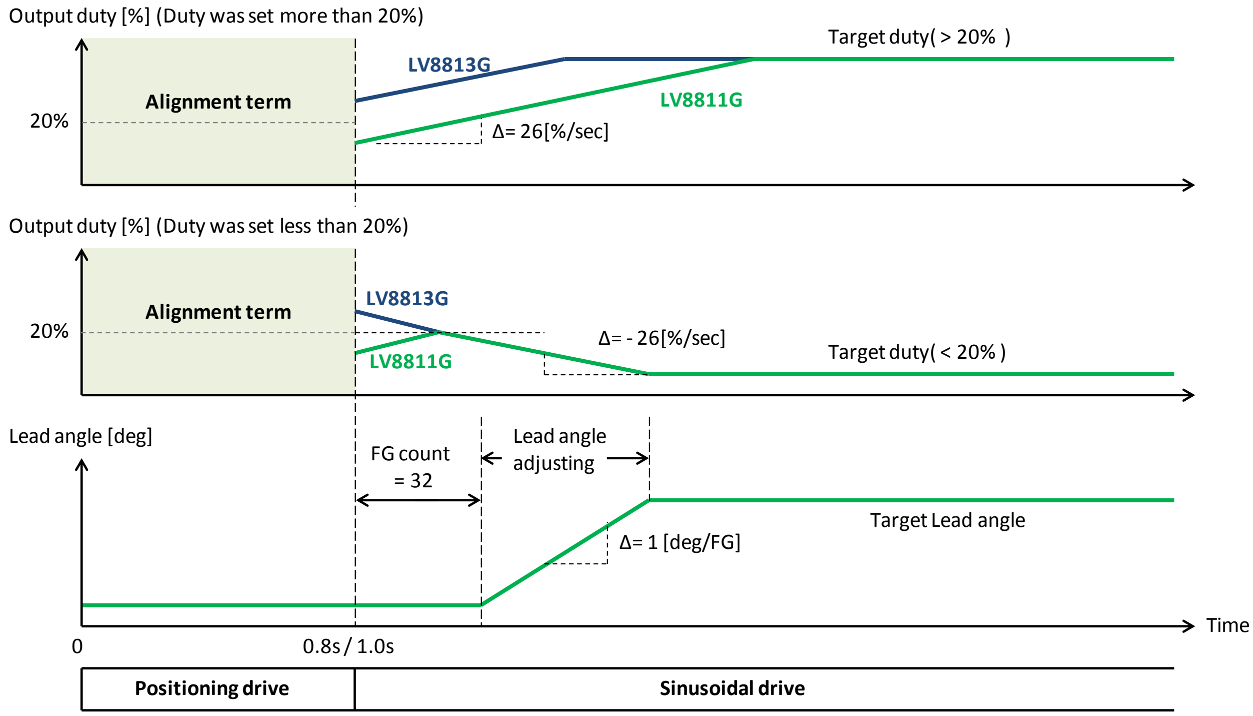
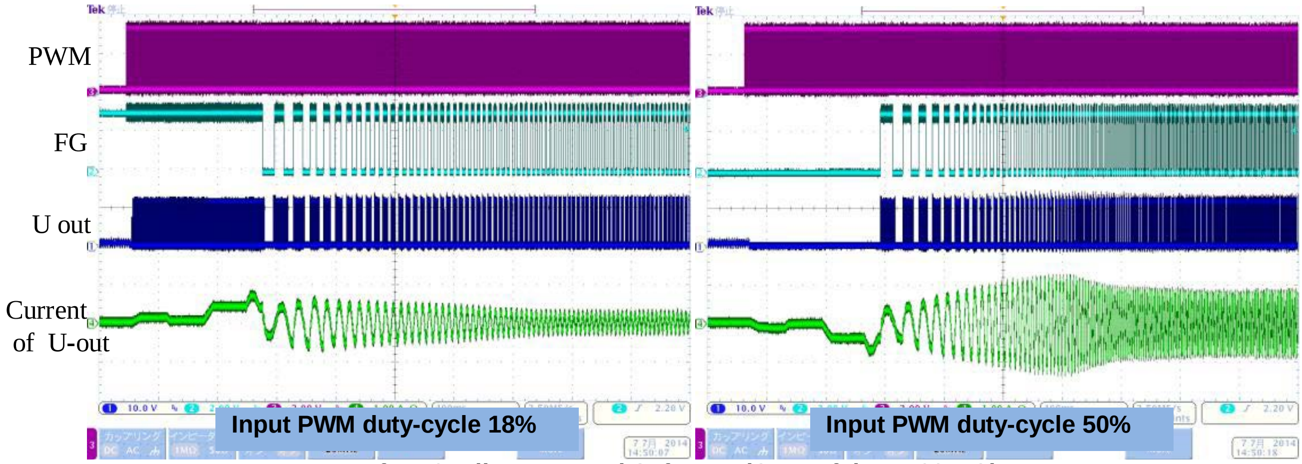


Figure32. Timing chart example: Positioning and Soft start



Waveform2. Alignment and Soft start (Case of the LV8811G)

Duty cycle decreasing and Stop

When input PWM duty cycle is changed from 80% to 20%, the output duty cycle decreases gradually to 20% with the decrement slope of 26[%/s]. The target duty-cycle is always updated at positive edge of FG. (Figure33)

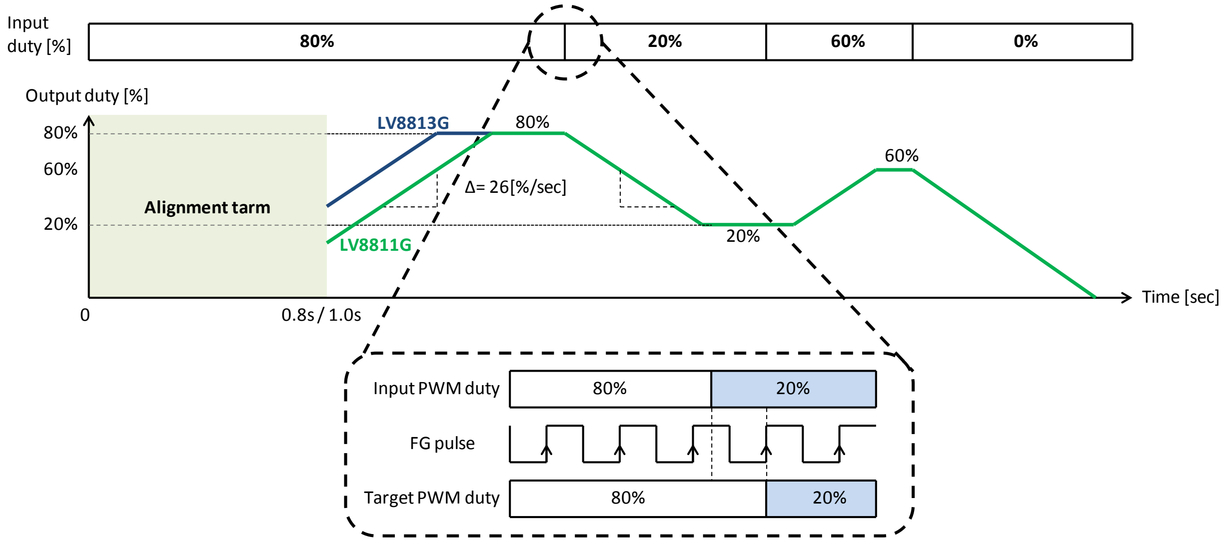
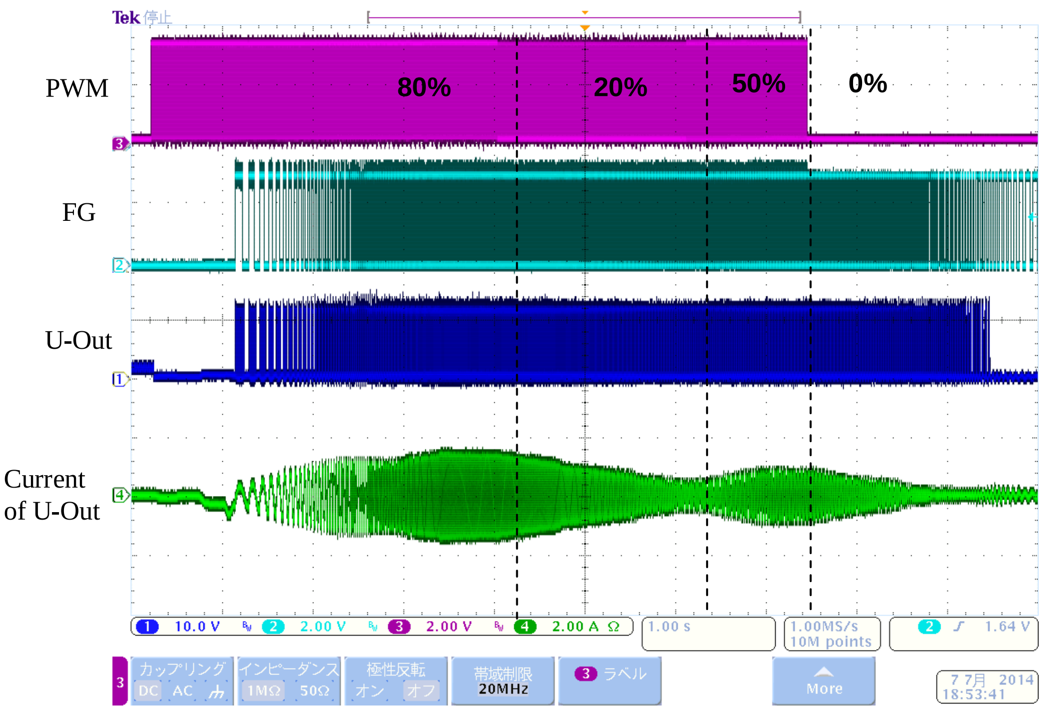


Figure33. Timing chart example: When PWM Duty changed



Waveform3. Input duty changing (Case of the LV8811G)

Output Frequency

When input PWM duty-cycle is 100%, the output frequency is 66k Hz generated from the internal oscillator. When input PWM duty-cycle is changed from 100% to 50% with 30k Hz, output frequency is changed from 66k Hz to 30k Hz. When input PWM duty-cycle is changed to 100% again, output frequency will remain 30k Hz. (Figure34)

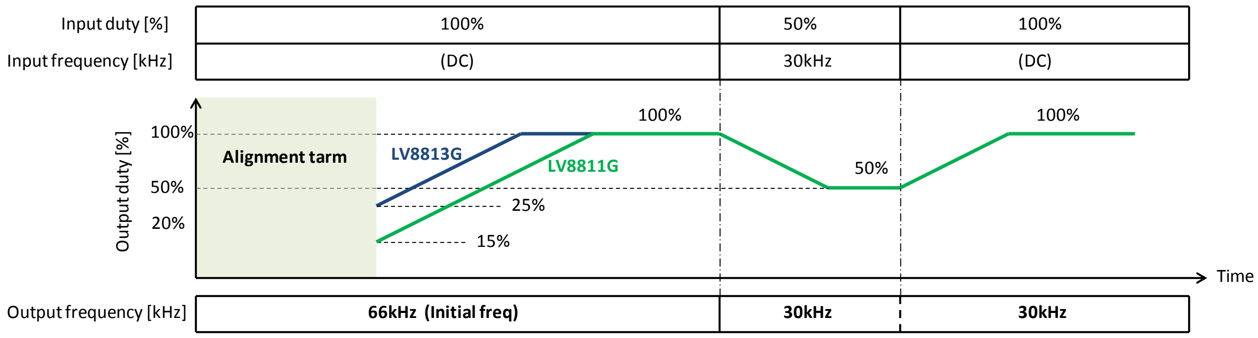


Figure34. Timing chart example: Output frequency changing

Protections

When THP (Thermal Protection) or CLM (Current Limiter) is detected, the output duty cycle decreases to the minimum duty cycle rapidly. After exiting the protection mode, the output duty cycle increases with 26%/sec slope. When OVP or LVD signal are detected, all outputs are turned off. After OVP and LVD are released, outputs are restored to the duty controlling state. (Figure35)

When the current limiter is activated with 80% input duty cycle, the output duty cycle may be restricted before achieving target duty cycle(80%). When the PWM input changes from less than low duty cycle such as 50%, the output duty cycle decreases gradually to 50% with normal slope rate. (Figure36)

When current limiter activates with 100% input duty, the output duty is restricted before achieving target duty cycle (100%). When the PWM input changes from less than low duty cycle such as 50%, the output duty cycle decreases to 50% immediately without slope rate. (Figure37)

The level of current limiter is adjustable using the value of RF resistor.

The value of RF resistor should be set higher than the current drawn at 100% input duty cycle.

Lock detection and Lock protection

[LV8811G]

It takes 5.8s for Lock-stop release. Lock restart time is 1.16s. This equals the total of lock detect time and the alignment time. The lock restart time ratio is approx. 1:5. Output under lock protection is in Hi-Z state. (Figure 38)

[LV8813G]

The lock protection behavior is same as LV8811G. However, the release time and restart time are changed as follows:

Lock-stop release time: 5.23s Lock restart time: 1.77s

Lock restart ratio: approx. 1:3 (Figure 39)

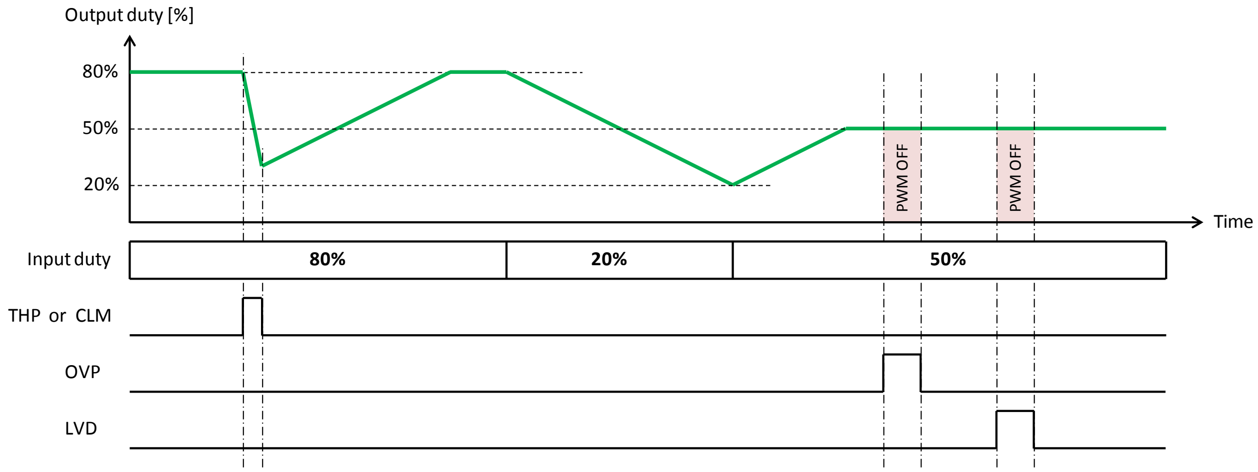


Figure35. Timing chart example: Protections

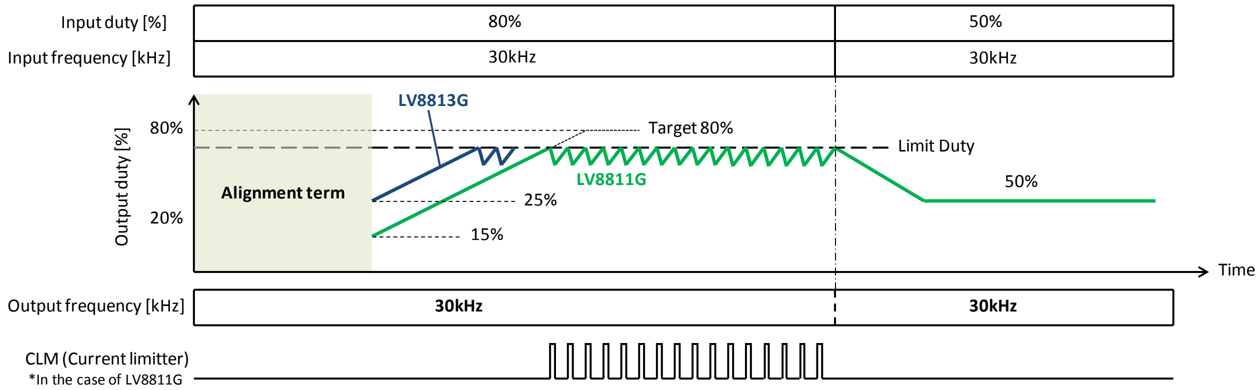


Figure36. Timing chart example: Normal current limiter

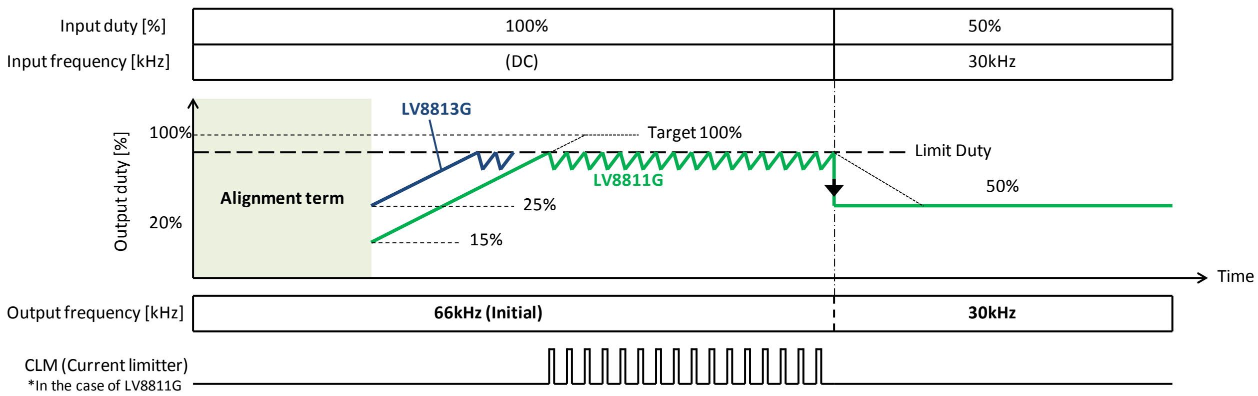
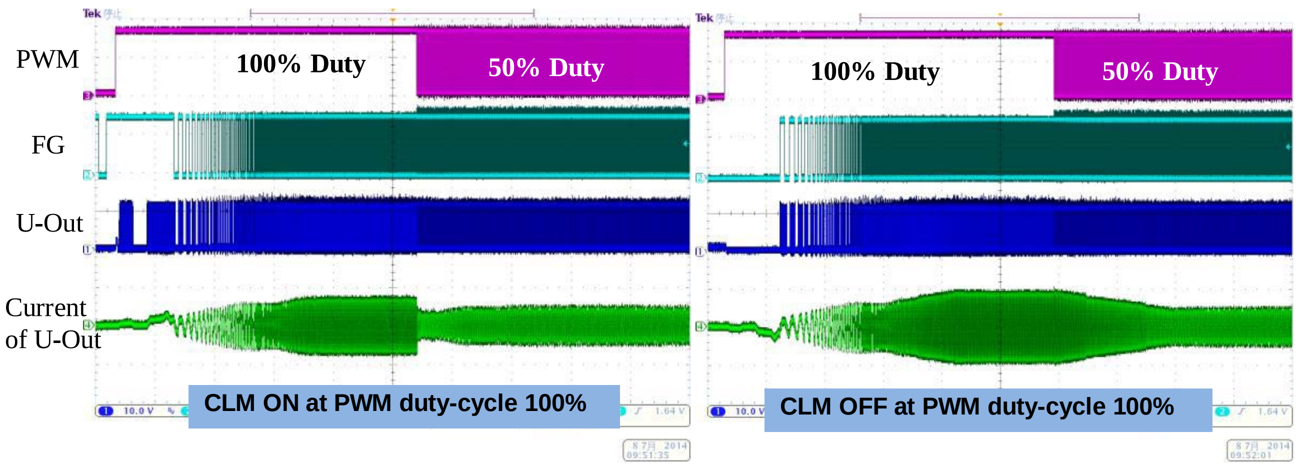


Figure37. Timing chart example: Current limiter at input duty 100%



Waveform4. Inputting 100% with and without CLM (Case of the LV8811G)

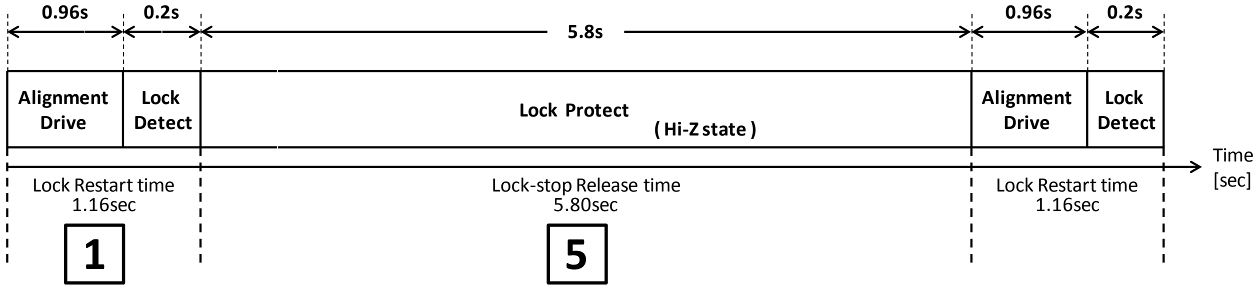


Figure38. Timing chart example: Lock Protection for LV8811G

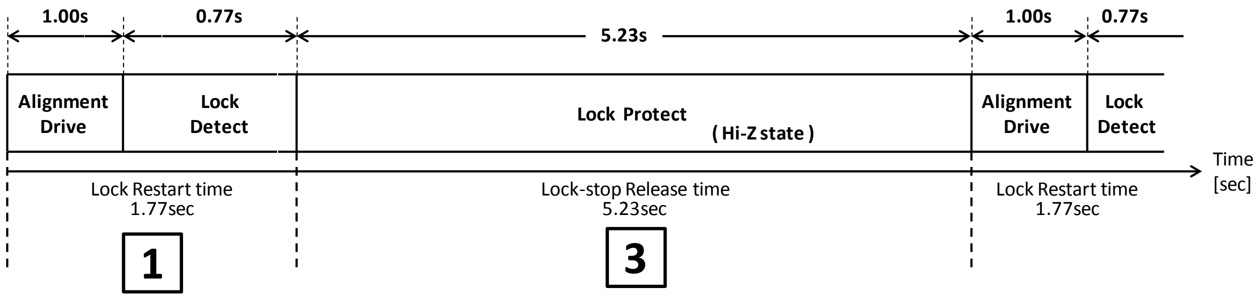
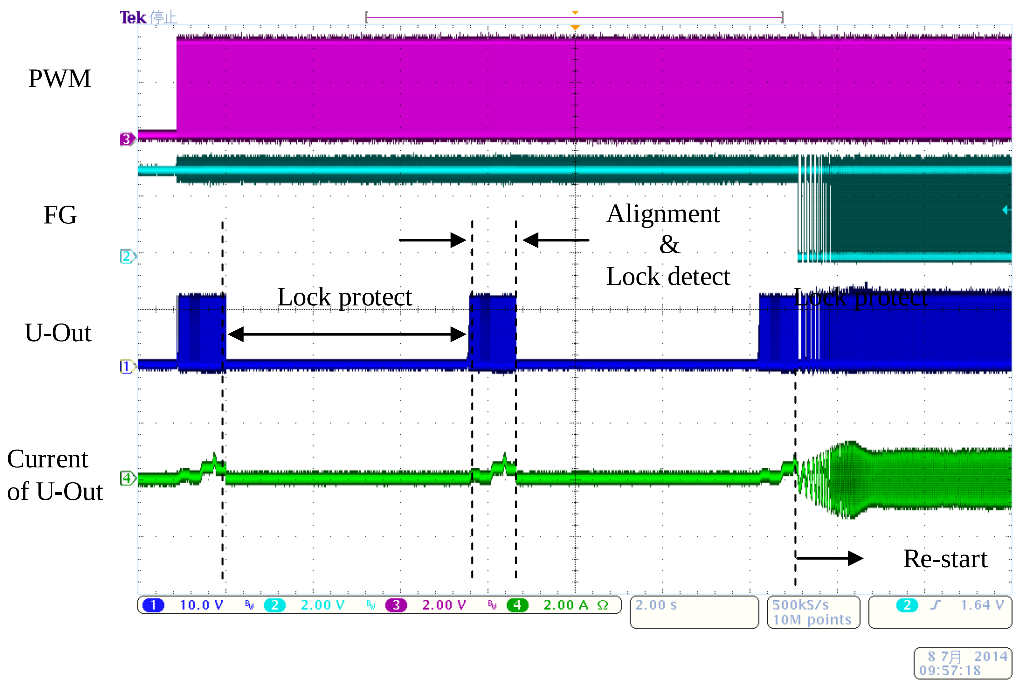


Figure39. Timing chart example: Lock Protection for LV8813G



Waveform5. Lock Protection (Case of the LV8811G)

PWM duty control by analog voltage

The duty cycle of PWM output is determined by comparison of CPWM oscillation and DC level which is input to VTH pin. When CPWM level is lower than VTH, the PWM output applies the voltage to the coil from the power supply. When CPWM level is higher than VTH, the PWM output is switched to the current circulation state with self-induction of the coil.

The DC level of VTH must be within a range of VREG×18% to VREG×67%. The PWM pulse width must not make less than 200ns. (Figure40)

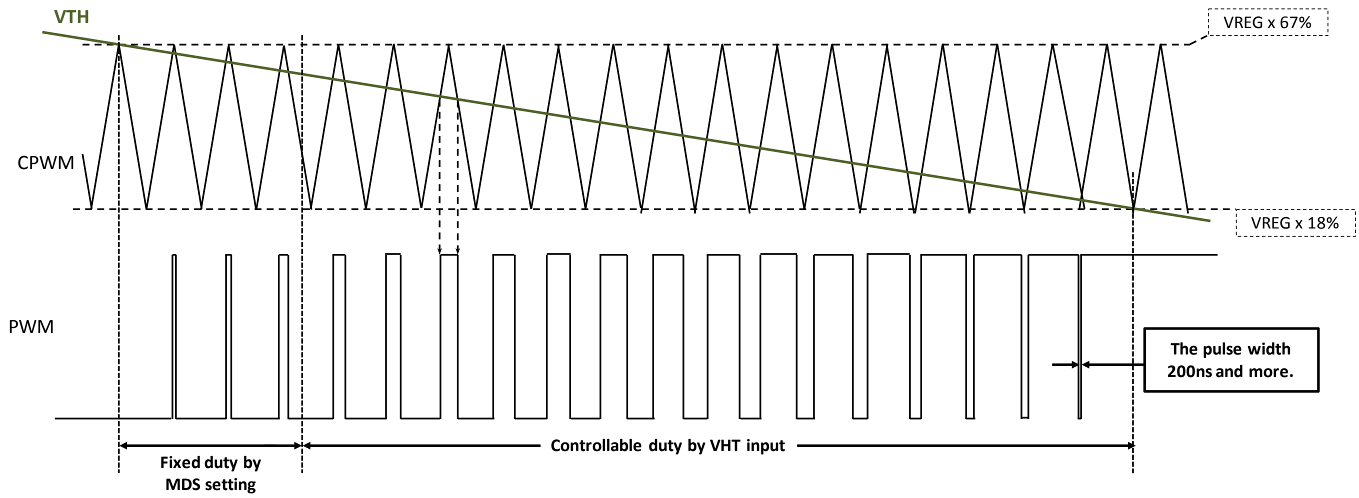


Figure40. PWM Duty control by CPWM and the VTH voltage

Parameter Setting by Constant Voltage

PH1, PH2 and MDS can be set by an external DC voltage. PH1 and PH2 are used for setting the lead angle. MDS is for setting minimum duty cycle. The input span of these pins is 0 to 3V (VREG). The full scale is divided by 64 steps, thus the resolution is 47mV/step. Excluding the lowest 3 steps and the highest 2 steps, the DC voltage is translated to the parameters linearly. Hence, the linear setting range is 0.141V to 2.906V. The voltage within the lowest 3 steps (0 to 0.141V) selects the default value. As for the highest 2 steps, it is described in the following sections. (Figure41)

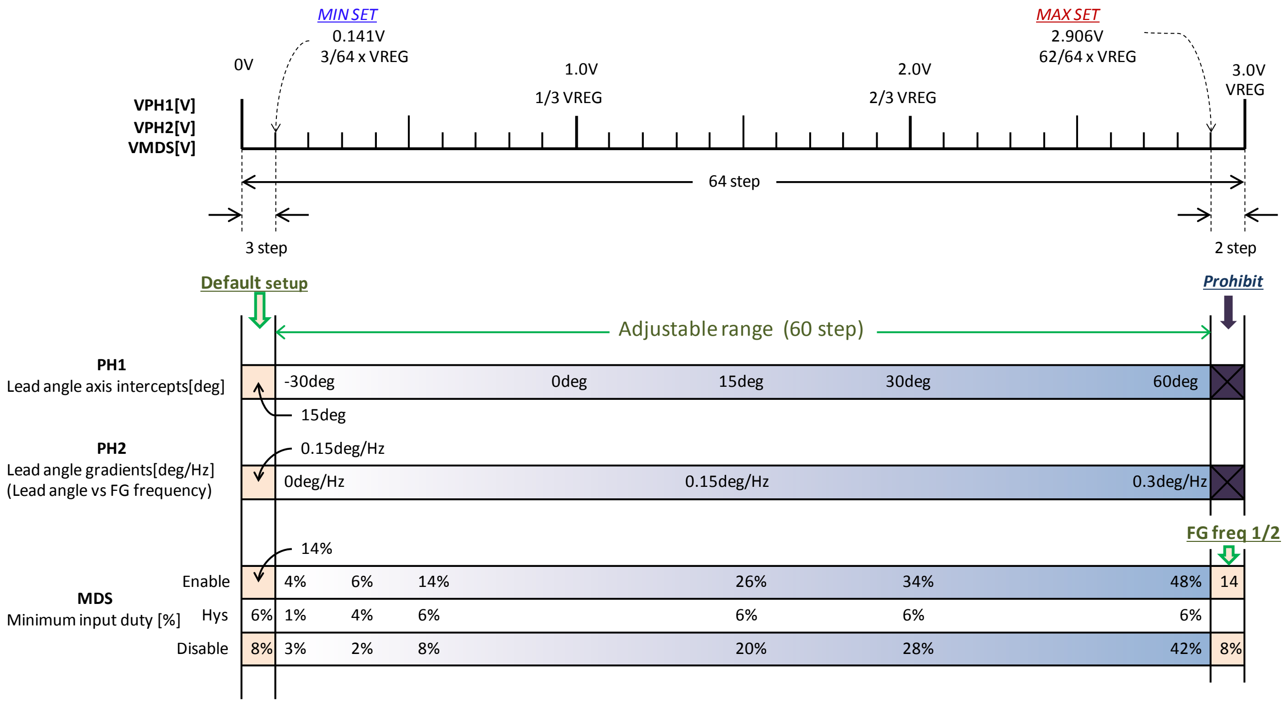


Figure41. Pin-set PH1, PH2 and MDS

Setting Minimum PWM Duty Cycle

When the input PWM duty cycle is less than the minimum duty cycle, which is set by MDS pin voltage, the output duty cycle becomes 0%. (Figure 42, 43) And, this threshold has hysteresis. In the meantime, MDS pin is also used for the FG frequency setting.

V_{MDS} range [V]	0.141	0.282	0.752	2.906	3.0
	0	0.141	0.282	0.752	2.906
Minimum input duty cycle hysteresis [%]	6	1	4	6	6
Minimum input duty cycle for enable [%]	14	$15.9V_{MDS} + 1.763$			14
Minimum input duty cycle for disable [%]	8	$15.9V_{MDS} + 1.763 - hys$			8
FG cycle	1 electrical				2 electrical

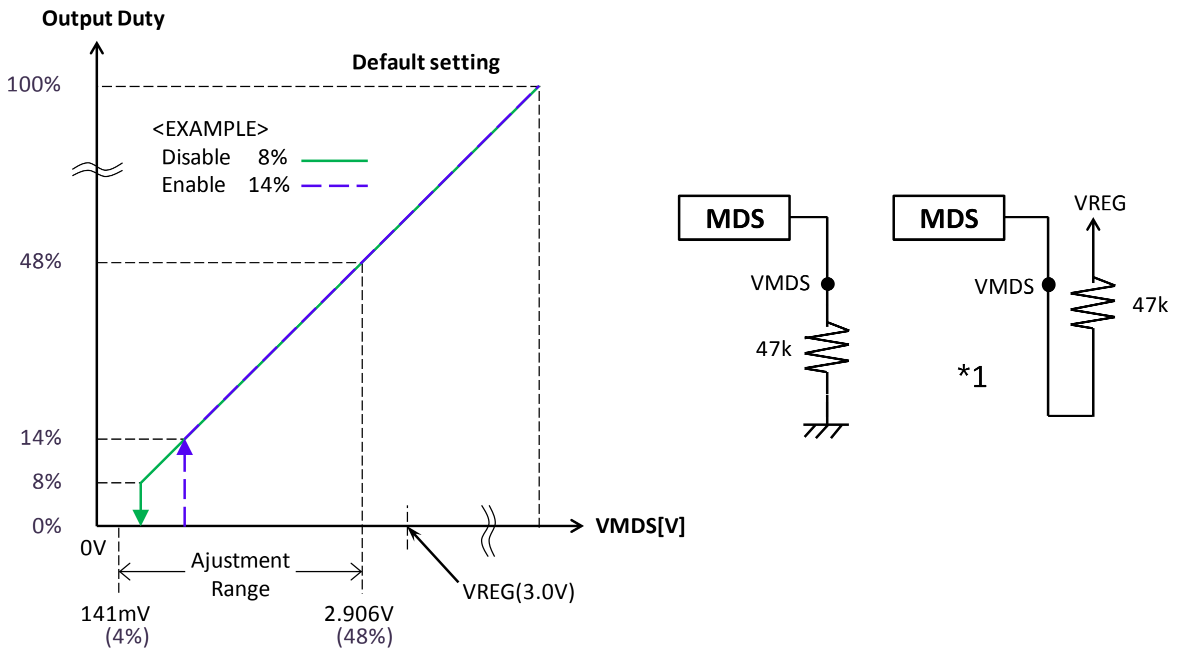


Figure42. Setting Minimum PWM duty 1 (Default set)

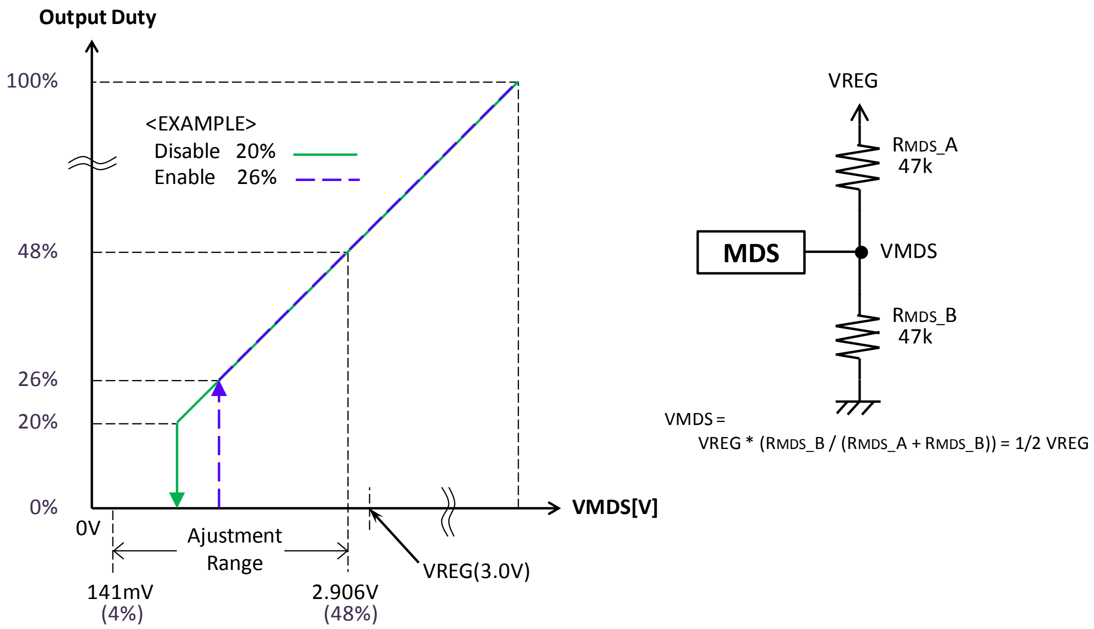


Figure43. Setting Minimum PWM duty 2

Setting Lead Angle

PH1 and PH2 pin determine the optimum lead angle for a specific speed range. PH1 provides lead angle at the low speed, The PH2 pin provides lead angle slant for speed (FG frequency). Both pins become the initial value in GND. (Figure44, 45, 46)

The lead angle P (typ.) is determined by the following equation.

$$P = Af_{FG} + B$$
$$A = 0.1081V_{PH2} - 0.015$$
$$B = 32.54V_{PH1} - 34.58$$

where f_{FG} is FG frequency [Hz]

when $V_{PH2} = 0$

$$A = 0.15[\mathrm{deg/Hz}]$$
$$B = 15[\mathrm{deg}]$$

Note: The equations above are based on the ideal case as a reference for the user application design. It must be readjusted by an experimental confirmation with the actual movement and the motor to be used.

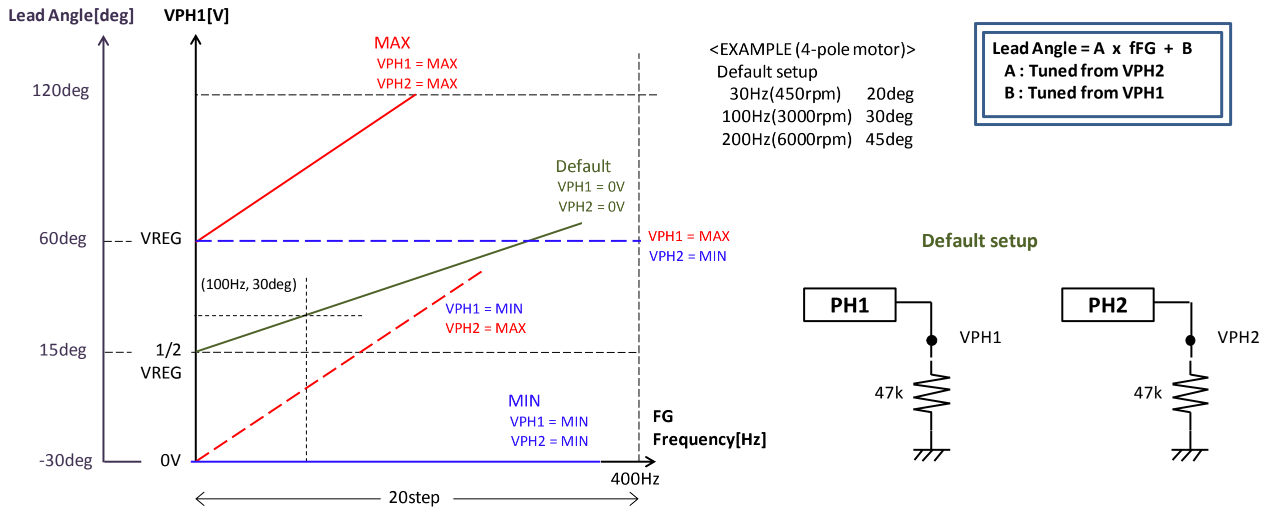


Figure44. Setting Lead Angle 1 (Default set)

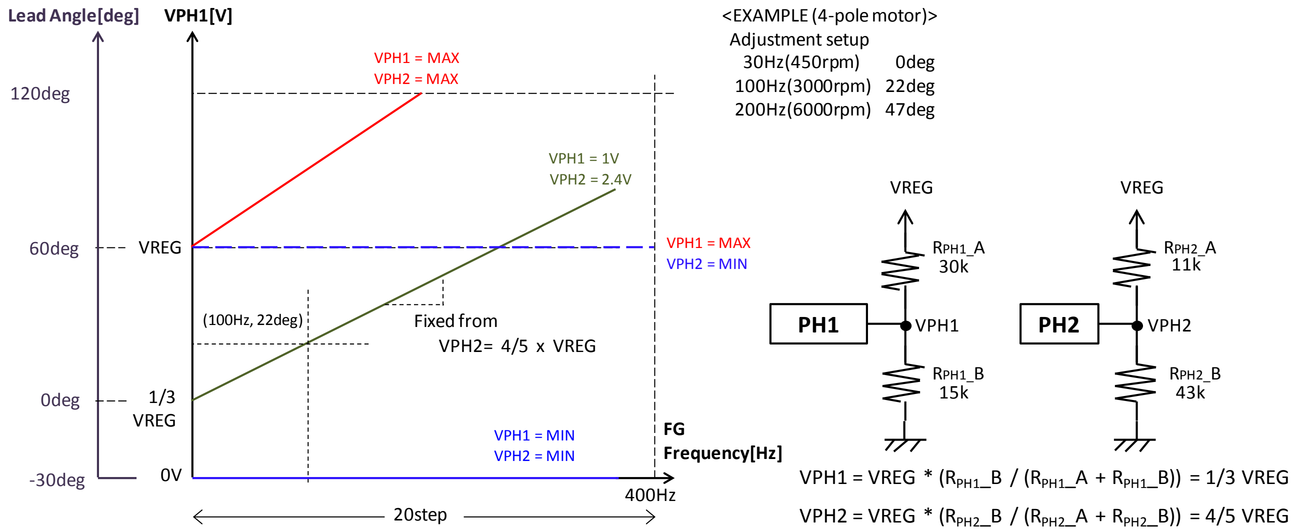


Figure45. Setting Lead Angle 2

Sinusoidal PWM signals are generated from 1-hall signal, handling the lead angle parameters.

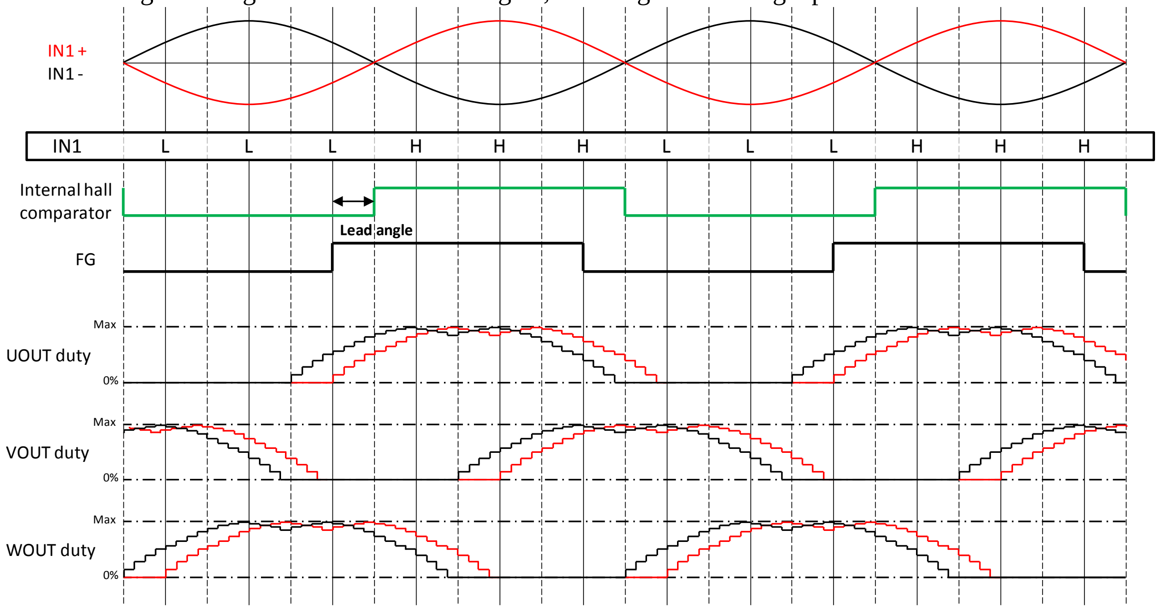
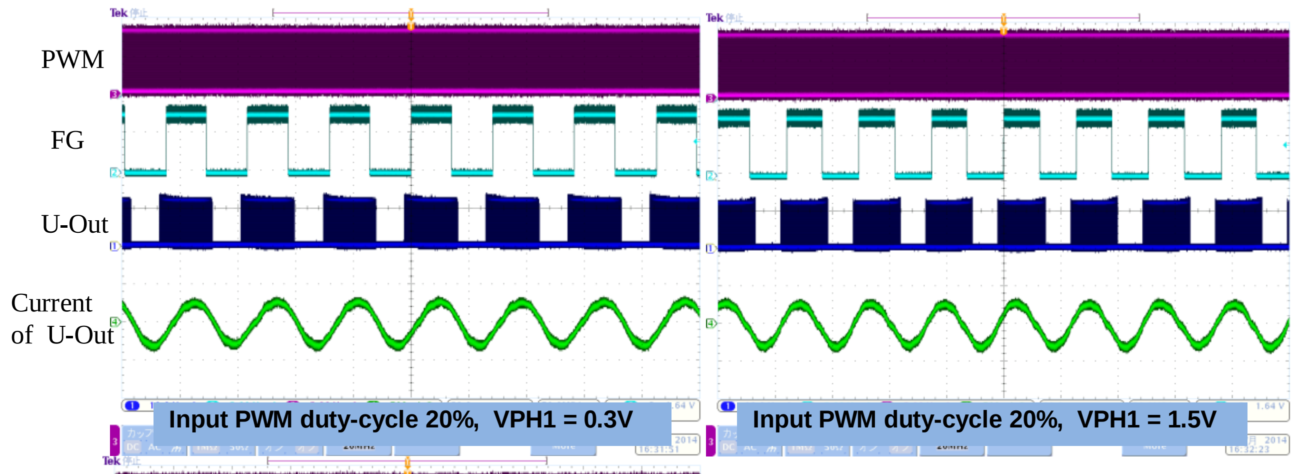
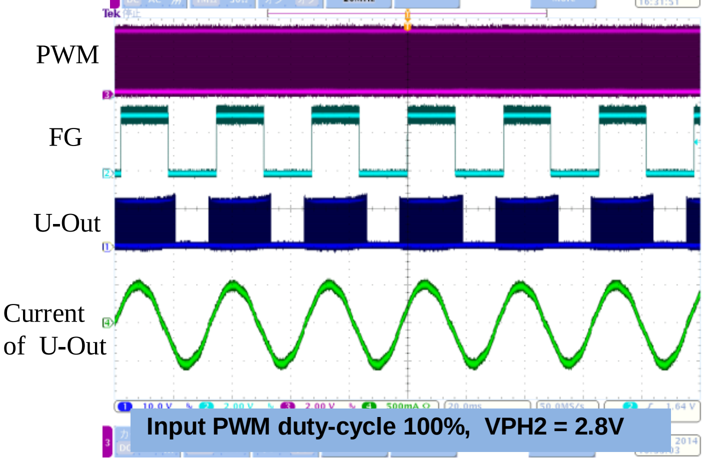
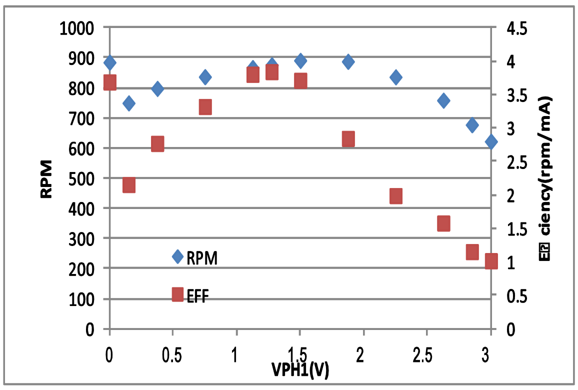


Figure46. Timing chart example: Lead Angle

Efficiency and sinusoidal waveform can be optimized by changing the voltage levels of PH1 and PH2. First, adjust PH1 in low speed (low PWM duty-cycle) such as 20%. In the examples below, VPH1 = ~1.5V is the best case for efficiency and the shape of sinusoidal wave. After optimizing VPH1, adjust VPH2 adjusted in high speed (high PWM duty-cycle) such as 100%. (Figure47, Waveform6)







Waveform6. Lead Angle at input PWM = 20% (Case of the LV8811G)
Figure47. Lead angle VS Speed and Efficiency at input PWM = 20% (Case of the LV8811G)

PCB GUIDELINES

VCC and Ground Routing

Make sure to short-circuit VCC line externally by a low impedance route on one side of PCB. As high current flows into PGND, connect it to GND through a low impedance route.

The capacitance connected between the VCC pin and the opposite ground is to stabilize the battery. Make sure to connect an electrolytic capacitor with capacitance value of about 10uF (3.3uF or greater) to eliminate low frequency noise. Also, to eliminate high frequency noise, connect a capacitor of superior frequency characteristics, with capacitance value of about 0.1uF and make sure that the capacitor is connected as close to the pin as possible. Allow enough room in the design so the impact of PWM drive and kick-back does not affect other components. Especially, when the coil inductance is large and/or the coil resistance is small, current ripple will rise so it is necessary to use a high-capacity capacitor with superior frequency characteristics. Please note that if the battery voltage rises due to the impact of the coil kick-back as a result of the use of diode for preventing the break down caused by reverse connection, it is necessary to either increase the capacitance value or place Zener diode between the battery and the ground so that the voltage does not exceed absolute maximum voltage.

When the electrolytic capacitor cannot be used, add the resistor with the value of about 1Ω (R20) and a ceramic capacitor with the capacitor value of about 10μF (C20) in series for the alternative use. When the battery line is extended, (20-30 cm to 2-3 m), the battery voltage may overshoot when the power is supplied due to the impact of the routing of the inductance. Make sure that the voltage does not exceed the absolute maximum standard voltage when the power supply turns on.

These capacitance values are just for reference, so the confirmation with the actual application is essential to determine the values appropriately.

Exposed Pad

The exposed pad is connected to the frame of the LV8811G. Therefore, do not connect it to anywhere else other than ground. If GND and PGND are in the same plane, connect the exposed pad to the ground plane. Else, if GND and PGND are separated, connect the exposed pad to GND.

RF Routing

Power current (output current) flows through the RF line. Make sure to short-circuit the line from VCC through RF as well as VCC. The RF resistance should choose the enough power rating.

NC Pin Utilization

NC pins are not connected internally inside the LV8811G. If the NC pin has to be connected to another pin for the development of the PCB board, make sure to assign the pin using wires of stable voltage and current with lower impedance value.

Motor Driver Output Pins

Since the pins have to tolerate surge of current, make sure that the wires are thick and short enough when designing the PCB board.

Thermal Test Conditions

Size: 56.5mm × 56.5mm × 1.8mm (Double layer PCB)
Material: Glass epoxy
Copper wiring density: L1 = 80% / L2 = 85%

Recommendation

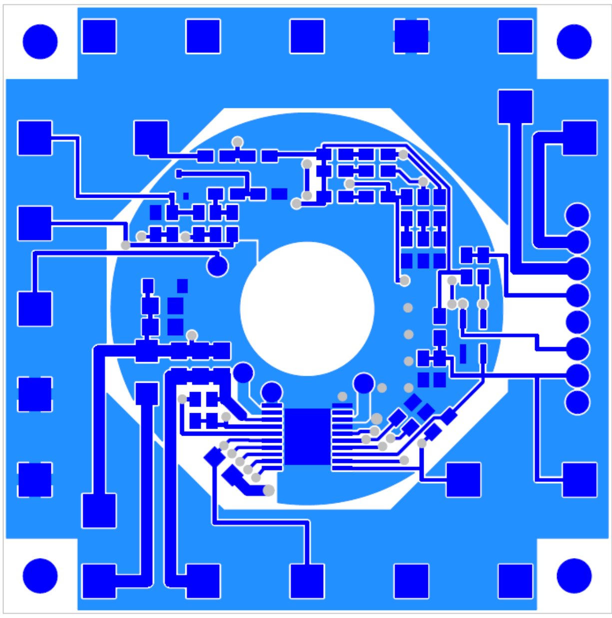
The thermal data provided is for the thermal test condition where 90% or more of the exposed die pad is soldered.

It is recommended to derate critical rating parameters for a safe design. Electrical parameters that are recommended to be derated are operating voltage, operating current, junction temperature, and device power dissipation. The recommended derating for a safe design is as shown below:

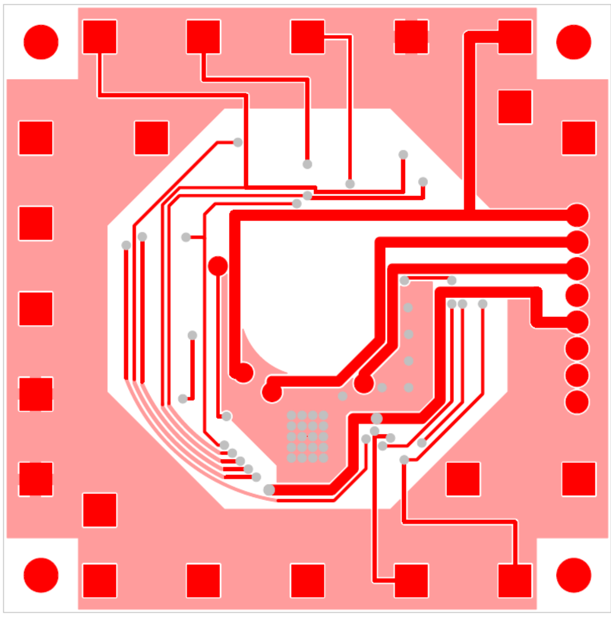
- Maximum 80% or less for operating voltage
- Maximum 80% or less for operating current
- Maximum 80% or less for junction temperature

Check solder joints and verify reliability of solder joints for critical areas such as exposed die pad, power pins and grounds.

Any void or deterioration, if observed, in solder joint of these critical areas parts, may cause deterioration in thermal conduction and that may lead to thermal destruction of the device.



L1 : Copper wiring pattern diagram (top)

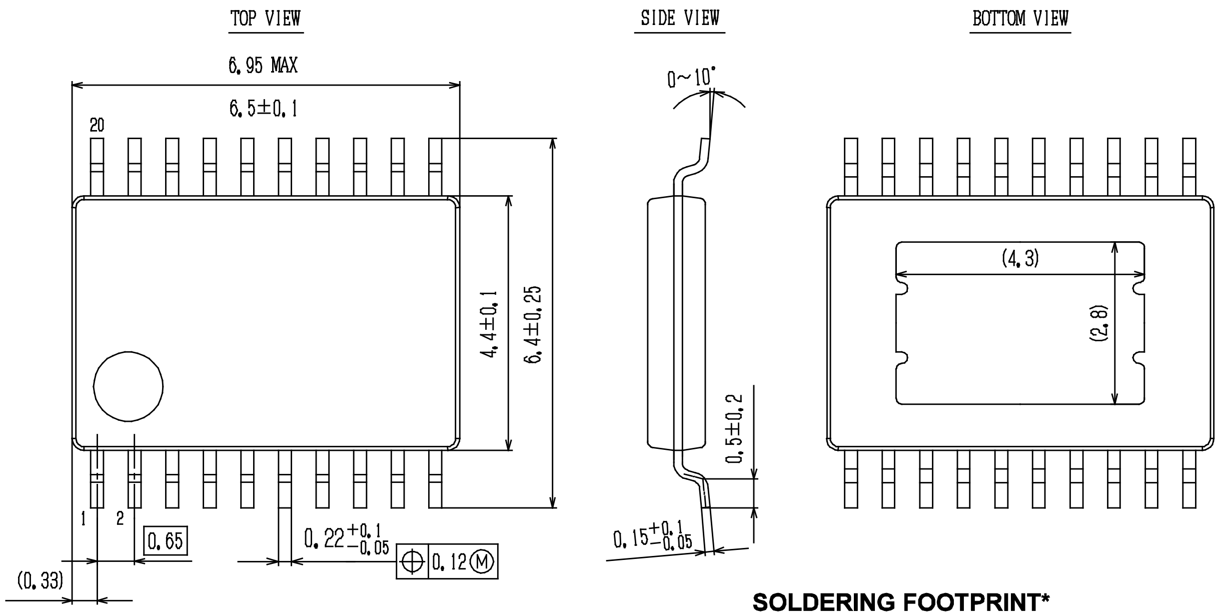


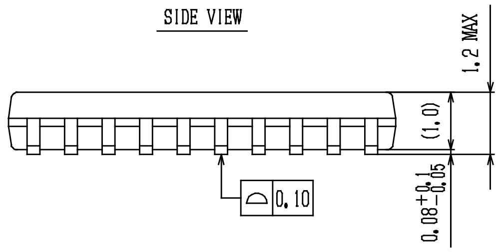
L2 : Copper wiring pattern diagram (bottom)

Figure48. Pattern Diagram of Top and Bottom Layer

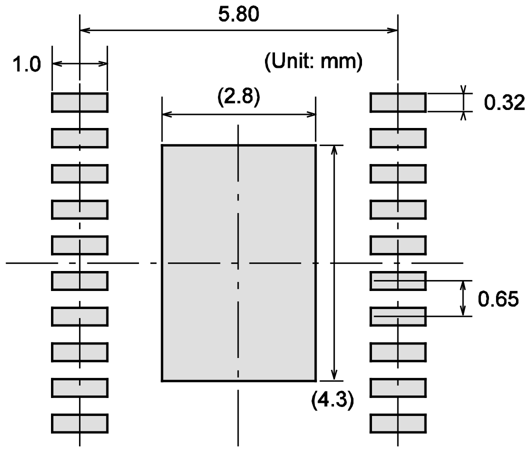
PACKAGE DIMENSIONS

TSSOP20 4.4x6.5 / TSSOP20J (225 mil)
CASE 948AZ
ISSUE A





SOLDERING FOOTPRINT*



NOTES: 1. The measurements are not to guarantee but for reference only.
2. Please take appropriate action to design the actual Exposed Die Pad and Fin portion.
3. After setting, verification on the product must be done.
(Although there are no recommended design for Exposed Die Pad and Fin portion Metal mask and shape for Through! Hole pitch (Pitch & Via etc), checking the soldered joint condition and reliability verification of soldered joint will be needed. Void • gradient • insufficient thickness of soldered joint or bond degradation could lead to IC destruction because thermal conduction to substrate becomes poor.)

*For additional information on our Pb! Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.