

# MC14020B

## 14-Bit Binary Counter

The MC14020B 14-stage binary counter is constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

### Features

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- Pin-for-Pin Replacement for CD4020B
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

#### 1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

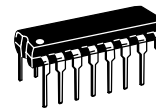
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

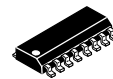


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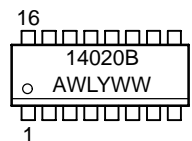
### MARKING DIAGRAMS



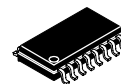
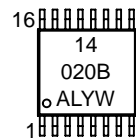
PDIP-16  
P SUFFIX  
CASE 648



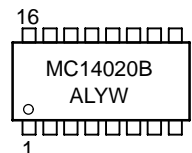
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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## PIN ASSIGNMENT

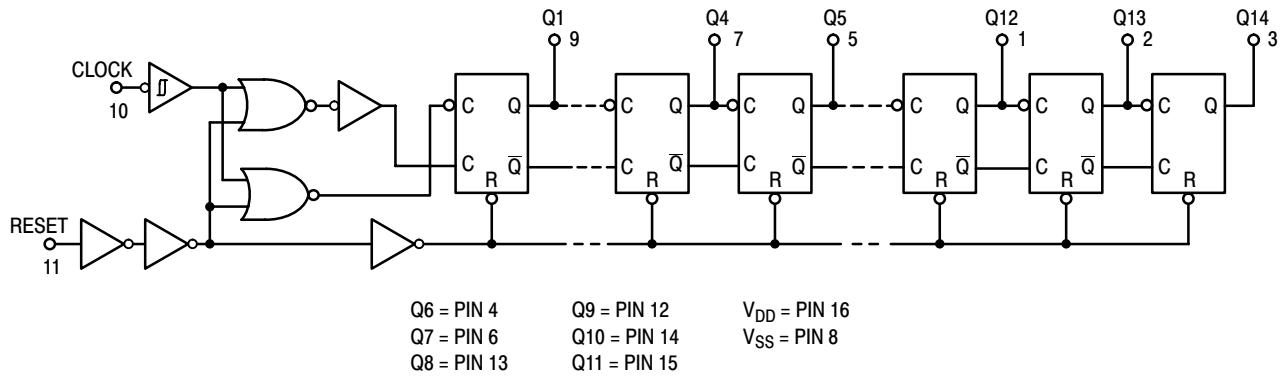
Q12	1 ●	16	V <sub>DD</sub>
Q13	2	15	Q11
Q14	3	14	Q10
Q6	4	13	Q8
Q5	5	12	Q9
Q7	6	11	R
Q4	7	10	C
V <sub>SS</sub>	8	9	Q1

## TRUTH TABLE

Clock	Reset	Output State
	0	No Change
	0	Advance to Next State
X	1	All Outputs are Low

X = Don't Care

## LOGIC DIAGRAM



## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC14020BCP	PDIP-16	500 Units / Rail
MC14020BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14020BD	SOIC-16	48 Units / Rail
MC14020BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14020BDR2	SOIC-16	2500 Units / Tape & Reel
MC14020BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC14020BDT	TSSOP-16*	96 Units / Rail
MC14020BFEL	SOEIAJ-16	2000 Units / Tape & Reel
MC14020BFELG	SOEIAJ-16 (Pb-Free)	2000 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55 °C		25 °C			125 °C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level	V <sub>OL</sub>	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
			10	–	0.05	–	0	0.05	–	0.05	
15			–	0.05	–	0	0.05	–	0.05	–	
V <sub>in</sub> = 0 or V <sub>DD</sub>	"1" Level	V <sub>OH</sub>	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level	V <sub>IL</sub>	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
			10	–	3.0	–	4.50	3.0	–	3.0	
15			–	4.0	–	6.75	4.0	–	4.0	–	
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"1" Level	V <sub>IH</sub>	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
			10	7.0	–	7.0	5.50	–	7.0	–	
			15	11	–	11	8.25	–	11	–	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	I <sub>OH</sub>	5.0	– 3.0	–	– 2.4	– 4.2	–	– 1.7	–	mAdc
			5.0	– 0.64	–	– 0.51	– 0.88	–	– 0.36	–	
10			– 1.6	–	– 1.3	– 2.25	–	– 0.9	–		
15			– 4.2	–	– 3.4	– 8.8	–	– 2.4	–		
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink	I <sub>OL</sub>	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
			10	1.6	–	1.3	2.25	–	0.9	–	
			15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I <sub>in</sub>	15	–	± 0.1	–	± 0.00001	± 0.1	–	± 1.0	µAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	–	–	–	–	5.0	7.5	–	–	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	–	5.0	–	0.005	5.0	–	150	µAdc	
		10	–	10	–	0.010	10	–	300		
		15	–	20	–	0.015	20	–	600		
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (0.42 µA/kHz)f + I <sub>DD</sub> I <sub>T</sub> = (0.85 µA/kHz)f + I <sub>DD</sub> I <sub>T</sub> = (1.43 µA/kHz)f + I <sub>DD</sub>							µAdc	

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25 °C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in µA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> – V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

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## SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q1 $t_{PHL}$ , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 175 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 82 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 55 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	– – –	260 115 80	520 230 160	ns
Clock to Q14 $t_{PHL}$ , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 1735 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 772 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 535 \text{ ns}$		5.0 10 15	– – –	1820 805 560	3900 1725 1200	ns
Propagation Delay Time Reset to $Q_n$ $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 285 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 122 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$	$t_{PHL}$	5.0 10 15	– – –	370 155 115	740 310 230	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	500 165 125	140 55 38	– – –	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	– – –	2.0 6.0 8.0	1.0 3.0 4.0	MHz
Clock Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	No Limit			–
Reset Pulse Width	$t_{WL}$	5.0 10 15	3000 550 420	320 120 80	– – –	ns
Reset Removal Time	$t_{rem}$	5.0 10 15	130 50 30	65 25 15	– – –	ns

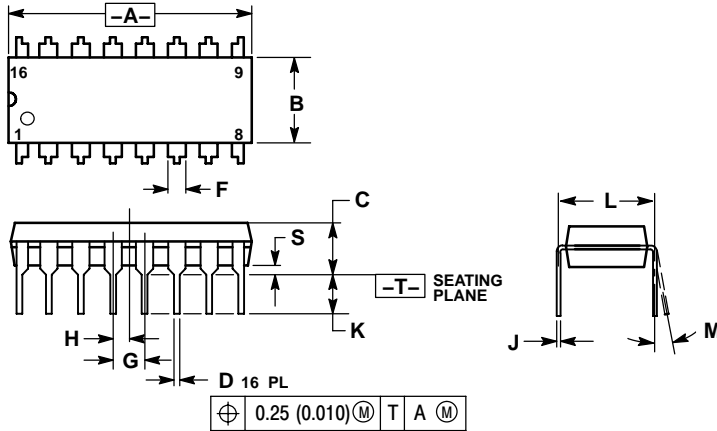
5. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14020B

## PACKAGE DIMENSIONS

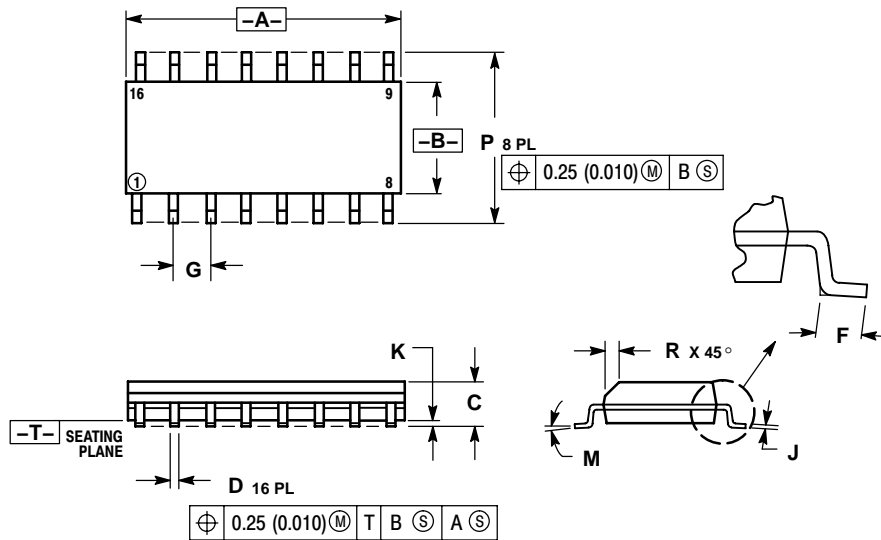
PDIP-16  
P SUFFIX  
PLASTIC DIP PACKAGE  
CASE 648-08  
ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC-16  
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751B-05  
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019