

MC74HC4040A

12-Stage Binary Ripple Counter

High-Performance Silicon-Gate CMOS

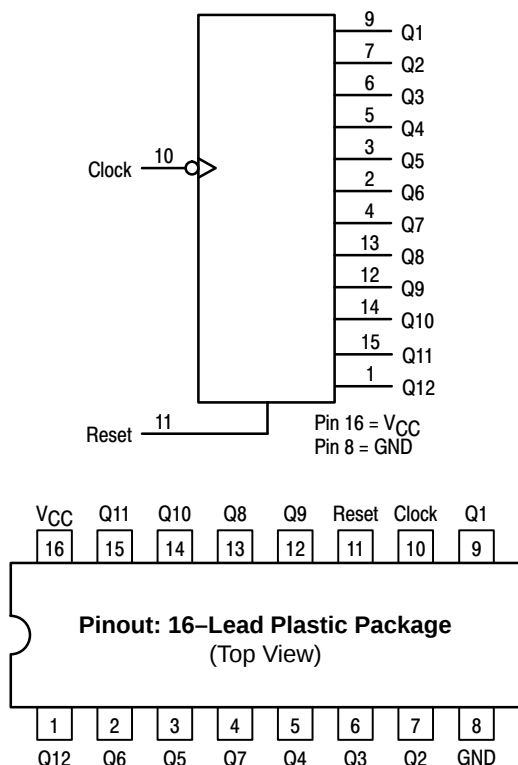
The MC74HC4040A is identical in pinout to the standard CMOS MC14040. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 12 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half of that of the preceding one. The state counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4040A for some designs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With JEDEC Standard No. 7A Requirements
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates

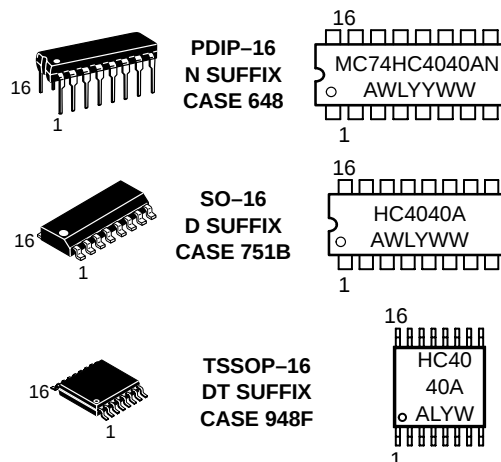
LOGIC DIAGRAM



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MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

FUNCTION TABLE

Clock	Reset	Output State
	L	No Charge
	L	Advance to Next State
X	H	All Outputs Are Low

ORDERING INFORMATION

Device	Package	Shipping
MC74HC4040AN	PDIP-16	2000 / Box
MC74HC4040AD	SOIC-16	48 / Rail
MC74HC4040ADR2	SOIC-16	2500 / Reel
MC74HC4040ADT	TSSOP-16	96 / Rail
MC74HC4040ADTR2	TSSOP-16	2500 / Reel

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T _{stg}	Storage Temperature Range	– 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C

SOIC Package: – 7 mW/°C from 65° to 125°C

TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature Range, All Package Types	– 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V 0 V _{CC} = 3.0 V 0 V _{CC} = 4.5 V 0 V _{CC} = 6.0 V 0	1000 600 500 400	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1V or V _{CC} – 0.1V I _{out} ≤ 20μA	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1V or V _{CC} – 0.1V I _{out} ≤ 20μA	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4mA	3.0	2.48	2.34	2.20	
		I _{out} ≤ 4.0mA	4.5	3.98	3.84	3.70	
		I _{out} ≤ 5.2mA	6.0	5.48	5.34	5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V

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DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4mA I _{out} ≤ 4.0mA I _{out} ≤ 5.2mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	10 15 30 50	9.0 14 28 45	8.0 12 25 40	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q1* (Figures 1 and 4)	2.0 3.0 4.5 6.0	96 63 31 25	106 71 36 30	115 88 40 35	ns
t _{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0 3.0 4.5 6.0	45 30 30 26	52 36 35 32	65 40 40 35	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Q _n to Q _{n+1} (Figures 3 and 4)	2.0 3.0 4.5 6.0	69 40 17 14	80 45 21 15	90 50 28 22	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 15	110 36 22 19	ns
C _{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

* For T_A = 25°C and C_L = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

$$V_{CC} = 2.0 \text{ V: } t_p = [93.7 + 59.3 (n-1)] \text{ ns}$$

$$V_{CC} = 4.5 \text{ V: } t_p = [30.25 + 14.6 (n-1)] \text{ ns}$$

$$V_{CC} = 3.0 \text{ V: } t_p = [61.5 + 34.4 (n-1)] \text{ ns}$$

$$V_{CC} = 6.0 \text{ V: } t_p = [24.4 + 12 (n-1)] \text{ ns}$$

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		31	

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}² f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25°C	≤85°C	≤125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	30	40	50	ns
		3.0	20	25	30	
		4.5	5	8	12	
		6.0	4	6	9	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	15	19	24	
		6.0	13	16	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	15	19	24	
		6.0	13	16	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

Clock (Pin 10)

Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter.

Reset (Pin 11)

Active-high reset. A high level applied to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

OUTPUTS

Q1 thru Q12 (Pins 9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1)

Active-high outputs. Each Q_n output divides the Clock input frequency by 2^N.

SWITCHING WAVEFORMS

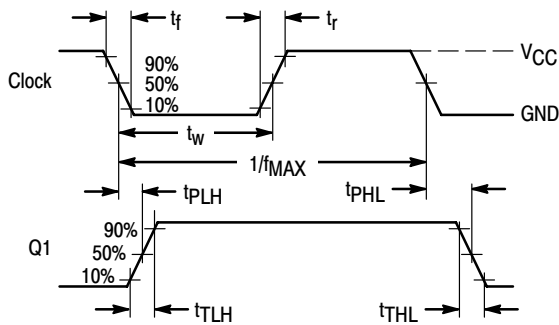


Figure 1.

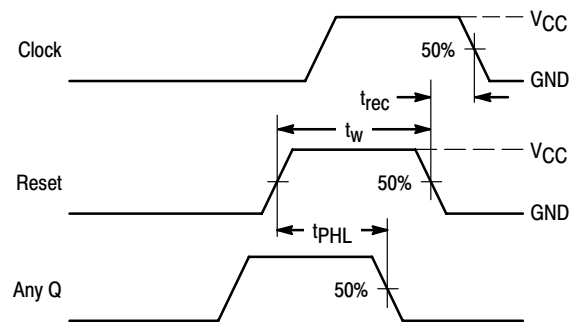


Figure 2.

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SWITCHING WAVEFORMS (continued)

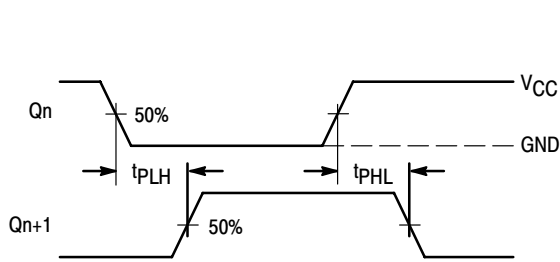
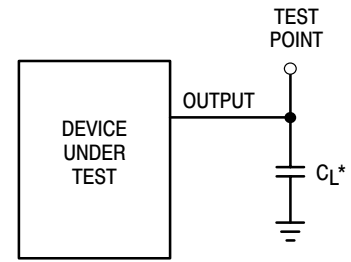


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

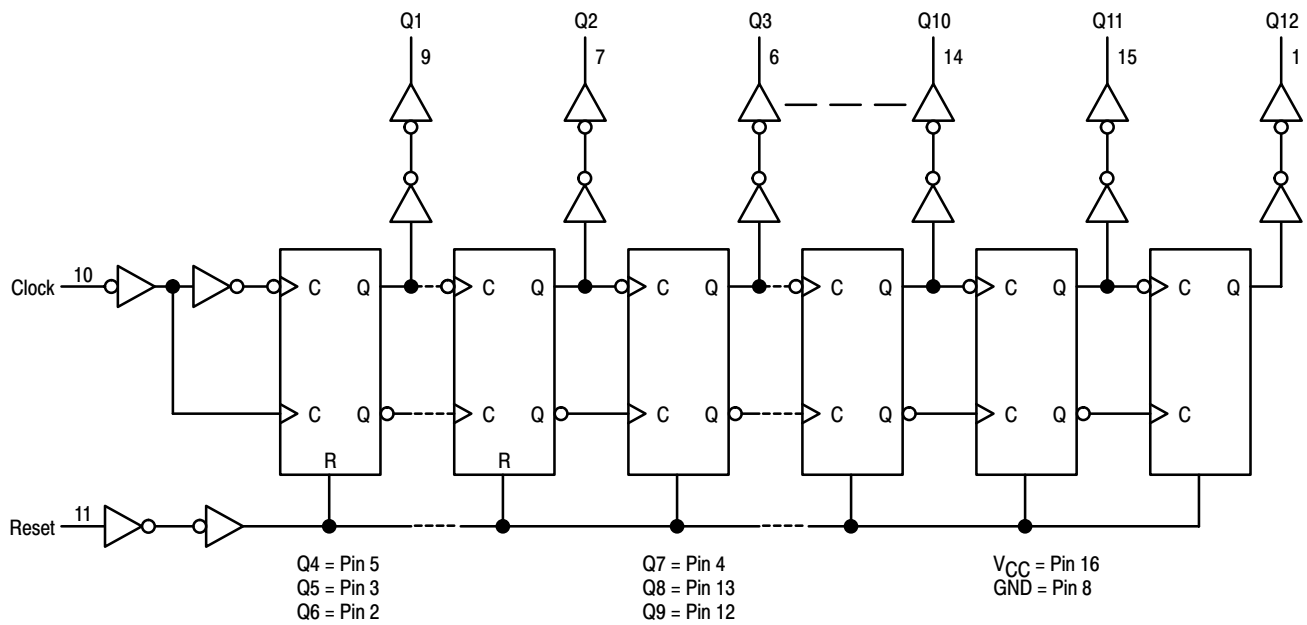


Figure 5. Expanded Logic Diagram

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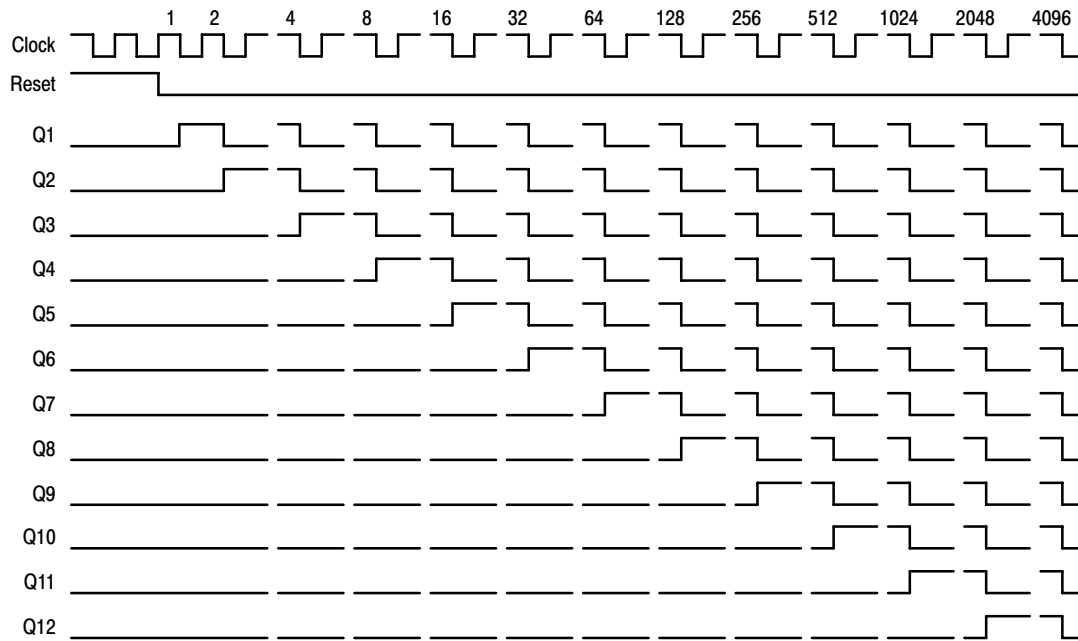


Figure 6. Timing Diagram

APPLICATIONS INFORMATION

Time-Base Generator

A 60Hz sinewave obtained through a 100 K resistor connected to a 120 Vac power line through a step down transformer is applied to the input of the MC54/74HC14A, Schmitt-trigger inverter. The HC14A squares-up the input

waveform and feeds the HC4040A. Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.

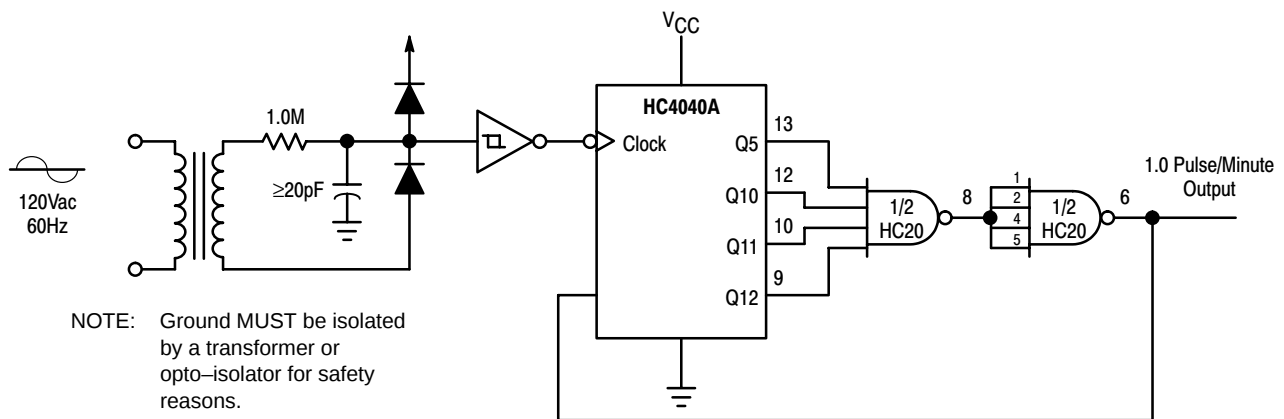
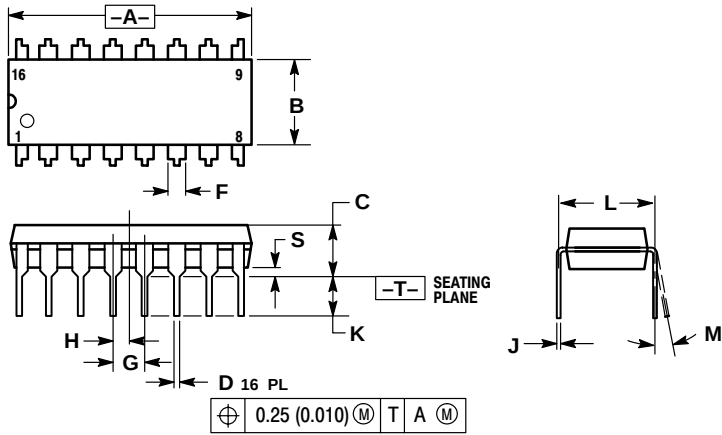


Figure 7. Time-Base Generator

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PACKAGE DIMENSIONS

PDIP-16
N SUFFIX
CASE 648-08
ISSUE R

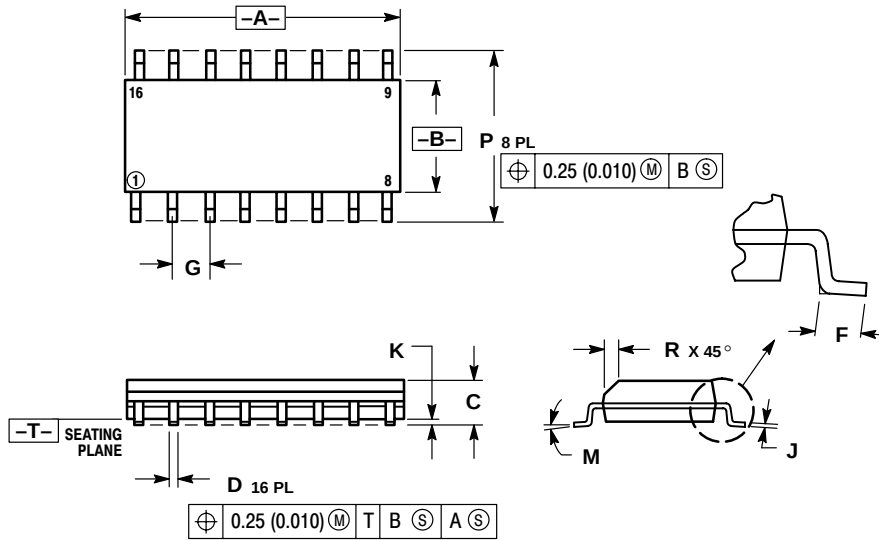


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC-16
D SUFFIX
CASE 751B-05
ISSUE J



NOTES:

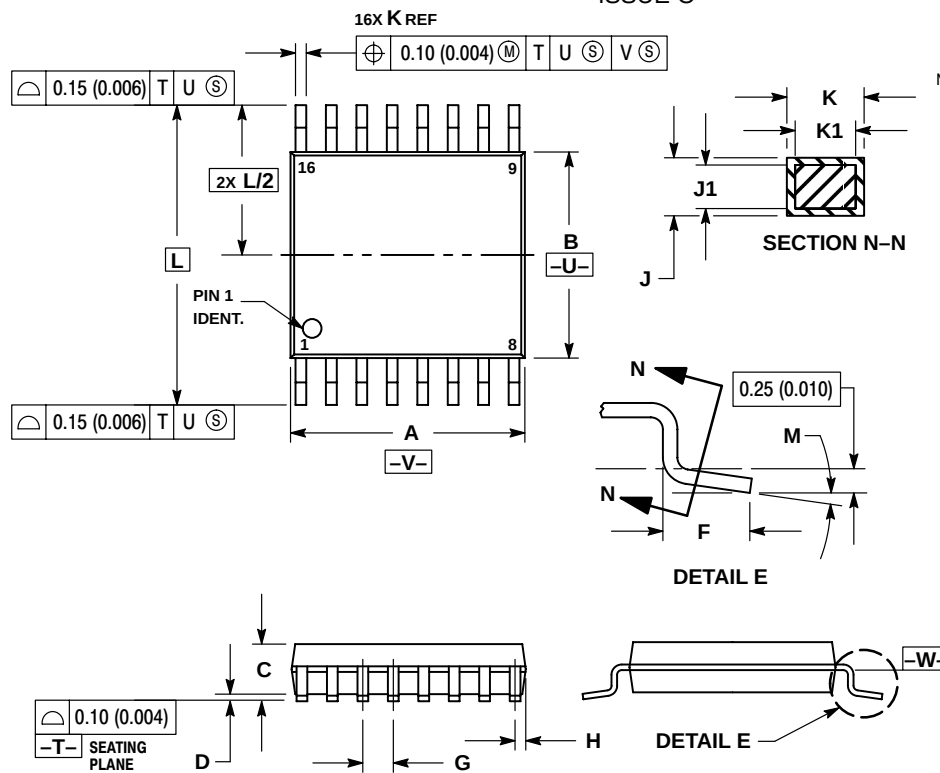
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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PACKAGE DIMENSIONS

TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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