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Jameco Part Number 872255



September 1983 Revised February 1999

MM74HC138 3-to-8 Line Decoder

General Description

The MM74HC138 decoder utilizes advanced silicon-gate CMOS technology and is well suited to memory address decoding or data routing applications. The circuit features high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

The MM74HC138 has 3 binary select inputs (A, B, and C). If the device is enabled, these inputs determine which one of the eight normally HIGH outputs will go LOW. Two active LOW and one active HIGH enables (G1, $\overline{\text{G2A}}$ and $\overline{\text{G2B}}$) are provided to ease the cascading of decoders.

The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally and pin equivalent to the 74LS138. All inputs are protected from damage due to static discharge by diodes to $\rm V_{CC}$ and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2V-6V
- Low quiescent current: 80 µA maximum (74HC Series)
- Low input current: 1 µA maximum
- Fanout of 10 LS-TTL loads

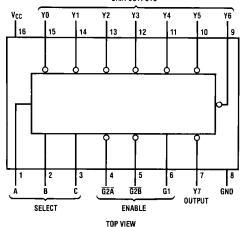
Ordering Code:

Order Number	Package Number	Package Description
MM74HC138M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC138MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC138N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignment for DIP, SOIC, SOP and TSSOP



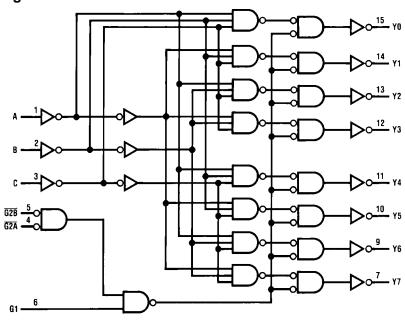
Truth Table

Inputs						Out	puts					
Enable			Select	t								
G1	G2 (Note 1)	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Х	Н	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
L	Χ	Х	Χ	Х	Н	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
Н	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
Н	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
Н	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
Н	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

H = HIGH Level, L = LOW Level, X = don't care

Note 1: $\overline{G2}$ = G2A+G2B

Logic Diagram



Absolute Maximum Ratings(Note 2)

(Note 3)

Supply Voltage (V _{CC})	-0.5 to + 7.0 V
DC Input Voltage (V _{IN})	$-$ 1.5 to V_{CC} + 1.5 V
DC Output Voltage (V _{OUT})	-0.5 to $V_{CC} + 0.5 V$
Clamp Diode Current (I _{IK} , I _{OK})	\pm 20 mA
DC Output Current, per pin (I _{OUT})	\pm 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	\pm 50 mA
Storage Temperature Range (T _{STG})	$-$ 65 $^{\circ}$ C to + 150 $^{\circ}$ C
Power Dissipation (P _D)	
(Note 4)	600 mW
S.O. Package only	500 mW
Lead Temperature (T ₁)	

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	2	6	V
DC Input or Output Voltage	0	V_{CC}	V
(V_{IN}, V_{OUT})			
Operating Temperature Range (T_A)	-40	+85	°C
Input Rise or Fall Times			
$(t_r, t_f) V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns
Note 2: Absolute Maximum Ratings are those	e values	beyond wh	ich dam-

Note 2: Absolute Maximum Ratings are those values beyond which dam age to the device may occur.

Note 3: Unless otherwise specified all voltages are referenced to ground.

Note 4: Power Dissipation temperature derating — plastic "N" package: – 12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 5)

(Soldering 10 seconds)

Symbol	Parameter	Conditions	v _{cc}	T _A = 25°C		T _A = -40 to 85°C	Units
Cymbol	i arameter	Conditions	• 66	Тур	Guai	T _A = -40 to 85°C anteed Limits 1.5 3.15 4.2 0.5 1.35 1.8 1.9 4.4 5.9 3.84 5.34 0.1 0.1 0.1 0.1 0.33 0.33 ±1.0	Oilita
V _{IH}	Minimum HIGH Level		2.0V		1.5	1.5	V
	Input Voltage		4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V _{IL}	Maximum LOW Level		2.0V		0.5	0.5	V
	Input Voltage		4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V _{OH}	Minimum HIGH Level	$V_{IN} = V_{IH}$ or V_{IL}					
	Output Voltage	I _{OUT} ≤ 20 μA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL}					
		I _{OUT} ≤ 4.0 mA	4.5V	4.2	3.98	3.84	V
		I _{OUT} ≤ 5.2 mA	6.0V	5.7	5.48	5.34	V
V _{OL}	Maximum LOW Level	$V_{IN} = V_{IH}$ or V_{IL}					
	Output Voltage	I _{OUT} ≤ 20 μA	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}					
		I _{OUT} ≤ 4.0 mA	4.5V	0.2	0.26	0.33	V
		I _{OUT} ≤ 5.2 mA	6.0V	0.2	0.26	0.33	V
I _{IN}	Maximum Input	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	μΑ
	Current						
I _{CC}	Maximum Quiescent	$V_{IN} = V_{CC}$ or GND	6.0V		8.0	80	μΑ
	Supply Current	$I_{OUT} = 0 \mu A$					

Note 5: For a power supply of 5V \pm 10% the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25$ °C, $C_L = 15$ pF, $t_r = t_f = 6$ ns

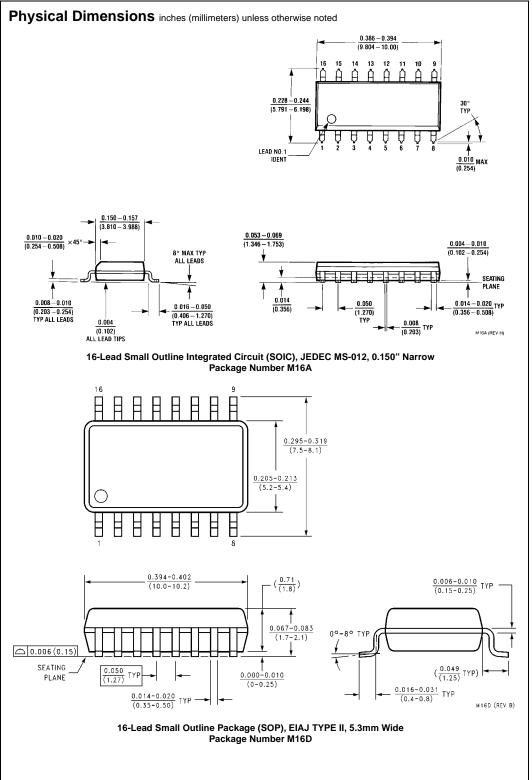
Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
t _{PLH}	Maximum Propagation		18	25	ns
	Delay, Binary Select to any Output				
t _{PHL}	Maximum Propagation		28	35	ns
	Delay, Binary Select to any Output				
t _{PHL} , t _{PLH}	Maximum Propagation		18	25	ns
	Delay, G1 to any Output				
t _{PHL}	Maximum Propagation		23	30	ns
	Delay G2A or G2B to				
	Output				
t _{PLH}	Maximum Propagation		18	25	ns
	Delay G2A or G2B to Output				

AC Electrical Characteristics

 $C_L = 50 \ \text{pF}, \ t_f = t_f = 6 \ \text{ns}$ (unless otherwise specified)

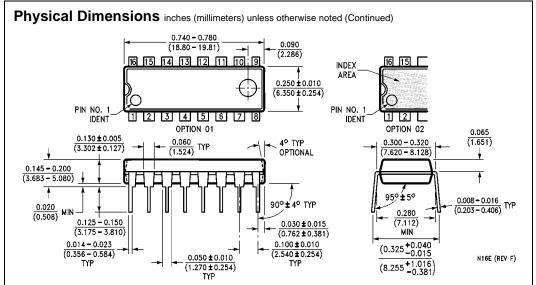
Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	Units
Symbol	Farameter	Conditions	VCC	Тур	Gua	T _A = -40 to 85°C aranteed Limits 189 38 32 252 50 43 189 38 32 221 44 37 189 38 32 95 19 16 10	Ullits
t _{PLH}	Maximum Propagation		2.0V	75	150	189	ns
	Delay Binary Select to		4.5V	15	30	38	ns
	any Output LOW-to-HIGH		6.0V	13	26	32	ns
t _{PHL}	Maximum Propagation		2.0V	100	200	252	ns
	Delay Binary Select to any		4.5V	20	40	50	ns
	Output HIGH-to-LOW		6.0V	17	34	43	ns
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	75	150	189	ns
	Delay G1 to any		4.5V	15	30	38	ns
	Output		6.0V	13	26	32	ns
t _{PHL}	Maximum Propagation		2.0V	82	175	221	ns
	Delay G2A or G2B to		4.5V	28	35	44	ns
	Output		6.0V	22	30	37	ns
t _{PLH}	Maximum Propagation		2.0V	75	150	189	ns
	Delay G2A or G2B to		4.5V	15	30	38	ns
	Output		6.0V	13	26	32	ns
t _{TLH} , t _{THL}	Output Rise and		2.0V	30	75	95	ns
	Fall Time		4.5V	8	15	19	ns
			6.0V	7	13	16	ns
C _{IN}	Maximum Input			3	10	10	pF
	Capacitance						
C _{PD}	Power Dissipation	(Note 6)		75			pF
	Capacitance						

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \ V_{CC}^2 f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} f + I_{CC}$.



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 7.72 TYP. DIMENSIONS METRIC ONLY (1.78 TYP) 0.42 TYP LAND PATTERN RECOMMENDATION GAGE PLANE 6.4 0.25 4.4 ± 0.1 -B-3.2 SEATING PLANE 0.6 ± 0.1 DETAIL A △ 0.2 C B A ALL LEAD TIPS TYPICAL, SCALE: 40X SEE DETAIL A PIN #1 IDENT. (0.90) O.1 C--c-0.10 ± 0.05 TYP 0.09-0.20 TYP 0.65 TYP - 0.30 TYP $\overline{\Phi}$ 0.13 M B (S) Α MTC16 (REV C)

16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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