

# NC7SZ38

## TinyLogic® UHS 2-Input NAND Gate, Open Drain Output


### Features

- Ultra-High Speed:  $t_{PD}$  2.4ns (Typical) into 50pF at 5V  $V_{CC}$
- Open Drain Output Stage for OR Tied Applications
- High Output Sink Drive: 24mA at 3V  $V_{CC}$
- Broad  $V_{CC}$  Operating Range: 1.65V to 5.5V
- Matches Performance of LCX Operated at 3.3V  $V_{CC}$
- Power Down High-Impedance Inputs/Outputs
- Over-Voltage Tolerance Inputs Facilitate 5V to 3V Translation
- Proprietary Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- Space-Saving SOT23 and SC70 Packages

### Description

The NC7SZ38 is a single 2-Input NAND gate with open drain output stage from Fairchild's Ultra-High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive while maintaining low static power dissipation over a very broad  $V_{CC}$  operating range. The device is specified to operate over the 1.65V to 5.5V  $V_{CC}$  range. The inputs and output are high impedance when  $V_{CC}$  is 0V. Inputs tolerate voltages up to 6V independent of  $V_{CC}$  operating voltage. The open drain output stage will tolerate voltages up to 6V independent of  $V_{CC}$  when in the high impedance state.

### Ordering Information

Part Number	Top Mark	 Eco Status	Package	Packing Method
NC7SZ38M5X	7Z38	RoHS	5-Lead SOT23, JEDEC MO-178 1.6mm	3000 Units on Tape & Reel
NC7SZ38P5X	Z38	RoHS	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
NC7SZ38L6X	A6	RoHS	6-Lead MicroPak™, 1.00mm Wide	5000 Units on Tape & Reel
NC7SZ38FHX	A6	Green	6-Lead, MicroPak2, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel

 For Fairchild's definition of Eco Status, please visit: [http://www.fairchildsemi.com/company/green/rohs\\_green.html](http://www.fairchildsemi.com/company/green/rohs_green.html).

## Connection Diagrams



Figure 1. Logic Symbol

## Pin Configurations

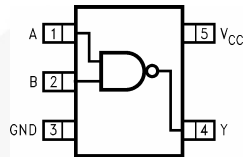


Figure 2. SC70 and SOT23 (Top View)

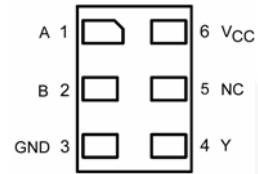


Figure 3. MicroPak™ (Top Through View)

## Pin Definitions

Pin # SC70 / SOT23	Pin # MicroPak	Name	Description
1	1	A	Input
2	2	B	Input
3	3	GND	Ground
4	4	Y	Output
5	6	V <sub>CC</sub>	Supply Voltage
	5	NC	No Connect

## Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	*H
L	H	*H
H	L	*H
H	H	L

H = HIGH Logic Level

L = LOW Logic Level

\*H = High Impedance Output State, Open Drain

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit	
$V_{CC}$	Supply Voltage	-0.5	6.0	V	
$V_{IN}$	DC Input Voltage	-0.5	6.0	V	
$V_{OUT}$	DC Output Voltage	-0.5	6.0	V	
$I_{IK}$	DC Input Diode Current	$V_{IN} < -0.5V$		-50	mA
		$V_{IN} > 6.0V$		+20	
$I_{OK}$	DC Output Diode Current	$V_{OUT} < -0.5V$		-50	mA
		$V_{OUT} > 6V, V_{CC}=GND$		+20	
$I_{OUT}$	DC Output Current		+50	mA	
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current		$\pm 50$	mA	
$T_{STG}$	Storage Temperature Range	-65	+150	$^{\circ}C$	
$T_J$	Junction Temperature Under Bias		+150	$^{\circ}C$	
$T_L$	Junction Lead Temperature (Soldering, 10 Seconds)		+260	$^{\circ}C$	
$P_D$	Power Dissipation at +85 $^{\circ}C$	SOT-23		200	mW
		SC70-5		150	
		MicroPak-6		130	
		MicroPak2-6		120	
ESD	Human Body Model, JEDEC:JESD22-A114		4000	V	
	Charge Device Model, JEDEC:JESD22-C101		2000		

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
$V_{CC}$	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.50	5.50	
$V_{IN}$	Input Voltage		0	5.5	V
$V_{OUT}$	Output Voltage		0	5.5	V
$T_A$	Operating Temperature		-40	+85	$^{\circ}C$
$t_r, t_f$	Input Rise and Fall Times	$V_{CC}=1.8V, 2.5V \pm 0.2V$	0	20	ns/V
		$V_{CC}=3.3V \pm 0.3V$	0	10	
		$V_{CC}=5.0V \pm 0.5V$	0	5	
$\theta_{JA}$	Thermal Resistance	SOT-23		300	$^{\circ}C/W$
		SC70-5		425	
		MicroPak-6		500	
		MicroPak2-6		560	

**Note:**

- Unused inputs must be held HIGH or LOW. They may not float.

### DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Conditions	T <sub>A</sub> =+25°C			T <sub>A</sub> =-40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V <sub>IH</sub>	HIGH Level Input Voltage	1.65 to 1.95		0.75V <sub>CC</sub>			0.75V <sub>CC</sub>		V
		2.30 to 5.50		0.70V <sub>CC</sub>			0.70V <sub>CC</sub>		
V <sub>IL</sub>	LOW Level Input Voltage	1.65 to 1.95				0.25V <sub>CC</sub>		0.25V <sub>CC</sub>	V
		2.30 to 5.50				0.30V <sub>CC</sub>		0.30V <sub>CC</sub>	
I <sub>LKG</sub>	HIGH Level Output Leakage	5.50	V <sub>IN</sub> =V <sub>IL</sub> , V <sub>OUT</sub> =V <sub>CC</sub> or GND			±5		±10	µA
V <sub>OL</sub>	LOW Level Output Voltage	1.65	V <sub>IN</sub> =V <sub>IH</sub> , I <sub>OL</sub> =100		0.00	0.10		0.10	V
		1.80			0.00	0.10		0.10	
		2.30			0.00	0.10		0.10	
		3.00			0.00	0.10		0.10	
		4.50			0.00	0.10		0.10	
		1.65		0.80	0.24		0.24		
		2.30	I <sub>OL</sub> =8mA		0.10	0.30		0.30	
		3.00	I <sub>OL</sub> =16mA		0.15	0.40		0.40	
		3.00	I <sub>OL</sub> =24mA		0.22	0.55		0.55	
		4.50	I <sub>OL</sub> =32mA		0.22	0.55		0.55	
I <sub>IN</sub>	Input Leakage Current	5.50	V <sub>IN</sub> =5.5V, GND			±1		±10	µA
I <sub>OFF</sub>	Power Off Leakage Current	0	V <sub>IN</sub> or V <sub>OUT</sub> =5.5V			1		10	µA
I <sub>CC</sub>	Quiescent Supply Current	5.50	V <sub>IN</sub> =5.5V, GND			2		20	µA

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Conditions	T <sub>A</sub> =+25°C			T <sub>A</sub> =-40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t <sub>PZL</sub>	Propagation Delay	1.65	C <sub>L</sub> =50pF, R <sub>U</sub> =500Ω, R <sub>D</sub> =500Ω, V <sub>IN</sub> =2•V <sub>CC</sub>	1.5	6.5	12.7	1.5	13.2	ns	Figure 4 Figure 5
		1.80		1.5	5.4	10.5	1.5	11.0		
		2.50 ± 0.20		0.8	3.5	7.0	0.8	7.5		
		3.30 ± 0.30		0.8	2.8	5.0	0.8	5.2		
		5.00 ± 0.50		0.5	2.2	4.3	0.5	4.5		
t <sub>PLZ</sub>		1.65	C <sub>L</sub> =50pF, R <sub>U</sub> =500Ω, R <sub>D</sub> =500Ω, V <sub>IN</sub> =2•V <sub>CC</sub>	1.5	5.5	12.7	1.5	13.2	ns	Figure 4 Figure 5
		1.80		1.5	4.6	10.5	1.5	11.0		
		2.50 ± 0.20		0.8	3.0	7.0	0.8	7.5		
		3.30 ± 0.30		0.8	2.1	6.0	0.8	5.2		
		5.00 ± 0.50		0.5	1.3	4.3	0.5	4.5		
C <sub>IN</sub>	Input Capacitance	0.00			4.0				pF	
C <sub>OUT</sub>	Output Capacitance	0.00			5.0				pF	
C <sub>PD</sub>	Power Dissipation Capacitance <sup>(2)</sup>	3.30			5.1				pF	Figure 6
		5.00			7.3					

**Note:**

2. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression: I<sub>CCD</sub>=(C<sub>PD</sub>)(V<sub>CC</sub>)(f<sub>IN</sub>)+(I<sub>CC</sub>Static).

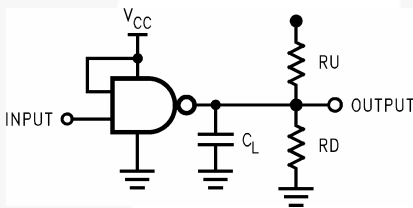


Figure 4. AC Test Circuit

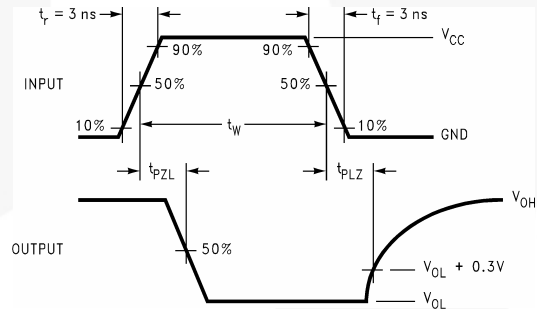


Figure 5. AC Waveforms

**Note:**

3. C<sub>L</sub> includes load and stray capacitance. Input PRR=10MHz t<sub>w</sub>=500ns.

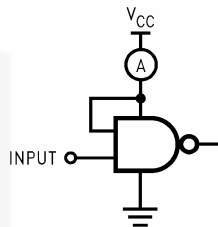
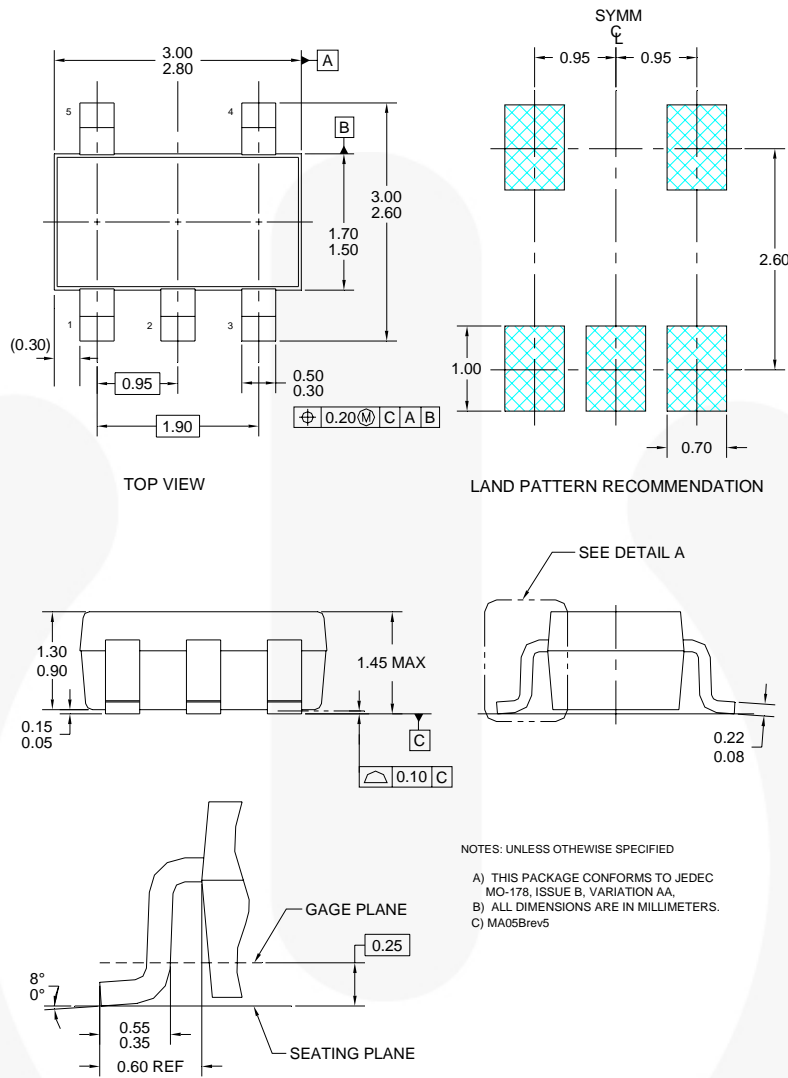


Figure 6. Test Circuit

**Note:**

4. Input=AC Waveform; t<sub>r</sub>=t<sub>f</sub>=1.8ns; PRR=10MHz; Duty Cycle=50%.

## Physical Dimensions



**Figure 7. 5-Lead SOT23, JEDEC MO-178 1.6mm**

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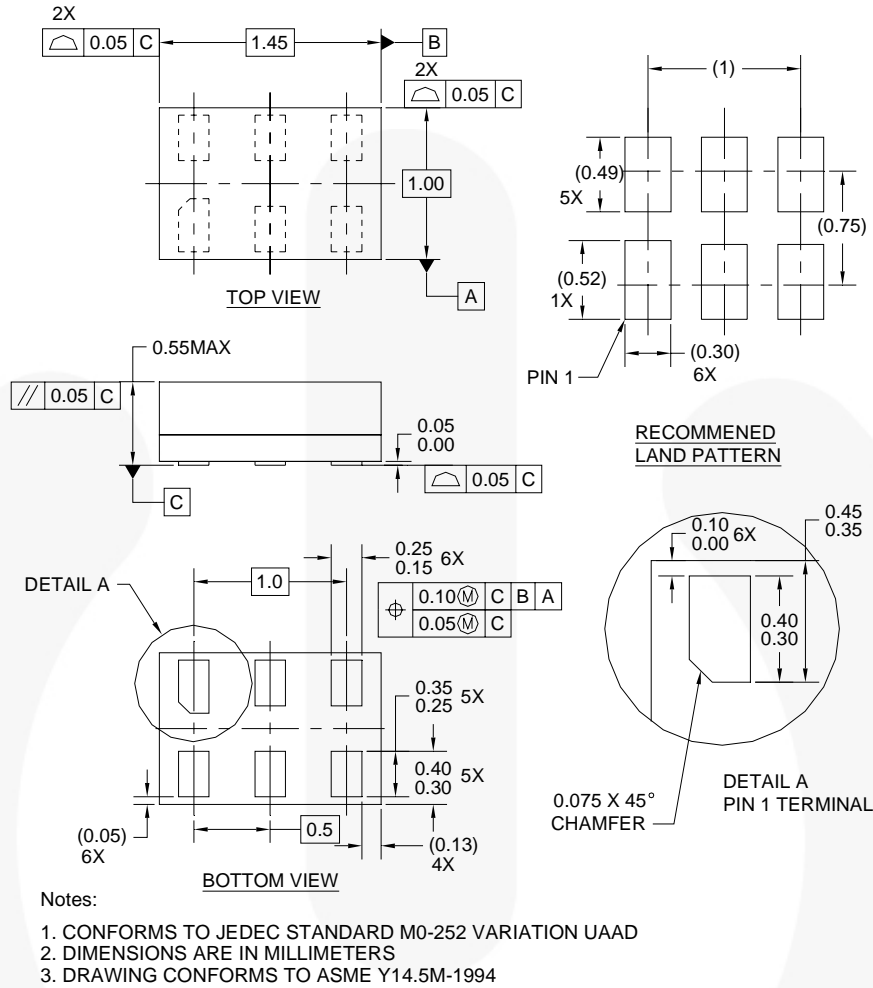
## Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:  
[http://www.fairchildsemi.com/packaging/SOT23-5L\\_tr.pdf](http://www.fairchildsemi.com/packaging/SOT23-5L_tr.pdf).

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
M5X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



## Physical Dimensions



MAC06AREVC

**Figure 9. 6-Lead, MicroPak™, 1.0mm Wide**

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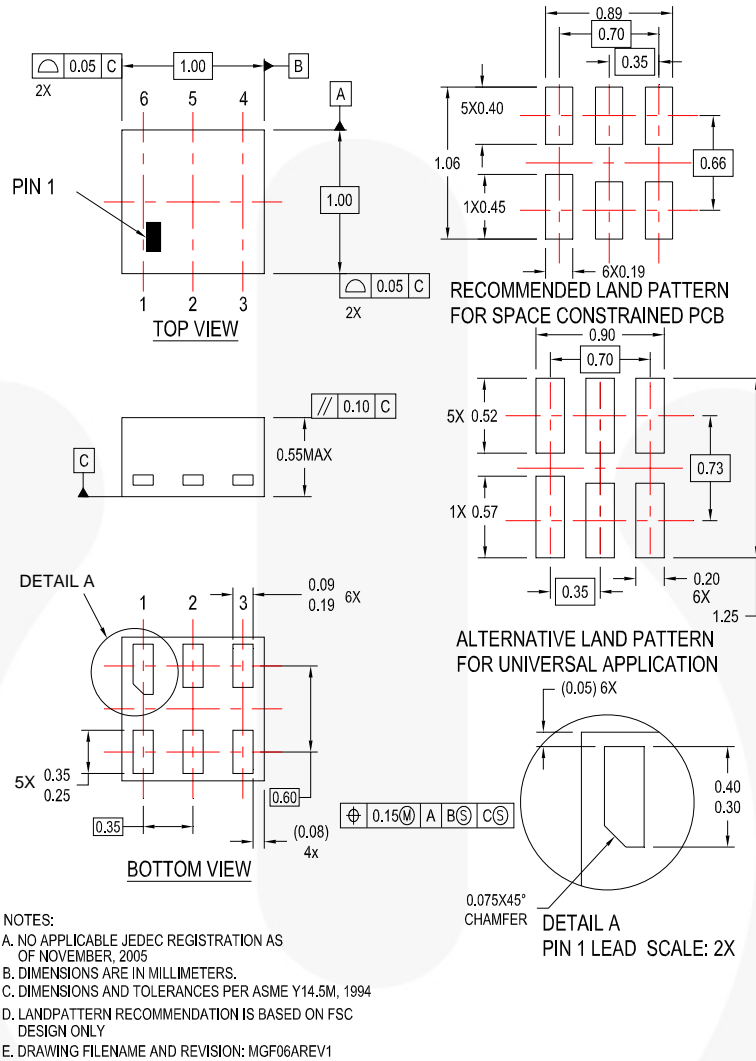
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
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## Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:  
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Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

## Physical Dimensions



**Figure 10.6-Lead, MicroPak2, 1x1mm Body, .35mm Pitch**

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## Tape and Reel Specifications





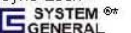
Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:  
[http://www.fairchildsemi.com/packaging/MicroPAK2\\_6L\\_tr.pdf](http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf).

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



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