NCN6001

Compact Smart Card Interface IC

The NCN6001 is an integrated circuit dedicated to the smart card interface applications. The device handles any type of smart card through a simple and flexible microcontroller interface. On top of that, thanks to the built−in chip select pin, several couplers can be connected in parallel.

The device is particularly suited for low cost, low power applications, with high extended battery life coming from extremely low quiescent current.

Features

- 100% Compatible with ISO 7816−3, EMV and GIE−CB Standards
- Fully GSM Compliant
- Wide Battery Supply Voltage Range: 2.7 < V_{CC} < 5.5 V
- Programmable CRD_VCC Supply Handles 1.8 V, 3.0 V or 5.0 V Card Operation
- Programmable Rise and Fall Card Clock Slopes
- Programmable Card Clock Divider
- Built−in Chip Select Logic Allows Parallel Coupling Operation
- ESD Protection on Card Pins (8.0 kV, Human Body Model)
- Supports up to 40 MHz Input Clock
- Built−in Programmable CRD_CLK Stop Function Handles Run or Low State
- Programmable CRD_CLK Slopes to Cope with Wide Operating Frequency Range
- Fast CRD_VCC Turn−on and Turn−off Sequence
- These are Pb−Free Devices

Typical Applications

- E−Commerce Interface
- Automatic Teller Machine (ATM) Smart Card
- Point of Sales (POS) System
- Pay TV System

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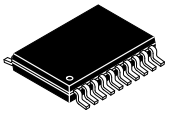
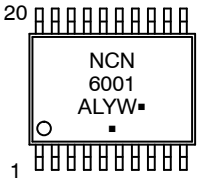
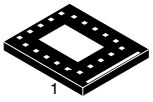
MARKING DIAGRAMS

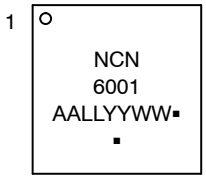


TSSOP−20
DTB SUFFIX
CASE 948E





LLGA 20
CASE 513AC



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 34 of this data sheet.

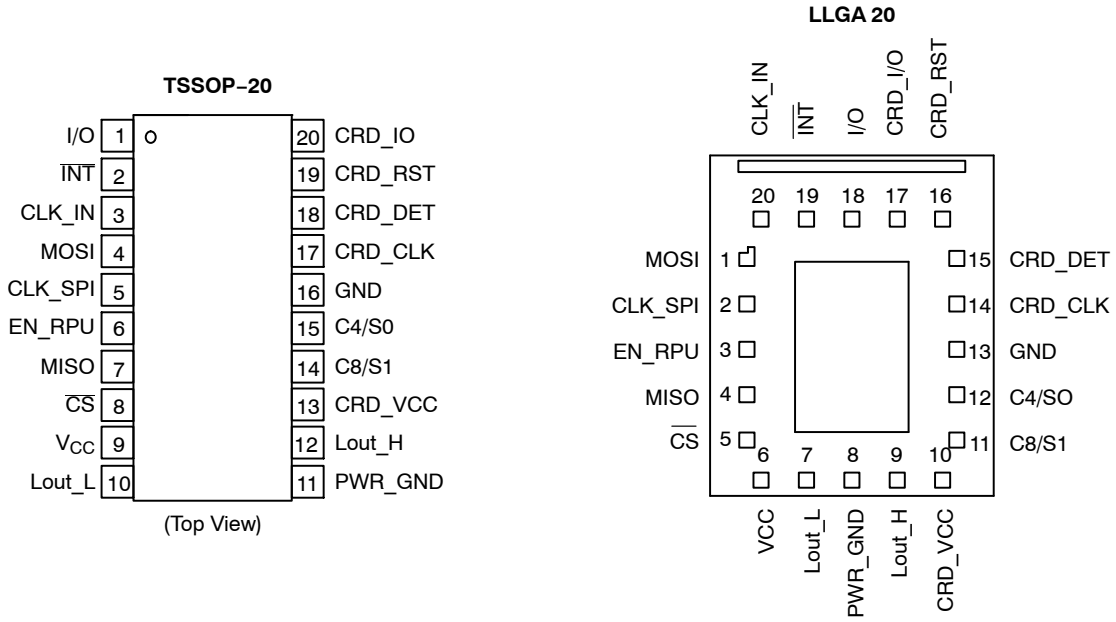


Figure 1. Pin Connections*

*All the pin numbers used in the document refer to the TSSOP package

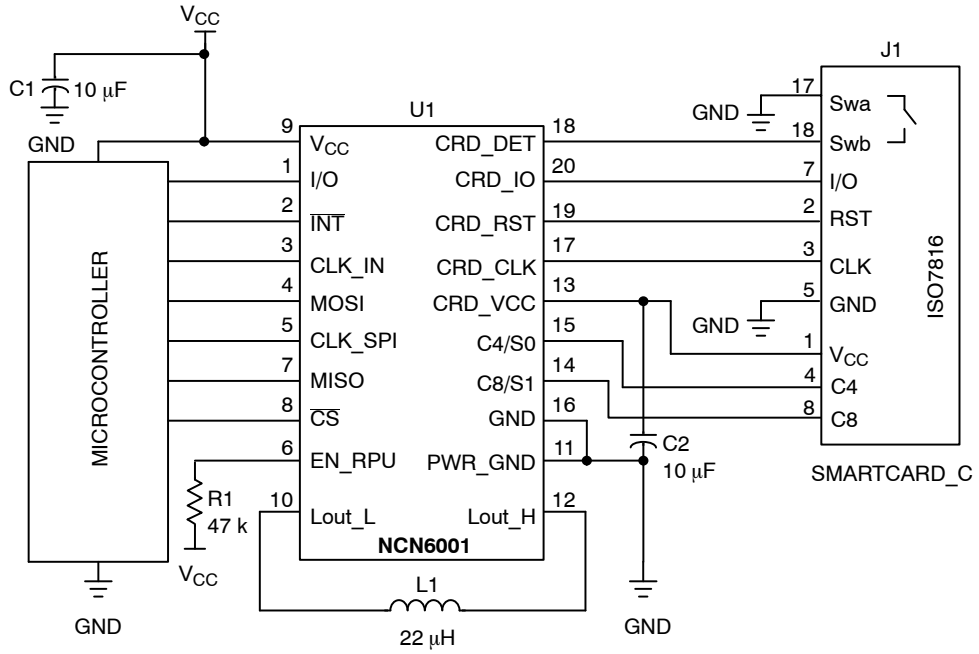


Figure 2. Typical Application

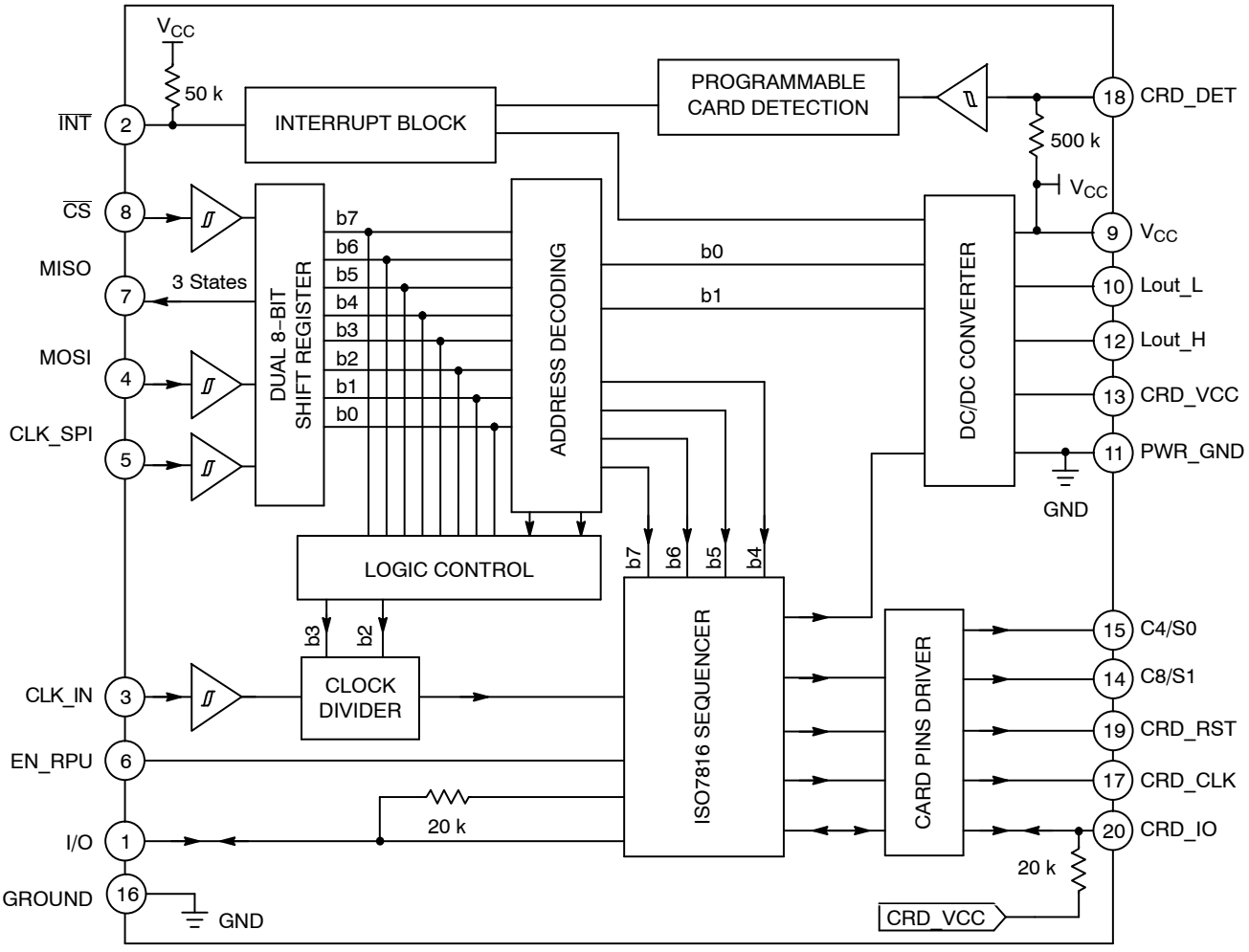


Figure 3. Block Diagram

PIN FUNCTIONS AND DESCRIPTION

TSSOP	LLGA	Name	Type	Description
1	18	I/O	Input/Output Pullup	This pin is connected to an external microcontroller interface. A bidirectional level translator adapts the serial I/O signal between the smart card and the microcontroller. The level translator is enabled when $\overline{CS}$ = L, the sub address has been selected and the system operates in the Asynchronous mode. When a Synchronous card is in use, this pin is disconnected and the data and the transaction take place with the MISO b3 register. The internal pullup resistor connected on the μC side is activated and visible by the selected chip only.
2	19	$\overline{INT}$	OUTPUT Pullup	This pin is activated LOW when a card has been inserted and detected by CRD_DET pin. Similarly, an interrupt is generated when the CRD_VCC output is overloaded, or when the card has been extracted whatever be the transaction status (running or standby). The $\overline{INT}$ signal is reset to High according to Table 7 and Figure 11. On the other hand, the pin is forced to a logic High when the input voltage V_{CC} drops below 2.0 V.
3	20	CLK_IN	CLOCK INPUT High impedance	The built−in Schmitt trigger receiver makes this pin suitable for a large type of clock signal (Figure 30). This pin can be connected to either the microcontroller master clock, or to a crystal signal, to drive the external smart cards. The signal is fed to the internal clock selector circuit and translated to the CRD_CLK pin at either the same frequency, or divided by 2 or 4, depending upon the programming mode. Note: The chip guarantees the EMV 50% Duty Cycle when the clock divider ratio is 1/2 or 1/4, even when the CLK_IN signal is out of the 45% to 55% range specified by ISO and EMV specifications. Care must be observed, at PCB level, to minimize the pick−up noise coming from the CLK_IN line.
4	1	MOSI	INPUT	Master Out Slave In: SPI Data Input from the external microcontroller. This byte contents the address of the selected chip among the four possible, together with the programming code for a given interface.
5	2	CLK_SPI	INPUT	Clock Signal to synchronize the SPI data transfer. The built−in Schmitt trigger receiver makes this pin compatible with a wide range of input clock signal (Figure 30). This clock is fully independent from the CLK_IN signal and does not play any role with the data transaction.
6	3	EN_RPU	INPUT, Logic	This pin is used to activate the I/O internal pullup resistor according to the here below true table: EN_RPU = Low → I/O Pullup resistor disconnected EN_RPU = High → I/O Pullup resistor connected When two or more NCN6001 chips shares the same I/O bus, one chip only shall have the internal pullup resistor enabled to avoid any overload of the I/O line. Moreover, when Asynchronous and Synchronous cards are handled by the interfaces, the activated I/O pullup resistor must preferably be the one associated with the Asynchronous circuit. On the other hand, since no internal pullup bias resistor is built in the chip, pin 6 must be connected to the right voltage level to make sure the logic function is satisfied.
7	4	MISO	OUTPUT	Master In Slave Out: SPI Data Output from the NCN6001. This byte carries the state of the interface, the serial transfer being achieved according to the programmed mode (Table 2), using the same CLK_SPI signal and during the same MOSI time frame. The three high bits [b7:b5] have no meaning and shall be discarded by the microcontroller. An external 4.7 kΩ Pull down resistor might be necessary to avoid misunderstanding of the pin 7 voltage during the High Z state.
8	5	$\overline{CS}$	INPUT	This pin synchronizes the SPI communication and provides the chip address and selected functions. All the NCN6001 functions, both programming and card transaction, are disabled when $\overline{CS}$ = H.
9	6	V_{CC}	POWER	This pin is connected to the NCN6001 supply voltage and must be bypassed to ground by a 10 μF/6.0 V capacitor. Since tantalum capacitors have relative high ESR, using low ESR ceramic type (MURATA X5R, Resr < 100 mΩ) is highly recommended.

PIN FUNCTIONS AND DESCRIPTION

TSSOP	LLGA	Name	Type	Description
10	7	Lout_L	POWER	The Low Side of the external inductor is connected between this pin and pin 12 to provide the DC/DC function. The current flowing into this inductor is internally sensed and no external shunt resistor is used. Typically, Lout = 22 μH, with DSR < 2.0 Ω, yields a good efficiency performance for a maximum 65 mA DC output load. Note: The inductor shall be sized to handle the 450 mA peak current flowing during the DC/DC operation (see CoilCraft manufacturer data sheet).
11	8	PWR_GND	POWER	This pin is the Power Ground associated with the built−in DC/DC converter and must be connected to the system ground together with GROUND pin 16. Using good quality ground plane is recommended to avoid spikes on the logic signal lines.
12	9	Lout_H	POWER	The High Side of the external inductor is connected between this pin and pin 10 to activate the DC/DC function. The built−in NMOS and PMOS devices provide the switching function together with the CRD_VCC voltage rectification (Figure 17).
13	10	CRD_VCC	POWER	This pin provides the power to the external card. It is the logic level “1” for CRD_IO, CRD_RST, CRD_C4, CRD_C8 and CRD_CLK signals. The energy stored by the DC/DC external inductor Lout must be smoothed by a 10 μF/Low ESR capacitor, connected across CRD_VCC and GND. Using ceramic type of capacitor (MURATA X5R, ESR < 50 mΩ) is strongly recommended. In the event of a CRD_VCC U_{VLOW} voltage, the NCN6001 detects the situation and feedback the information in the STATUS bit. The device does not take any further action, particularly the DC/DC converter is neither stopped nor re programmed by the NCN6001. It is up to the external MPU to handle the situation. However, when the CRD_VCC is overloaded, the NCN6001 shuts off the DC/DC converter, runs a Power Down ISO sequence and reports the fault in the STATUS register. Since high transient current flows from this pin to the load, care must be observed, at PCB level, to minimize the series ESR and ESL parasitic values. The NCN6001 demo board provides an example of a preferred PCB layout.
14	11	C8/S1	I/O	Auxiliary mixed analog/digital line to handle either a synchronous card, or as Chip Select Identification (MISO, Bit 0): see Figure 9. The pin is driven by an open drain stage, the pullup resistor being connected to the CRD_VCC supply. When the pin is used as a logic input (asynchronous cards), the positive logic condition applies: Connected to GND → Logic = Zero Connected to V_{CC} or left Open → Logic = One A built−in accelerator circuit makes sure the output positive going rise time is fully within the ISO/EMV specifications. NOTE: The pin is capable of reading the logic level when the chip operates an asynchronous interface, but is not intended to read the data from the external card when operated in the synchronous mode. It merely returns the logic state forced during a write instruction to the card.
15	12	C4/S0	I/O	Auxiliary mixed analog/digital line to handle either a synchronous card, or as Chip Select Identification (MISO, Bit 1): see Figure 9. The pin is driven by an open drain stage, the pullup resistor being connected to the CRD_VCC supply. When the pin is used as a logic input (asynchronous cards), the positive logic condition applies: Connected to GND → Logic = Zero Connected to V_{CC} or left Open → Logic = One A built−in accelerator circuit makes sure the output positive going rise time is fully within the ISO/EMV specifications. NOTE: The pin is capable of reading the logic level when the chip operates an asynchronous interface, but is not intended to read the data from the external card when operated in the synchronous mode. It merely returns the logic state forced during a write instruction to the card.
16	13	GND	SIGNAL	The logic and low level analog signals shall be connected to this ground pin. This pin must be externally connected to the PWR_GND pin 12. The designer must make sure no high current transients are shared with the low signal currents flowing into this pin.
17	14	CRD_CLK	OUTPUT	This pin is connected to the CLK pin of the card connector. The CRD_CLK signal comes from the clock selector circuit output. An internal active pull down NMOS device forces this pin to Ground during either the CRD_VCC startup sequence, or when CRD_VCC = 0 V. The rise and fall slopes, either FAST or SLOW, of this signal can be programmed by the MOSI message (Table 2). Care must be observed, at PCB level, to minimize the pick−up noise coming from the CRD_CLK line.

PIN FUNCTIONS AND DESCRIPTION

TSSOP	LLGA	Name	Type	Description
18	15	CRD_DET	INPUT	The signal coming from the external card connector is used to detect the presence of the card. A built−in pullup low current source biases this pin High, making it active LOW, assuming one side of the external switch is connected to ground. A built−in digital filter protect the system against voltage spikes present on this pin. The polarity of the signal is programmable by the MOSI message, according to the logic state depicted Table 2. On the other hand, the meaning of the feedback message contained in the MISO register bit b4, depends upon the SPI mode of operation as defined here below: SPI Normal Mode: The MISO bit b4 is High when a card is inserted, whatever be the polarity of the card detect switch. SPI Special Mode: The MISO bit b4 copies the logic state of the Card detect switch as depicted here below, whatever be the polarity of the switch used to handle the detection: CRD_DET = Low → MISO/b4 = Low CRD_DET = High → MISO/b4 = High In both cases, the chip must be programmed to control the right logic state (Table 2). Since the bias current supplied by the chip is very low, typically 5.0 μA, care must be observed to avoid low impedance or cross coupling when this pin is in the Open state.
19	16	CRD_RST	OUTPUT	This pin is connected to the RESET pin of the card connector. A level translator adapts the RESET signal from the microcontroller to the external card. The output current is internally limited to 15 mA. The CRD_RST is validated when $\overline{CS}$ = Low and hard wired to Ground when the card is deactivated, by and internal active pull down circuit. Care must be observed, at PCB design level, to avoid cross coupling between this signal and the CRD_CLK clock.
20	17	CRD_IO	I/O Pullup	This pin handles the connection to the serial I/O pin of the card connector. A bidirectional level translator adapts the serial I/O signal between the card and the microcontroller. An internal active pull down MOS device forces this pin to Ground during either the CRD_VCC startup sequence, or when CRD_VCC = 0 V. The CRD_IO pin current is internally limited to 15 mA. Care must be observed, at PCB design level, to avoid cross coupling between this signal and the CRD_CLK clock.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6.0	V
Power Supply Current Note: This current represents the maximum peak current the pin can sustain, not the NCN6001 average consumption.	I_{bat}	500	mA
Power Supply Current	I_{CC}	150 (Internally Limited)	mA
Digital Input Pins	V_{in}	−0.5 V < V_{in} < V_{CC} +0.5 V, but < 6.0 V	V
Digital Input Pins	I_{in}	±5.0	mA
Digital Output Pins	V_{out}	−0.5 V < V_{in} < V_{CC} +0.5 V, but < 6.0 V	V
Digital Output Pins	I_{out}	±10	mA
Card Interface Pins	V_{card}	−0.5 V < V_{card} < CRD_VCC +0.5 V	V
Card Interface Pins, excepted CRD_CLK	I_{card}	15 (Internally Limited)	mA
Inductor Current	I_{Lout}	500 (Internally Limited)	mA
ESD Capability (Note 1) Standard Pins Card Interface Pins CRD_DET	V_{ESD}	 2.0 8.0 4.0	 kV kV kV
Power Dissipation @ Tamb = +85°C Thermal Resistance, Junction−to−Air ($R_{\theta JA}$)	P_{DS} $R_{\theta JA}$	320 125	mW °C/W
Operating Ambient Temperature Range	T_A	−25 to +85	°C
Operating Junction Temperature Range	T_J	−25 to +125	°C
Maximum Junction Temperature (Note 2)	T_{Jmax}	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Human Body Model, R = 1500 Ω, C = 100 pF.
2. Absolute Maximum Rating beyond which damage to the device may occur.

DIGITAL PARAMETERS @ 2.7 V < V_{CC} < 5.5 V (−25°C to +85°C ambient temperature, unless otherwise noted).
Note: Digital inputs undershoot < − 0.3 V to ground, Digital inputs overshoot < 0.3 V to V_{CC}.

Rating	Pin	Symbol	Min	Typ	Max	Unit
Input Asynchronous Clock Duty Cycle = 50% @ V_{CC} = 3.0 V Over the Temperature Range @ V_{CC} = 5.0 V Over the Temperature Range	3	F_{CLKIN}	 − −	 − −	 30 40	MHz
Input Clock Rise Time Input Clock Fall Time	3	F_{tr} F_{tf}	2.5 2.5	− −	− −	ns ns
Input SPI Clock	5	F_{CLKSPI}	−	−	15	MHz
Input CLK_SPI Rise/Fall Time @ Cout = 30 pF	5	tr_{spi}, tf_{spi}	−	−	12	ns
Input MOSI Rise/Fall Time @ Cout = 30 pF	4	tr_{mosi}, tf_{mosi}	−	−	12	ns
Output MISO Rise/Fall Time @ Cout = 30 pF	7	tr_{miso}, tf_{miso}	−	−	12	ns
Input $\overline{CS}$ Rise/Fall Time	8	tr_{str}, tf_{str}	−	−	12	ns
I/O Data Transfer Switching Time, both directions (I/O and CRD_IO), @ Cout = 30 pF I/O Rise Time * (Note 4) I/O Fall Time	1, 20	 t_{RIO} t_{FIO}	 − −	 − −	 0.8 0.8	 μs μs
$\overline{INT}$ Pullup Resistance	2	R_{ITA}	20	50	80	kΩ
Positive Going Input High Voltage Threshold (CLK_IN, MOSI, CLK_SPI, EN_RPU, $\overline{CS}$)	2, 3, 4, 5, 6, 8	V_{IA}	0.70 * V_{CC}	−	V_{CC}	V
Negative Going Input High Voltage Threshold (CLK_IN, MOSI, CLK_SPI, EN_RPU, $\overline{CS}$)	2, 3, 4, 5, 6, 8	V_{ILLA}	0	−	0.3 * V_{CC}	V
Output High Voltage $\overline{INT}$, MISO @ O_H = −10 μA	2, 7	V_{OH}	 V_{CC} −1.0 V	 −	 V_{CC}	V
Output Low Voltage $\overline{INT}$, MISO @ O_H = 200 μA	2, 7	V_{OL}	 −	 −	 0.4	V
Delay Between Two Consecutive CLK_SPI Sequence	5	td_{clk}	33	−	−	ns

3. Since a 20 kΩ (typical) pullup resistor is provided by the NCN6001, the external MPU can use an Open Drain connection. On the other hand, NMOS smart cards can be used straightforward.

POWER SUPPLY @ 2.7 V < V_{CC} < 5.5 V (−25°C to +85°C ambient temperature, unless otherwise noted).

Rating	Pin	Symbol	Min	Typ	Max	Unit
Input Power Supply	9	V_{CC}	2.70	–	5.50V	V
Standby Supply Current Conditions: $\overline{INT}$ = CLK_IN = CLK_SPI = $\overline{CS}$ = H I/O = MOSI = EN_RPU = H, No Card Inserted V_{CC} = 3.0 V V_{CC} = 5.0 V	9	ICC_{sb}	 – –	 25 35	 50 60	μA
DC Operating Current CLK_IN = Low, All Card Pins Unloaded @ V_{CC} = 3.3 V, CRD_VCC = 5.0 V @ V_{CC} = 5.5 V, CRD_VCC = 5.0 V	9	ICC_{op}	 – –	 – –	 0.5 1.5	mA
V_{CC} Under Voltage Detection$_{High}$ V_{CC} Under Voltage Detection$_{Low}$ V_{CC} Under Voltage (Note 6)	9	VCC_{LH} VCC_{LL} VCC_{POR}	2.20 2.00 1.50	– – –	2.70 2.60 2.20	V
Output Card Supply Voltage @ 2.7 V < V_{CC} < 5.5 V CRD_VCC = 1.8 V @ Iload = 35 mA CRD_VCC = 3.0 V @ Iload = 60 mA CRD_VCC = 5.0 V @ Iload = 65 mA	13	 V_{C2H} V_{C3H} V_{C5H}	 1.65 2.75 4.75	 – 1.80 3.00 5.00	 1.95 3.25 5.25	V
Maximum Continuous Output Current @ CRD_VCC = 1.8 V @ CRD_VCC = 3.0 V @ CRD_VCC = 5.0 V	13	ICC	 35 60 65	 – – –	 – – –	mA
Output Over Current Limit V_{CC} = 3.3 V, CRD_VCC = 1.8 V, 3.0 V or 5.0 V V_{CC} = 5.0 V, CRD_VCC = 1.8 V, 3.0 V or 5.0 V	13	Iccov	 – –	 100 150	 – –	mA
Output Dynamic Peak Current @ CRD_VCC = 1.8 V, 3.0 V or 5.0 V, Cout = 10 μF (Notes 4 and 5)	13	Iccd	 100	 –	 –	mA
Output Card Supply Voltage Ripple @ V_{CC} = 3.6 V, Lout = 22 μH, Cout1 = Cout2 = 4.7 μF Ceramic X7R, Iout = 55 mA CRD_VCC = 5.0 V CRD_VCC = 3.0 V (Note 4) CRD_VCC = 1.8 V	13	–	 – – –	 35 35 35	 – – –	mV
Output Card Supply Turn On Time @ Lout = 22 μF, Cout1 = 10 μF Ceramic V_{CC} = 2.7 V, CRD_VCC = 5.0 V	13	VCC_{TON}	–	–	500	μs
Output Card Supply Shut Off Time @ Cout1 = 10 μF, Ceramic V_{CC} = 2.7 V, CRD_VCC = 5.0 V, VCC_{OFF} < 0.4 V	13	VCC_{TOFF}	–	100	250	μs

4. Ceramic X7R, SMD type capacitors are mandatory to achieve the CRD_VCC specifications. When an electrolytic capacitor is used, the external filter must include a 220 nF, max 50 mΩ ESR capacitor in parallel, to reduce both the high frequency noise and ripple to a minimum. Depending upon the PCB layout, it might be necessary to use two 4.7 μF/6.0 V/ceramic/X5R/SMD 0805 in parallel, yielding an improved CRD_VCC ripple over the temperature range.
5. Pulsed current, according to ISO7816−3, paragraph 4.3.2.
6. No function externally available during the V_{CC} POR sequence.

SMART CARD INTERFACE @ 2.7 V < V_{CC} < 5.5 V (−25°C to +85°C ambient temperature, unless otherwise noted).
Note: Digital inputs undershoot < − 0.3 V to ground, Digital inputs overshoot < 0.3 V to V_{CC}.

Rating	Pin	Symbol	Min	Typ	Max	Unit
CRD_RST @ CRD_VCC = 1.8 V, 3.0 V, 5.0 V	19					
Output RESET V_{OH} @ Irst = −200 μA		V_{OH}	CRD_VCC − 0.5	–	CRD_VCC	V
Output RESET V_{OL} @ Irst = 200 μA		V_{OL}	0	–	0.4	V
Output RESET Rise Time @ Cout = 30 pF		t_R	–	–	100	ns
Output RESET Fall Time @Cout = 30 pF		t_F	–	–	100	ns
CRD_CLK as a function of CRD_VCC	17					
CRD_VCC = +5.0 V or 3.0 V or 1.8V						
Output Frequency		F_{CRDCLK}	–		20	MHz
Output V_{OH} @ Icrd_clk = −200 μA		V_{OH}	CRD_VCC − 0.5		CRD_VCC	V
Output V_{OL} @ Icrd_clk = 200 μA		V_{OL}	0		+0.4	V
CRD_CLK Output Duty Cycle						
CRD_VCC = 5.0 V		F_{CRDDC}	45		55	%
CRD_VCC = 3.0 V			40		60	%
CRD_VCC = 1.8 V (Note 7)			40		60	%
Rise & Fall time @ CRD_VCC = 1.80 V to 5.0 V						
Fast Mode						
Output CRD_CLK Rise time @ Cout = 30 pF		t_{ress}	–	2.1	4	ns
Output CRD_CLK Fall time @ Cout = 30 pF		t_{fcs}	–	1.9	4	ns
Rise & Fall time @ CRD_VCC = 1.80 V to 5.0 V						
Slow Mode						
Output CRD_CLK Rise time @ Cout = 30 pF		t_{rills}	–	11.5	16	ns
Output CRD_CLK Fall time @ Cout = 30 pF		t_{ulsa}	–	10.8	16	ns
CRD_IO @ CRD_VCC = 1.8 V 3.0 V, 5.0 V	20					
CRD_IO Data Transfer Frequency		F_{IO}	–	400	–	kHz
CRD_IO Rise time @ Cout = 30 pF		t_{RIO}	–	–	0.8	μs
CRD_IO Fall time @ Cout = 30 pF		t_{FIO}	–	–	0.8	μs
Output V_{OH} @ Icrd_clk = −20 μA		V_{OH}	CRD_VCC − 0.5	–	CRD_VCC	V
Output V_{OL} @ Icrd_clk = 500 μA, V_{IL} = 0 V		V_{OL}	0	–	0.4	V
CRD_IO Pullup Resistor	20	R_{CRDPU}	14	20	26	kΩ
CRD_C8 Output Rise and Fall Time @ Cout = 30 pF	14	t_{RC8}, t_{FC8}	–	–	100	ns
CRD_C4 Output Rise and Fall Time @ Cout = 30 pF	15	t_{RC4}, t_{FC4}	–	–	100	ns
CRD_C4 and CRD_C8 Data Transfer Frequency	14, 15	F_{C48}	–	400	–	kHz
CRD_C8, CRD_C4 Output Voltages	14, 15	V_{OH}, V_{OL}				
High Level @ Irst = −200 μA			CRD_VCC − 0.5	–	–	V
Low Level @ Irst = +200 μA			0	–	0.4	V
C8/S0 and C4/S0 Address Bias Current (Note 8)	14, 15	I_{bc4c8}	–	1.0	–	μA
Card Detection Digital Filter Delay:	18					
Card Insertion		T_{CRDIN}	25	50	150	μs
Card Extraction		T_{CRDOFF}	25	50	150	μs
Card Insertion or Extraction Positive Going Input High Voltage	18	V_{IHDET}	0.70 * V_{CC}	–	V_{CC}	V
Card Insertion or Extraction Negative Going Input Low Voltage	18	V_{ILDET}	0	–	0.30 * V_{CC}	V
Card Detection Bias Pullup Current @ V_{CC} = 5.0 V	18	I_{DET}	–	10	–	μA
Output Peak Max Current Under Card Static Operation Mode @ CRD_VCC = 3.0 V or = 5.0 V CRD_RST, CRD_IO, CRD_C4, CRD_C8	1, 20	Icrd_iorst	–	–	15	mA
Output Peak Max Current Under Card Static Operation Mode @ CRD_VCC = 3.0 V or = 5.0 V CRD_CLK	17	Icrd_clk	–	–	70	mA

7. Parameter guaranteed by design, function 100% production tested.
8. Depending upon the environment, using and external pullup resistor might be necessary to cope with PCB surface leakage current.

PROGRAMMING

Write Register → WRT_REG

The WRT_REG register handles three command bits [b5:b7] and five data bits [b0:b4] as depicted in Table 1. These bits are concatenated into a single byte to accelerate the programming sequence. The register can be updated when $\overline{CS}$ is low only.

The CRD_RST pin reflects the content of the MOSI WRT_REG[b4] during the chip programming sequence. Since this bit shall be Low to address the internal register of the chip, care must be observed as this signal will be immediately transferred to the CRD_RST pin.

Table 1. WRT_REG BITS DEFINITIONS

b0
b1
	If (b7 + b6 + b5) <> 110 and (b7 + b6 + b5) <> 101 and (b7 + b6 + b5) <> 111 then
	Case 00
	CRD_VCC = 0 V
	Case 01
	CRD_VCC = 1.8 V
	Case 10
	CRD_VCC = 3.0 V
	Case 11
	CRD_VCC = 5.0 V
	Else if (b7 + b6 + b5) = 110 then
	b1 drives C4
	b0 drives C8
	Else if (b7 + b6 + b5) = 101 then
	Case (b4 + b3 + b2 + b1 + b0) = 0000
	CRD_DET = NO
	Case (b4 + b3 + b2 + b1 + b0) = 0001
	CRD_DET = NC
	Case (b4 + b3 + b2 + b1 + b0) = 0010
	SPI_MODE = Special
	Case (b4 + b3 + b2 + b1 + b0) = 0011
	SPI_MODE = Normal
	End if

b2
b3
	If (b7 + b6 + b5) <> 110 and (b7 + b6 + b5) <> 101 and (b7 + b6 + b5) <> 111 then
	Case 00
	CRD_CLK = L
	Case 01
	CRD_CLK = CLK_IN
	Case 10
	CRD_CLK = CLK_IN/2
	Case 11
	CRD_CLK = CLK_IN/4
	Else if (b7 + b6 + b5) = 110 then
	b3 drives CRD_CLK
	b2 drives CRD_IO
	Else if (b7 + b6 + b5) = 101 then
	Case (b4 + b3 + b2 + b1 + b0) = 0000
	CRD_DET = NO
	Case (b4 + b3 + b2 + b1 + b0) = 0001
	CRD_DET = NC
	Case (b4 + b3 + b2 + b1 + b0) = 0010
	SPI_MODE = Special
	Case (b4 + b3 + b2 + b1 + b0) = 0011
	SPI_MODE = Normal
	End if

b4	Drives CRD_RST pin (Note 10)
b5, b6, b7	000 Select Asynchronous Card #0 (Note 9), four chips bank $\overline{CS}$ signal 001 Select Asynchronous Card #1 (Note 9), four chips bank $\overline{CS}$ signal 010 Select Asynchronous Card #2 (Note 9), four chips bank $\overline{CS}$ signal 011 Select Asynchronous Card #3 (Note 9), four chips bank $\overline{CS}$ signal 100 Select External Asynchronous Card, dedicated $\overline{CS}$ signal 110 Select External Synchronous Card, dedicated $\overline{CS}$ signal 101 Set Card Detection Switch polarity, Set SPI_MODE normal or special. Set CRD_CLK slopes Fast or Slow. 111 Reserved for future use

9. When operating in Asynchronous mode, [b5:b7] are compared with the external voltage levels present pins C4/S0 and C8/S1 (respectively pins 15 and 14).
10. The CRD_RST pin reflects the content of the MOSI WRT_REG[b4] during the chip programming sequence. Since this bit shall be Low to address the internal register of the chip, care must be observed as this signal will be immediately transferred to the CRD_RST pin.

Table 2. WRT_REG BITS DEFINITIONS AND FUNCTIONS

ADDRESS				PARAMETERS							
CHIP BANK									MOSI bits [b3:b2]	MOSI bits [b1:b0]	MOSI bits [b7:b0]
1	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**	CRD_CLK	CRD_VCC	CRD_DET
1	0	X	X	RST	0	0	0	0	Low	0	–
1	0	X	X	RST	0	1	0	1	1/1	1.8 V	–
1	0	X	X	RST	1	0	1	0	1/2	3.0 V	–
1	0	X	X	RST	1	1	1	1	1/4	5.0 V	–
1	1	0	1	0	0	0	0	0	–	–	NO
1	1	0	1	0	0	0	0	1	–	–	NC
1	1	0	1	0	0	0	1	0	–	–	Special
1	1	0	1	0	0	0	1	1	–	–	Normal
1	1	0	1	0	0	1	0	0	–	–	SLO_SLP
1	1	0	1	0	0	1	0	1	–	–	FST_SLP
1	1	1	1	–	–	–	–	–	–	–	RFU
2	1	0	0	RST	0	0	0	0	Low	0	–
2	1	0	0	RST	0	1	0	1	1/1	1.8 V	–
2	1	0	0	RST	1	0	1	0	1/2	3.0 V	–
2	1	0	0	RST	1	1	1	1	1/4	5.0 V	–
2	1	1	0	RST	CLK	I/O	C4	C8	–	–	Data to Sync. Card
2	1	0	1	0	0	0	0	0	–	–	NO
2	1	0	1	0	0	0	0	1	–	–	NC
2	1	0	1	0	0	0	1	0	–	–	Special
2	1	0	1	0	0	0	1	1	–	–	Normal
2	1	0	1	0	0	1	0	0	–	–	SLO_SLP
2	1	0	1	0	0	1	0	1	–	–	FST_SLP
2	1	1	1	–	–	–	–	–	–	–	RFU

11. Chip Bank 1 = Asynchronous cards, four slots addresses 1 to 4.
    Chip Bank 2 = Asynchronous or synchronous card, single slot.
12. Address 101 and bits [b0 : b4] not documented in the table are reserved for future use.
    Address 111 is reserved for future use.

Although using the %111XXXXX code is harmless from a NCN6001 silicon standpoint, care must be observed to avoid uncontrolled operation of the interface sharing the same digital bus. When this code is presented on the digital bus, the CRD_RST signal of any interface sharing the $\overline{CS}$ signal, immediately reflects the digital content of the MOSI bit b4 register. Similarly, the MISO register of the shared interface is presented on the SPI port. Consequently, data collision, at MISO level, and uncontrolled card operation are likely to happen if the system uses a common Chip Select line. It is strongly recommended to run a dedicated $\overline{CS}$ bit to any external circuit intended to use the $111xxxxx code.

On the other hand, the CRD_RST signal will be forced to Low when the internal register of the chip is programmed to accommodate different hardware conditions (NO/NC, Special/Normal, SLO_SLP/FST_SLP). Generally speaking, such a configuration shall take place during the Power On Reset to avoid CRD_RST activation.

Read Register → READ_REG

The READ_REG register contains the data read from the interface and from the external card. The selected register is transferred to the MISO pin during the MOSI sequence ($\overline{CS}$ = Low). Table 3 gives the bits definition.

Depending upon the programmed SPI_MODE, the content of READ_REG is transferred on the MISO line either on the Positive going (SPI_MODE = Special) or upon the Negative going slope (SPI_MODE = Normal) of the CLK_SPI signal. The external microcontroller shall discard the three high bytes since they carry no valid data.

Table 3. MOSI AND MISO BITS IDENTIFICATIONS AND FUNCTIONS

MOSI	b7	b6	b5	b4	b3	b2	b1	b0	Operating Mode
	0	0	0	RST	CLK	CLK	V_{CC}	V_{CC}	Asynchronous, Program Chip
	0	0	1	RST	CLK	CLK	V_{CC}	V_{CC}	Asynchronous, Program Chip
	0	1	0	RST	CLK	CLK	V_{CC}	V_{CC}	Asynchronous, Program Chip
	0	1	1	RST	CLK	CLK	V_{CC}	V_{CC}	Asynchronous, Program Chip
	1	0	0	RST	CLK	CLK	V_{CC}	V_{CC}	Asynchronous, Program Chip
	1	1	0	RST	CLK	I/O	C4	C8	Synchronous, Sets Card Bits
MISO	z	z	z	Card Detect	I/O	C4	C8	PWR Monitor	Read Back Data

ASYNCHRONOUS MODE

In this mode, the CRD_C4 and CRD_C8 pins are used to define the physical addresses of the interfaces when a bank of up to four NCN6001 share the same digital bus.

SYNCHRONOUS MODE

In this mode, CRD_C4 and CRD_C8 are connected to the smart card and it is no longer possible to share the $\overline{CS}$ signal with other device. Consequently, a dedicated Chip Select signal must be provided when the interfaces operate in a multiple operation mode (Figure 34).

On the other hand, since bits [b4 – b0] of the MOSI register contain the smart card data, programming the CRD_VCC output voltage shall be done by sending a previous MOSI message according to Table 1 and Table 2.

The CRD_RST pin reflects the content of the MOSI WRT_REG[b4] during the chip programming sequence. Since this bit shall be Low to address the internal register of the chip, care must be observed as this signal will be immediately transferred to the CRD_RST pin.

Since no physical address can exist when the chip operates in this mode, the MOSI register must use the format %100XXXXX to program the chip (%100 prefix, XXXXX data).

Example:

```
LDAA  #%10010111        ;set RST = H, CLK = 1/1, VCC = 5.0 V
STAA  MOSI
LDAA  #%11010011        ;SYNC. Card: set RST = H, CLK = L, IO = L, C4 = H, C8= H
STAA  MOSI
LDAA  #%00111110        ;ASYNC. Card: set RST = H, CLK = ¼, VCC = 3.0 V
STAA  MOSI
```

STARTUP DEFAULT CONDITIONS

At startup, when the V_{CC} power supply is turned on, the internal POR circuit sets the chip in the default conditions as defined in Table 4.

Table 4. STARTUP DEFAULT CONDITIONS

CRD_DET	Normally Open
CRD_VCC	Off
CRD_CLK	t_r and t_f = SLOW
CRD_CLK	Low
Protocol	Special Mode

CARD DETECTION

The card is detected by the external switch connected pin 18. The internal circuit provides a positive bias of this pin and the polarity of the insertion/extraction is programmable by the MOSI protocol as depicted in Table 2.

The bias current is 1.0 μA typical and care must be observed to avoid leakage to ground from this pin to maintain the logic function. In particular, using a low impedance probe (< 1.0 MΩ) may lead to uncontrolled operation during the debug.

Depending upon the programmed condition, the card can be detected either by a Normally Open (default condition) or a Normally Close switch (Table 2). On the other hand, the meaning of the feedback message contained in the MISO register bit b4, depends upon the SPI mode of operation as defined here below:

SPI Normal Mode: the MISO bit b4 is High when a card is inserted, whatever be the polarity of the card detect switch.

SPI Special Mode: the MISO bit b4 copies the logic state of the Card detect switch as depicted here below, whatever be the polarity of the switch used to handle the detection:

CRD_DET = Low → MISO/b4 = Low

CRD_DET = High → MISO/b4 = High

CRD_VCC OPERATION

The built−in DC/DC converter provides the CRD_VCC voltage and can be programmed to run one of the three possible values, 1.8 V, 3.0 V or 5.0 V, assuming the input voltage V_{CC} is within the 2.7 V to 5.5 V range. In any case, CRD_VCC is voltage regulated, together with a current overload detection. On the other hand, the power conversion is automatically switched to handle either a boost or a buck mode of operation, depending upon the difference between the input voltage V_{CC} and the output supply CRD_VCC.

The CRD_VCC output current is a function of the V_{CC} input value as depicted in Table 5.

Table 5. CRD_VCC OUTPUT VOLTAGE RANGE

CRD_VCC	Comments
1.80 V	Maximum Output DC Current = 35 mA
3.0 V	Maximum Output DC Current = 60 mA
5.0 V	Maximum Output DC Current = 65 mA

Whatever the CRD_VCC output voltage may be, a built−in comparator makes sure the voltage is within the ISO7816−3/ EMV specifications. If the voltage is no longer within the minimum/maximum values, the DC/DC is switched Off, the Power Down sequence takes place and an interrupt is presented at the $\overline{INT}$ pin 2.

POWERUP SEQUENCE

The Powerup Sequence makes sure all the card related signals are Low during the CRD_VCC positive going slope. These lines are validated when CRD_VCC is above the minimum specified voltage (depending upon the programmed CRD_VCC value).

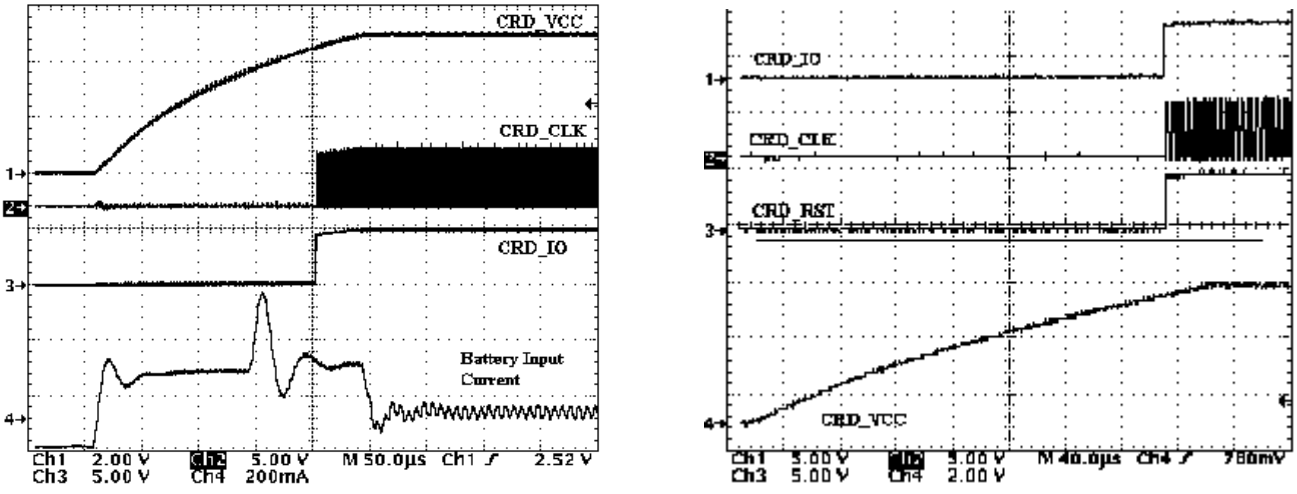


Figure 4. Typical Startup CRD_VCC Sequence

At powerup, the CRD_VCC voltage rise time depends upon the current capability of the DC/DC converter associated with the external inductor L1 and the reservoir capacitor connected across CRD_VCC and GROUND. During this sequence, the average input current is 300 mA typical (Figure 4), assuming the system is fully loaded during the startup. Finally, the application software is responsible for the smart card signal sequence.

On the other hand, at turn off, the CRD_VCC fall time depends upon the external reservoir capacitor and the peak current absorbed by the internal NMOS transistor built across CRD_VCC and GROUND. These behaviors are depicted in Figure 5.

Since these parameters have finite values, depending upon the external constraints, the designer must take care of these limits if the t_{ON} or the t_{OFF} provided by the data sheets does not meet his requirements.

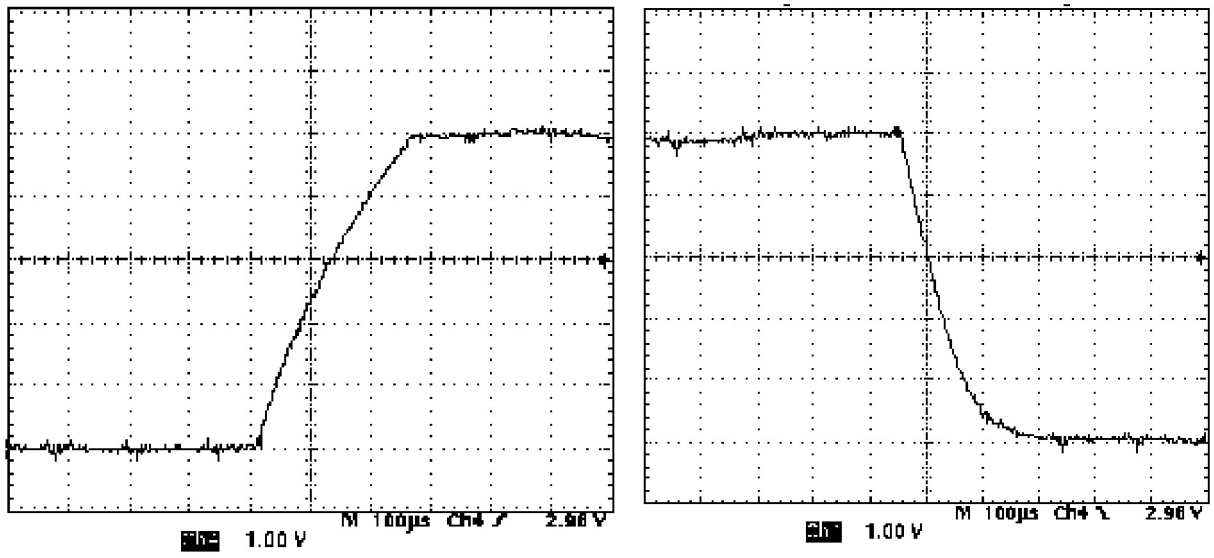


Figure 5. CRD_VCC Typical Rise and Fall Time

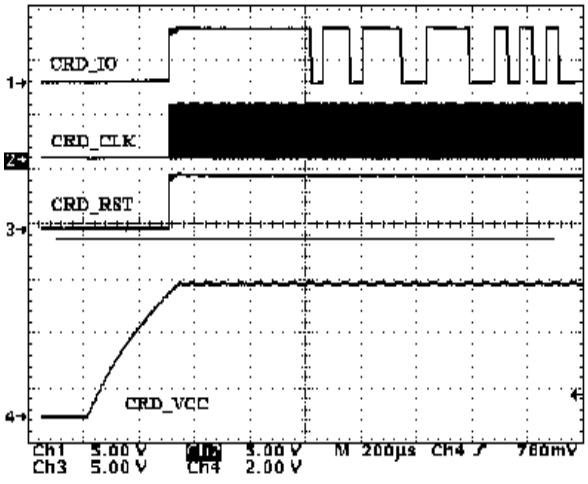


Figure 6. Startup Sequence with ATR

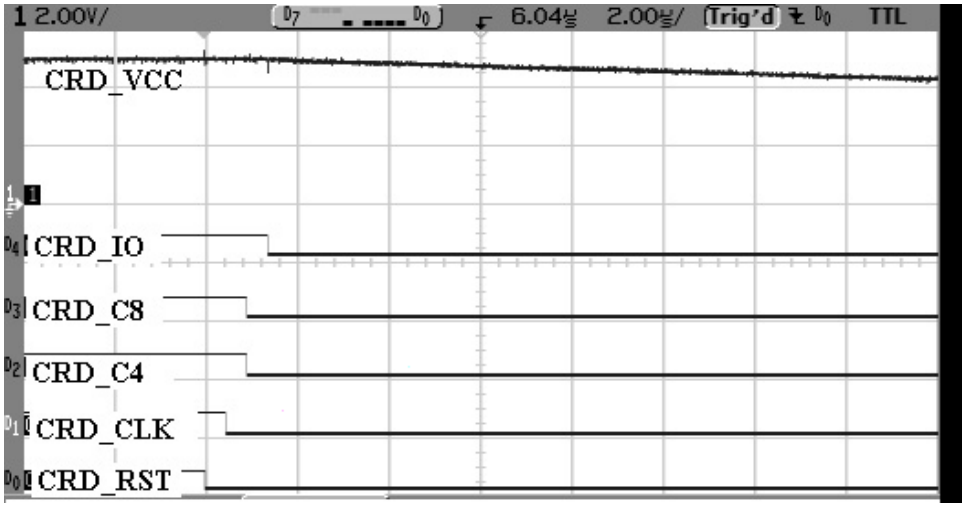
POWER DOWN SEQUENCE

The NCN6001 provides an automatic Power Down sequence, according to the ISO7816−3 specifications, and the communication session terminates immediately. The sequence is launched when the card is extracted, or when the CRD_VCC voltage is overloaded as described by the ISO/CEI 7816−3 sequence depicted hereafter:

ISO7816−3 sequence:
→Force RST to Low
→Force CLK to Low, unless it is already in this state
→Force C4 & C8 to Low
→Force CRD_IO to Low
→Shut Off the CRD_VCC supply

Since the internal digital filter is activated for any card insertion or extraction, the physical power sequence will be activated 50 μs (typical) after the card has been extracted. Of course, such a delay does not exist when the MPU intentionally launches the power down. Figure 7 shows the oscillogram captured in the NCN6001 demo board.

The internal active pull down NMOS connected across CRD_VCC and GND discharges the external reservoir capacitor in 100 μs (typical), assuming Cout = 10 μF.



Typical delay between each signal is 500 ns

Figure 7. Typical Power Down Sequence

The internal active pull down NMOS connected across CRD_VCC and GND discharges the external reservoir capacitor in 100 μs (typical), assuming Cout = 10 μF.

DATA I/O LEVEL SHIFTER

The level shifter accommodates the voltage difference that might exist between the microcontroller and the smart card. A pulsed accelerator built−in circuit provides the fast positive going transient according to the ISO7816−3 specifications. The basic I/O level shifter is depicted in Figure 8.

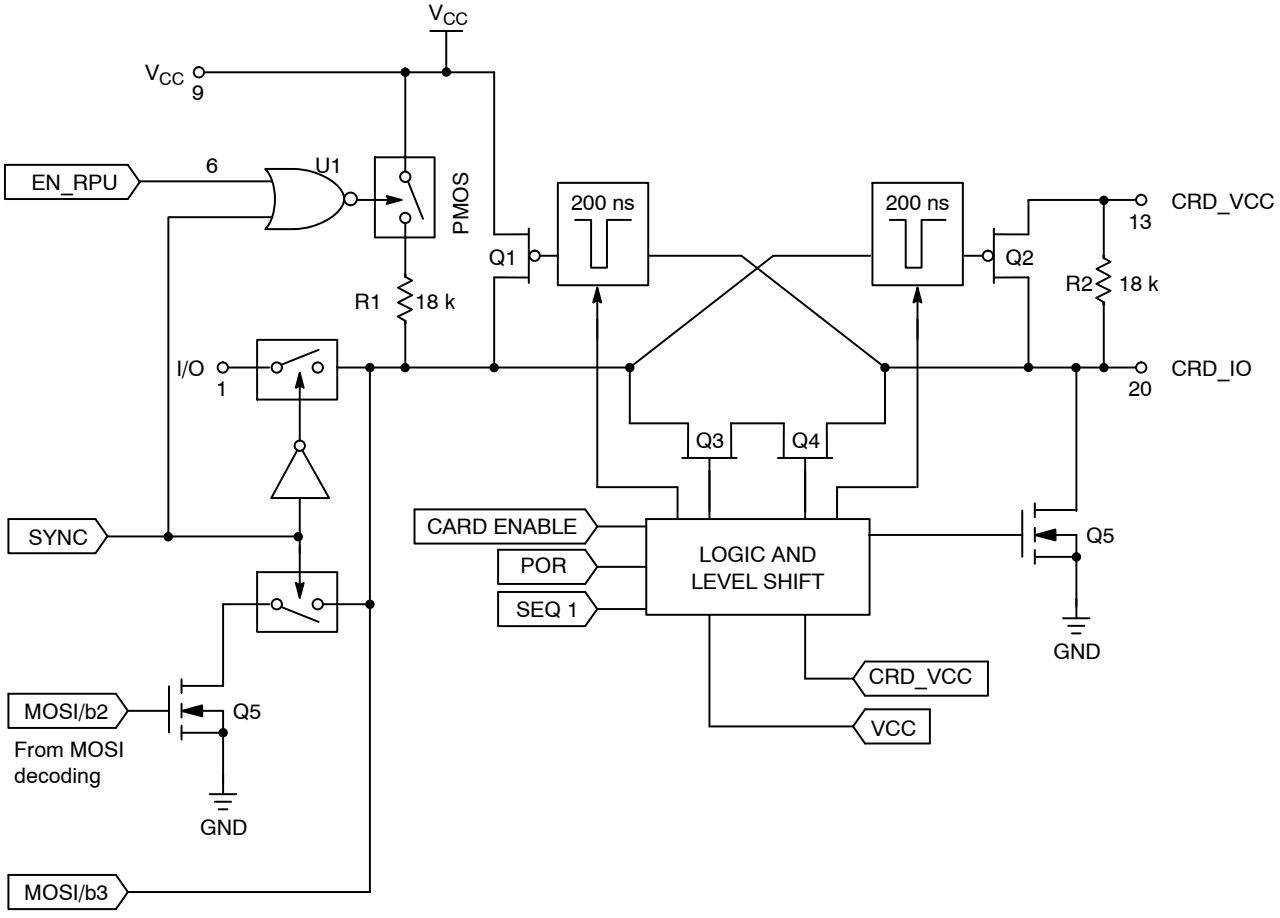


Figure 8. Basic I/O Internal Circuit

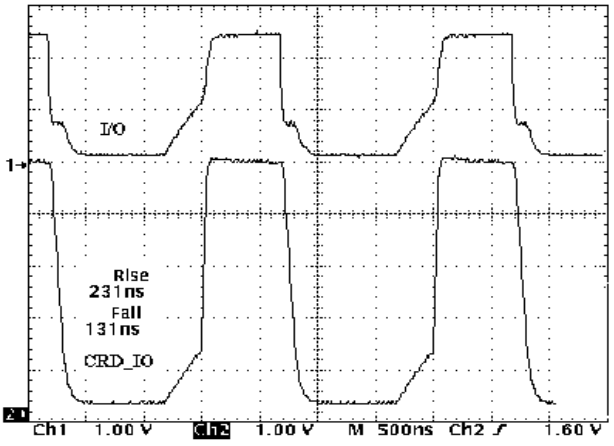
The transaction is valid when the Chip Select pin is Low, the I/O signal being Open Drain or Totem Pole on either sides.

Since the device can operate either in a single or a multiple card system, provisions have been made to avoid CRD_IO current overload. Depending upon the selected mode of operation (ASYNC. or Sync), the card I/O line is respectively connected to either I/O pin 1, or to the MOSI register byte bit 2. On the other hand, the logic level present at the card I/O is feedback to the μC via the MISO register bit 3. The logic level present at pin 6 controls the connection of the internal pullup as depicted in Table 6.

Table 6. I/O PULLUP RESISTOR TRUE TABLE

EN_RPU	I/O Pullup Resistor	Device Operation
Low	Open, 18 kΩ disconnected	Parallel Mode
High	Internal 18 kΩ pullup active	Single Device

NOTE: 18 kΩ typical value



NOTE: Both sides of the interface run with open drain load (worst case condition).

Figure 9. Typical I/O Rise and Fall Time

GENERAL PURPOSE CRD_C4 AND CRD_C8

These two pins can be used as a logic input to define the address of a given interface (in the range $00 to $11), or as a standard C4/C8 access to the smart card's channels. Since these pins can be directly connected to the V_{CC} power supply, both output stages are built with switched NMOS/PMOS totem pole as depicted in Figure 10.

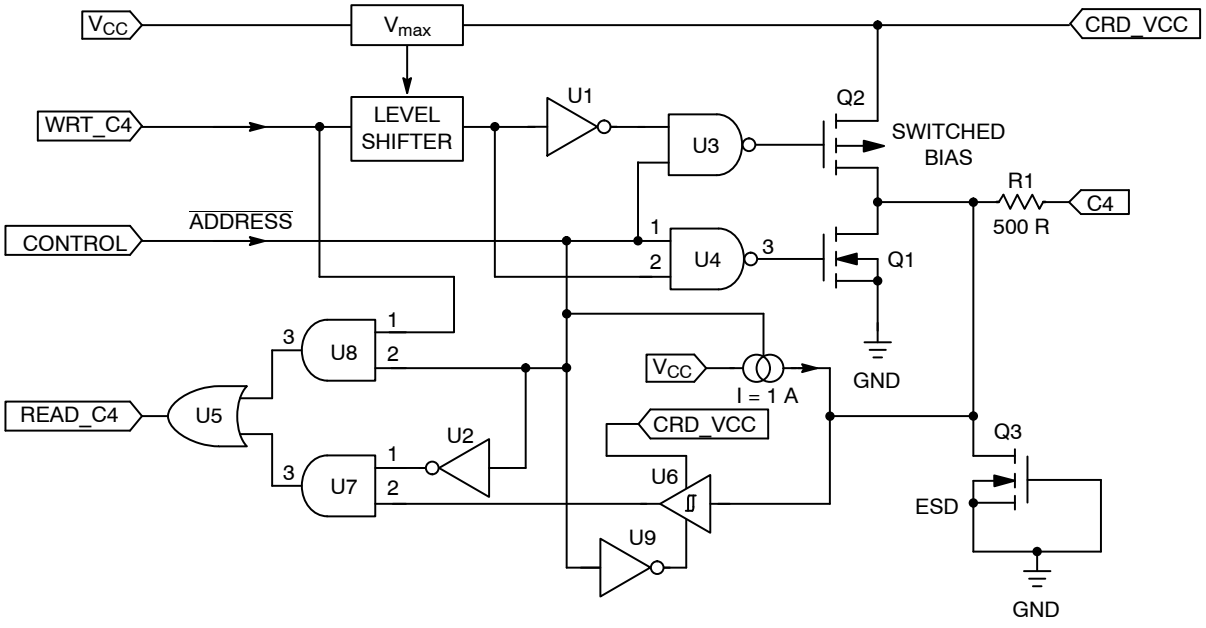


Figure 10. Typical CRD_C4 Output Drive and Logic Control

The C4 and C8 pins are biased by an internal current source to provide a logic one when the pin is left open. In this case, care must be observed to avoid relative low impedance to ground to make sure the pin is at a High logic level. However, it is possible to connect the pin to V_{CC} (battery supply) to force the logic input to a High level, regardless of the input bias. Thanks to the CONTROL internal signal, the system automatically adapts the mode of operation (chip address or data communication) and, except the leakage, no extra current is drawn from the battery to bias these pins when the logic level is High.

When any of these pins is connected to GND, a continuous 1 μA typical sink current will be absorbed from the battery supply.

The switched Totem Pole structure provides the fast positive going transient when the related pin is forced to the High state during a data transfer. In the event of a low impedance connected across C4 or C8 to ground, the current flow is limited to 15 mA, according to the ISO7816−3 specification.

The two general purpose pins can transfer data from the external microcontroller to the card and read back the logic state, but none of these pins can read the data coming from the external smart card. On the other hand, both C4 and C8 can read input logic, hence the physical address of a given chip.

In order to sustain the 8 kV ESD specified for these pins, an extra protection structure Q3 has been implemented to protect the MOS gates of the input circuit.

INTERRUPT

When the system is powered up, the $\overline{INT}$ pin is set to High upon POR signal. The interrupt pin 2 is forced LOW when either a card is inserted/extracted, or when a fault is developed across the CRD_VCC output voltage. This signal is neither combined with the $\overline{CS}$ signal, nor with the chip address. Consequently, an interrupt is placed on the μC input as soon as one of the condition is met.

The $\overline{INT}$ signal is clear to High upon one of the condition given in Table 7.

Table 7. INTERRUPT RESET LOGIC

Interrupt Source	$\overline{CS}$	CRD_VCC	Chip Address
Card Insertion	L	> 0	Selected Chip MOSI[b7 : B5] = 0xx or MOSI[b7 : B5] = 101
Card Insertion	L	= 0	Selected Chip MOSI[b7 :B5] = 0xx or MOSI[b7 : B5] = 101
Over Load	L	= 0	Selected Chip MOSI[b7 : B5] = 0xx or MOSI[b7 : B5] = 101

When several interfaces share the same digital μC bus, it is up to the software to pool the chips, using the MISO register to identify the source of the interrupt.

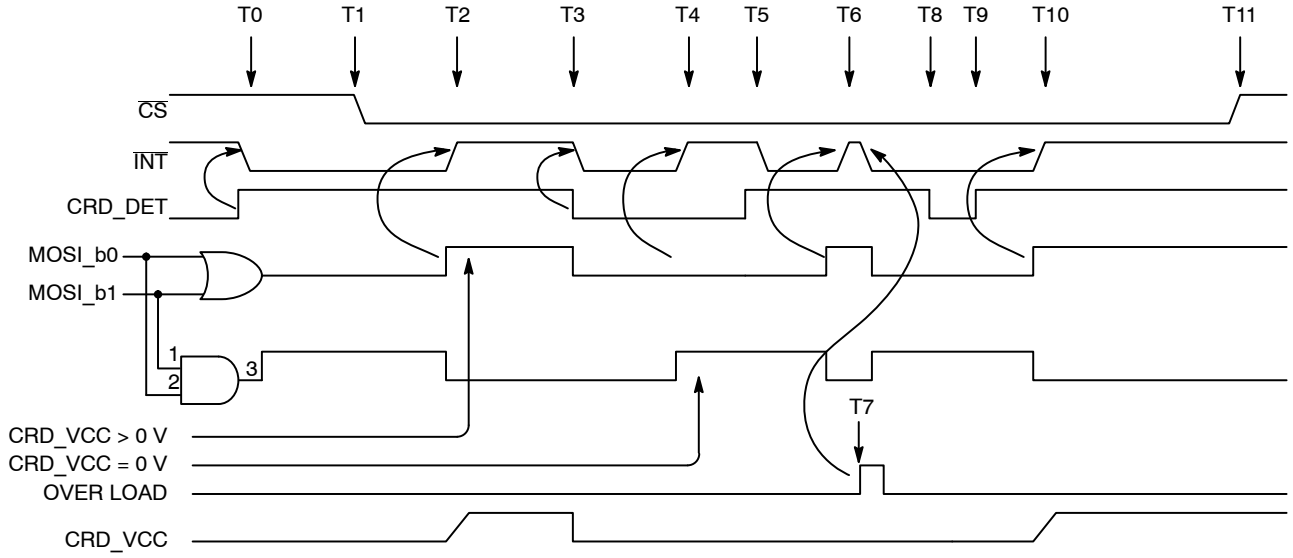


Figure 11. Basic Interrupt Function

Table 8. INTERRUPT RESET LOGIC OPERATION

T0	A card has been inserted into the reader and detected by the CRD_DET signal. The NCN6001 pulls down the interrupt line.
T1	The μC sets the $\overline{CS}$ signal to Low, the chip is now active, assuming the right address has been placed by the MOSI register.
T2	The μC acknowledges the interrupt and resets the $\overline{INT}$ to High by the MOSI [B1 : B0] logic state: CRD_VCC is programmed higher than zero volt.
T3	The card has been extracted from the reader, CRD_DET goes Low and an interrupt is set ($\overline{INT}$ = L). On the other hand, the PWR_DOWN sequence is activated by the NCN6001.
T4	The interrupt pin is clear by the zero volt programmed to the interface.
T5	Same as T0
T6	The μC start the DC/DC converter, the interrupt is cleared (same as T2)
T7	An overload has been detected by the chip : the CRD_VCC voltage is zero, the $\overline{INT}$ goes Low.
T8	The card is extracted from the reader, CRD_DET goes Low and an interrupt is set ($\overline{INT}$ = L).
T9	The card is re−inserted before the interrupt is acknowledged by the μC: the $\overline{INT}$ pin stays Low.
T10	The μC acknowledges the interrupt and reset the $\overline{INT}$ to High by the MOSI [B1 : B0] logic state: CRD_VCC is programmed higher than zero volt.
T11	The Chip Select signal goes High, all the related NCN6001 interface(s) are deactivated and no further programming or transaction can take place.

SPI PORT

The product communicates to the external microcontroller by means of a serial link using a Synchronous Port Interface protocol, the CLK_SPI being Low or High during the idle state. The NCN6001 is not intended to operate as a Master controller, but execute commands coming from the MPU.

The CLK_SPI, the $\overline{CS}$ and the MOSI signals are under the microcontroller's responsibility. The MISO signal is generated by the NCN6001, using the CLK_SPI and $\overline{CS}$ lines to synchronize the bits carried out by the data byte. The basic timings are given in Figure 12 and Figure 13. The system runs with two internal registers associated with the MOSI and MISO data:

WRT_REG is a write only register dedicated to the MOSI data.

READ_REG is a read only register dedicated to the MISO data.

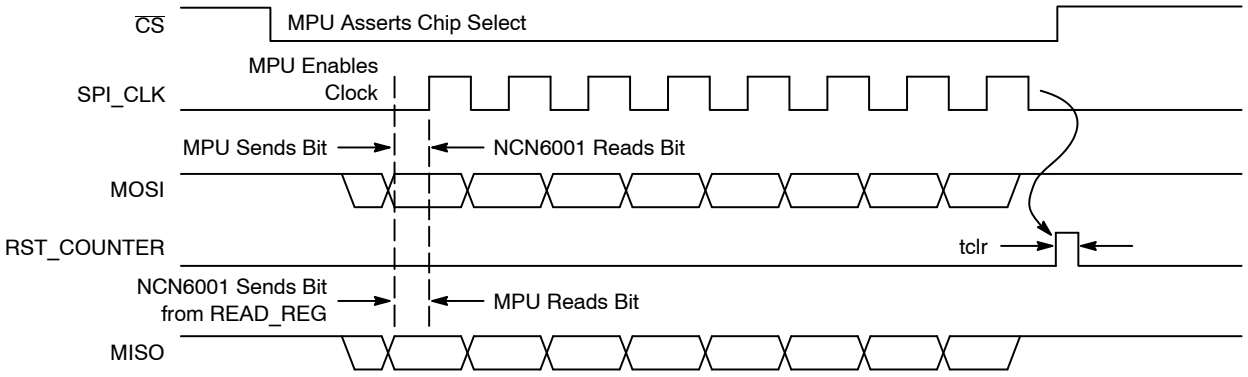


Figure 12. Basic SPI Timings and Protocol

When the $\overline{CS}$ line is High, no data can be written or read on the SPI port. The two data lines becomes active when $\overline{CS}$ = Low, the internal shift register is cleared and the communication is synchronized by the negative going edge of the $\overline{CS}$ signal. The data present on the MOSI line is considered valid on the negative going edge of the CLK_SPI clock and is transferred to the shift register on the next positive edge of the same CLK_SPI clock.

To accommodate the simultaneous MISO transmit, an internal logic identifies the chip address on the fly (reading and decoding the three first bits) and validates the right data present on the line. Consequently, the data format is MSB first to read the first three signal as bits B5, B6 and B7. The chip address is decoded from this logic value and validates the chip according to the C4 and C8 conditions (Figure 13).

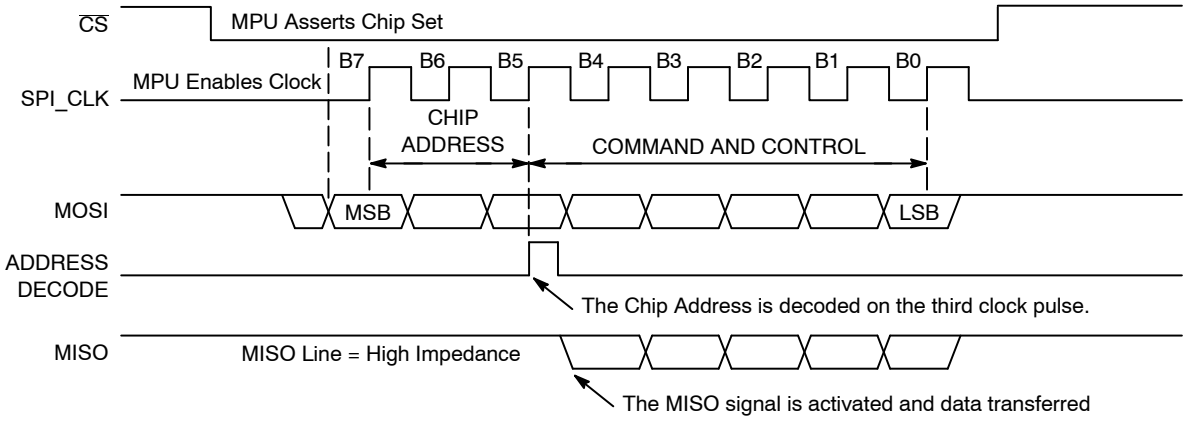


Figure 13. Chip Address Decoding Protocol and MISO Sequence

When the eight bits transfer is completed, the content of the internal shift register is latched on the positive going edge of the $\overline{CS}$ signal and the NCN6001 related functions are updated accordingly.

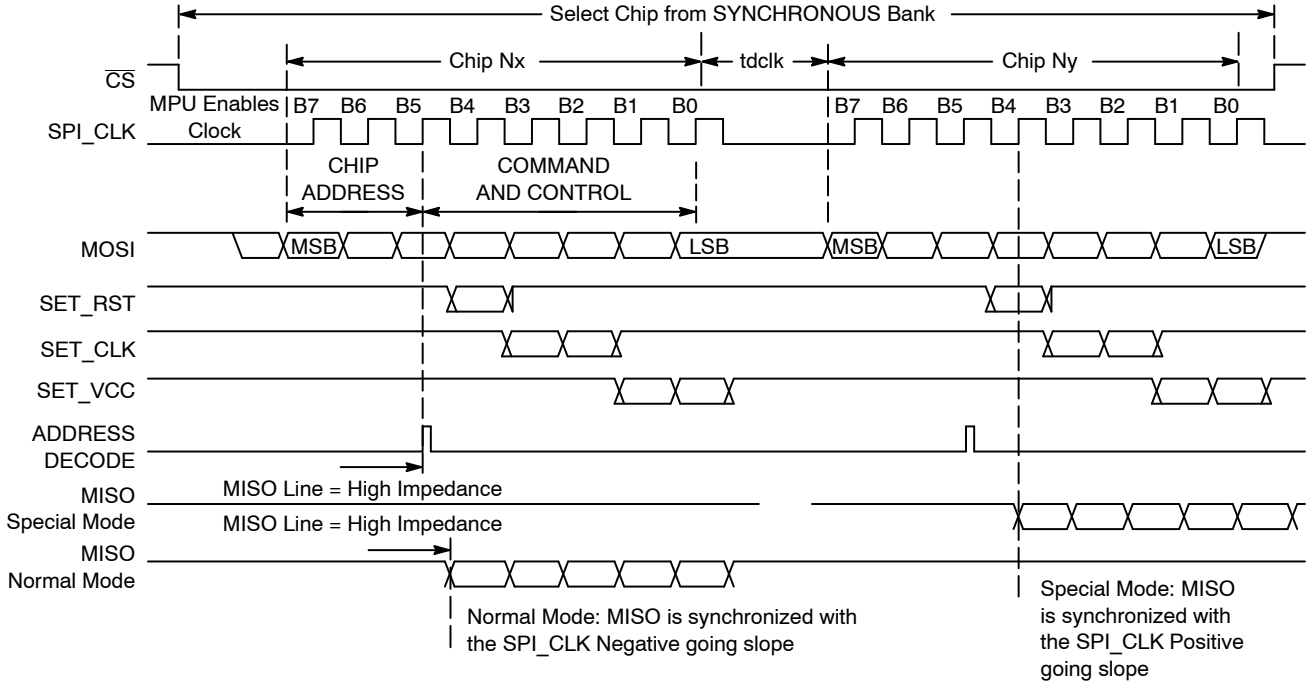


Figure 14. Basic Multi Command SPI Bytes

Since the four chips present in the Asynchronous Bank have an individual physical address, the system can control several of these chips by sending the data content within the same $\overline{CS}$ frame as depicted in Figure 14. The bits are decoded on the fly and the related sub blocks are updated accordingly. According to the SPI general specification, no code or activity will be transferred to any chip when the $\overline{CS}$ is High.

When two SPI bytes are sequentially transferred on the MOSI line, the CLK_SPI sequence must be separated by at least one half positive period of this clock (see td_{clk} parameter).

The oscillograms shown in Figure 15 and Figure 16 illustrate the SPI communication protocol (source: NCN6001 demo board).

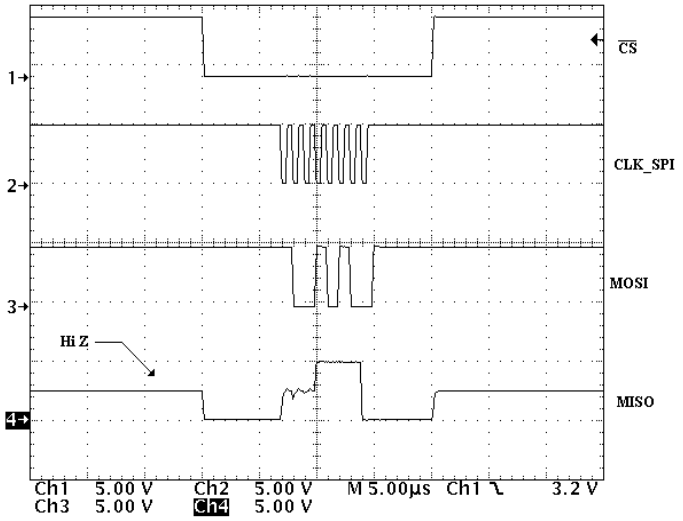
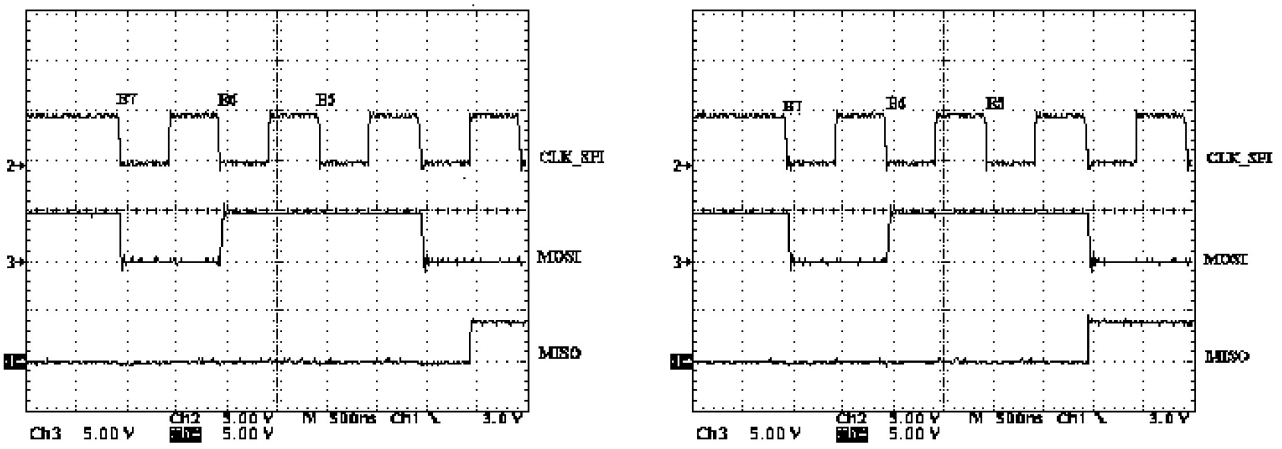


Figure 15. Programming Sequence, Chip Address = $03



Protocol: Special Mode

Protocol: Standard SPI

Figure 16. MISO Read Out Sequences

DC/DC OPERATION

The power conversion is based on a full bridge structure capable to handle either step up or step down power supply (Figure 17). The operation is fully automatic and, beside the output voltage programming, does not need any further adjustments.

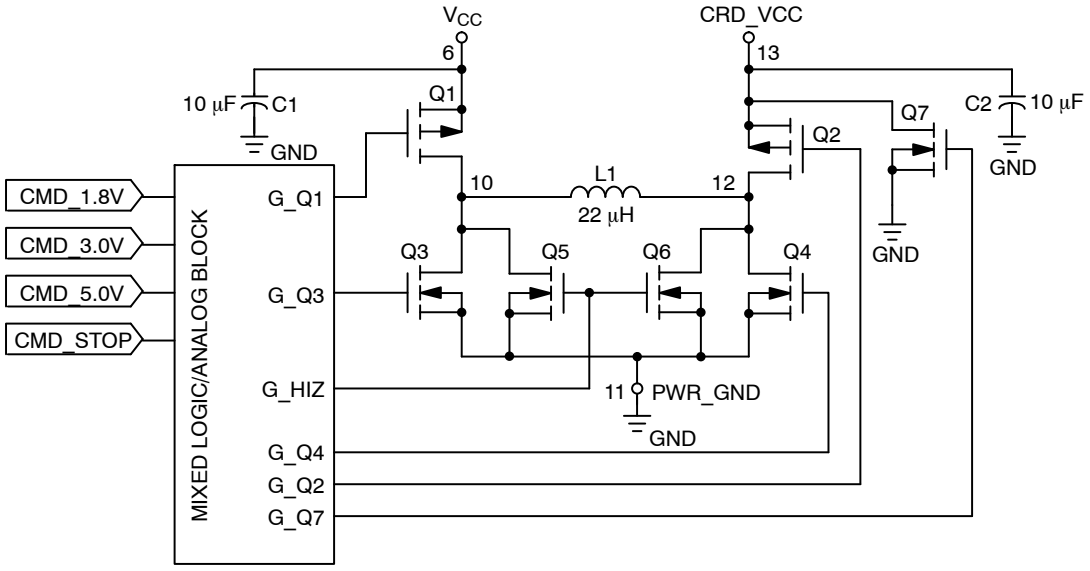


Figure 17. Basic DC/DC Converter

In order to achieve the 250 μs max time to discharge CRD_VCC to 400 mV called by the EMV specifications, an active pull down NMOS is provided (Q7) to discharge the external CRD_VCC reservoir capacitor. This timing is guaranteed for a 10 μF maximum load reservoir capacitor value (Figure 5).

The system operates with a two cycles concept (all comments are referenced to Figure 17 and Figure 18):

1 – Cycle 1 Q1 and Q4 are switched ON and the inductor L1 is charged by the energy supplied by the external battery. During this phase, the pair Q2/Q3 and the pair Q5/Q6 are switched OFF.

The current flowing the two MOSFET Q1 and Q4 is internally monitored and will be switched OFF when the Ipeak value (depending upon the programmed output voltage value) is reached. At this point, Cycle 1 is completed and Cycle 2 takes place. The ON time is a function of the battery voltage and the value of the inductor network (L and Zr) connected across pins 10/11.

A 4 μs timeout structure ensures the system does run in a continuous Cycle 1 loop

2 – Cycle 2 Q2 and Q3 are switched ON and the energy stored into the inductor L1 is dumped into the external load through Q2. During this phase, the pair Q1/Q4 and the pair Q5/Q6 are switched OFF.

The current flow period is constant (900 ns typical) and Cycle 1 repeats after this time if the CRD_VCC voltage is below the specified value.

When the output voltage reaches the specified value (1.8 V, 3.0 V or 5.0 V), Q2 and Q3 are switched OFF immediately to avoid over voltage on the output load. In the meantime, the two extra NMOS Q5 and Q6 are switched ON to fully discharge any current stored into the inductor, avoiding ringing and voltage spikes over the system. Figure 18 illustrates the theoretical waveforms present in the DC/DC converter.

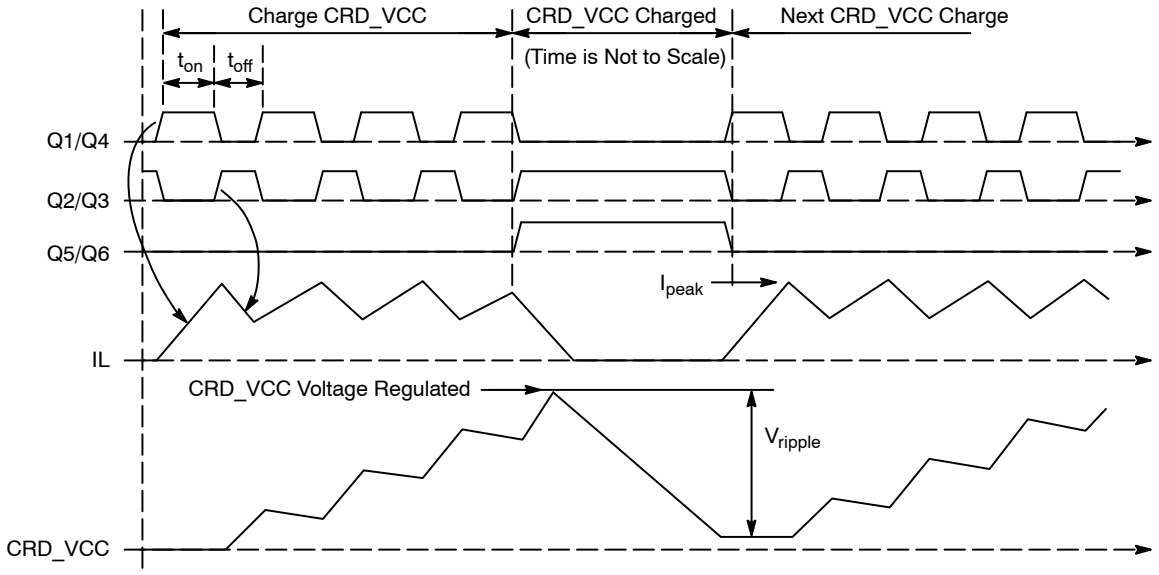


Figure 18. Theoretical DC/DC Operating Waveforms

When the CRD_VCC is programmed to zero volt, or when the card is extracted from the socket, the active pull down Q7 rapidly discharges the output reservoir capacitor, making sure the output voltage is below 0.4 V when the card slides across the ISO contacts.

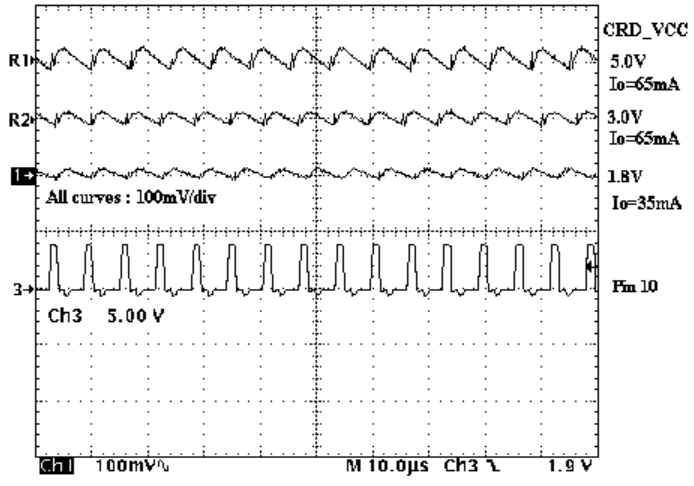
Based on the experiments carried out during the NCN6001 characterization, the best comprise, at time of printing this document, is to use two 4.7 μF/10 V/ ceramic/X7R capacitors in parallel to achieve the CRD_VCC filtering. The ESR will not extend 50 mΩ over the temperature range and the combination of standard parts provide an acceptable –20% to +20% tolerance, together with a low cost. Table 9 gives a quick comparison between the most common type of capacitors. Obviously, the capacitor must be SMD type to achieve the extremely low ESR and ESL necessary for this application. Figure 19 illustrates the CRD_VCC ripple observed in the NCN6001 demo board depending upon the type of capacitor used to filter the output voltage.

Table 9. CERAMIC/ELECTROLYTIC CAPACITORS COMPARISON

Manufacturers	Type/Series	Format	Max Value	Tolerance	Typ. Z @ 500 kHz
MURATA	CERAMIC/GRM225	0805	10 μF/6.3 V	−20%/+20%	30 mΩ
MURATA	CERAMIC/GRM225	0805	4.7 μF/6.3 V	−20%/+20%	30 mΩ
VISHAY	Tantalum/594C/593C	−	10 μF/16 V	−	450 mΩ
VISHAY	Electrolytic/94SV	−	10 μF/10 V	−20%/+20%	400 mΩ
−	Electrolytic Low Cost	−	10 μF/10 V	−35%/+50%	2.0 Ω

The DC/DC converter is capable to start with a full load connected to the CRD_VCC output as depicted in Figure 20.

In this example, the converter is fully loaded when the system starts from zero.



Test Conditions: Cout = 2x 4.7 μF/6 V/ceramic X7R,
Temp = +25°C
Iout = Maximum Specification

Figure 19. Typical CRD_VCC Ripple Voltage

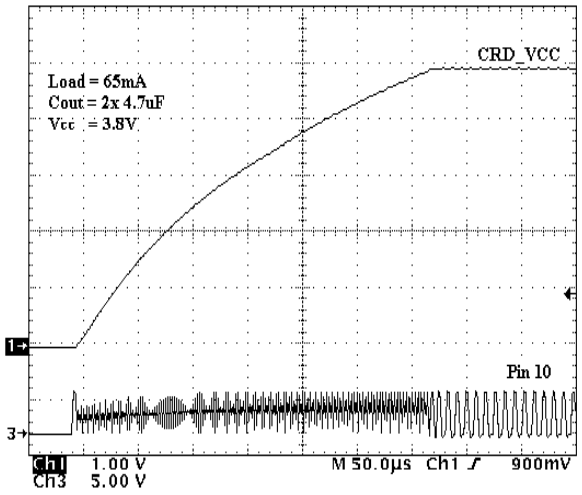
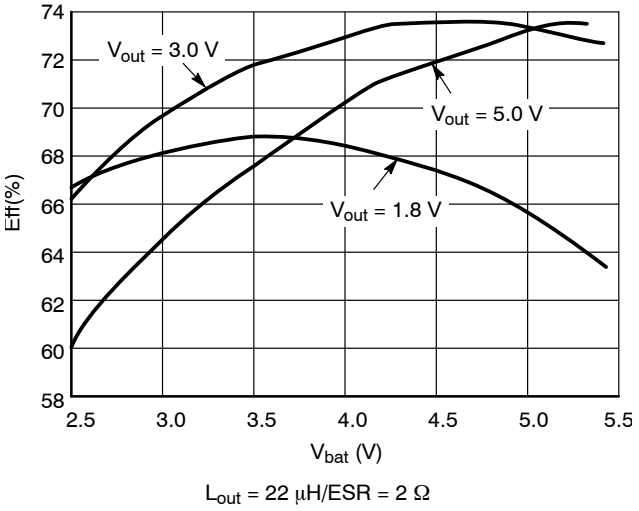


Figure 20. Output Voltage Startup Under Full Load Conditions

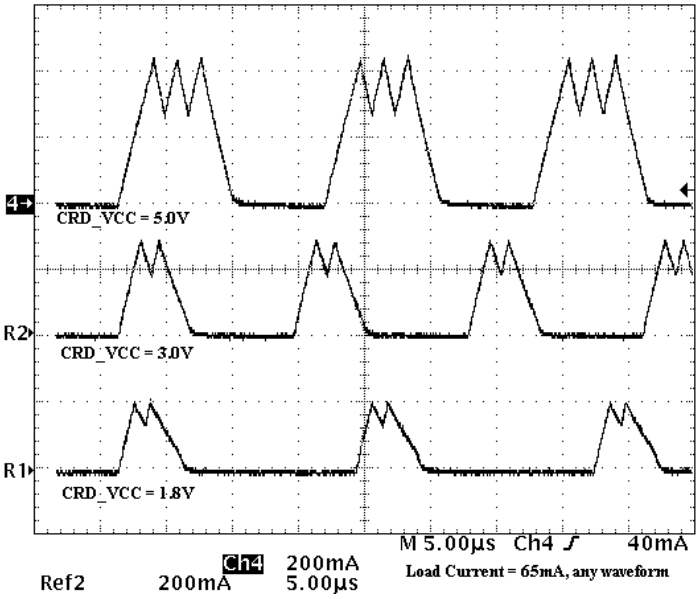


L_{out} = 22 μH/ESR = 2 Ω

Figure 21. CRD_VCC Efficiency as a Function of the Input Supply Voltage

The curves illustrate the typical behavior under full output current load (35 mA, 60 mA and 65 mA), according to EMV specifications.

During the operation, the inductor is subject to high peak current as depicted Figure 22 and the magnetic core must sustain this level of current without damage. In particular, the ferrite material shall not be saturated to avoid uncontrolled current spike during the charge up cycle. Moreover, since the DC/DC efficiency depends upon the losses developed into the active and passive components, selecting a low ESR inductor is preferred to reduce these losses to a minimum.



Test Conditions: Input VCC voltage = 5.0 V
Current = 200 mA/div
Tamb = +20°C

Figure 22. Typical Inductor Current

According to the ISO7816−3 and EMV specifications, the interface shall limits the CRD_VCC output current to 200 mA maximum, under short circuit conditions. The NCN6001 supports such a parameter, the limit being depending upon the input and output voltages as depicted in Figure 23.

On the other hand, the circuit is designed to make sure no over current exist over the full temperature range. As a matter of fact, the output current limit is reduced when the temperature increases: see Figure 24.

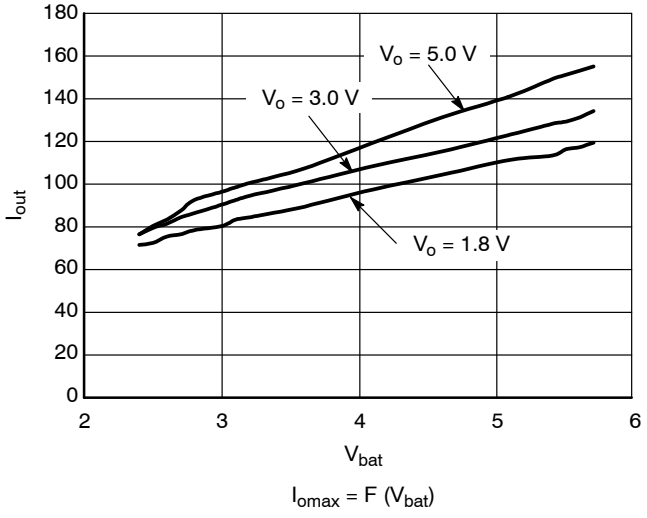


Figure 23. Output Current Limits

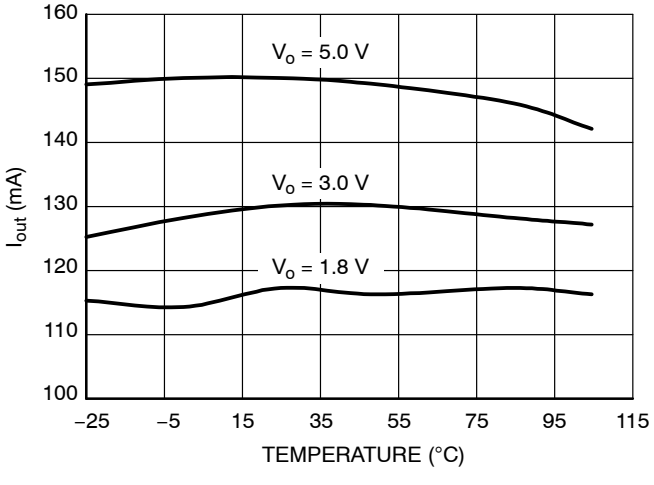


Figure 24. Output Current Limit as a Function of the Temperature

SMART CARD CLOCK DIVIDER

The main purpose of the built−in clock generator is threefold:

1. Adapts the voltage level shifter to cope with the different voltages that might exist between the MPU and the Smart Card.
2. Provides a frequency division to adapt the Smart Card operating frequency from the external clock source.
3. Controls the clock state according to the smart card specification.

In addition, the NCN6001 adjusts the signal coming from the microprocessor to get the Duty Cycle window as defined by the ISO7816−3 specification.

The byte content of the SPI port, B2 & B3, fulfills the programming functions when $\overline{CS}$ is Low as depicted in Figure 26 and Figure 25. The clock input stage (CLK_IN) can handle a 20 MHz frequency maximum signal, the divider being capable to provide a 1:4 ratio. Of course, the ratio must be defined by the engineer to cope with the Smart Card considered in a given application and, in any case, the output clock [CRD_CLK] shall be limited to 20 MHz maximum. In order to minimize the dI/dt and dV/dV developed in the CRD_CLK line, the output stage includes a special function to adapt the slope of the clock signal for different applications. This function is programmed by the MOSI register (Table 2: WRT_REG Bits Definitions and Functions) whatever be the clock division.

In order to avoid any duty cycle out of the smart card ISO7816−3 specification, the divider is synchronized by the last flip flop, thus yielding a constant 50% duty cycle, whatever be the divider ratio (Figure 25). Consequently, the output CRD_CLK frequency division can be delayed by four CLK_IN pulses and the microcontroller software must take this delay into account prior to launch a new data transaction. On the other hand, the output signal Duty Cycle cannot be guaranteed 50% if the division ratio is 1 and if the input Duty Cycle signal is not within the 46–56% range.

The input signals CLK_IN and MOSI/b3 are automatically routed to the level shifter and control block according to the mode of operation.

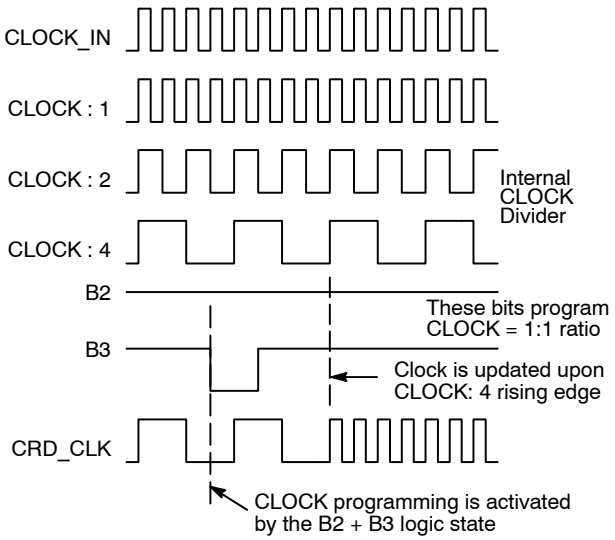


Figure 25. Typical Clock Divider Synchronization

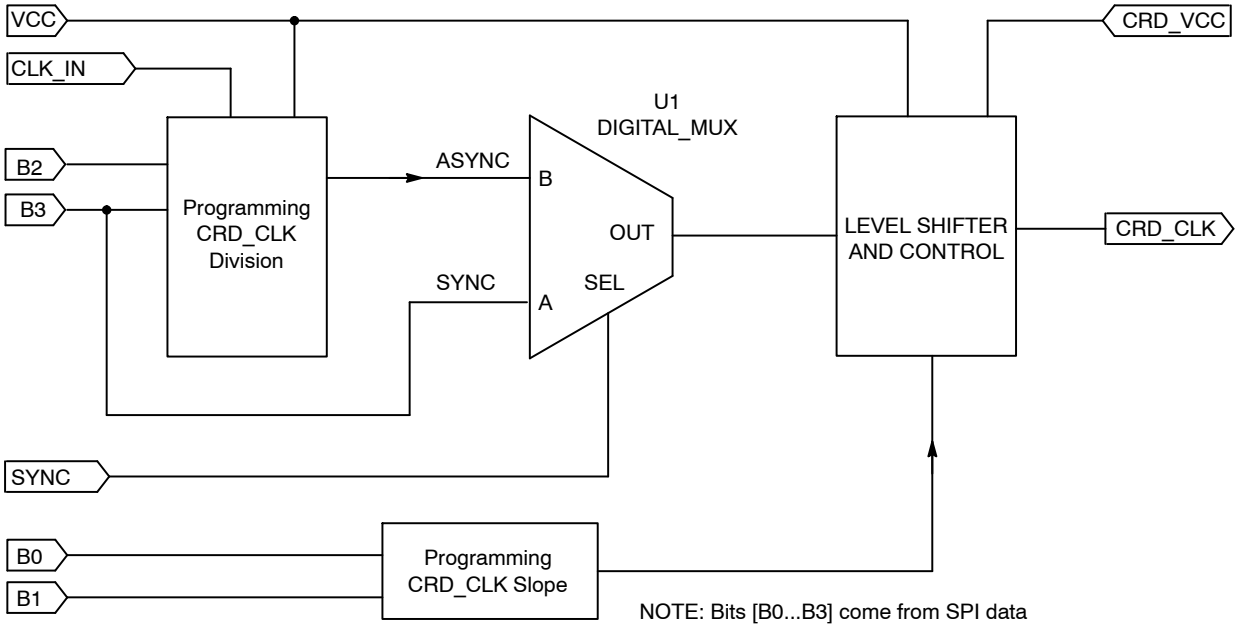


Figure 26. Basic Clock Divider and Level Shifter

The input clock can be divided by 1/1, ½ or ¼, depending upon the specific application, prior to be applied to the smart card driver. On the other hand, the positive and negative going slopes of the output clock (CRD_CLK) can be programmed to optimize the operation of the chip (Table 10). The slope of the output clock can be programmed on the fly, independently of either the CRD_VCC voltage or the operating frequency, but care must be observed as the CRD_RST will reflect the logic state present at MOSI/b4 register.

Table 10. OUTPUT CLOCK RISE AND FALL TIME SELECTION

B0	B1	CRD_CLK Division Ratio	CRD_CLK SLO_SLP	CRD_CLK FST_SLP
0	0	–	Output Clock = Low	Output Clock = Low
0	1	1	10 ns (typ.)	2 ns (typ.)
1	0	1/2	10 ns (typ.)	2 ns (typ.)
1	1	1/4	10 ns (typ.)	2 ns (typ.)

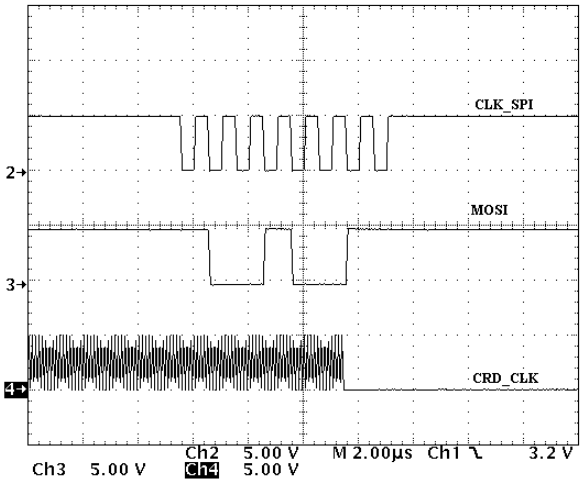


Figure 27. Force CRD_CLK to Low

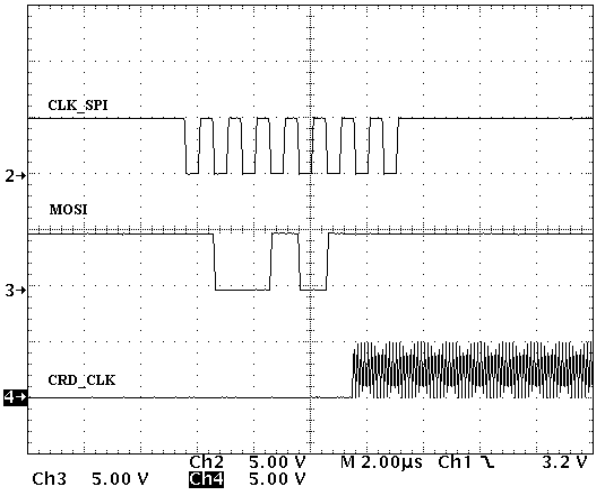


Figure 28. Force CRD_CLK to Active Mode

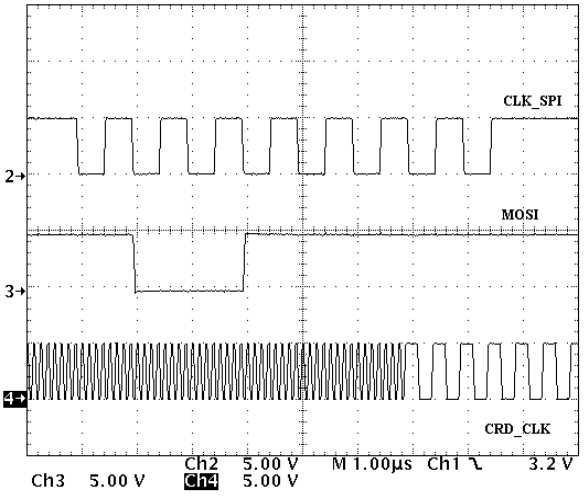
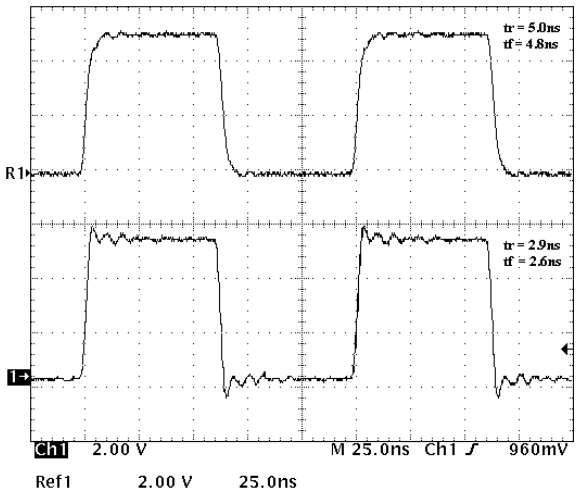


Figure 29. CRD_CLK Programming



Note: Waveforms recorded without external compensation network.

Figure 30. CRD_CLK Operating Low Speed (Top Trace), Full Speed (Bottom Trace)

INPUT SCHMITT TRIGGERS

All the Logic Input pins have built−in Schmitt trigger circuits to protect the NCN6001 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted in Figure 31.

The output signal is guaranteed to go High when the input voltage is above 0.70* V_{CC}, and will go Low when the input voltage is below 0.30* V_{CC}.

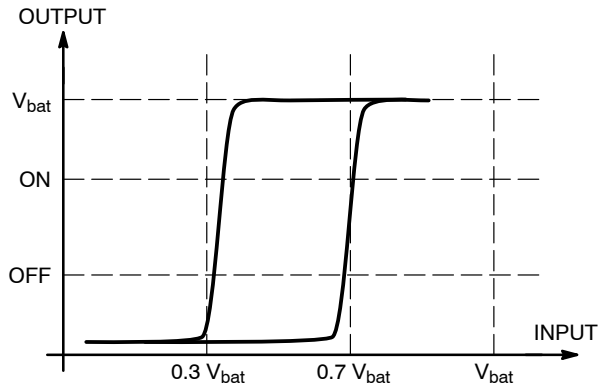


Figure 31. Typical Schmitt Trigger Characteristic

SECURITY FEATURES

In order to protect both the interface and the external smart card, the NCN6001 provides security features to prevent catastrophic failures as depicted hereafter.

Pin Current Limitation: In the case of a short circuit to ground, the current forced by the device is limited to 15 mA for any pins, except CRD_CLK pin. No feedback is provided to the external MPU.

DC/DC Operation: The internal circuit continuously senses the CRD_VCC voltage and, in the case of either over or under voltage situation, updates the READ_REG register accordingly and forces $\overline{INT}$ pin to Low. This register can be read out by the MPU.

Battery Voltage: Both the over and under voltage are detected by the NCN6001, the READ_REG register being updated accordingly. The external MPU can read the register through the MISO pin to take whatever is appropriate to cope with the situation.

ESD PROTECTION

The NCN6001 includes silicon devices to protect the pins against the ESD spikes voltages. To cope with the different ESD voltages developed across these pins, the built−in structures have been designed to handle either 2.0 kV, when related to the microcontroller side, or 8.0 kV when connected with the external contacts. Practically, the CRD_RST, CRD_CLK, CRD_IO, CRD_C4, and CRD_C8 pins can sustain 8.0 kV, the maximum short circuit current being limited to 15 mA. The CRD_VCC pin has the same ESD protection, but can source up to 65 mA continuously, the absolute maximum current being internally limited to 150 mA.

PRINTED CIRCUIT BOARD LAYOUT

Since the NCN6001 carries high speed currents together with high frequency clock, the printed circuit board must be carefully designed to avoid the risk of uncontrolled operation of the interface.

A typical single sided PCB layout is provided in Figure 33 highlighting the ground technique. Dual face printed circuit board may be necessary to solve ringing and cross talk with the rest of the system.

TEST BOARD SCHEMATIC DIAGRAM

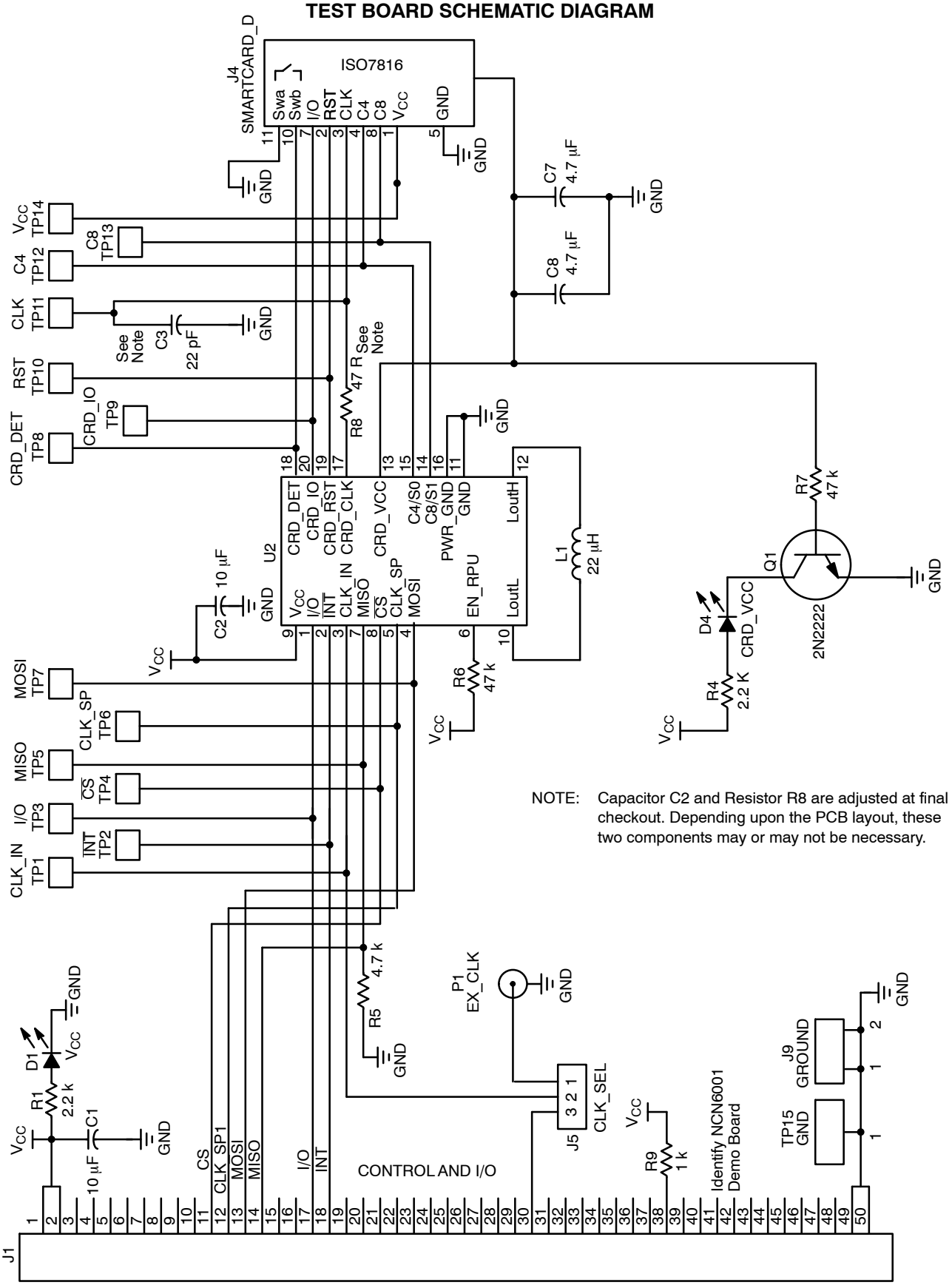
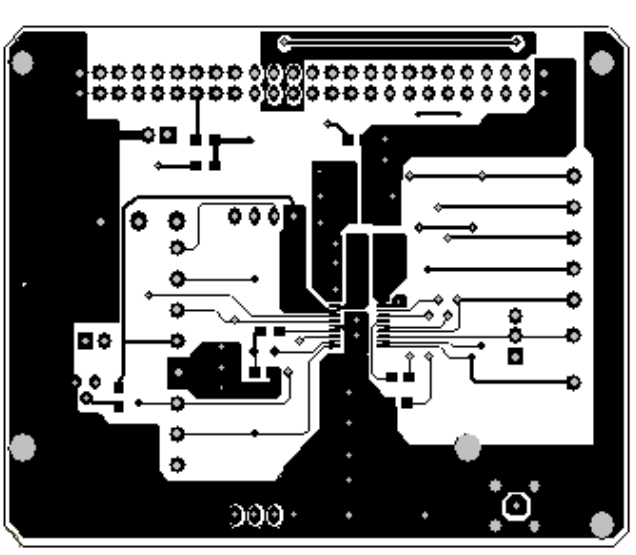
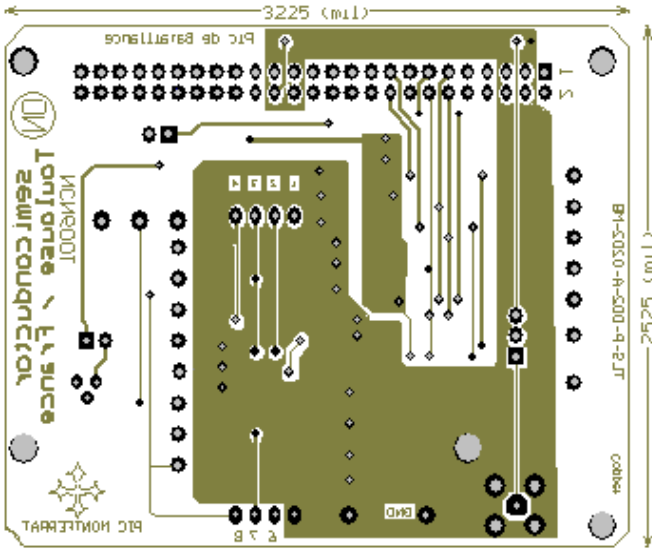


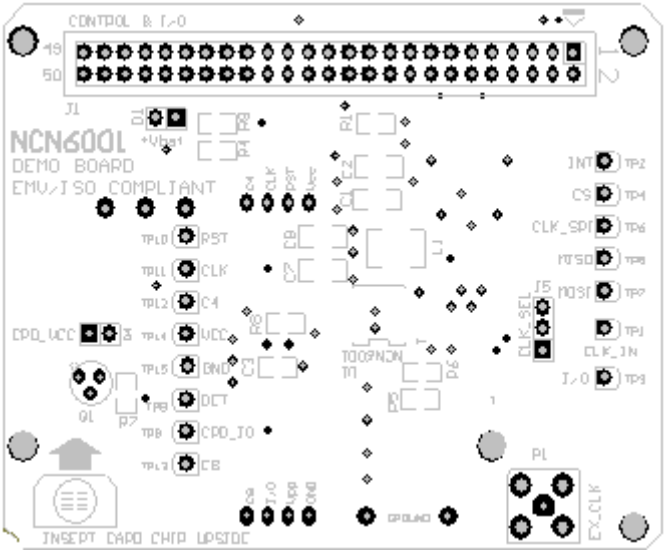
Figure 32. NCN6001 Engineering Test Board Schematic Diagram



Component Side (Top)



Copper Side (Bottom)



Top side

Figure 33. NCN6001 Demo Board Printed Circuit Board Layout

Table 11. DEMO BOARD BILL OF MATERIAL

Desig.	Part Type	Footprint	Description	Supplier	Part Number
C1	10 μF	1206	Capacitor	MURATA	GRM40−X5R−106K6.3
C2	10 μF	1206	Capacitor	MURATA	GRM40−X5R−106K6.3
C3	22 pF	805	Capacitor	MURATA	
C7	4.7 μF	1206	Capacitor	MURATA	GRM40−034X5R−475K6.3
C8	4.7 μF	1206	Capacitor	MURATA	GRM40−034X5R−475K6.3
D1	V_{CC}	SIP2	LED diode	Radio Spares	180−8467
D4	CRD_VCC	SIP2	LED diode	Radio Spares	180−8495
J1	CONTROL & I/O	IDC50		Fujitsu	FCN−704Q050−AU/M
J4	SMARTCARD	SMARTCARD_ISO	Smart Card Connector	FCI	7434−L01−35S01
J5	CLK_SEL	SIP3	Connector		
J9	GROUND	GND_TEST	Connector		
L1	22 μH	1008	Inductor	CoilCraft	1008PS−223−M
P1	EX_CLK	SMB	SMB Connector	Radio Spares	112−2993
Q1	2N2222	TO−18	NPN	ON Semiconductor	
R1	2.2 k	805	Radio Spares		
R4	2.2 k	805	Radio Spares		
R5	4.7 k	805	Radio Spares		
R6	47 k	805	Radio Spares		
R7	47 k	805	Radio Spares		
R8	47 R	805	Radio Spares		
R9	1.0 k	805	Radio Spares		
TP1	CLK_IN	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP10	RST	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP11	CLK	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP12	C4	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP13	C8	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP14	VCC	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP15	GND	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP2	INT	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP3	I/O	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP4	CS	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP5	MISO	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP6	CLK_SPI	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP7	MOSI	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP8	DET	TEST_POINT	TEST_POINT	Radio Spares	203−4910
TP9	CRD_IO	TEST_POINT	TEST_POINT	Radio Spares	203−4910
U1	NCN6001	ON Semiconductor			

13. All resistors are ±5%, ¼ W , unless otherwise noted. All capacitors are ceramic, ±10%, 6.3 V, unless otherwise noted.

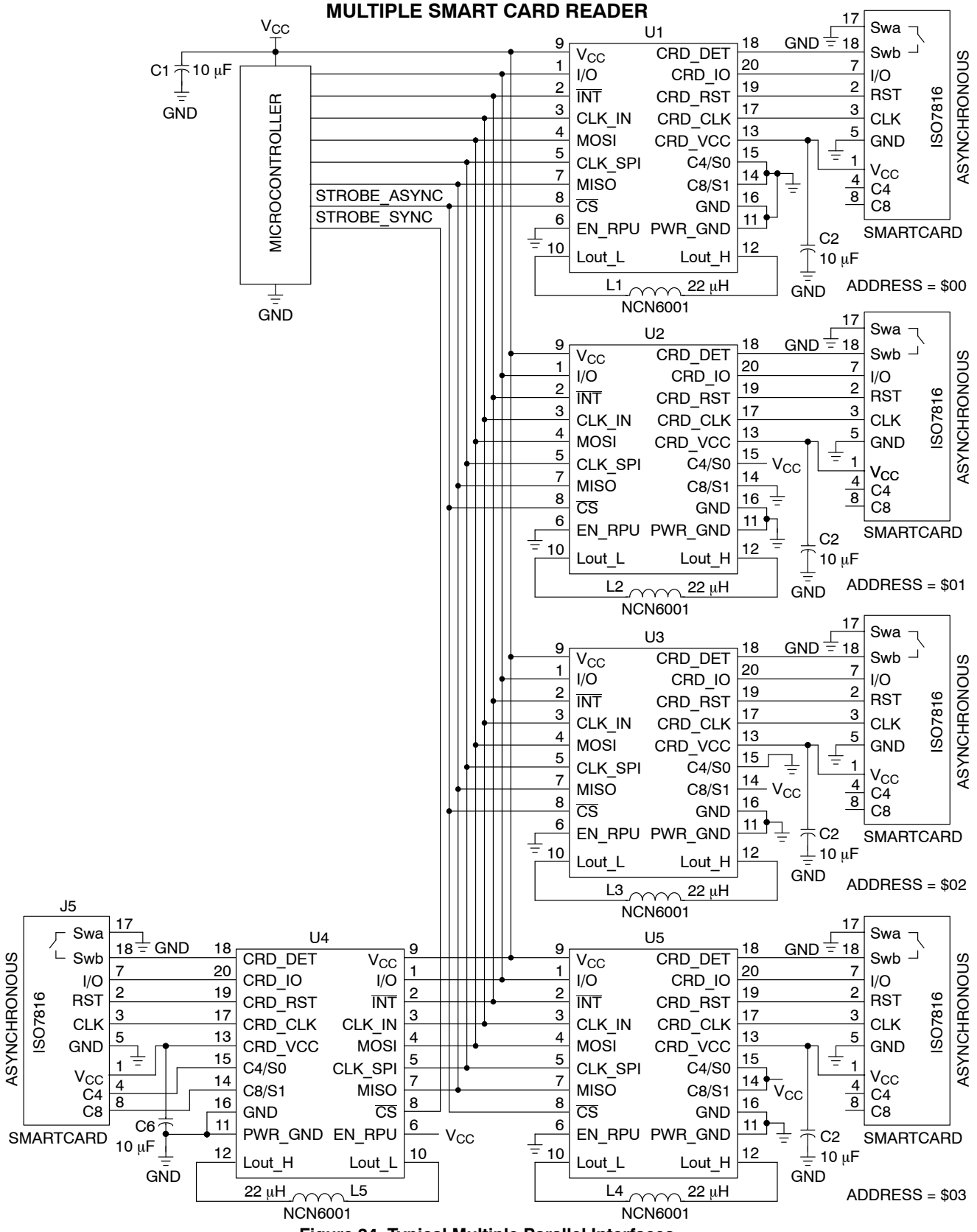


Figure 34. Typical Multiple Parallel Interfaces

The five interfaces share a common microcontroller bus, a bank of four NCN6001 supporting asynchronous card with a dedicated $\overline{CS}$ line, the fifth one being used by to the synchronous or asynchronous transactions with a unique $\overline{CS}$ line. On the other hand, the only activated I/O pullup resistor shall be one of the Asynchronous bank.

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ABBREVIATIONS

Lout_L and Lout_H	DC/DC External Inductor
Cout	Output Capacitor
Class A	5V Smart Card
Class B	3V Smart Card
CRD_C4	Interface IC Card Digital Control
CRD_C8	Interface IC Card Digital Control
CRD_CLK	Interface IC Card Clock Input
CRD_DET	Card Insertion/Extraction Detection
CRD_IO	Interface IC Card Data Link
CRD_RST	Interface IC Card RESET Input
CRD_VCC	Interface IC Card Power Supply Line
CRD_V_{CC}	Card Power Supply Input
Cs	Parasitic Stray Capacitance
$\overline{CS}$	Chip Select
EMV	Europay Master Card Visa
FST_SLP	CRD_CLK Fast Slope (t_r and t_f)
GIE−CB	Groupement Inter Economique − Carte Bancaire
ICC	Current at Card V_{CC} pin
$\overline{INT}$	Interrupt
ISO	International Standards Organization
μC	Microcontroller
MISO	Master In Slave Out: Data from the Interface
MOSI	Master Out Slave In: Data from the External Microcontroller
NC	Normally Close
NO	Normally Open
POR	Power On Reset
RFU	Reserved Future Use
SPI	Serial Port Interface
T0	Smart Card Data Transfer Procedure by Bytes
T1	Smart Card Data Transfer Procedure by Strings
SLO_SLP	CRD_CLK Slow Slope (t_r and t_f)
VCC	MPU Power Supply Voltage

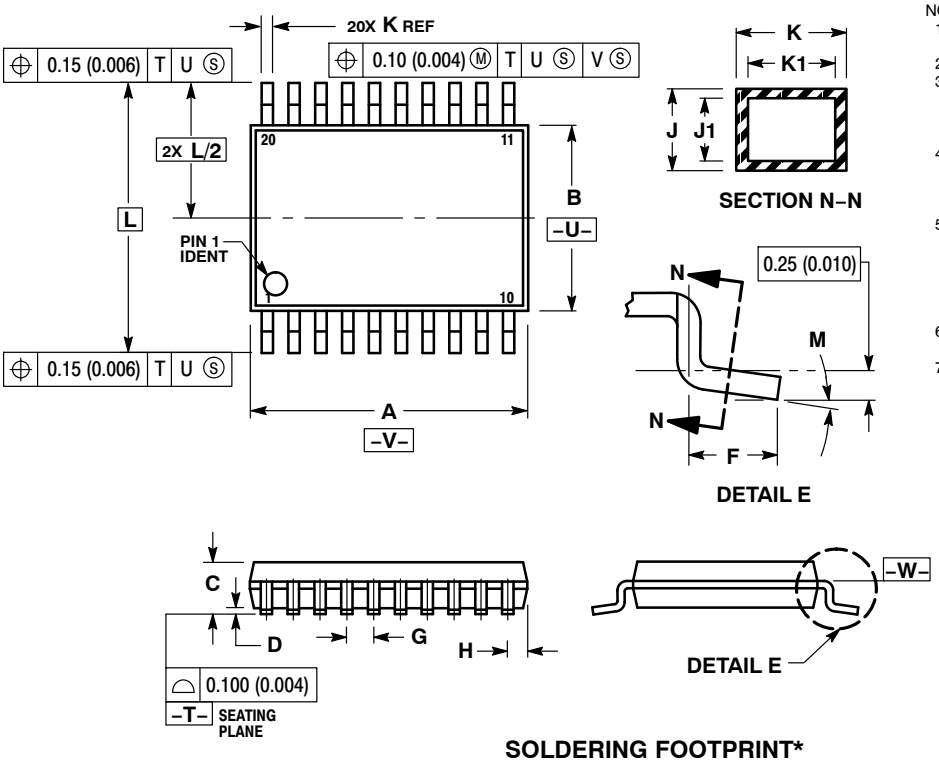
ORDERING INFORMATION

Device	Package	Shipping†
NCN6001DTBR2G	TSSOP−20 (Pb−Free)	2,500 / Tape & Reel
NCN6001MUTWG	LLGA−20 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

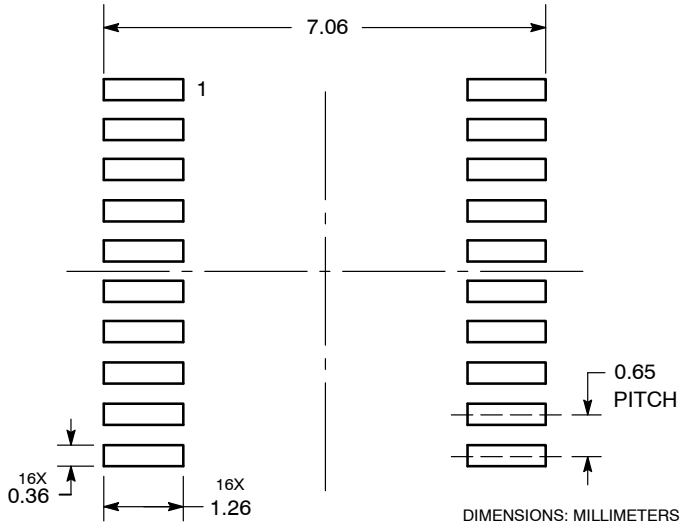
TSSOP−20
CASE 948E−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

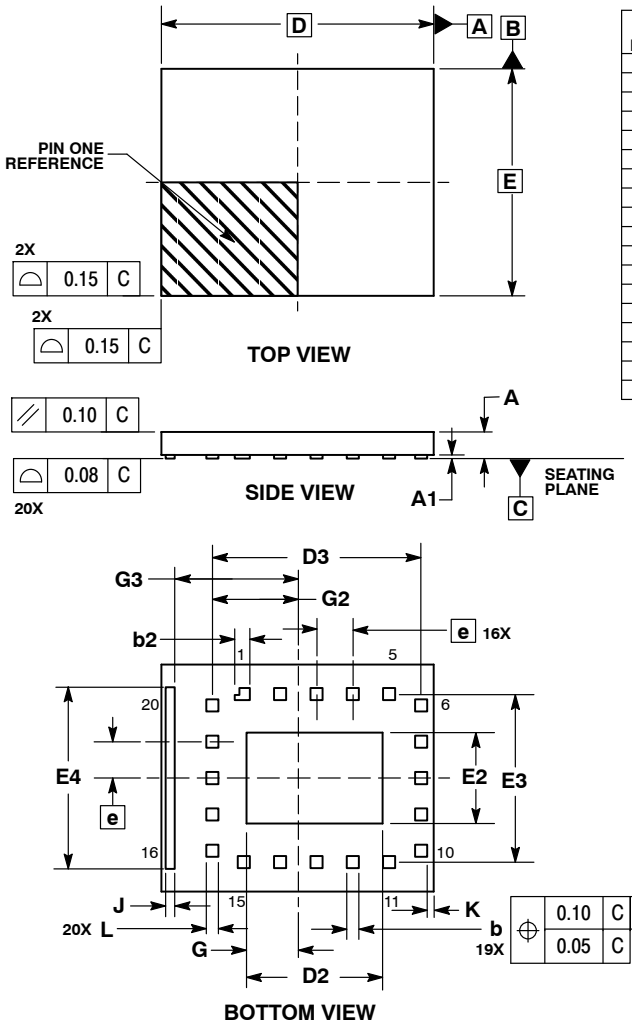
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

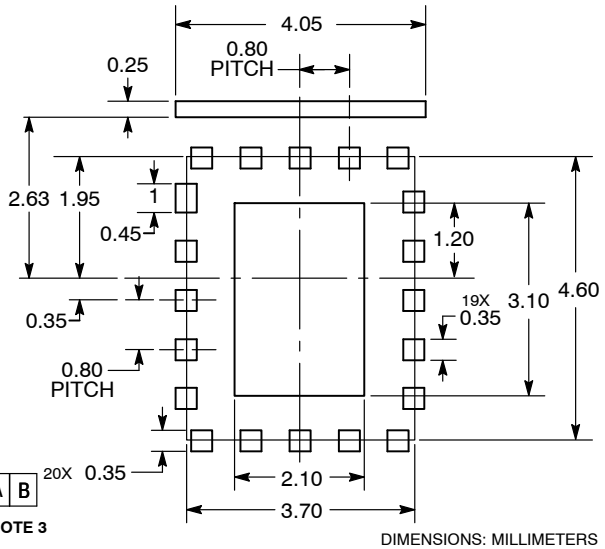
20 PIN LLGA, 6x5, 0.8P
CASE 513AC−01
ISSUE B



DIM	MILLIMETERS MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.25	0.35
b2	0.35	0.45
D	6.00 BSC	
D2	2.90	3.10
D3	4.60 BSC	
E	5.00 BSC	
E2	1.90	2.10
E3	3.70 BSC	
E4	3.90	4.10
e	0.80 BSC	
G	1.05	1.25
G2	1.95 BSC	
G	2.55	2.75
J	0.15	0.25
K	0.10 MIN	
L	0.25	0.35

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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