NTMFD4C87N

Advance Information

PowerPhase, Dual N-Channel SO8FL

30 V, High Side 20 A / Low Side 26 A

ON Semiconductor®

www.onsemi.com

Features

- Co−Packaged Power Stage Solution to Minimize Board Space
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- DC−DC Converters
- System Voltage Rails
- Point of Load

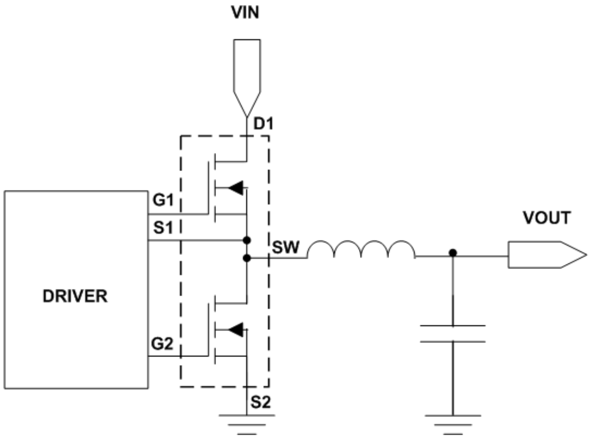


Figure 1. Typical Application Circuit

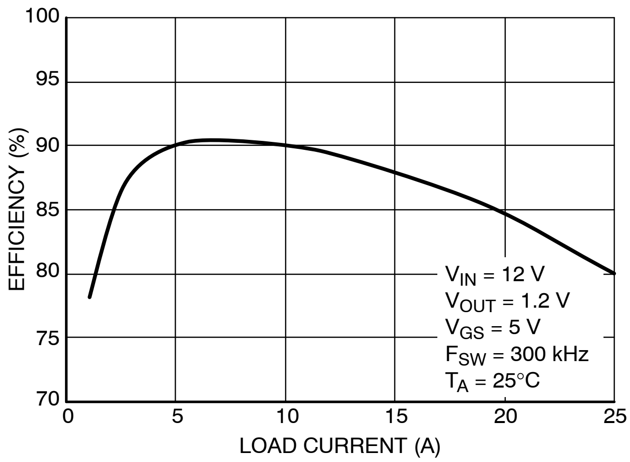
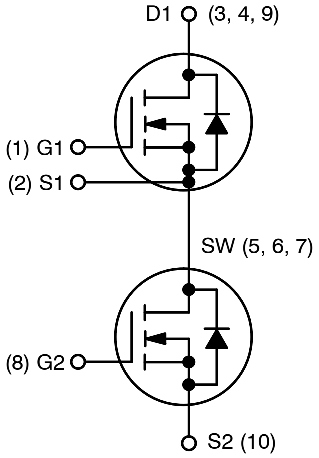


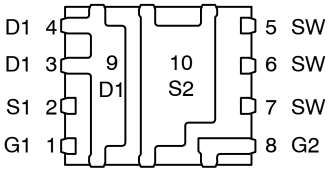
Figure 2. Typical Efficiency Performance POWERPHASEGEVB Evaluation Board

This document contains information on a new product. Specifications and information herein are subject to change without notice.

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
Q1 Top FET 30 V	5.4 mΩ @ 10 V	20 A
	8.1 mΩ @ 4.5 V	
Q2 Bottom FET 30 V	3.1 mΩ @ 10 V	26 A
	4.3 mΩ @ 4.5 V	

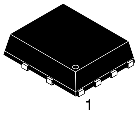


PIN CONNECTIONS

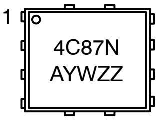


(Bottom View)

MARKING DIAGRAM



DFN8
CASE 506CR



4C87N = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

November, 2014 − Rev. P10

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter				Symbol	Value	Unit
Drain−to−Source Voltage			Q1	V_{DSS}	30	V
Drain−to−Source Voltage			Q2			
Gate−to−Source Voltage			Q1	V_{GS}	±20	V
Gate−to−Source Voltage			Q2			
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	Q1	I_D	15.4	A
		T_A = 85°C			11.1	
		T_A = 25°C	Q2		19.5	
		T_A = 85°C			14.1	
Power Dissipation RθJA (Note 1)		T_A = 25°C	Q1	P_D	1.89	W
			Q2			
Continuous Drain Current $R_{\theta JA} \leq$ 10 s (Note 1)		T_A = 25°C	Q1	I_D	21.0	A
		T_A = 85°C			15.1	
		T_A = 25°C	Q2		26.6	
		T_A = 85°C			19.2	
Power Dissipation $R_{\theta JA} \leq$ 10 s (Note 1)		T_A = 25°C	Q1	P_D	3.51	W
			Q2			
Continuous Drain Current $R_{\theta JA}$ (Note 2)		T_A = 25°C	Q1	I_D	11.7	A
		T_A = 85°C			8.5	
		T_A = 25°C	Q2		14.9	
		T_A = 85°C			10.7	
Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25 °C	Q1	P_D	1.10	W
			Q2			
Pulsed Drain Current		T_A = 25°C t_p = 10 μs	Q1	I_{DM}	160	A
			Q2		260	
Operating Junction and Storage Temperature			Q1	T_J, T_{STG}	−55 to +150	°C
			Q2			
Source Current (Body Diode)			Q1	I_S	10	A
			Q2		10	
Drain to Source DV/DT				dV/dt	6	V/ns
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25C, V_{DD} = 50 V, V_{GS} = 10 V, L = 0.1 mH, R_G = 25 Ω)		I_L = 20 A_{pk}	Q1	EAS	20	mJ
		I_L = 30 A_{pk}	Q2	EAS	45	
Lead Temperature for Soldering Purposes (1/8” from case for 10 s)				T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 sq−in pad, 2 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size of 100 mm^2.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Ambient – Steady State (Note 3)	$R_{\theta JA}$	66.0	°C/W
Junction−to−Ambient – Steady State (Note 4)	$R_{\theta JA}$	113.7	
Junction−to−Ambient – ($t \leq 10$ s) (Note 3)	$R_{\theta JA}$	35.6	

3. Surface−mounted on FR4 board using 1 sq−in pad, 2 oz Cu.
4. Surface−mounted on FR4 board using the minimum recommended pad size of 100 mm^2.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage	Q1	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		30			V
	Q2				30			
Drain−to−Source Breakdown Voltage Temperature Coefficient	Q1	$V_{(BR)DSS} / T_J$				15.8		mV / °C
	Q2					15.3		
Zero Gate Voltage Drain Current	Q1	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1	µA
				T_J = 125°C			10	
	Q2		V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1	
Gate−to−Source Leakage Current	Q1	I_{GSS}	V_{GS} = 0 V, VDS = ±20 V				100	nA
	Q2						100	
ON CHARACTERISTICS (Note 5)								
Gate Threshold Voltage	Q1	$V_{GS(TH)}$	V_{GS} = VDS, I_D = 250 µA		1.3		2.2	V
	Q2				1.3		2.2	
Negative Threshold Temperature Coefficient	Q1	$V_{GS(TH)} / T_J$				5.0		mV / °C
	Q2					5.1		
Drain−to−Source On Resistance	Q1	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 30 A		4.3	5.4	mΩ
			V_{GS} = 4.5 V	I_D = 18 A		6.5	8.1	
	Q2		V_{GS} = 10 V	I_D = 30 A		2.5	3.1	
			V_{GS} = 4.5 V	I_D = 30 A		3.4	4.3	
Forward Transconductance	Q1	g_{FS}	V_{DS} = 1.5 V, I_D = 15 A			TBD		S
	Q2					TBD		
CAPACITANCES								
Input Capacitance	Q1	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 15 V			1252		pF
	Q2					1939		
Output Capacitance	Q1	C_{OSS}				610		
	Q2					1055		
Reverse Capacitance	Q1	C_{RSS}				129		
	Q2					49		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 µs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
CHARGES, CAPACITANCES & GATE RESISTANCE							
Total Gate Charge	Q1	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 30 A		10.9		nC
	Q2				13.8		
Threshold Gate Charge	Q1	$Q_{G(TH)}$			TBD		
	Q2				TBD		
Gate−to−Source Charge	Q1	Q_{GS}			3.4		
	Q2				5.5		
Gate−to−Drain Charge	Q1	Q_{GD}			5.4		
	Q2				3.6		
Total Gate Charge	Q1	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V; I_D = 30 A		22.2		nC
	Q2				30.3		
Gate Resistance	Q1	R_G	T_A = 25°C		1.0		Ω
	Q2				1.0		
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	Q1	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω		8.9		ns
	Q2				10.6		
Rise Time	Q1	t_r			21.2		
	Q2				4.6		
Turn−Off Delay Time	Q1	$t_{d(OFF)}$			15.3		
	Q2				21		
Fall Time	Q1	t_f			4.4		
	Q2				4.9		
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	Q1	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω		6.7		ns
	Q2				8.1		
Rise Time	Q1	t_r			19.5		
	Q2				2.8		
Turn−Off Delay Time	Q1	$t_{d(OFF)}$			20.1		
	Q2				26.2		
Fall Time	Q1	t_f			2.8		
	Q2				3.1		

DRAIN−SOURCE DIODE CHARACTERISTICS

Parameter	FET	Symbol	Test Condition		Min	Typ	Max	Unit
Forward Voltage	Q1	V_{SD}	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.82		V
				T_J = 125°C		1.15		
	Q2		V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.8		
				T_J = 125°C		1.10		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN–SOURCE DIODE CHARACTERISTICS							
Reverse Recovery Time	Q1	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 30 A		29.1		ns
	Q2				40.2		
Charge Time	Q1	ta			14.2		
	Q2				19.5		
Discharge Time	Q1	tb			14.6		
	Q2				20.6		
Reverse Recovery Charge	Q1	Q_{RR}			21		nC
	Q2				39		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS – Q1

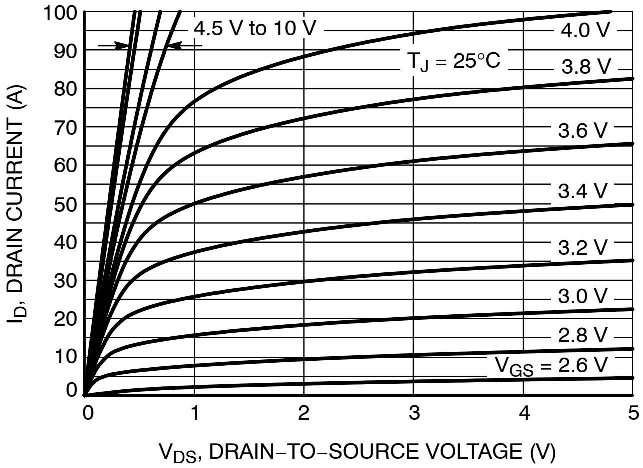


Figure 3. On–Region Characteristics

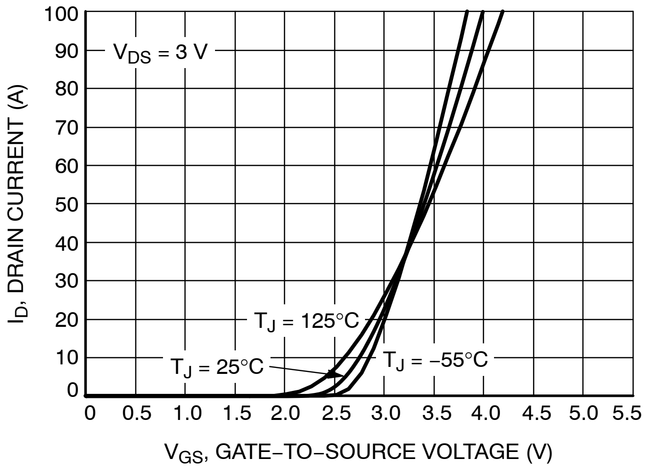


Figure 4. Transfer Characteristics

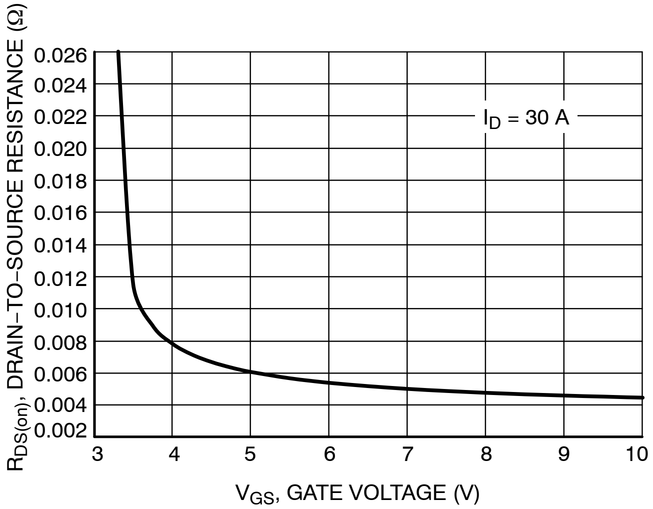


Figure 5. On–Resistance vs. Gate–to–Source Voltage

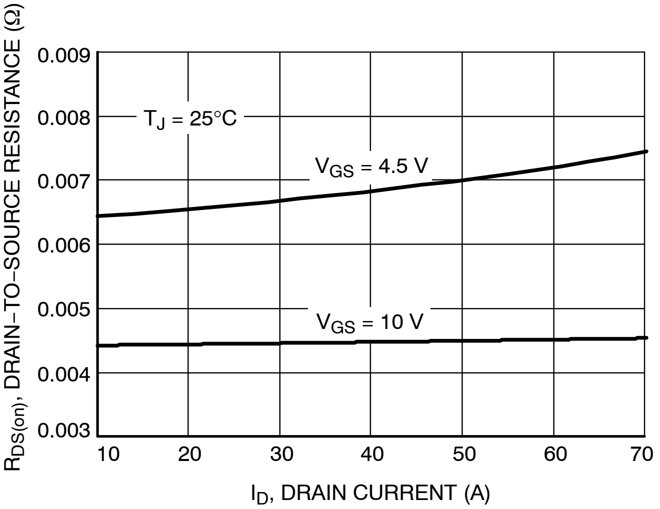


Figure 6. On–Resistance vs. Drain Current and Gate Voltage

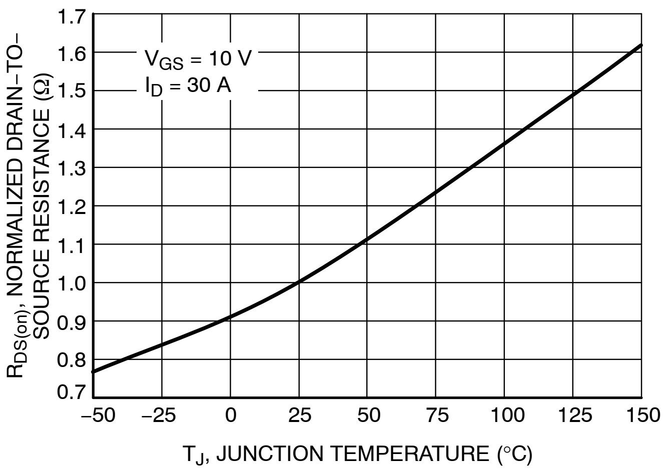


Figure 7. On–Resistance Variation with Temperature

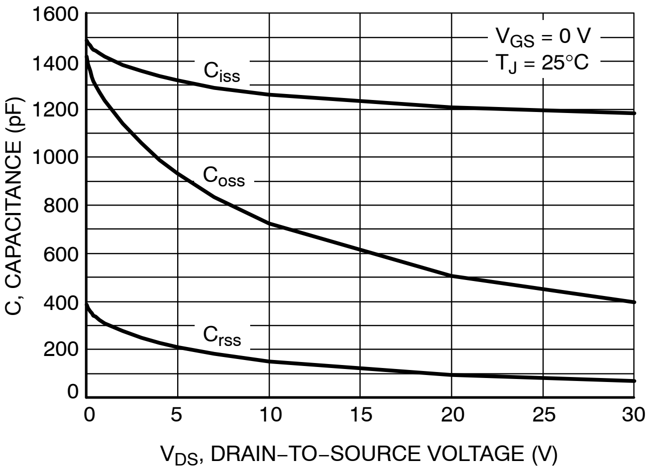


Figure 8. Capacitance Variation

TYPICAL CHARACTERISTICS – Q1

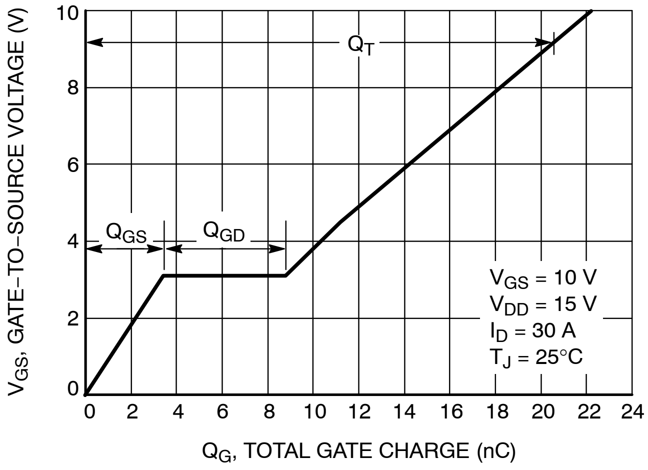


Figure 9. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge

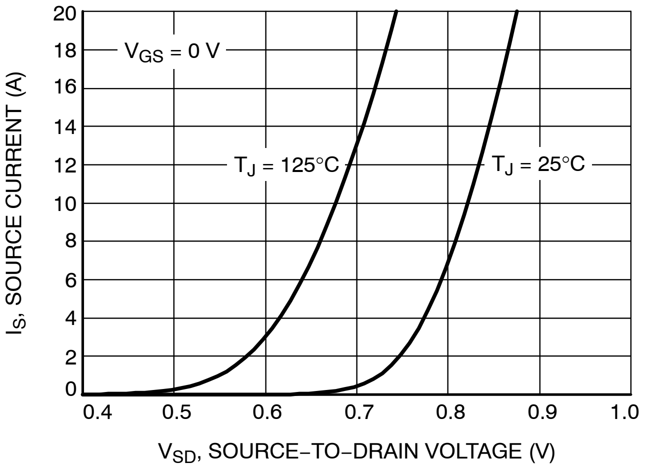


Figure 10. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS – Q2

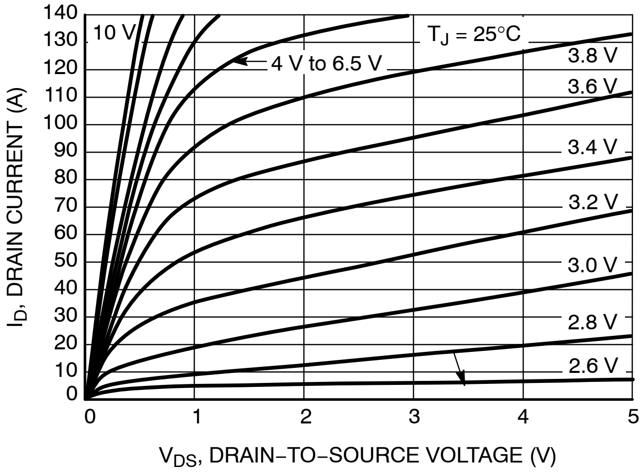


Figure 11. On–Region Characteristics

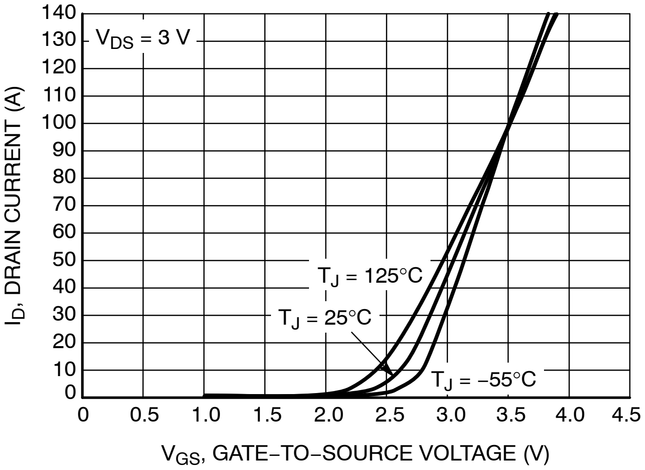


Figure 12. Transfer Characteristics

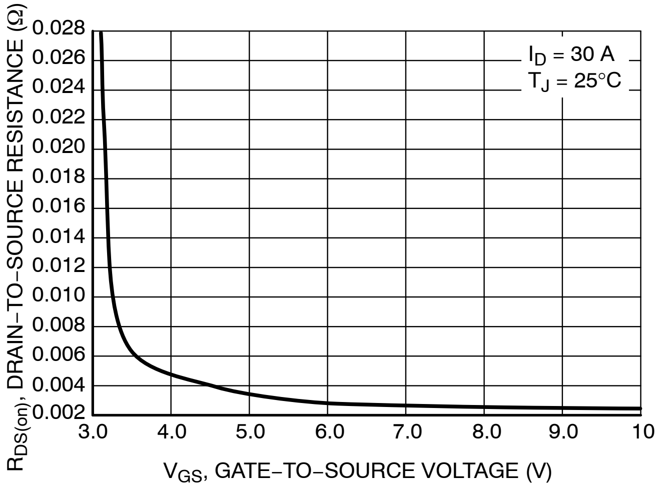


Figure 13. On–Resistance vs. V_{GS}

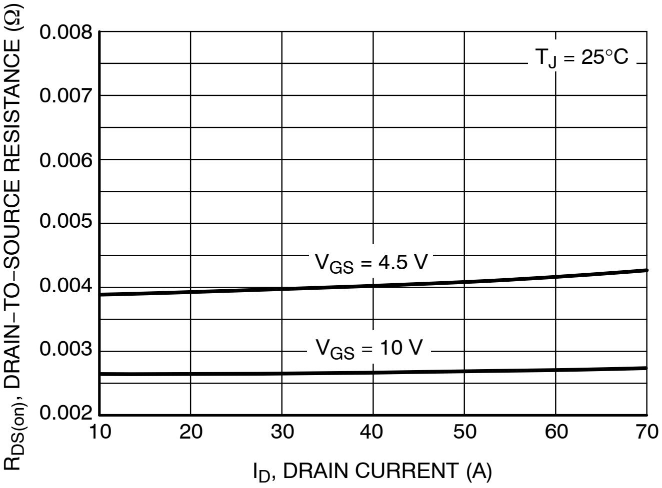


Figure 14. On–Resistance vs. Drain Current and Gate Voltage

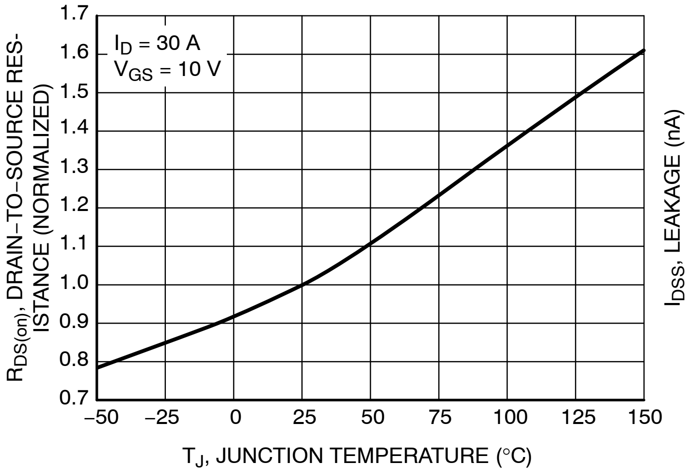


Figure 15. On–Resistance Variation with Temperature

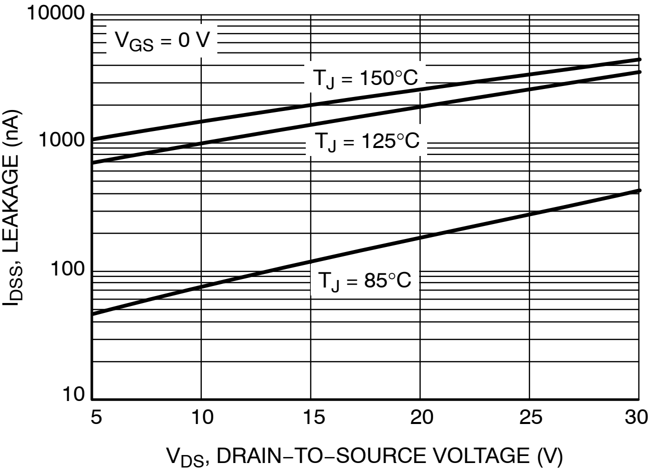


Figure 16. Drain–to–Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – Q2

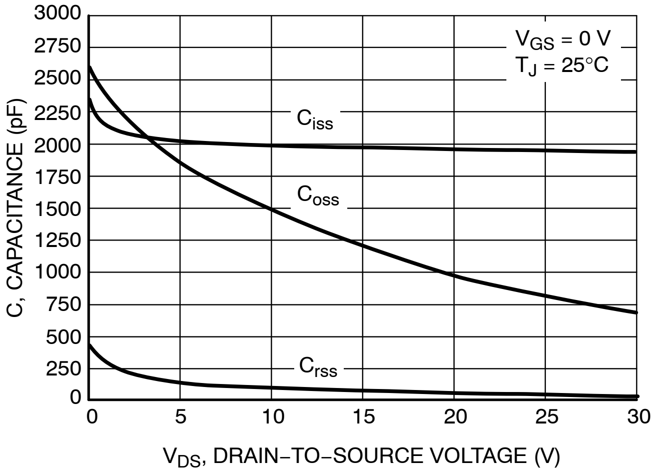


Figure 17. Capacitance Variation

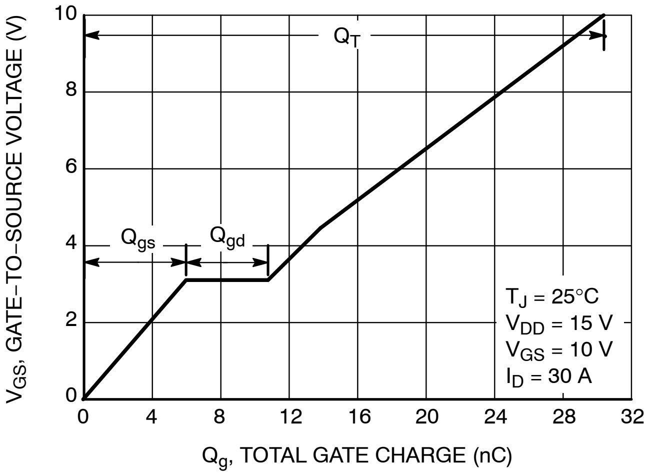


Figure 18. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge

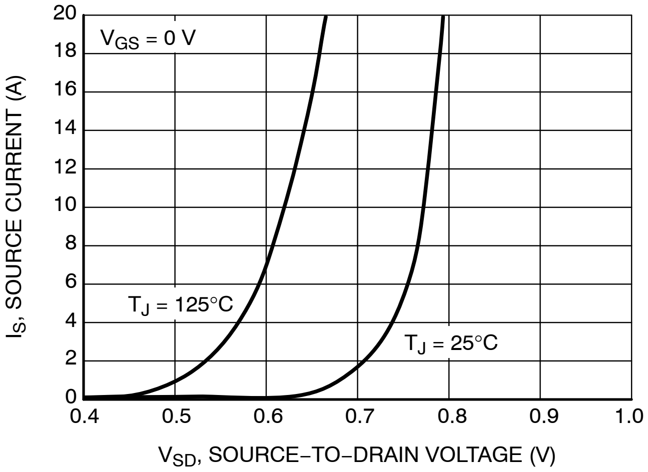


Figure 19. Diode Forward Voltage vs. Current

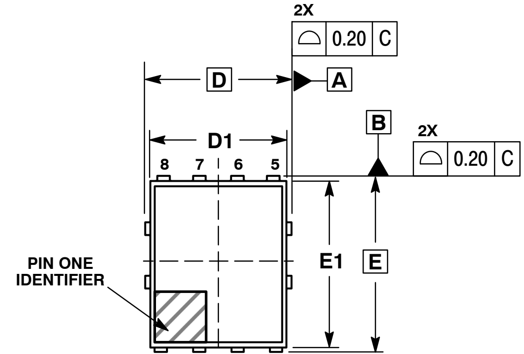
ORDERING INFORMATION

Device	Package	Shipping†
NTMFD4C87NT1G	DFN8 (Pb–Free)	1500 / Tape & Reel
NTMFD4C87NT3G	DFN8 (Pb–Free)	5000 / Tape & Reel

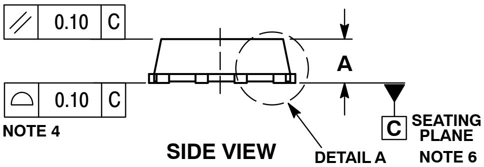
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

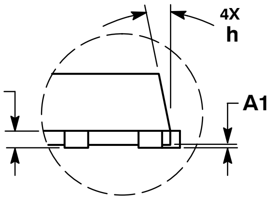
DFN8 5x6, 1.27P PowerPhase FET
CASE 506CR
ISSUE A



TOP VIEW



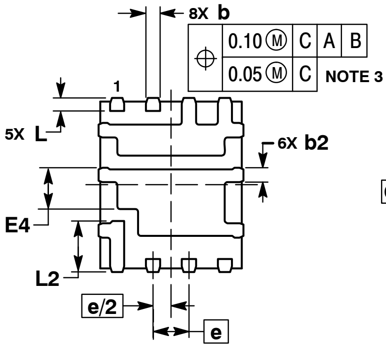
SIDE VIEW



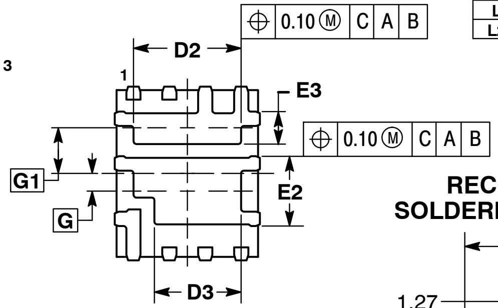
DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND b1 APPLY TO PLATED TERMINAL AND ARE MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	1.35	1.55
A1	0.00	0.05
b	0.40	0.60
b2	0.40	0.60
c	0.20	0.30
D	5.15 BSC	
D1	4.90	5.10
D2	3.70	3.90
D3	2.96	3.16
E	6.15 BSC	
E1	5.80	6.00
E2	2.37	2.57
E3	1.05	1.25
E4	1.36	1.56
e	1.27 BSC	
G	0.625 BSC	
G1	1.615 BSC	
h	---	12 °
L	0.34	0.59
L2	1.68	1.93

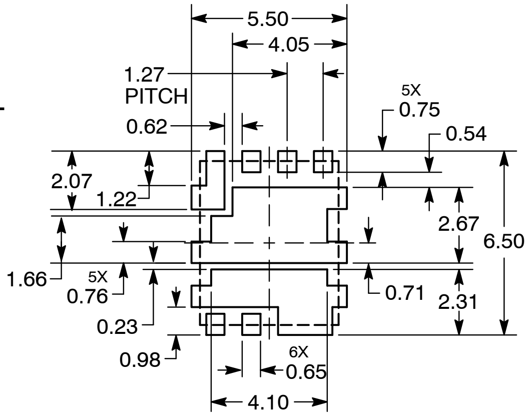


BOTTOM VIEW



SUPPLEMENTAL BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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