

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## **1. Overview**

### **1.1 Features**

The M16C/6C Group microcomputer (MCU) incorporates the M16C/60 Series CPU core and flash memory, employing sophisticated instructions for a high level of efficiency. This MCU has 1 MB of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

This MCU consumes little power, and supports operating modes that allow additional power control. The MCU also uses an anti-noise configuration to reduce emissions of electromagnetic noise and is designed to withstand electromagnetic interference (EMI). By integrating many of the peripheral functions, including the multifunction timer and serial interface, the number of system components has been reduced.

#### **1.1.1 Applications**

This MCU can be used in Peripherals (USB applicable), audio components, cameras, televisions, household appliances, office equipment, communication devices, mobile devices, industrial equipment, and other applications.

## 1.2 Specifications

Table 1.1 to Table 1.2 list specifications.

**Table 1.1 Specifications (1/2)**

Item	Function	Description
CPU	Central processing unit	Core ((multiplier: 16-bit × 16-bit → 32-bit, multiply and accumulate instruction: 16-bit × 16-bit + 32-bit → 32-bit)) <ul style="list-style-type: none"> <li>• Number of basic instructions: 91</li> <li>• Minimum instruction execution time: 31.25 ns (f(BCLK) = 32 MHz, VCC1 = VCC2 = 2.7 to 5.5 V)</li> <li>• Operating modes: Single-chip, memory expansion, and microprocessor</li> </ul>
Memory	ROM, RAM, data flash	See "Refer to Table 1.3 "Product List" ."
Voltage Detection	Voltage detector	<ul style="list-style-type: none"> <li>• Power-on reset</li> <li>• 3 voltage detection points (detection level of voltage detection 0 selectable)</li> </ul>
Clock	Clock generator	<ul style="list-style-type: none"> <li>• 5 circuits: Main clock, sub clock, low-speed on-chip oscillator (125 kHz), high-speed on-chip oscillator (40 MHz ± 10%), PLL frequency synthesizer</li> <li>• Oscillation stop detection: Main clock oscillation stop/reoscillation detection function</li> <li>• Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, and 16</li> <li>• Power saving features: Wait mode, stop mode</li> <li>• Real-time clock</li> </ul>
External Bus Expansion	Bus memory expansion	<ul style="list-style-type: none"> <li>• Address space: 1 MB</li> <li>• External bus interface: 0 to 3 wait states, 4 chip select outputs, 3 V and 5 V interfaces</li> <li>• Bus format: Separate bus or multiplexed bus selectable, data bus width (8 bits), number of address buses(12, 16, or 20)</li> </ul>
I/O Ports	Programmable I/O ports	<ul style="list-style-type: none"> <li>• CMOS I/O ports: 85 (selectable pull-up resistors)</li> <li>• N-channel open drain ports: 3</li> </ul>
Interrupts		<ul style="list-style-type: none"> <li>• Interrupt vectors: 70</li> <li>• External interrupt inputs: 13 (<math>\overline{\text{NMI}}</math>, <math>\overline{\text{INT}} \times 8</math>, key input × 4)</li> <li>• Interrupt priority levels: 7</li> </ul>
Watchdog Timer		15-bit timer × 1 (with prescaler) Automatic reset start function selectable
DMA	DMAC	<ul style="list-style-type: none"> <li>• 4 channels, cycle steal mode</li> <li>• Trigger sources:55</li> <li>• Transfer modes: 2 (single transfer, repeat transfer)</li> </ul>

**Table 1.2 Specifications (2/2)**

Item	Function	Description
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode Event counter two-phase pulse signal processing (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Three-phase motor control timer functions	<ul style="list-style-type: none"> <li>• Three-phase inverter control (timer A1, timer A2, timer A4, timer B2)</li> <li>• On-chip dead time timer</li> </ul>
	Real-time clock	• Count: second, minute, hour, day of the week
	Timer S (Input capture/output compare)	<ul style="list-style-type: none"> <li>• Input base timer: 16 bits X 1</li> <li>• I/O: 8 channels</li> <li>• Time measurement register, Waveform generation register: 16 bits X 8</li> </ul>
Serial Interface	UART0 to UART5	Clock synchronous/asynchronous × 6 channels I <sup>2</sup> C-bus, IEBus <sup>(1)</sup> , Special mode 2, SIM (UART2)
Multi-master I <sup>2</sup> C-bus Interface		1 channel
USB Functions		<ul style="list-style-type: none"> <li>• Full speed (12 Mbps, USB 2.0 compliant)</li> <li>• Transfer type: Control IN/OUT, Bulk IN X 2, Bulk OUT X 2, Interrupt IN X 2</li> <li>• FIFO size: 584 bytes <ul style="list-style-type: none"> <li>• Setup 8 bytes</li> <li>• Control IN 16 bytes</li> <li>• Control OUT 16 bytes</li> <li>• Interrupt IN 16 bytes: 2 channels</li> <li>• Bulk IN 64 bytes X 2: 2 channels</li> <li>• Bulk OUT 64 bytes X 2: 2 channels</li> </ul> </li> </ul>
A/D Converter		10-bit resolution × 26 channels (2 circuits), including sample and hold function Conversion time: 1.72 μs
D/A Converter		8-bit resolution × 2 circuits
CRC Calculator		CRC-CCITT ( $X^{16} + X^{12} + X^5 + 1$ ), CRC-16 ( $X^{16} + X^{15} + X^2 + 1$ ) compliant
Flash Memory		<ul style="list-style-type: none"> <li>• Program/erase power supply voltage: 2.7 to 5.5 V</li> <li>• Program/erase cycles: 1,000 times (program ROM 1, program ROM 2), or 10,000 times (data flash)</li> <li>• Program security: ROM code protect, ID code check</li> </ul>
Debug Functions		On-chip debug, on-board flash rewrite, address match interrupt × 4
Operation Frequency/Supply Voltage		32 MHz/VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1
Current Consumption		27 mA (32 MHz/VCC1 = VCC2 = 3 V) 2.0 μA(VCC1 = VCC2 = 3 V (in stop mode))
Operating Temperature		-20°C to 85°C, -40°C to 85°C <sup>(2)</sup> ,
Package		100-pin QFP: PRQP0100JD-B (Previous package code: 100P6F-A) 100-pin LQFP: PLQP0100KB-A (Previous package code: 100P6Q-A)

## Notes:

1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Refer to Table 1.2 "Specifications (2/2)" and Table 1.3 "Product List" regarding operating temperature.

### 1.3 Product List

Table 1.3 lists product information. Figure 1.1 shows the Part No. with Memory Size and Package, and Figure 1.2 shows the Marking Diagram (Top View).

**Table 1.3 Product List**

Part No.	ROM Capacity			RAM Capacity	Package Code	Remarks
	Program ROM 1	Program ROM 2	Data flash			
R5F36CAMNFA (P)	512KB	16KB	4KB x2 blocks	31KB	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F36CAMNFB (D)					PLQP0100KB-A	
R5F36CAMDFA (P)	512KB	16KB	4KB x2 blocks	31KB	PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F36CAMDFB (D)					PLQP0100KB-A	
R5F36CAKNFA (P)	384KB	16KB	4KB x2 blocks	31KB	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F36CAKNFB (P)					PLQP0100KB-A	
R5F36CAKDFA (P)	384KB	16KB	4KB x2 blocks	31KB	PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F36CAKDFB (P)					PLQP0100KB-A	
R5F36CAENFA (P)	256KB	16KB	4KB x2 blocks	20KB	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F36CAENFB (P)					PLQP0100KB-A	
R5F36CAEDFA (P)	256KB	16KB	4KB x2 blocks	20KB	PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F36CAEDFB (P)					PLQP0100KB-A	
R5F36CA6NFA (P)	128KB	16KB	4KB x2 blocks	12KB	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F36CA6NFB (P)					PLQP0100KB-A	
R5F36CA6DFA (P)	128KB	16KB	4KB x2 blocks	12KB	PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F36CA6DFB (P)					PLQP0100KB-A	

(D): Under development

(P): Planning

Note:

1. Previous package codes are as follows:  
PRQP0100JD-B: 100P6F-A  
PLQP0100KB-A: 100P6Q-A

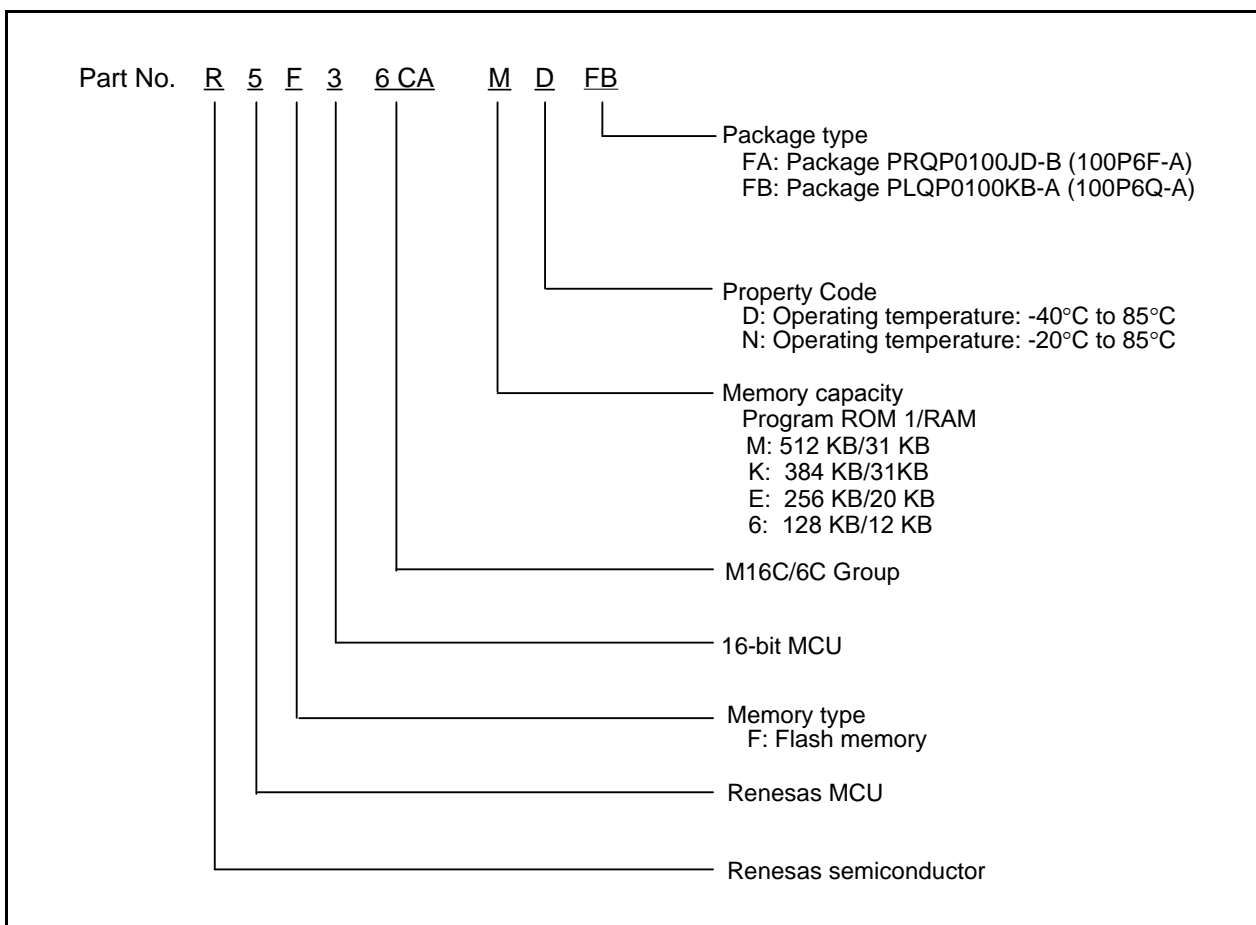


Figure 1.1 Part No. with Memory Size and Package

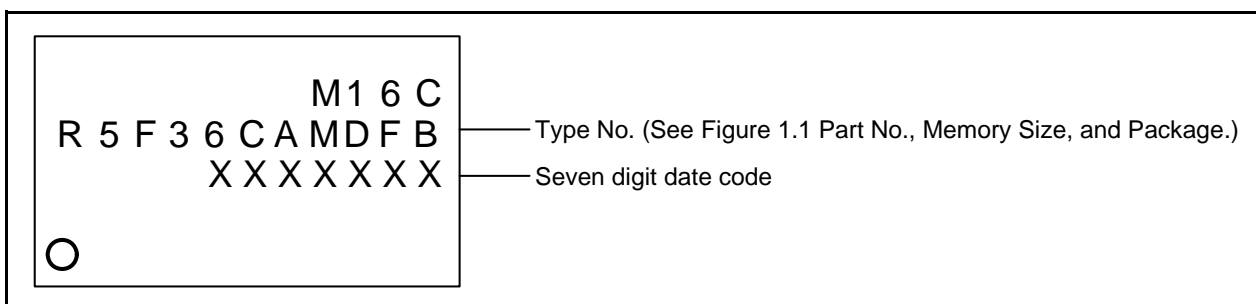


Figure 1.2 Marking Diagram (Top View)

### 1.4 Block Diagram

Figure 1.3 shows block diagrams.

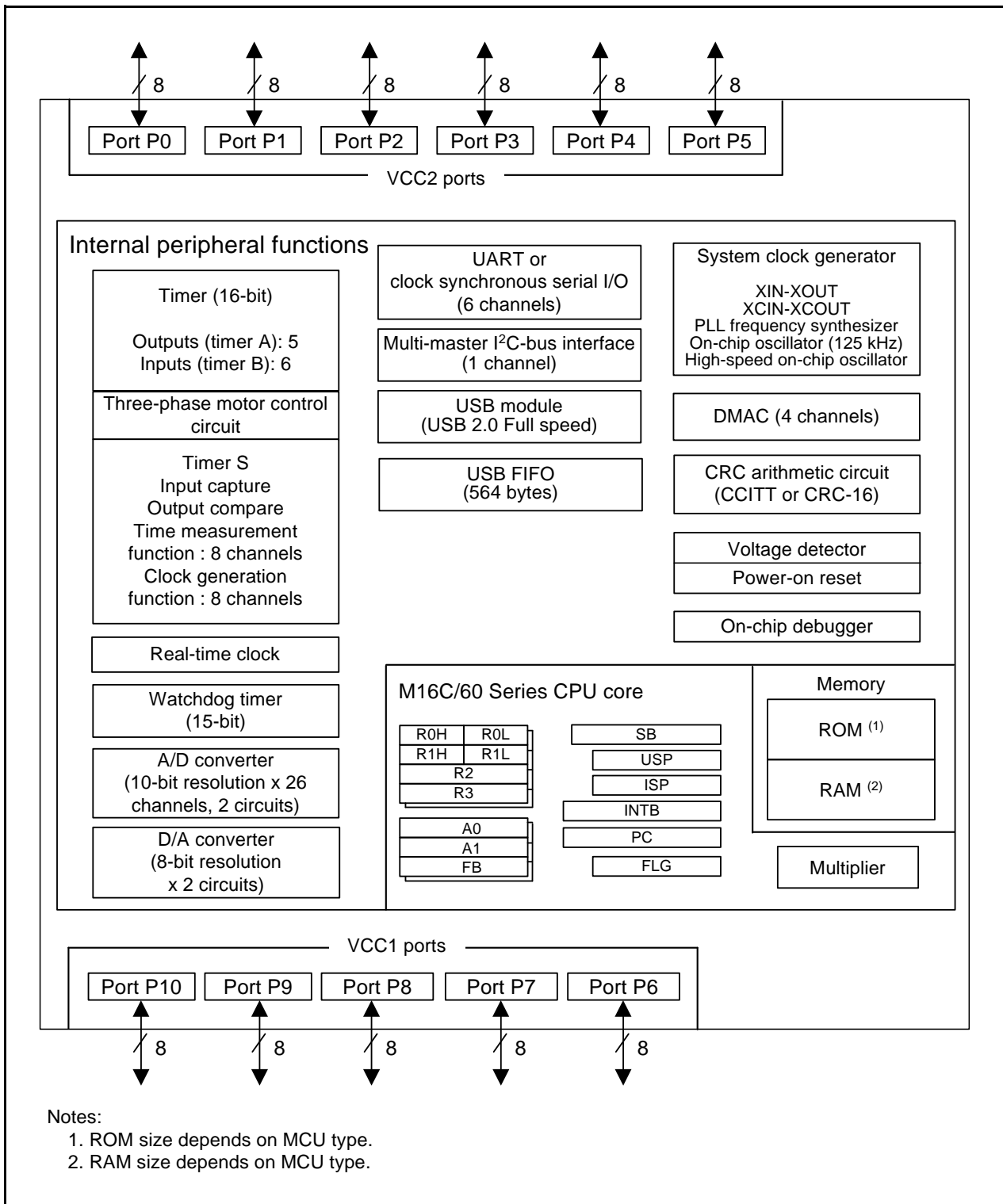


Figure 1.3 Block Diagram



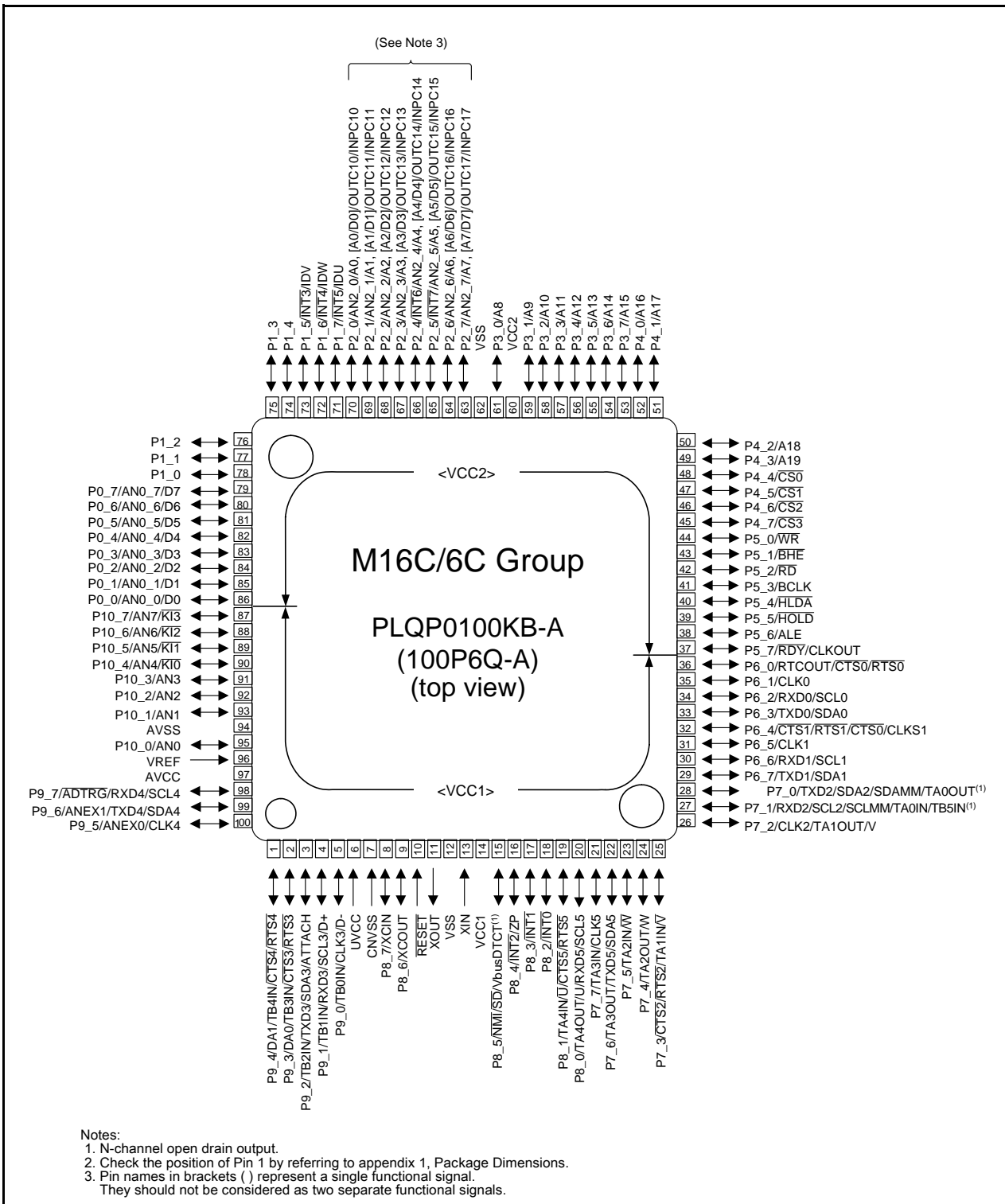


Figure 1.5 Pin Assignment

Table 1.4 Pin Names (1/2)

Pin No.		Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
FA	FB			Interrupt	Timer	Serial interface, USB	A/D converter, D/A converter	
1	99		P9_6			TXD4/SDA4	ANEX1	
2	100		P9_5			CLK4	ANEX0	
3	1		P9_4		TB4IN	CTS4/RTS4	DA1	
4	2		P9_3		TB3IN	CTS3/RTS3	DA0	
5	3		P9_2		TB2IN	TXD3/SDA3/ATTACH		
6	4		P9_1		TB1IN	RXD3/SCL3/D+		
7	5		P9_0		TB0IN	CLK3/D-		
8	6					UVCC		
9	7	CNVSS						
10	8	XCIN	P8_7					
11	9	XCOUT	P8_6					
12	10	RESET						
13	11	XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	NMI	SD	VbusDTCT		
18	16		P8_4	INT2	ZP			
19	17		P8_3	INT1				
20	18		P8_2	INT0				
21	19		P8_1		TA4IN/U	CTS5/RTS5		
22	20		P8_0		TA4OUT/U	RXD5/SCL5		
23	21		P7_7		TA3IN	CLK5		
24	22		P7_6		TA3OUT	TXD5/SDA5		
25	23		P7_5		TA2IN/W			
26	24		P7_4		TA2OUT/W			
27	25		P7_3		TA1IN/V	CTS2/RTS2		
28	26		P7_2		TA1OUT/V	CLK2		
29	27		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM		
30	28		P7_0		TA0OUT	TXD2/SDA2/SDAMM		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		P6_4			CTS1/RTS1/CTS0/ CLKS1		
35	33		P6_3			TXD0/SDA0		
36	34		P6_2			RXD0/SCL0		
37	35		P6_1			CLK0		
38	36		P6_0		RTCOUT	CTS0/RTS0		
39	37		P5_7					RDY/CLKOUT
40	38		P5_6					ALE
41	39		P5_5					HOLD
42	40		P5_4					HLDA
43	41		P5_3					BCLK
44	42		P5_2					RD
45	43		P5_1					BHE
46	44		P5_0					WR
47	45		P4_7					CS3
48	46		P4_6					CS2
49	47		P4_5					CS1
50	48		P4_4					CS0

**Table 1.5 Pin Names (2/2)**

Pin No.		Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
FA	FB			Interrupt	Timer	Serial interface, USB	A/D converter, D/A converter	
51	49		P4_3					A19
52	50		P4_2					A18
53	51		P4_1					A17
54	52		P4_0					A16
55	53		P3_7					A15
56	54		P3_6					A14
57	55		P3_5					A13
58	56		P3_4					A12
59	57		P3_3					A11
60	58		P3_2					A10
61	59		P3_1					A9
62	60	VCC2						
63	61		P3_0					A8
64	62	VSS						
65	63		P2_7		OUTC17/ INPC17		AN2_7	A7, [A7/D7]
66	64		P2_6		OUTC16/ INPC16		AN2_6	A6, [A6/D6]
67	65		P2_5	INT7	OUTC15/ INPC15		AN2_5	A5, [A5/D5]
68	66		P2_4	INT6	OUTC14/ INPC14		AN2_4	A4, [A4/D4]
69	67		P2_3		OUTC13/ INPC13		AN2_3	A3, [A3/D3]
70	68		P2_2		OUTC12/ INPC12		AN2_2	A2, [A2/D2]
71	69		P2_1		OUTC11/ INPC11		AN2_1	A1, [A1/D1]
72	70		P2_0		OUTC10/ INPC10		AN2_0	A0, [A0/D0]
73	71		P1_7	INT5	IDU			
74	72		P1_6	INT4	IDW			
75	73		P1_5	INT3	IDV			
76	74		P1_4					
77	75		P1_3					
78	76		P1_2					
79	77		P1_1					
80	78		P1_0					
81	79		P0_7				AN0_7	D7
82	80		P0_6				AN0_6	D6
83	81		P0_5				AN0_5	D5
84	82		P0_4				AN0_4	D4
85	83		P0_3				AN0_3	D3
86	84		P0_2				AN0_2	D2
87	85		P0_1				AN0_1	D1
88	86		P0_0				AN0_0	D0
89	87		P10_7	KI3			AN7	
90	88		P10_6	KI2			AN6	
91	89		P10_5	KI1			AN5	
92	90		P10_4	KI0			AN4	
93	91		P10_3				AN3	
94	92		P10_2				AN2	
95	93		P10_1				AN1	
96	94	AVSS						
97	95		P10_0				AN0	
98	96	VREF						
99	97	AVCC						
100	98		P9_7			RXD4/SCL4	ADTRG	

## 1.5 Pin Functions

**Table 1.6 Pin Functions (1/3)**

Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1, VCC2, VSS	I	-	Apply 2.7 to 5.5 V to pins VCC1 and VCC2 ( $VCC1 \geq VCC2$ ). Input 0V to VSS. <sup>(1)</sup>
Analog power supply input	AVCC, AVSS	I	VCC1	This is the power supply for the A/D converter. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor modes. After a reset, to start operating in single-chip mode, connect the CNVSS pin to VSS via a resistor. To start operating in microprocessor mode, connect the pin to VCC1.
Bus control pins	D0 to D7	I/O	VCC2	Inputs or outputs data (D0 to D7) while accessing an external area with a separate bus.
	A0 to A19	O	VCC2	Outputs address bits A0 to A19.
	A0/D0 to A7/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A0 to A7) by timesharing, while accessing an external area with an 8-bit multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Outputs chip-select signals $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ to specify an external area.
	$\overline{\text{WR}}$ $\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Outputs $\overline{\text{WR}}$ , $\overline{\text{BHE}}$ , and $\overline{\text{RD}}$ signals. • Data is written to an external area when $\overline{\text{WR}}$ is driven low. Data in an external area is read when $\overline{\text{RD}}$ is driven low. An odd address is accessed when $\overline{\text{BHE}}$ is driven low.
	ALE	O	VCC2	Outputs ALE signal to latch address.
	$\overline{\text{HOLD}}$	I	VCC2	The MCU is placed in a hold state while the $\overline{\text{HOLD}}$ pin is driven low.
	$\overline{\text{HLDA}}$	O	VCC2	In a hold state, $\overline{\text{HLDA}}$ outputs a low-level signal.
	$\overline{\text{RDY}}$	I	VCC2	The MCU bus is placed in a wait state while the $\overline{\text{RDY}}$ pin is driven low.

Power supply: VCC2 is used to supply power to the external bus associated pins. The dual power supply configuration allows VCC2 to interface at a different voltage than VCC1.

Note:

1. VCC means VCC1 except as otherwise noted.

**Table 1.7 Pin Functions (2/3)**

Signal Name	Pin Name	I/O	Power Supply	Description
Main clock input	XIN	I	VCC1	I/O for the main clock oscillator. Connect a ceramic resonator or crystal between pins XIN and XOUT. <sup>(1)</sup> Input an external clock to XIN pin and leave XOUT pin open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O for a sub clock oscillator. Connect a crystal between XCIN pin and XCOUT pin. <sup>(1)</sup> Input an external clock to XCIN pin and leave XCOUT pin open.
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	Outputs the BCLK signal.
Clock output	CLKOUT	O	VCC2	Outputs a clock with the same frequency as f <sub>C</sub> , f <sub>1</sub> , f <sub>8</sub> , or f <sub>32</sub> .
INT interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	Input for the $\overline{\text{INT}}$ interrupt.
	INT3 to INT7	I	VCC2	
NMI interrupt input	NMI	I	VCC1	Input for the $\overline{\text{NMI}}$ interrupt.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Input for the key input interrupt.
Timer A	TA0OUT to TA4OUT	I/O	VCC1	I/O for timers A0 to A4 (TA0OUT is N-channel open drain output).
	TA0IN to TA4IN	I	VCC1	Input for timers A0 to A4.
	ZP	I	VCC1	Input for Z-phase.
Timer B	TB0IN to TB5IN	I	VCC1	Input for timers B0 to B5.
Three-phase motor control timer	U, $\overline{\text{U}}$ , V, $\overline{\text{V}}$ , W, $\overline{\text{W}}$	O	VCC1	Output for the three-phase motor control timer.
	$\overline{\text{SD}}$	I	VCC1	Forced cutoff input.
	IDU, IDV, IDW	I	VCC2	Input for the position data.
Real-time clock output	RTCOUT	O	VCC1	Output for the real-time clock.
Timer S	INPC10 to INPC17	I	VCC2	Input for the time measurement function.
	OUTC10 to OUTC17		VCC2	Output for the waveform generation function.
Serial interface UART0 to UART5	$\overline{\text{CTS0}}$ to $\overline{\text{CTS5}}$	I	VCC1	Input pins to control data transmission.
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS5}}$	O	VCC1	Output pins to control data reception.
	CLK0 to CLK5	I/O	VCC1	Transmit/receive clock I/O.
	RXD0 to RXD5	I	VCC1	Serial data input.
	TXD0 to TXD5	O	VCC1	Serial data output. <sup>(2)</sup>
	CLKS1	O	VCC1	Output for the transmit/receive clock multiple-pin output function.

## Notes:

- Contact the oscillator manufacturer regarding the oscillation characteristics.
- TXD2, SDA2, and SCL2 are N-channel open drain output pins. TXDi (i = 0, 1, 3 to 5), SDAi, and SCLi can be selected as CMOS output pins or N-channel open drain output pins.

**Table 1.8 Pin Functions (3/3)**

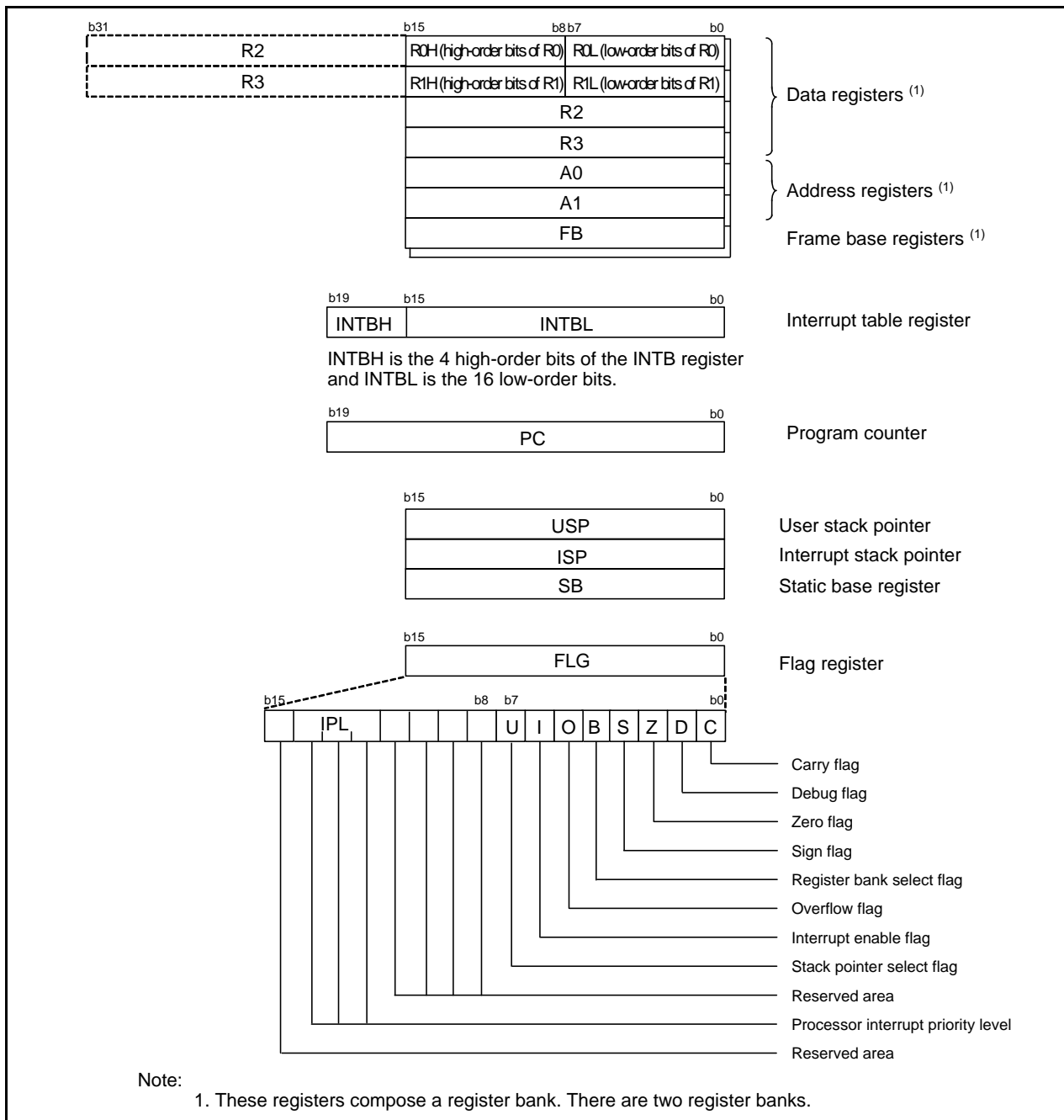
Signal Name	Pin Name	I/O	Power Supply	Description
UART0 to UART5 I <sup>2</sup> C mode	SDA0 to SDA5	I/O	VCC1	Serial data I/O for I <sup>2</sup> C mode. <sup>(2)</sup>
	SCL0 to SCL5	I/O	VCC1	Transmit/receive clock I/O for I <sup>2</sup> C mode. <sup>(2)</sup>
Multi-master I <sup>2</sup> C-bus interface	SDAMM	I/O	VCC1	Serial data I/O (N-channel open drain output).
	SCLMM	I/O	VCC1	Transmit/receive clock I/O (N-channel open drain output).
USB module	ATTACH	O	UVCC	Output used for D+ 1.5 k $\Omega$ pull-up
	VbusDTCT	I	UVCC	Input the power supply signal from a host PC
	UVCC	I		Input power supply for pins ATTACH, D+ and D-
	D+	I/O	UVCC	USB D+ input/output
	D-	I/O	UVCC	USB D- input/output
Reference voltage input	VREF	I	VCC1	Reference voltage input for the A/D and D/A converters.
A/D converter	AN0 to AN7	I	VCC1	Analog input for the A/D converter.
	AN0_0 to AN0_7 AN2_0 to AN2_7	I	VCC2	
	ADTRG	I	VCC1	External A/D trigger input.
	ANEX0, ANEX1	I	VCC1	Extended analog input for the A/D converter.
D/A converter	DA0, DA1	O	VCC1	Output for the D/A converter.
I/O ports	P0_0 to P0_7 P1_0 to P1_7 P2_0 to P2_7 P3_0 to P3_7 P4_0 to P4_7 P5_0 to P5_7	I/O	VCC2	8-bit CMOS I/O ports. A direction register determines whether each pin is used as an input port or an output port. A pull-up resistor may be enabled or disabled for input ports in 4-bit units.
	P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_7 P9_0 to P9_7 P10_0 to P10_7	I/O	VCC1	8-bit I/O ports having equivalent functions to P0. However, P7_0, P7_1, and P8_5 are N-channel open drain output ports. No pull-up resistor is provided. P8_5 is an input port for verifying the NMI pin level and shares a pin with NMI.

## Notes:

- Contact the oscillator manufacturer regarding the oscillation characteristics.
- TXD2, SDA2, and SCL2 are N-channel open drain output pins. TXDi (i = 0, 1, 3 to 5), SDAi, and SCLi can be selected as CMOS output pins or N-channel open drain output pins.

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. Seven registers (R0, R1, R2, R3, A0, A1, and FB) out of 13 compose a register bank, and there are two register banks.



**Figure 2.1 CPU Register**

### 2.1 Data Registers (R0, R1, R2, and R3)

R0, R1, R2, and R3 are 16-bit registers used for transfer, arithmetic, and logic operations. R0 and R1 can be split into high-order (R0H/R1H) and low-order (R0L/R1L) bits to be used separately as 8-bit data registers.

R0 can be combined with R2, and R3 can be combined with R1 and be used as 32-bit data registers R2R0 and R3R1, respectively.

## 2.2 Address Registers (A0 and A1)

A0 and A1 are 16-bit registers used for indirect addressing, relative addressing, transfer, arithmetic, and logic operations. A0 can be combined with A1 and used as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register that is used for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

## 2.5 Program Counter (PC)

The PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The USP and ISP stack pointers (SP) are each comprised of 16 bits. The U flag is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

### 2.8.1 Carry Flag (C Flag)

The C flag retains a carry, borrow, or shift-out bit generated by the arithmetic/logic unit.

### 2.8.2 Debug Flag (D Flag)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z Flag)

The Z flag becomes 1 when an arithmetic operation results in 0. Otherwise, it becomes 0.

### 2.8.4 Sign Flag (S Flag)

The S flag becomes 1 when an arithmetic operation results in a negative value. Otherwise, it becomes 0.

### 2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

### 2.8.6 Overflow Flag (O Flag)

The O flag becomes 1 when an arithmetic operation results in an overflow. Otherwise, it becomes 0.

### 2.8.7 Interrupt Enable Flag (I Flag)

The I flag enables maskable interrupts.

Maskable interrupts are disabled when the I flag is 0, and enabled when it is 1. The I flag becomes 0 when an interrupt request is accepted.

### **2.8.8 Stack Pointer Select Flag (U Flag)**

ISP is selected when the U flag is 0. USP is selected when the U flag is 1.

The U flag becomes 0 when a hardware interrupt request is accepted, or the INT instruction of software interrupt number 0 to 31 is executed.

### **2.8.9 Processor Interrupt Priority Level (IPL)**

IPL is 3 bits wide and assigns processor interrupt priority levels from 0 to 7.

If a requested interrupt has higher priority than IPL, the interrupt request is enabled.

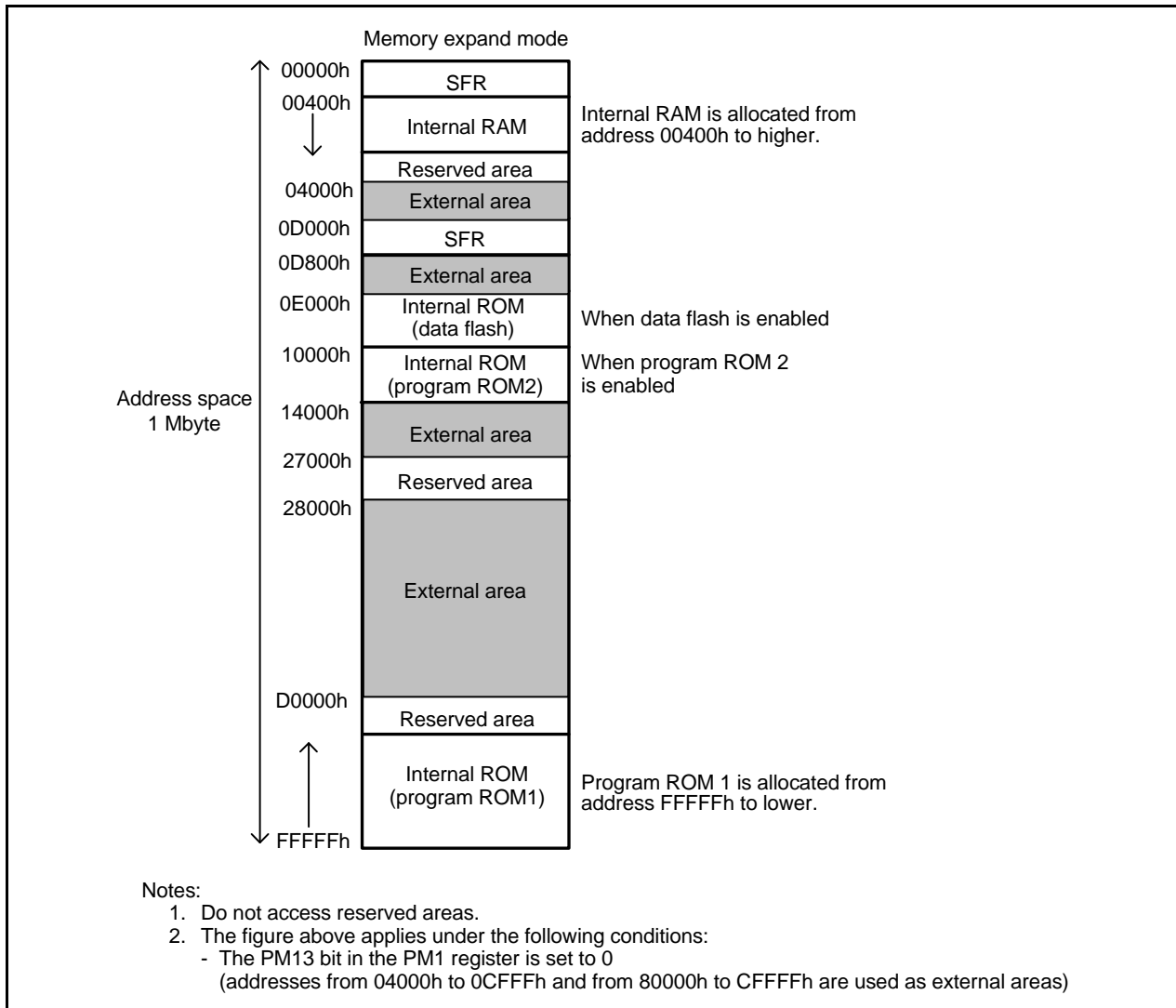
### **2.8.10 Reserved Areas**

Only set these bits to 0. The read value is undefined.

### 3. Address Space

#### 3.1 Address Space

The M16C/6C Group has a 1 MB address space from 00000h to FFFFFh. Figure 3.1 shows the Address Space. Areas that can be accessed vary depending on processor mode and the status of each control bit.



**Figure 3.1 Address Space**

### 3.2 Memory Map

Special function registers (SFRs) are allocated from address 00000h to 003FFh and from 0D000h to 0D7FFh. Peripheral function control registers are located here. All blank areas within SFRs are reserved. Do not access these areas.

Internal RAM is allocated from address 00400h higher, with 10 KB of internal RAM allocated from 00400h to 02BFFh. Internal RAM is used not only for data storage, but also for the stack area when subroutines are called or when an interrupt request is accepted.

The internal ROM is flash memory. Three internal ROM areas are available: data flash, program ROM 1, and program ROM 2.

The data flash is allocated from 0E000h to 0FFFFh. This data flash area is mostly used for data storage, but can also store programs.

Program ROM 2 is allocated from 10000h to 13FFFh. Program ROM 1 is allocated from FFFFFh lower, with the 64-KB program ROM 1 area allocated from address F0000h to FFFFFh.

The special page vectors are allocated from FFE00h to FFFD7h. They are used for the JMPS and JSRS instructions. Refer to the M16C/60, M16C/20, M16C/Tiny Series Software Manual for details.

The fixed vector table for interrupts is allocated from FFFDCh to FFFFFh.

The 256 bytes beginning with the start address set in the INTB register compose the relocatable vector table for interrupts.

Figure 3.2 shows the Memory Map.

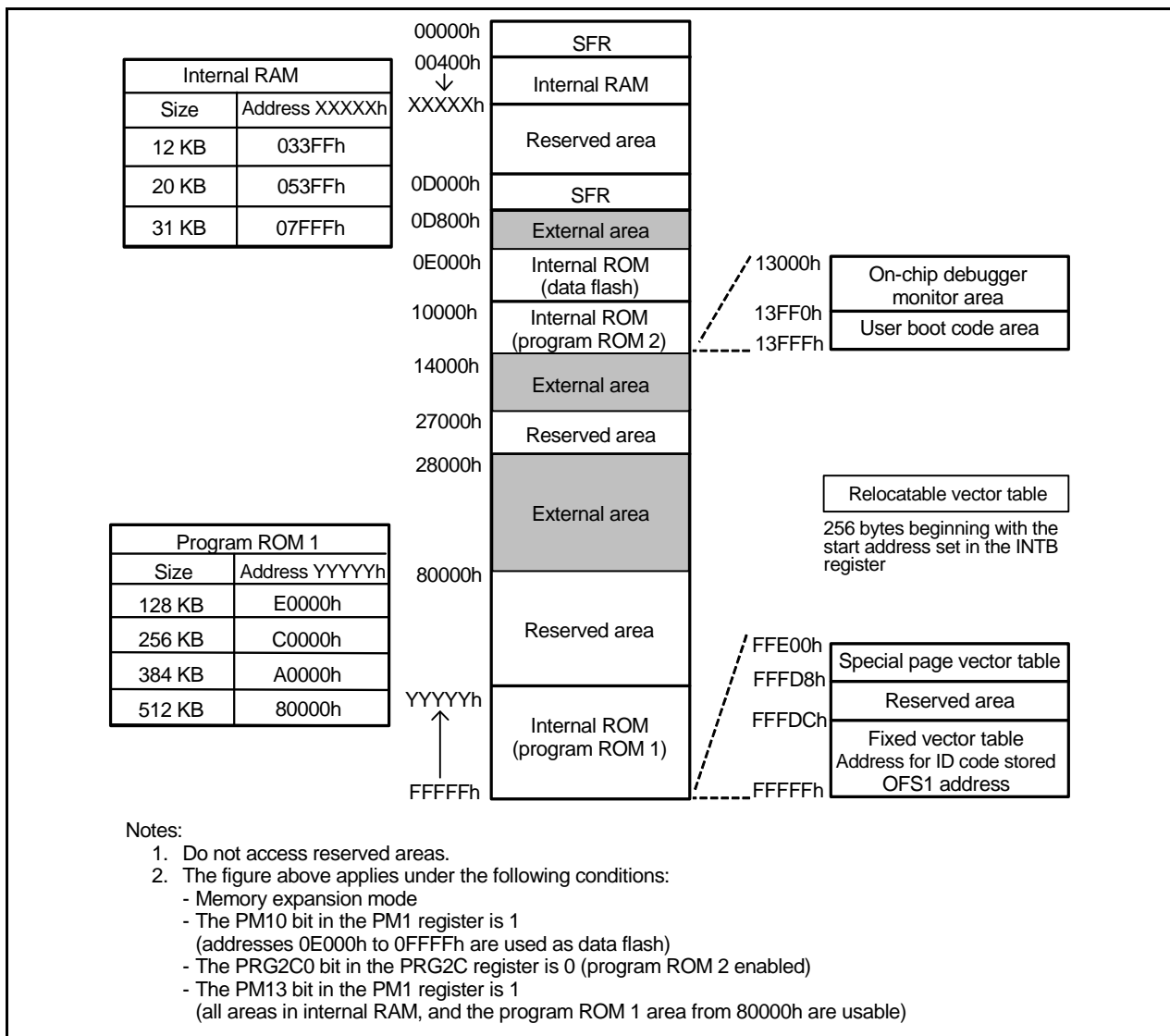


Figure 3.2 Memory Map

### 3.3 Accessible Area in Each Mode

Areas that can be accessed vary depending on processor mode and the status of each control bit. Figure 3.3 shows the Accessible Area in Each Mode.

In single-chip mode, the SFRs, internal RAM, and internal ROM can be accessed.

In memory expansion mode, the SFRs, internal RAM, internal ROM, and external areas can be accessed.

In microprocessor mode, the SFRs, internal RAM, and external areas can be accessed. Allocate ROM to the fixed vector table from FFFDCh to FFFFFh.

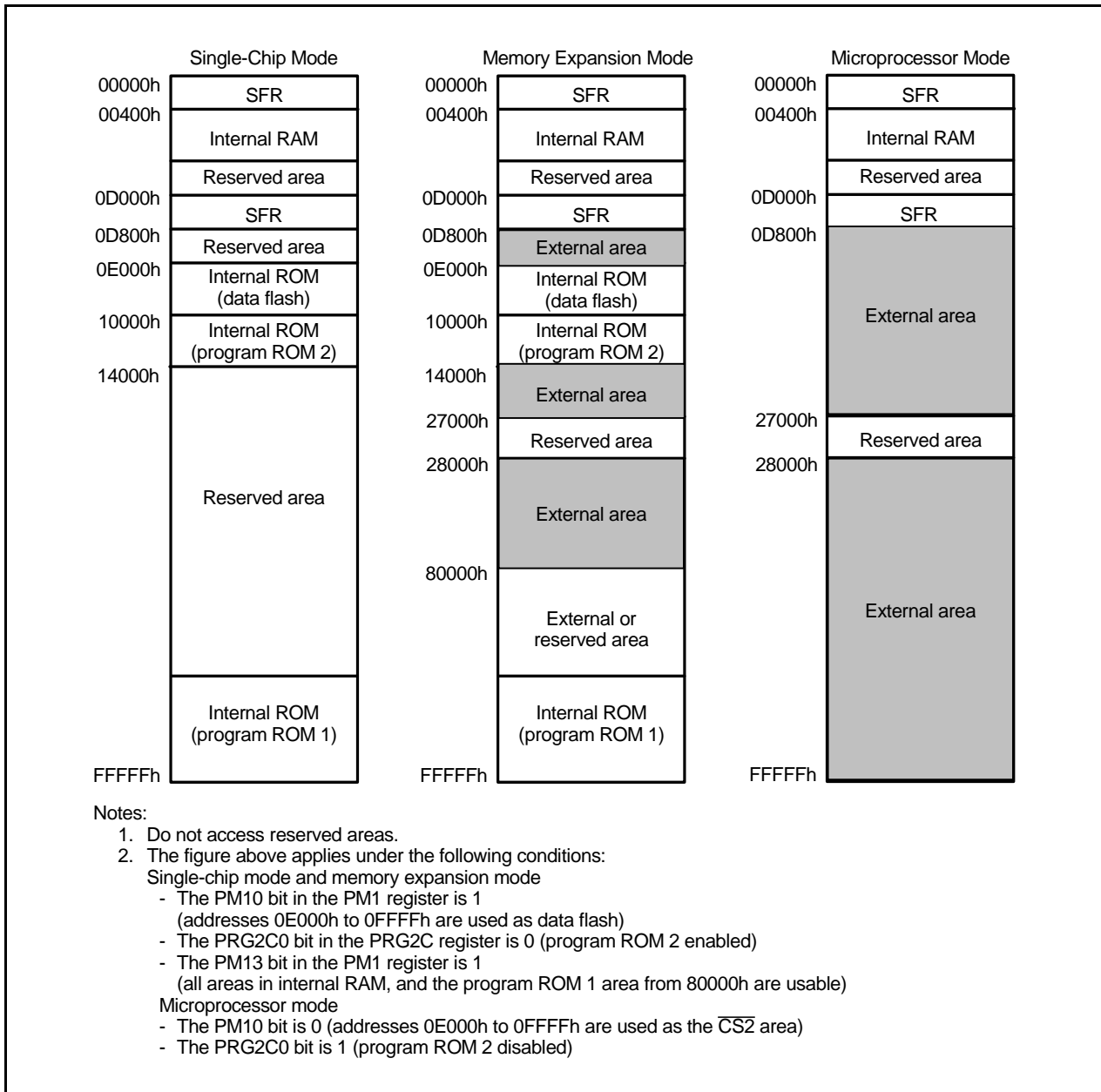


Figure 3.3 Accessible Area in Each Mode

## 4. Special Function Registers (SFRs)

### 4.1 SFRs

An SFR is a control register for a peripheral function. Table 4.1 to Table 4.21 list SFR information.

**Table 4.1 SFR Information (1/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	0000 0000b (CNVSS pin is low) 0000 0011b (CNVSS pin is high) <sup>(2)</sup>
0005h	Processor Mode Register 1	PM1	0000 1000b
0006h	System Clock Control Register 0	CM0	0100 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
0008h	Chip Select Control Register	CSR	01h
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	CM2	0X00 0010b <sup>(3)</sup>
000Dh			
000Eh			
000Fh			
0010h	Program 2 Area Control Register	PRG2C	XXXX XX00b
0011h			
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0013h			
0014h			
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
0016h			
0017h			
0018h	Reset Source Determine Register	RSTFR	XX00 001Xb (hardware reset) <sup>(4)</sup>
0019h	Voltage Detector 2 Flag Register	VCR1	0000 X000b <sup>(2)</sup>
001Ah	Voltage Detector Operation Enable Register	VCR2	000X 0000b <sup>(2, 5)</sup> 001X 0000b <sup>(2, 6)</sup>
001Bh	Chip Select Expansion Control Register	CSE	00h
001Ch	PLL Control Register 0	PLC0	0001 X010b
001Dh	PLLFCR Control Register	PLCF	00h
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
001Fh			

Notes:

X: Undefined

- The blank areas are reserved. No access is allowed.
- Software reset, watchdog timer reset, oscillator stop detect reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect the following bits and registers: The VCR1 register, the VCR2 register, and bits PM01 and PM00 in the PM0 register.
- Oscillator stop detect reset does not affect bits CM20, CM21, and CM27.
- The state of bits in the RSTFR register depends on the reset type.
- This is the reset value when the LVDAS bit of address OFS1 is 1 during hardware reset.
- This is the reset value after voltage monitor 0 reset, power-on reset, and when the LVDAS bit of address OFS1 is 0 during hardware reset.

**Table 4.2 SFR Information (2/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0020h			
0021h			
0022h	40 MHz On-Chip Oscillator Control Register 0	FRA0	XXXX XX00b
0023h			
0024h			
0025h			
0026h	Voltage Monitor Function Select Register	VWCE	00h
0027h			
0028h			
0029h			
002Ah	Voltage Monitor 0 Control Register	VW0C	1100 XX10b <sup>(2,3)</sup> 1100 XX11b <sup>(2,4)</sup>
002Bh	Voltage Monitor 1 Control Register	VW1C	1000 XX10b <sup>(6)</sup>
002Ch	Voltage Monitor 2 Control Register	VW2C	1000 0X10b <sup>(6)</sup>
002Dh			
002Eh			
002Fh			
0030h			
0031h			
0032h			
0033h			
0034h			
0035h			
0036h			
0037h			
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h			
0042h	INT7 Interrupt Control Register	INT7IC	XX00 X000b
0043h	INT6 Interrupt Control Register	INT6IC	XX00 X000b
0044h	INT3 Interrupt Control Register	INT3IC	XX00 X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register UART1 Bus Collision Detection Interrupt Control Register	TB4IC U1BCNIC	XXXX X000b
0047h	Timer B3 Interrupt Control Register UART0 Bus Collision Detection Interrupt Control Register	TB3IC U0BCNIC	XXXX X000b
0048h	INT5 Interrupt Control Register	INT5IC	XX00 X000b
0049h	INT4 Interrupt Control Register	INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register, A/D Conversion (A/D1) Interrupt Control Register	KUPIC, ADEIC	XXXX X000b
004Eh	A/D Conversion (A/D0) Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b

Notes:

X: Undefined

1. The blank areas are reserved. No access is allowed.
2. Software reset, watchdog timer reset, oscillator stop detect reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect the following registers or bit: the VW0C register, and the VW2C3 bit in the VW2C register.
3. This is the reset value when the LVDAS bit of address OFS1 is 1 during hardware reset
4. This is the reset value after voltage monitor 0 reset, power-on reset, and when the LVDAS bit of address OFS1 is 0 during hardware reset.
5. Hardware reset, power-on reset, voltage monitor 0 reset, voltage monitor 1 reset, or voltage monitor 2 reset
6. Hardware reset, power-on reset, or voltage monitor 0 reset

**Table 4.3 SFR Information (3/21) (1)**

Address	Register	Symbol	Reset Value
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00 X000b
005Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
005Fh	INT2 Interrupt Control Register	INT2IC	XX00 X000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
006Bh	UART5 Bus Collision Detection Interrupt Control Register	U5BCNIC	XXXX X000b
006Ch	UART5 Transmit Interrupt Control Register	S5TIC	XXXX X000b
006Dh	UART5 Receive Interrupt Control Register	S5RIC	XXXX X000b
006Eh	UART4 Bus Collision Detection Interrupt Control Register Real-Time Clock Period Interrupt Control Register	U4BCNIC RTCTIC	XXXX X000b
006Fh	UART4 Transmit Interrupt Control Register Real-Time Clock Compare Interrupt Control Register	S4TIC RTCCIC	XXXX X000b
0070h	UART4 Receive Interrupt Control Register	S4TIC	XXXX X000b
0071h	UART3 Bus Collision Detection Interrupt Control Register	U3BCNIC	XXXX X000b
0072h	UART3 Transmit Interrupt Control Register	S3TIC	XXXX X000b
0073h	UART3 Receive Interrupt Control Register	S3RIC	XXXX X000b
0074h			
0075h			
0076h	USB Interrupt 0 Control Register	USBINT0IC	XXXX X000b
0077h	USB Interrupt 1 Control Register	USBINT1IC	XXXX X000b
0078h	USB RESUME Interrupt Control Register	USBRSMIC	XXXX X000b
0079h	IC/OC Interrupt 0 Control Register	ICOC0IC	XXXX X000b
007Ah	IC/OC Channel 0 Interrupt Control Register	ICOCH0IC	XXXX X000b
007Bh	IC/OC Interrupt 1 Control Register I <sup>2</sup> C-bus Interface Interrupt Control Register	ICOC1IC, IICIC	XXXX X000b
007Ch	IC/OC Channel 1 Interrupt Control Register SCL/SDA Interrupt Control Register	ICOCH1IC, SCLDAIC	XXXX X000b
007Dh	IC/OC Channel 2 Interrupt Control Register	ICOCH2IC	XXXX X000b
007Eh	IC/OC Channel 3 Interrupt Control Register	ICOCH3IC	XXXX X000b
007Fh	IC/OC Base Timer Interrupt Control Register	BTIC	XXXX X000b
0080h to 011Fh			

Note:

- The blank areas are reserved. No access is allowed.

X: Undefined

**Table 4.4 SFR Information (4/21) (1)**

Address	Register	Symbol	Reset Value
0120h			
0121h			
0122h			
0123h			
0124h			
0125h			
0126h			
0127h			
0128h			
0129h			
012Ah			
012Bh			
012Ch			
012Dh			
012Eh			
012Fh			
0130h to 013Fh			
0140h	A/D1 Register 0	AD10	XXXX XXXXb 0000 00XXb
0141h			
0142h	A/D1 Register 1	AD11	XXXX XXXXb 0000 00XXb
0143h			
0144h	A/D1 Register 2	AD12	XXXX XXXXb 0000 00XXb
0145h			
0146h	A/D1 Register 3	AD13	XXXX XXXXb 0000 00XXb
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h	A/D1 Trigger Control Register	AD1TRGCON	XXXX 00XXb
0153h			
0154h	A/D1 Control Register 2	AD1CON2	0000 X00Xb
0155h			
0156h	A/D1 Control Register 0	AD1CON0	0000 0XXXb
0157h	A/D1 Control Register 1	AD1CON1	0000 X000b
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h to 017Fh			

Note:

- The blank areas are reserved. No access is allowed.

X: Undefined

**Table 4.5 SFR Information (5/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0180h 0181h 0182h	DMA0 Source Pointer	SAR0	XXh XXh 0Xh
0183h			
0184h 0185h 0186h	DMA0 Destination Pointer	DAR0	XXh XXh 0Xh
0187h			
0188h 0189h	DMA0 Transfer Counter	TCR0	XXh XXh
018Ah			
018Bh			
018Ch	DMA0 Control Register	DM0CON	0000 0X00b
018Dh			
018Eh			
018Fh			
0190h 0191h 0192h	DMA1 Source Pointer	SAR1	XXh XXh 0Xh
0193h			
0194h 0195h 0196h	DMA1 Destination Pointer	DAR1	XXh XXh 0Xh
0197h			
0198h 0199h	DMA1 Transfer Counter	TCR1	XXh XXh
019Ah			
019Bh			
019Ch	DMA1 Control Register	DM1CON	0000 0X00b
019Dh			
019Eh			
019Fh			
01A0h 01A1h 01A2h	DMA2 Source Pointer	SAR2	XXh XXh 0Xh
01A3h			
01A4h 01A5h 01A6h	DMA2 Destination Pointer	DAR2	XXh XXh 0Xh
01A7h			
01A8h 01A9h	DMA2 Transfer Counter	TCR2	XXh XXh
01AAh			
01ABh			
01ACh	DMA2 Control Register	DM2CON	0000 0X00b
01ADh			
01AEh			
01AFh			

Note:

1. The blank areas are reserved. No access is allowed.

X: Undefined

**Table 4.6 SFR Information (6/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
01B0h 01B1h 01B2h 01B3h	DMA3 Source Pointer	SAR3	XXh XXh 0Xh
01B4h 01B5h 01B6h 01B7h	DMA3 Destination Pointer	DAR3	XXh XXh 0Xh
01B8h 01B9h 01BAh 01BBh	DMA3 Transfer Counter	TCR3	XXh XXh
01BCh 01BDh 01BEh 01BFh	DMA3 Control Register	DM3CON	0000 0X00b
01C0h 01C1h	Timer B0-1 Register	TB01	XXh XXh
01C2h 01C3h	Timer B1-1 Register	TB11	XXh XXh
01C4h 01C5h	Timer B2-1 Register	TB21	XXh XXh
01C6h 01C7h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C8h 01C9h 01CAh	Timer B Count Source Select Register 0 Timer B Count Source Select Register 1	TBCS0 TBCS1	00h X0h
01CBh 01CCh 01CDh 01CEh 01CFh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01D0h 01D1h 01D2h 01D3h	Timer A Count Source Select Register 0 Timer A Count Source Select Register 1 Timer A Count Source Select Register 2	TACS0 TACS1 TACS2	00h 00h X0h
01D4h 01D5h 01D6h 01D7h	16-Bit Pulse Width Modulation Mode Function Select Register Timer A Waveform Output Function Select Register	PWMFS TAPOFS	0XX0 X00Xb XXX0 0000b
01D8h 01D9h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
01DAh 01DBh 01DCh 01DDh 01DEh 01DFh	Three-Phase Protect Control Register	TPRC	00h

Note:

1. The blank areas are reserved. No access is allowed.

X: Undefined

**Table 4.7 SFR Information (7/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
01E0h	Timer B3-1 Register	TB31	XXh
01E1h			XXh
01E2h	Timer B4-1 Register	TB41	XXh
01E3h			XXh
01E4h	Timer B5-1 Register	TB51	XXh
01E5h			XXh
01E6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 2	PPWFS2	XXXX X000b
01E7h			
01E8h	Timer B Count Source Select Register 2	TBCS2	00h
01E9h	Timer B Count Source Select Register 3	TBCS3	X0h
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			
0200h			
0201h			
0202h			
0203h			
0204h			
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h
0207h	Interrupt Source Select Register	IFSR	00h
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh	Address Match Interrupt Enable Register	AIER	XXXX XX00b
020Fh	Address Match Interrupt Enable Register 2	AIER2	XXXX XX00b

Note:

1. The blank areas are reserved. No access is allowed.

X: Undefined

**Table 4.8 SFR Information (8/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0210h 0211h 0212h 0213h	Address Match Interrupt Register 0	RMAD0	00h 00h X0h
0214h 0215h 0216h 0217h	Address Match Interrupt Register 1	RMAD1	00h 00h X0h
0218h 0219h 021Ah 021Bh	Address Match Interrupt Register 2	RMAD2	00h 00h X0h
021Ch 021Dh 021Eh 021Fh	Address Match Interrupt Register 3	RMAD3	00h 00h X0h
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

Note:

1. The blank areas are reserved. No access is allowed.

X: Undefined

**Table 4.9 SFR Information (9/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0240h			
0241h			
0242h			
0243h			
0244h	UART0 Special Mode Register 4	U0SMR4	00h
0245h	UART0 Special Mode Register 3	U0SMR3	000X 0X0Xb
0246h	UART0 Special Mode Register 2	U0SMR2	X000 0000b
0247h	UART0 Special Mode Register	U0SMR	X000 0000b
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	00XX 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0250h	UART Transmit/Receive Control Register 2	UCON	X000 0000b
0251h			
0252h	UART Clock Select Register	UCLKSEL0	X0h
0253h			
0254h	UART1 Special Mode Register 4	U1SMR4	00h
0255h	UART1 Special Mode Register 3	U1SMR3	000X 0X0Xb
0256h	UART1 Special Mode Register 2	U1SMR2	X000 0000b
0257h	UART1 Special Mode Register	U1SMR	X000 0000b
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	00XX 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0260h			
0261h			
0262h			
0263h			
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh

Note:

1. The blank areas are reserved. No access is allowed.

X: Undefined

**Table 4.10 SFR Information (10/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0270h			
0271h			
0272h			
0273h			
0274h			
0275h			
0276h			
0277h			
0278h			
0279h			
027Ah			
027Bh			
027Ch			
027Dh			
027Eh			
027Fh			
0280h			
0281h			
0282h			
0283h			
0284h	UART5 Special Mode Register 4	U5SMR4	00h
0285h	UART5 Special Mode Register 3	U5SMR3	000X 0X0Xb
0286h	UART5 Special Mode Register 2	U5SMR2	X000 0000b
0287h	UART5 Special Mode Register	U5SMR	X000 0000b
0288h	UART5 Transmit/Receive Mode Register	U5MR	00h
0289h	UART5 Bit Rate Register	U5BRG	XXh
028Ah	UART5 Transmit Buffer Register	U5TB	XXh
028Bh			XXh
028Ch	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
028Dh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
028Eh	UART5 Receive Buffer Register	U5RB	XXh
028Fh			XXh
0290h			
0291h			
0292h			
0293h			
0294h	UART4 Special Mode Register 4	U4SMR4	00h
0295h	UART4 Special Mode Register 3	U4SMR3	000X 0X0Xb
0296h	UART4 Special Mode Register 2	U4SMR2	X000 0000b
0297h	UART4 Special Mode Register	U4SMR	X000 0000b
0298h	UART4 Transmit/Receive Mode Register	U4MR	00h
0299h	UART4 Bit Rate Register	U4BRG	XXh
029Ah	UART4 Transmit Buffer Register	U4TB	XXh
029Bh			XXh
029Ch	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
029Dh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
029Eh	UART4 Receive Buffer Register	U4RB	XXh
029Fh			XXh

Note:

1. The blank areas are reserved. No access is allowed.

X: Undefined

**Table 4.11 SFR Information (11/21) (1)**

Address	Register	Symbol	Reset Value
02A0h			
02A1h			
02A2h			
02A3h			
02A4h	UART3 Special Mode Register 4	U3SMR4	00h
02A5h	UART3 Special Mode Register 3	U3SMR3	000X 0X0Xb
02A6h	UART3 Special Mode Register 2	U3SMR2	X000 0000b
02A7h	UART3 Special Mode Register	U3SMR	X000 0000b
02A8h	UART3 Transmit/Receive Mode Register	U3MR	00h
02A9h	UART3 Bit Rate Register	U3BRG	XXh
02AAh	UART3 Transmit Buffer Register	U3TB	XXh
02ABh			XXh
02ACh	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
02ADh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
02AEh	UART3 Receive Buffer Register	U3RB	XXh
02AFh			XXh
02B0h	I2C0 Data Shift Register	S00	XXh
02B1h			
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	00h
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb
02BCh			
02BDh			
02BEh			
02BFh			
02C0h	Time measurement register, Waveform generation register 0	G1TM0	XXh
02C1h		G1PO0	XXh
02C2h	Time measurement register, Waveform generation register 1	G1TM1	XXh
02C3h		G1PO1	XXh
02C4h	Time measurement register, Waveform generation register 2	G1TM2	XXh
02C5h		G1PO2	XXh
02C6h	Time measurement register, Waveform generation register 3	G1TM3	XXh
02C7h		G1PO3	XXh
02C8h	Time measurement register, Waveform generation register 4	G1TM4	XXh
02C9h		G1PO4	XXh
02CAh	Time measurement register, Waveform generation register 5	G1TM5	XXh
02CBh		G1PO5	XXh
02CCh	Time measurement register, Waveform generation register 6	G1TM6	XXh
02CDh		G1PO6	XXh
02CEh	Time measurement register, Waveform generation register 7	G1TM7	XXh
02CFh		G1PO7	XXh
02D0h	Waveform generation control register 0	G1POCR0	0X00XX00b
02D1h	Waveform generation control register 1	G1POCR1	0X00XX00b
02D2h	Waveform generation control register 2	G1POCR2	0X00XX00b
02D3h	Waveform generation control register 3	G1POCR3	0X00XX00b
02D4h	Waveform generation control register 4	G1POCR4	0X00XX00b
02D5h	Waveform generation control register 5	G1POCR5	0X00XX00b
02D6h	Waveform generation control register 6	G1POCR6	0X00XX00b
02D7h	Waveform generation control register 7	G1POCR7	0X00XX00b
02D8h	Time measurement control register 0	G1TMCR0	00h
02D9h	Time measurement control register 1	G1TMCR1	00h
02DAh	Time measurement control register 2	G1TMCR2	00h
02DBh	Time measurement control register 3	G1TMCR3	00h
02DCh	Time measurement control register 4	G1TMCR4	00h
02DDh	Time measurement control register 5	G1TMCR5	00h
02DEh	Time measurement control register 6	G1TMCR6	00h
02DFh	Time measurement control register 7	G1TMCR7	00h

Note:

1. The blank areas are reserved. No access is allowed.

X: Undefined

**Table 4.12 SFR Information (12/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
02E0h	Base timer register	G1BT	XXh
02E1h			XXh
02E2h	Base timer control register 0	G1BCR0	00h
02E3h	Base timer control register 1	G1BCR1	00h
02E4h	Time measurement prescaler register 6	G1TPR6	00h
02E5h	Time measurement prescaler register 7	G1TPR7	00h
02E6h	Function enable register	G1FE	00h
02E7h	Function select register	G1FS	00h
02E8h	Base timer reset register	G1BTRR	XXh
02E9h			XXh
02EAh	Count source divide register	G1DV	00h
02EBh			
02ECh	Waveform output master enable register	G1OER	00h
02EDh			
02EEh	Timer S I/O control register 0	G1IOR0	00h
02EFh	Timer S I/O control register 1	G1IOR1	00h
02F0h	Interrupt request register	G1IR	XXh
02F1h	Interrupt enable register 0	G1IE0	00h
02F2h	Interrupt enable register 1	G1IE1	00h
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh			
02FDh			
02FEh			
02FFh			
0300h	Timer B3/B4/B5 Count Start Flag	TBSR	000X XXXXb
0301h			
0302h	Timer A1-1 Register	TA11	XXh
0303h			XXh
0304h	Timer A2-1 Register	TA21	XXh
0305h			XXh
0306h	Timer A4-1 Register	TA41	XXh
0307h			XXh
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh	Position-Data-Retain Function Control Register	PDRF	XXXX 0000b
030Fh			

Note:

1. The blank areas are reserved. No access is allowed.

X: Undefined

**Table 4.13 SFR Information (13/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0310h 0311h	Timer B3 Register	TB3	XXh XXh
0312h 0313h	Timer B4 Register	TB4	XXh XXh
0314h 0315h	Timer B5 Register	TB5	XXh XXh
0316h			
0317h			
0318h	Port Function Control Register	PFCR	0011 1111b
0319h			
031Ah			
031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
031Eh			
031Fh			
0320h	Count Start Flag	TABSR	00h
0321h			
0322h	One-Shot Start Flag	ONSF	00h
0323h	Trigger Select Register	TRGSR	00h
0324h	Up/Down Flag	UDF	00h
0325h			
0326h 0327h	Timer A0 Register	TA0	XXh XXh
0328h 0329h	Timer A1 Register	TA1	XXh XXh
032Ah 032Bh	Timer A2 Register	TA2	XXh XXh
032Ch 032Dh	Timer A3 Register	TA3	XXh XXh
032Eh 032Fh	Timer A4 Register	TA4	XXh XXh
0330h 0331h	Timer B0 Register	TB0	XXh XXh
0332h 0333h	Timer B1 Register	TB1	XXh XXh
0334h 0335h	Timer B2 Register	TB2	XXh XXh
0336h	Timer A0 Mode Register	TA0MR	00h
0337h	Timer A1 Mode Register	TA1MR	00h
0338h	Timer A2 Mode Register	TA2MR	00h
0339h	Timer A3 Mode Register	TA3MR	00h
033Ah	Timer A4 Mode Register	TA4MR	00h
033Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
033Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
033Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
033Eh	Timer B2 Special Mode Register	TB2SC	X000 0000b
033Fh			

Note:

1. The blank areas are reserved. No access is allowed.

X: Undefined

**Table 4.14 SFR Information (14/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0340h	Real-Time Clock Second Data Register	RTCSEC	00h
0341h	Real-Time Clock Minute Data Register	RTCMIN	X000 0000b
0342h	Real-Time Clock Hour Data Register	RTCHR	XX00 0000b
0343h	Real-Time Clock Day Data Register	RTCWK	XXXX X000b
0344h	Real-Time Clock Control Register 1	RTCCR1	0000 X00Xb
0345h	Real-Time Clock Control Register 2	RTCCR2	X000 0000b
0346h	Real-Time Clock Count Source Select Register	RTCCSR	XXX0 0000b
0347h			
0348h	Real-Time Clock Second Compare Data Register	RTCCSEC	X000 0000b
0349h	Real-Time Clock Minute Compare Data Register	RTCCMIN	X000 0000b
034Ah	Real-Time Clock Hour Compare Data Register	RTCCHR	X000 0000b
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h			
0351h			
0352h			
0353h			
0354h			
0355h			
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh			
035Ch			
035Dh			
035Eh			
035Fh			
0360h	Pull-Up Control Register 0	PUR0	00h
0361h	Pull-Up Control Register 1	PUR1	0000 0000b <sup>(2)</sup> 0000 0010b
0362h	Pull-Up Control Register 2	PUR2	00h
0363h			
0364h			
0365h			
0366h	Port Control Register	PCR	0000 0XX0b
0367h			
0368h			
0369h	NMI/SD Digital Filter Register	NMIDF	XXXX X000b
036Ah			
036Bh			
036Ch			
036Dh			
036Eh			
036Fh			

Notes:

X: Undefined

- The blank areas are reserved. No access is allowed.
- Values after hardware reset, power-on reset, or voltage monitor 0 reset are as follows:
  - 00000000b when a low-level signal is input to the CNVSS pin
  - 00000010b when a high-level signal is input to the CNVSS pin
 Values after voltage monitor 1 reset, voltage monitor 2 reset, software reset, watchdog timer reset, or oscillation stop detect reset are as follows:
  - 00000000b when bits PM01 and PM00 in the PM0 register are 00b (single-chip mode).
  - 00000010b when bits PM01 and PM00 in the PM0 register are 01b (memory expansion mode) or 11b (microprocessor mode).

**Table 4.15 SFR Information (15/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0370h			
0371h			
0372h			
0373h			
0374h			
0375h			
0376h			
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch	Count Source Protection Mode Register	CSPR	00h <sup>(2)</sup>
037Dh	Watchdog Timer Refresh Register	WDTR	XXh
037Eh	Watchdog Timer Start Register	WDTS	XXh
037Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0380h			
0381h			
0382h			
0383h			
0384h			
0385h			
0386h			
0387h			
0388h			
0389h			
038Ah			
038Bh			
038Ch			
038Dh			
038Eh			
038Fh			
0390h	DMA2 Source Select Register	DM2SL	00h
0391h			
0392h	DMA3 Source Select Register	DM3SL	00h
0393h			
0394h			
0395h			
0396h			
0397h			
0398h	DMA0 Source Select Register	DM0SL	00h
0399h			
039Ah	DMA1 Source Select Register	DM1SL	00h
039Bh			
039Ch			
039Dh			
039Eh			
039Fh			

Notes:

1. The blank areas are reserved. No access is allowed.
2. When the CSPROINI bit in the OFS1 address is 0, the reset value is 10000000b.

X: Undefined

**Table 4.16 SFR Information (16/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
03A0h			
03A1h			
03A2h			
03A3h			
03A4h			
03A5h			
03A6h			
03A7h			
03A8h			
03A9h			
03AAh			
03ABh			
03ACh			
03ADh			
03AEh			
03AFh			
03B0h			
03B1h			
03B2h			
03B3h			
03B4h	SFR Snoop Address Register	CRCSAR	XXXX XXXXb 00XX XXXXb
03B5h			
03B6h	CRC Mode Register	CRCMR	0XXX XXX0b
03B7h			
03B8h			
03B9h			
03BAh			
03BBh			
03BCh	CRC Data Register	CRCD	XXh XXh
03BDh			
03BEh	CRC Input Register	CRCIN	XXh
03BFh			
03C0h	A/D0 Register 0	AD00	XXXX XXXXb 0000 00XXb
03C1h			
03C2h	A/D0 Register 1	AD01	XXXX XXXXb 0000 00XXb
03C3h			
03C4h	A/D0 Register 2	AD02	XXXX XXXXb 0000 00XXb
03C5h			
03C6h	A/D0 Register 3	AD03	XXXX XXXXb 0000 00XXb
03C7h			
03C8h	A/D0 Register 4	AD04	XXXX XXXXb 0000 00XXb
03C9h			
03CAh	A/D0 Register 5	AD05	XXXX XXXXb 0000 00XXb
03CBh			
03CCh	A/D0 Register 6	AD06	XXXX XXXXb 0000 00XXb
03CDh			
03CEh	A/D0 Register 7	AD07	XXXX XXXXb 0000 00XXb
03CFh			

Note:

- The blank areas are reserved. No access is allowed.

X: Undefined

**Table 4.17 SFR Information (17/21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
03D0h			
03D1h			
03D2h	A/D0 Trigger Control Register	AD0TRGCON	XXXX 00XXb
03D3h			
03D4h	A/D0 Control Register 2	AD0CON2	0000 X00Xb
03D5h			
03D6h	A/D0 Control Register 0	AD0CON0	0000 0XXXb
03D7h	A/D0 Control Register 1	AD0CON1	0000 X000b
03D8h	D/A0 Register	DA0	00h
03D9h			
03DAh	D/A1 Register	DA1	00h
03DBh			
03DCh	D/A Control Register	DACON	XXXX XX00b
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h			
03F6h	Port P10 Direction Register	PD10	00h
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh			
0400h to D0FFh			

Note:

1. The blank areas are reserved. No access is allowed.

X: Undefined

**Table 4.18 SFR Information (18/21) (1)**

Address	Register	Symbol	After Reset
D100h	USB interrupt flag register 0	USBIFR0	00h
D101h	USB interrupt flag register 1	USBIFR1	XXX00000b
D102h	USB interrupt flag register 2	USBIFR2	XX000110b
D103h	USB interrupt flag register 3	USBIFR3	XX000110b
D104h			
D105h			
D106h			
D107h			
D108h	USB interrupt enable register 0	USBIER0	000000X0b
D109h	USB interrupt enable register 1	USBIER1	XXX00000b
D10Ah	USB interrupt enable register 2	USBIER2	XX000000b
D10Bh	USB interrupt enable register 3	USBIER3	XX000000b
D10Ch			
D10Dh			
D10Eh			
D10Fh			
D110h	USB interrupt select register 0	USBISR0	00X000X0b
D111h	USB interrupt select register 1	USBISR1	XXX00000b
D112h	USB interrupt select register 2	USBISR2	XX000000b
D113h	USB interrupt select register 3	USBISR3	XX000000b
D114h			
D115h			
D116h			
D117h			
D118h			
D119h			
D11Ah			
D11Bh			
D11Ch			
D11Dh			
D11Eh			
D11Fh			
D120h	USB endpoint 0 IN data register	USBEPDR0I	XXh
D121h			
D122h			
D123h			
D124h	USB endpoint 0 OUT data register	USBEPDR0O	00h
D125h			
D126h			
D127h			
D128h	USB endpoint 0 S data register	USBEPDR0S	00h
D129h			
D12Ah			
D12Bh			
D12Ch			
D12Dh			
D12Eh			
D12Fh			

X: Undefined

Note:

1. Blanks are reserved. No access is allowed.

**Table 4.19 SFR Information (19/21) (1)**

Address	Register	Symbol	After Reset
D130h	USB endpoint 1 data register	USBEPDR1	00h
D131h			
D132h			
D133h			
D134h	USB endpoint 2 data register	USBEPDR2	XXh
D135h			
D136h			
D137h			
D138h	USB endpoint 3 data register	USBEPDR3	XXh
D139h			
D13Ah			
D13Bh			
D13Ch			
D13Dh			
D13Eh			
D13Fh			
D140h	USB endpoint 4 data register	USBEPDR4	00h
D141h			
D142h			
D143h			
D144h	USB endpoint 5 data register	USBEPDR5	XXh
D145h			
D146h			
D147h			
D148h	USB endpoint 6 data register	USBEPDR6	XXh
D149h			
D14Ah			
D14Bh			
D14Ch			
D14Dh			
D14Eh			
D14Fh			
D150h to D17Fh			
D180h	USB endpoint 0 OUT receive data size register	USBEPSZ0	000XXXXXb
D181h	USB endpoint 1 receive data size register	USBEPSZ1	0XXXXXXXb
D182h	USB endpoint 4 receive data size register	USBEPSZ4	0XXXXXXXb
D183h			
D184h			
D185h			
D186h			
D187h			
D188h	USB data status register 0	USBDASTS0	XXXXXX0b
D189h	USB data status register 1	USBDASTS1	XXXXX00Xb
D18Ah	USB data status register 2	USBDASTS2	XXXXX00Xb
D18Bh			
D18Ch			
D18Dh			
D18Eh			
D18Fh			

X: Undefined

Note:

1. Blanks are reserved. No access is allowed.

**Table 4.20 SFR Information (20/21) (1)**

Address	Register	Symbol	After Reset
D190h	USB trigger register 0	USBTRG0	XXh
D191h	USB trigger register 1	USBTRG1	XXh
D192h	USB trigger register 2	USBTRG2	XXh
D193h			
D194h			
D195h			
D196h			
D197h			
D198h	USB FIFO clear register 0	USBFCLR0	XXh
D199h	USB FIFO clear register 1	USBFCLR1	XXh
D19Ah	USB FIFO clear register 2	USBFCLR2	XXh
D19Bh			
D19Ch			
D19Dh			
D19Eh			
D19Fh			
D1A0h	USB endpoint stall register 0	USBEPSTL0	XXXXXXXX0b
D1A1h	USB endpoint stall register 1	USBEPSTL1	XXXXX000b
D1A2h	USB endpoint stall register 2	USBEPSTL2	XXXXX000b
D1A3h			
D1A4h			
D1A5h			
D1A6h			
D1A7h			
D1A8h			
D1A9h	USB stall status register 1	USBSTLSR1	X000X000b
D1AAh	USB stall status register 2	USBSTLSR2	X000X000b
D1ABh			
D1ACh			
D1ADh			
D1AEh			
D1AFh			
D1B0h	USB DMA transfer setting register	USBDMAR	XXX00X00b
D1B1h			
D1B2h			
D1B3h			
D1B4h	USB configuration value register	USBCVR	0000X000b
D1B5h			
D1B6h			
D1B7h			
D1B8h	USB control register	USBCTLR	0XX00001b
D1B9h			
D1BAh			
D1BBh			
D1BCh			
D1BDh			
D1BEh			
D1BFh			

X: Undefined

Note:

- Blanks are reserved. No access is allowed.

**Table 4.21 SFR Information (21/21) (1)**

Address	Register	Symbol	After Reset
D1C0h	USB endpoint information register	USBEPiR	XXh
D1C1h			
D1C2h			
D1C3h			
D1C4h			
D1C5h			
D1C6h			
D1C7h			
D1C8h			
D1C9h			
D1CAh			
D1CBh			
D1CCh	USB module control register	USBMC	11X10XX0b
D1CDh			
D1CEh			
D1CFh			

X: Undefined

Note:

1. Blanks are reserved. No access is allowed.

## 4.2 Notes on SFRs

### 4.2.1 Register Settings

Table 4.22 lists Registers with Write-Only Bits and registers whose function differs between reading and writing. Set these registers with immediate values. When establishing the next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM.

**Table 4.22 Registers with Write-Only Bits**

Register	Symbol	Address
Watchdog Timer Refresh Register	WDTR	037Dh
Watchdog Timer Start Register	WDTS	037Eh
Timer A0 Register	TA0	0327h to 0326h
Timer A1 Register	TA1	0329h to 0328h
Timer A2 Register	TA2	032Bh to 032Ah
Timer A3 Register	TA3	032Dh to 032Ch
Timer A4 Register	TA4	032Fh to 032Eh
Timer A1-1 Register	TA11	0303h to 0302h
Timer A2-1 Register	TA21	0305h to 0304h
Timer A4-1 Register	TA41	0307h to 0306h
Three-Phase Output Buffer Register 0	IDB0	030Ah
Three-Phase Output Buffer Register 1	IDB1	030Bh
Dead Time Timer	DTT	030Ch
Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	030Dh
UART0 Bit Rate Register	U0BRG	0249h
UART1 Bit Rate Register	U1BRG	0259h
UART2 Bit Rate Register	U2BRG	0269h
UART3 Bit Rate Register	U3BRG	02A9h
UART4 Bit Rate Register	U4BRG	0299h
UART5 Bit Rate Register	U5BRG	0289h
UART0 Transmit Buffer Register	U0TB	024Bh to 024Ah
UART1 Transmit Buffer Register	U1TB	025Bh to 025Ah
UART2 Transmit Buffer Register	U2TB	026Bh to 026Ah
UART3 Transmit Buffer Register	U3TB	02ABh to 02AAh
UART4 Transmit Buffer Register	U4TB	029Bh to 029Ah
UART5 Transmit Buffer Register	U5TB	028Bh to 028Ah
I2C0 control register 1	S3D0	02B6h
I2C0 status register	S10	02B8h

**Table 4.23 Registers with Write-Only Bits**

Register	Symbol	Address
USB endpoint 0 IN data register	USBEPDR0I	D120h
USB endpoint 2 data register	USBEPDR2	D134h
USB endpoint 3 data register	USBEPDR3	D138h
USB endpoint 5 data register	USBEPDR5	D144h
USB endpoint 6 data register	USBEPDR6	D148h
USB trigger register 0	USBTRG0	D190h
USB trigger register 1	USBTRG1	D191h
USB Trigger Register 2	USBTRG2	D192h
USB FIFO Clear Register 0	USBFCLR0	D198h
USB FIFO Clear Register 1	USBFCLR1	D199h
USB FIFO Clear Register 2	USBFCLR2	D19Ah
USB Endpoint Stall Register 0	USBEPSTL0	D1A0h
USB Endpoint Stall Register 1	USBEPSTL1	D1A1h
USB Endpoint Stall Register 2	USBEPSTL2	D1A2h
USB Endpoint Information Register	USBEPPIR	D1C0h

## 5. Electrical Characteristics

### 5.1 Electrical Characteristics (Common to 3 V and 5 V)

#### 5.1.1 Absolute Maximum Rating

**Table 5.1 Absolute Maximum Ratings**

Symbol	Parameter		Condition	Rated Value	Unit
$V_{CC1}, V_{CC2}$	Supply voltage		$V_{CC1} = AV_{CC}$	-0.3 to 6.5	V
$V_{CC2}$	Supply voltage		$V_{CC2}$	-0.3 to $V_{CC1} + 0.1$	V
$AV_{CC}$	Analog supply voltage		$V_{CC1} = AV_{CC}$	-0.3 to 6.5	V
$V_I$	Input voltage	$\overline{RESET}$ , CNVSS P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, UVCC		-0.3 to $V_{CC1} + 0.3$	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		-0.3 to $V_{CC2} + 0.3$	V
		P7_0, P7_1, P8_5		-0.3 to 6.5	V
$V_O$	Output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 XOUT, UVCC		-0.3 to $V_{CC1} + 0.3$	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		-0.3 to $V_{CC2} + 0.3$	V
		P7_0, P7_1, P8_5		-0.3 to 6.5	V
$P_d$	Power consumption		$-40^\circ\text{C} < T_{opr} \leq 85^\circ\text{C}$	300	mW
$T_{opr}$	Operating ambient temperature	When the microcomputer is operating		-20 to 85/-40 to 85	°C
		Flash program erase		0 to 60	
$T_{stg}$	Storage temperature			-65 to 150	°C

### 5.1.2 Recommended Operating Conditions

**Table 5.2 Recommended Operating Conditions (1/3) (1)**

Symbol	Parameter		Standard			Unit	
			Min.	Typ.	Max.		
$V_{CC1}$ , $V_{CC2}$	Supply voltage ( $V_{CC1} \geq V_{CC2}$ )		When USB function is used	3.0	5.0	5.5	V
			When USB function is not used	2.7	5.0	5.5	V
$AV_{CC}$	Analog supply voltage			$V_{CC1}$		V	
UVCC	USB Supply Voltage (When UVCC pin is input)	When USB function is used	$V_{CC1} = 3.6$ to $5.5$ V	3.0	3.3	3.6	V
			$V_{CC1} = 3.0$ to $3.6$ V	3.0	-	$V_{CC1}$	V
		When USB function is not used	$V_{CC2} = 2.7$ to $5.5$ V	-	$V_{CC1}$	-	V
$V_{SS}$	Supply voltage			0		V	
$AV_{SS}$	Analog supply voltage			0		V	
$V_{IH}$	High input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7		$0.8V_{CC2}$		$V_{CC2}$	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (in single-chip mode)		$0.8V_{CC2}$		$V_{CC2}$	V
		P0_0 to P0_7, P2_0 to P2_7, P3_0 (data input in memory expansion and microprocessor modes)		$0.5V_{CC2}$		$V_{CC2}$	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS		$0.8V_{CC1}$		$V_{CC1}$	V
		P7_0, P7_1, P8_5		$0.8V_{CC1}$		6.5	V
$V_{IL}$	Low input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7		0		$0.2V_{CC2}$	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (in single-chip mode)		0		$0.2V_{CC2}$	V
		P0_0 to P0_7, P2_0 to P2_7, P3_0 (data input in memory expansion and microprocessor mode)		0		$0.16V_{CC2}$	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS		0		$0.2V_{CC1}$	V
$I_{OH(peak)}$	High peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7				-10.0	mA
$I_{OH(avg)}$	High average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7				-5.0	mA

## Notes:

1. Referenced to  $V_{CC1} = V_{CC2} = 2.7$  to  $5.5$  V at  $T_{opr} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified.
2. The average output current is the mean value within 100 ms.
3. The total  $I_{OL(peak)}$  for ports P0, P1, P2, P8\_6, P8\_7, P9, and P10 must be 80 mA max. The total  $I_{OL(peak)}$  for ports P3, P4, P5, P6, P7, and P8\_0 to P8\_5 must be 80 mA max. The total  $I_{OH(peak)}$  for ports P0, P1, and P2 must be -40 mA max. The total  $I_{OH(peak)}$  for ports P3, P4, and P5 must be -40 mA max. The total  $I_{OH(peak)}$  for ports P6, P7\_2 to P7\_7 and P8\_0 to P8\_4 must be -40 mA max.  $I_{OH(peak)}$  for ports P8\_6, P8\_7, P9, and P10 must be -40 mA max.

**Table 5.3 Recommended Operating Conditions (2/3) (1)**

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$I_{OL(peak)}$	Low peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7			10.0	mA
$I_{OL(avg)}$	Low average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7			5.0	mA
$f_{(XIN)}$	Main clock input oscillation frequency	$V_{CC1} = 2.7\text{ V to }5.5\text{ V}$	2		16	MHz
$f_{(XCIN)}$	Sub-clock oscillation frequency			32.768	50	kHz
$f_{(PLL)}$	PLL clock oscillation frequency	$V_{CC1} = 2.7\text{ V to }5.5\text{ V}$	10		32	MHz
$f_{(BCLK)}$	CPU operation clock		$f_{OCO-S}$ divided by 16		32	MHz
$t_{SU(PLL)}$	PLL frequency synthesizer stabilization wait time	$V_{CC1} = 5.0\text{ V}$			2	ms
		$V_{CC1} = 3.0\text{ V}$			3	ms

Notes:

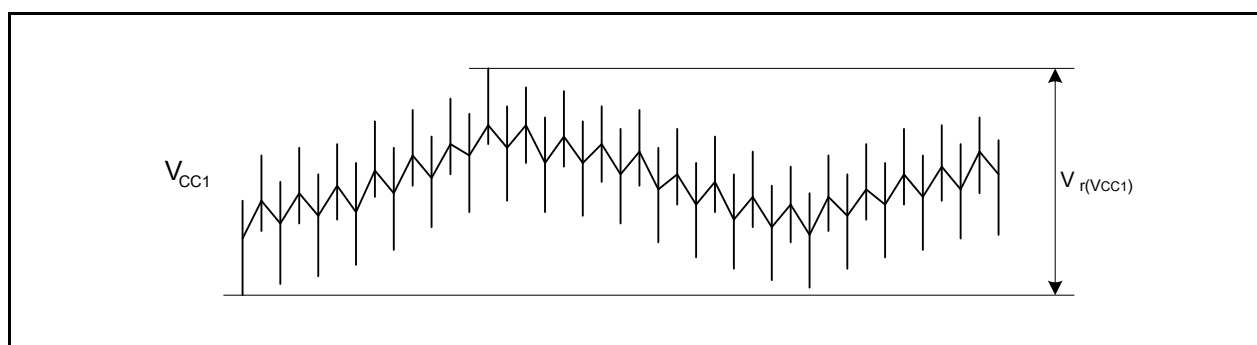
1. Referenced to  $V_{CC1} = V_{CC2} = 2.7$  to  $5.5\text{ V}$  at  $T_{opr} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified.
2. The average output current is the mean value within 100 ms.
3. The total  $I_{OL(peak)}$  for ports P0, P1, P2, P8\_6, P8\_7, P9, and P10 must be 80 mA max. The total  $I_{OL(peak)}$  for ports P3, P4, P5, P6, P7, and P8\_0 to P8\_5 must be 80 mA max. The total  $I_{OH(peak)}$  for ports P0, P1, and P2 must be  $-40$  mA max. The total  $I_{OH(peak)}$  for ports P3, P4, and P5 must be  $-40$  mA max. The total  $I_{OH(peak)}$  for ports P6, P7\_2 to P7\_7 and P8\_0 to P8\_4 must be  $-40$  mA max.  $I_{OH(peak)}$  for ports P8\_6, P8\_7, P9, and P10 must be  $-40$  mA max.

**Table 5.4 Recommended Operating Conditions (3/3) (1, 2)**Supply ripple is to implement either  $V_{r(VCC1)}$  or  $dV_{r(VCC1)}/dt$ , or both of them.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$V_{r(VCC1)}$	Supply ripple available voltage	$V_{CC1} = 5.0\text{ V}$			0.5	Vp-p
		$V_{CC1} = 3.0\text{ V}$			0.3	Vp-p
$dV_{r(VCC1)}/dt$	Supply ripple fall gradient	$V_{CC1} = 5.0\text{ V}$			0.3	V/ms
		$V_{CC1} = 3.0\text{ V}$			0.3	V/ms

Notes:

1. The device is operationally guaranteed under these operating conditions.
2. Referenced to  $V_{CC1} = 2.7$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$  and at  $T_{opr} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified.

**Figure 5.1 Ripple waveform**

### 5.1.3 A/D Conversion Characteristics

Table 5.5 A/D Conversion Characteristics (1, 2, 3)

Symbol	Parameter		Measuring Condition	Standard			Unit	
				Min.	Typ.	Max.		
-	Resolution					10	Bits	
I <sub>NL</sub>	Integral non-linearity error	10bit	V <sub>CC1</sub> = 5.0 V (4)	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
			V <sub>CC1</sub> = 3.3 V (4)	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
			V <sub>CC1</sub> = 3.0 V (4)	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
-	Absolute accuracy	10bit	V <sub>CC1</sub> = 5.0 V (4)	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
			V <sub>CC1</sub> = 3.3 V (4)	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
			V <sub>CC1</sub> = 3.0 V (4)	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB

Notes:

1. Referenced to  $AV_{CC} = V_{CC1} = V_{CC2} = V_{REF} = 3.0$  to  $5.5$  V,  $V_{SS} = AV_{SS} = 0$  V at  $T_{opr} = -20$  to  $85^{\circ}\text{C}/-40$  to  $85^{\circ}\text{C}$  unless otherwise specified.
2. This applies when using one A/D converter, with the ADSTBY bit for the unused A/D converter set to 0 (A/D operation stopped (standby)).
3. Use when  $AV_{CC} = V_{CC1} = V_{CC2}$ .
4. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to  $V_{SS}$ . See Figure 5.2 "A/D accuracy measure circuit".

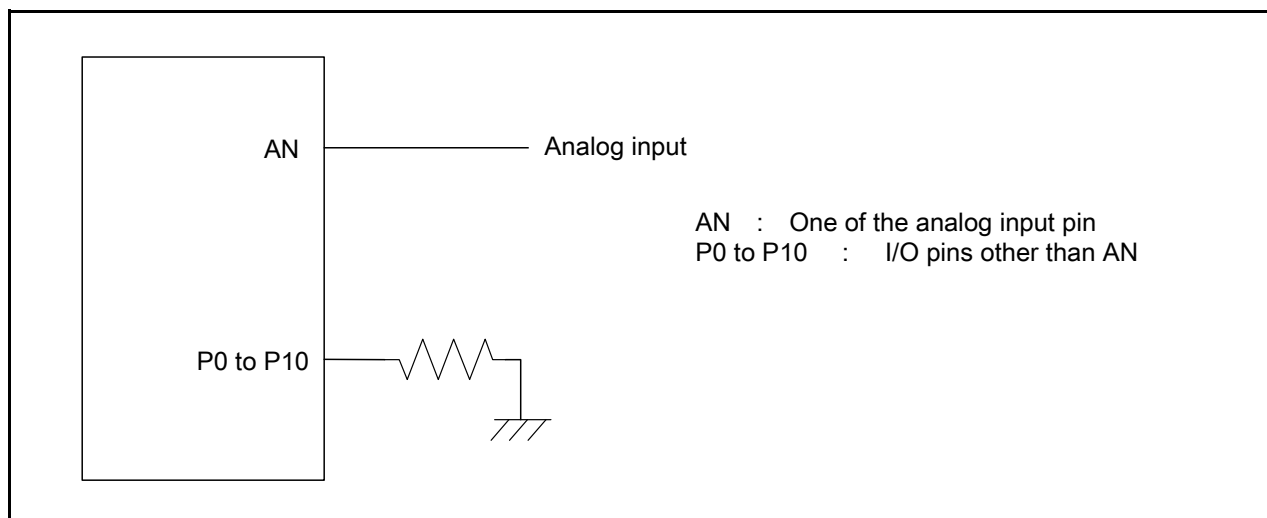


Figure 5.2 A/D accuracy measure circuit

**Table 5.6 A/D Conversion Characteristics (1, 2, 3)**

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$\phi$ AD	AD operation clock frequency	$4.0\text{ V} \leq V_{\text{REF}} \leq AV_{\text{CC}} \leq 5.5\text{ V}$	2		25	MHz
		$3.2\text{ V} \leq V_{\text{REF}} \leq AV_{\text{CC}} \leq 5.5\text{ V}$	2		16	MHz
		$3.0\text{ V} \leq V_{\text{REF}} \leq AV_{\text{CC}} \leq 5.5\text{ V}$	2		10	MHz
-	Tolerance level impedance			3		k $\Omega$
$D_{\text{NL}}$	Differential non-linearity error				$\pm 1$	LSB
-	Offset error				$\pm 3$	LSB
-	Gain error				$\pm 3$	LSB
$t_{\text{CONV}}$	10-bit conversion time	$V_{\text{CC1}} = 5\text{ V}, \phi\text{AD} = 25\text{ MHz}$	1.60			$\mu\text{s}$
$t_{\text{SAMP}}$	Sampling time		0.60			$\mu\text{s}$
$V_{\text{REF}}$	Reference voltage		3.0		$AV_{\text{CC}}$	V
$V_{\text{IA}}$	Analog input voltage <sup>(4, 5)</sup>		0		$V_{\text{REF}}$	V

Notes:

1. Referenced to  $AV_{\text{CC}} = V_{\text{CC1}} = V_{\text{CC2}} = V_{\text{REF}} = 3.0$  to  $5.5\text{ V}$ ,  $V_{\text{SS}} = AV_{\text{SS}} = 0\text{ V}$  at  $T_{\text{opr}} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified.
2. This applies when using one A/D converter, with the ADSTBY bit for the unused A/D converter set to 0 (A/D operation stopped (standby)).
3. Use when  $AV_{\text{CC}} = V_{\text{CC1}} = V_{\text{CC2}}$ .
4. Do not use A/D converter  $V_{\text{CC1}} > V_{\text{CC2}}$ .
5. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.

### 5.1.4 D/A Conversion Characteristics

**Table 5.7 D/A Conversion Characteristics (1)**

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				2.5	LSB
$t_{\text{SU}}$	Setup Time				3	$\mu\text{s}$
$R_{\text{O}}$	Output Resistance		5	6	8.2	k $\Omega$
$I_{\text{VREF}}$	Reference Power Supply Input Current	Notes 2 and 3			1.5	mA

Notes:

1. Referenced to  $V_{\text{CC1}} = AV_{\text{CC}} = V_{\text{REF}} = 3.0$  to  $5.5\text{ V}$ ,  $V_{\text{SS}} = AV_{\text{SS}} = 0\text{ V}$  at  $T_{\text{opr}} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified.
2. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to 00h.
3. The current consumption of the A/D converter is not included. Also, the  $I_{\text{VREF}}$  of the D/A converter will flow even if the ADSTBY bit in the ADCON1 register is 0 (A/D operation stopped (standby)).

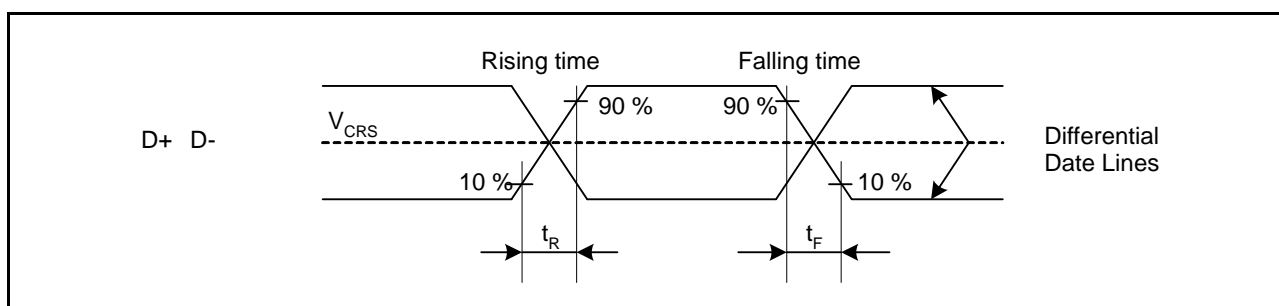
### 5.1.5 USB Characteristics

**Table 5.8 USB Characteristics <sup>(1)</sup>**

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
$V_{IH}$	Input Characteristics	HIGH Input Voltage	Figure 5.3, Figure 5.4	2.0	-	-	V
$V_{IL}$		LOW Input Voltage		-	-	0.8	V
$V_{DI}$		Differential Input Sensitivity		0.2	-	-	V
$V_{CM}$		Differential Common Mode Range		0.8	-	2.5	V
$V_{OH}$	Output Characteristics	HIGH Output Voltage	Figure 5.3, Figure 5.4 $I_{OH} = 200 \mu A$	2.8	-	-	V
$V_{OL}$		LOW Output Voltage		-	-	0.3	V
$V_{CRS}$		Crossover Voltage	Figure 5.3, Figure 5.4	1.3	-	2.0	V
$t_R$		Rise Time	Figure 5.3, Figure 5.4	4.0	-	20.0	ns
$t_F$		Fall Time	Figure 5.3, Figure 5.4	4.0	-	20.0	ns
$t_{RFM}$		Rise Time / Fall Time Matching	Figure 5.3, Figure 5.4 ( $t_R/t_F$ )	90.0	-	111.1	%
$Z_{DRV}$		Output Resistance	Figure 5.3, Figure 5.4 Includes $R_s = 27 \Omega$	28.0	-	44.0	$\Omega$
UVCC		UVCC Output Voltage	$V_{CC1} = 4.0$ to $5.5V$ , PXXCON = VDDUSBE = 1	3.0	3.3	3.6	V
		PXXCON = 0	-	$V_{CC1}$	-	V	
$I_{susp}$	Consumption current of the Internal Power Supply for USB	$V_{CC1} = 4.0$ to $5.5 V$ $UV_{CC} - V_{SS} \ 0.33 \mu F$ $V_{CC1} - V_{SS} \ 0.1 \mu F$		50		$\mu A$	

**Notes:**

1. Referenced to  $V_{CC1} = 3.0$  to  $5.5 V$ ,  $UV_{CC} = 3.0$  to  $3.6 V$ , at  $T_{opr} = -20$  to  $85 \text{ }^\circ C$  /  $-40$  to  $85 \text{ }^\circ C$  unless otherwise specified.


**Figure 5.3 Data Signal Timing Diagram**

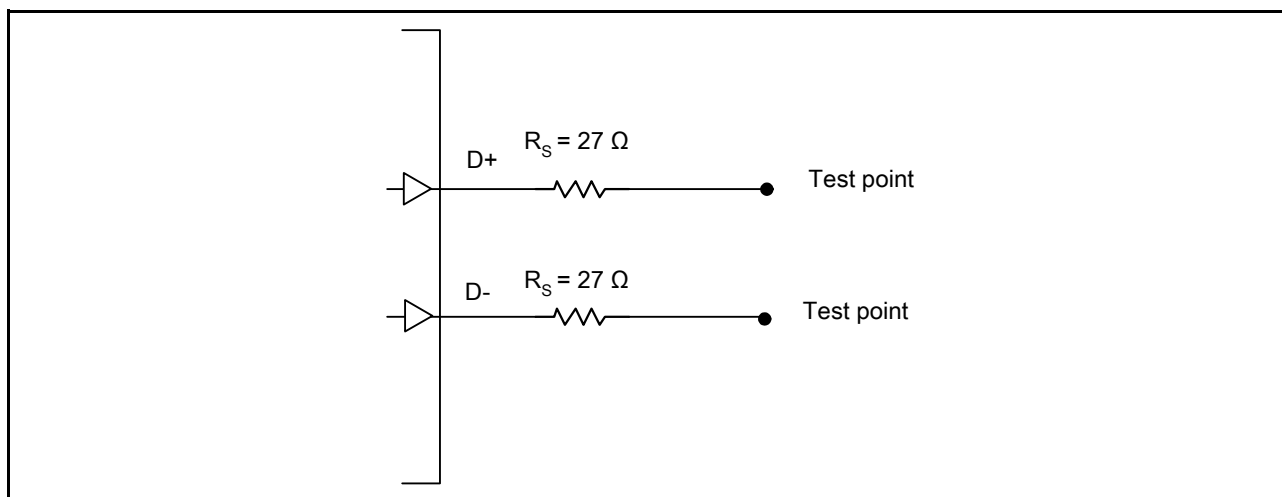


Figure 5.4 Load Condition

### 5.1.6 Flash Memory Electrical Characteristics

**Table 5.9 CPU Clock When Operating Flash Memory ( $f_{(BCLK)}$ )**

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	CPU rewrite mode				10 (1)	MHz
f(SLOW_R)	Slow read mode				5(3)	MHz
-	Low current consumption read mode				35	kHz
-	Data flash read	$2.7\text{ V} \leq V_{CC1} \leq 3.0\text{ V}$			16 (2)	MHz
		$3.0\text{ V} < V_{CC1} \leq 5.5\text{ V}$			20 (2)	MHz

**Notes:**

1. Set the PM17 bit in the PM1 register to 1 (one wait).
2. When the frequency is over this value, set the FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait)
3. Set the PM17 bit in the PM1 register to 1(one wait). A wait is not necessary when using 125 kHz on-chip oscillator clock or sub clock as the CPU clock source.

**Table 5.10 Flash Memory (Program ROM 1, 2) Electrical Characteristics**

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program/erase cycles (2, 4, 5)	$V_{CC1} = 3.3\text{ V}$ , $T_{opr} = 25^\circ\text{C}$	1,000 (3)			times
-	Two words program time	$V_{CC1} = 3.3\text{ V}$ , $T_{opr} = 25^\circ\text{C}$		150	4000	$\mu\text{s}$
-	Lock bit program time	$V_{CC1} = 3.3\text{ V}$ , $T_{opr} = 25^\circ\text{C}$		70	3000	$\mu\text{s}$
-	Block erase time	$V_{CC1} = 3.3\text{ V}$ , $T_{opr} = 25^\circ\text{C}$		0.2	3.0	s
-	Program, erase voltage		2.7		5.5	V
-	Read voltage		2.7		5.5	V
-	Program, erase temperature		0		60	$^\circ\text{C}$
t <sub>PS</sub>	Flash Memory Circuit Stabilization Wait Time				50	$\mu\text{s}$
-	Data hold time (7)	Ambient temperature = $55^\circ\text{C}$		20		year

**Notes:**

1.  $V_{CC1} = 2.7$  to  $5.5\text{ V}$  at  $T_{opr} = 0$  to  $60^\circ\text{C}$  (option:  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ ), unless otherwise specified.
2. Definition of program and erase cycles  
The program and erase cycles refer to the number of per-block erasures.  
If the program and erase cycles are n ( $n=1,000$ ), each block can be erased n times.  
For example, if a 4 Kbyte block is erased after writing two word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
3. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.11 Flash Memory (Data Flash) Electrical Characteristics**

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program/erase cycles <sup>(2, 4, 5)</sup>	$V_{CC1} = 3.3 \text{ V}$ , $T_{opr} = 25^\circ\text{C}$	10,000 <sup>(3)</sup>			times
-	Two words program time	$V_{CC1} = 3.3 \text{ V}$ , $T_{opr} = 25^\circ\text{C}$		300	4000	$\mu\text{s}$
-	Lock bit program time	$V_{CC1} = 3.3 \text{ V}$ , $T_{opr} = 25^\circ\text{C}$		140	3000	$\mu\text{s}$
-	Block erase time	$V_{CC1} = 3.3 \text{ V}$ , $T_{opr} = 25^\circ\text{C}$		0.2	3.0	s
-	Program, erase voltage		2.7		5.5	V
-	Read voltage		2.7		5.5	V
-	Program, erase temperature		0		60	$^\circ\text{C}$
$t_{PS}$	Flash Memory Circuit Stabilization Wait Time				50	$\mu\text{s}$
-	Data hold time <sup>(7)</sup>	Ambient temperature = $55^\circ\text{C}$		20		year

## Notes:

- $V_{CC1} = 2.7$  to  $5.5 \text{ V}$  at  $T_{opr} = 0$  to  $60^\circ\text{C}$  unless otherwise specified.
- Definition of program and erase cycles  
The program and erase cycles refer to the number of per-block erasures.  
If the program and erase cycles are  $n$  ( $n=10,000$ ), each block can be erased  $n$  times.  
For example, if a 4 Kbyte block is erased after writing two word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
- Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- The data hold time includes time that the power supply is off or the clock is not supplied.

### 5.1.7 Voltage Detection Circuit and Power Supply Circuit Electrical Characteristics

**Table 5.12 Voltage Detection 0 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det0</sub>	Voltage detection level Vdet0_0 (2)		1.60	1.90	2.20	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.15	V
-	Voltage detection 0 circuit response time(4)	At the falling of V <sub>CC</sub> from 5 V to (Vdet 0_0 - 0.1)V	-	-	200	μs
-	Voltage detection circuit self power consumption	VC25 = 1, V <sub>CC1</sub> = 5.0 V		1.5		μA
t <sub>d(E-A)</sub>	Waiting time until voltage detection circuit operation starts (3)				100	μs

Notes:

1. The measurement condition is T<sub>opr</sub> = -20 to 85°C/-40 to 85°C.
2. Select the voltage detection level with the VDSEL1 bit in the OFS1 address.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.
4. Necessary time until the voltage monitor 0 reset generates after passing through V<sub>det0</sub>.

**Table 5.13 Voltage Detection 1 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det1</sub>	Voltage detection level Vdet1	When V <sub>CC</sub> is falling	2.95	3.25	3.55	V
-	Hysteresis width at the rising of V <sub>CC</sub> of Voltage detection 1 circuit		-	0.15	-	V
-	Voltage detection 1 circuit response time(2)	At the falling of V <sub>CC</sub> from 5 V to (Vdet 1 - 0.1)V	-	-	200	μs
-	Voltage detection circuit self power consumption	VC26 = 1, V <sub>CC1</sub> = 5.0 V		1.7		μA
t <sub>d(E-A)</sub>	Waiting time until voltage detection circuit operation starts (3)				100	μs

Notes:

1. The measurement condition is T<sub>opr</sub> = -20 to 85°C/-40 to 85°C.
2. Necessary time until the voltage monitor 1 interrupt request generates after passing through V<sub>det1</sub>.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VC26 bit in the VCR2 register to 0.

**Table 5.14 Voltage Detection 2 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det2</sub>	Voltage detection level Vdet2	When V <sub>CC</sub> is falling	3.70	4.00	4.30	V
-	Hysteresis width at the rising of V <sub>CC</sub> in voltage detection 2 circuit		-	0.15	-	V
-	Voltage detection 2 circuit response time(2)	At the falling of V <sub>CC</sub> from 5 V to (Vdet 2 - 0.1)V	-	-	200	μs
-	Voltage detection circuit self power consumption	VC27 = 1, V <sub>CC1</sub> = 5.0 V		1.7		μA
t <sub>d(E-A)</sub>	Waiting time until voltage detection circuit operation starts (2)				100	μs

Notes:

1. The measurement condition is T<sub>opr</sub> = -20 to 85°C/-40 to 85°C.
2. Necessary time until the voltage monitor 2 interrupt request generates after passing through V<sub>det2</sub>
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VC27 bit in the VCR2 register to 0.

**Table 5.15 Power-On Reset Circuit**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{rth}$	External power $V_{CC1}$ rise gradient	$V_{CC1} = 2.0$ to $5.5V$	2.0		50000	mV/ms

## Notes:

1. The measurement condition is  $T_{opr} = -20$  to  $85^{\circ}C$  /  $-40$  to  $85^{\circ}C$ , unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0.

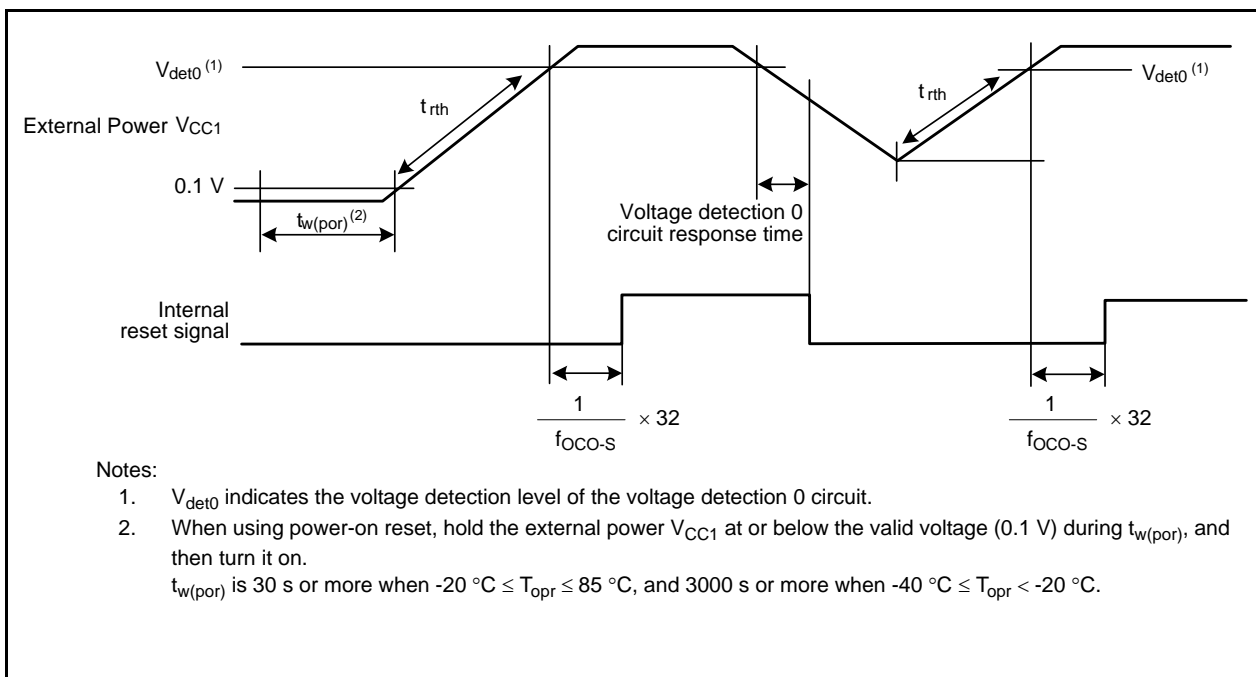


Figure 5.5 Power-On Reset Circuit Electrical Characteristics

Table 5.16 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Internal power supply stability time when power is on <sup>(2)</sup>				5	ms
$t_{d(R-S)}$	STOP release time				150	$\mu\text{s}$
$t_{d(W-S)}$	Low power mode wait mode release time				150	$\mu\text{s}$

Notes:

- The measurement condition is  $V_{CC1} = 2.7$  to  $5.5\text{ V}$  and  $T_{opr} = 25\text{ }^{\circ}\text{C}$ .
- Waiting time until the internal power supply generation circuit stabilizes when power is on.

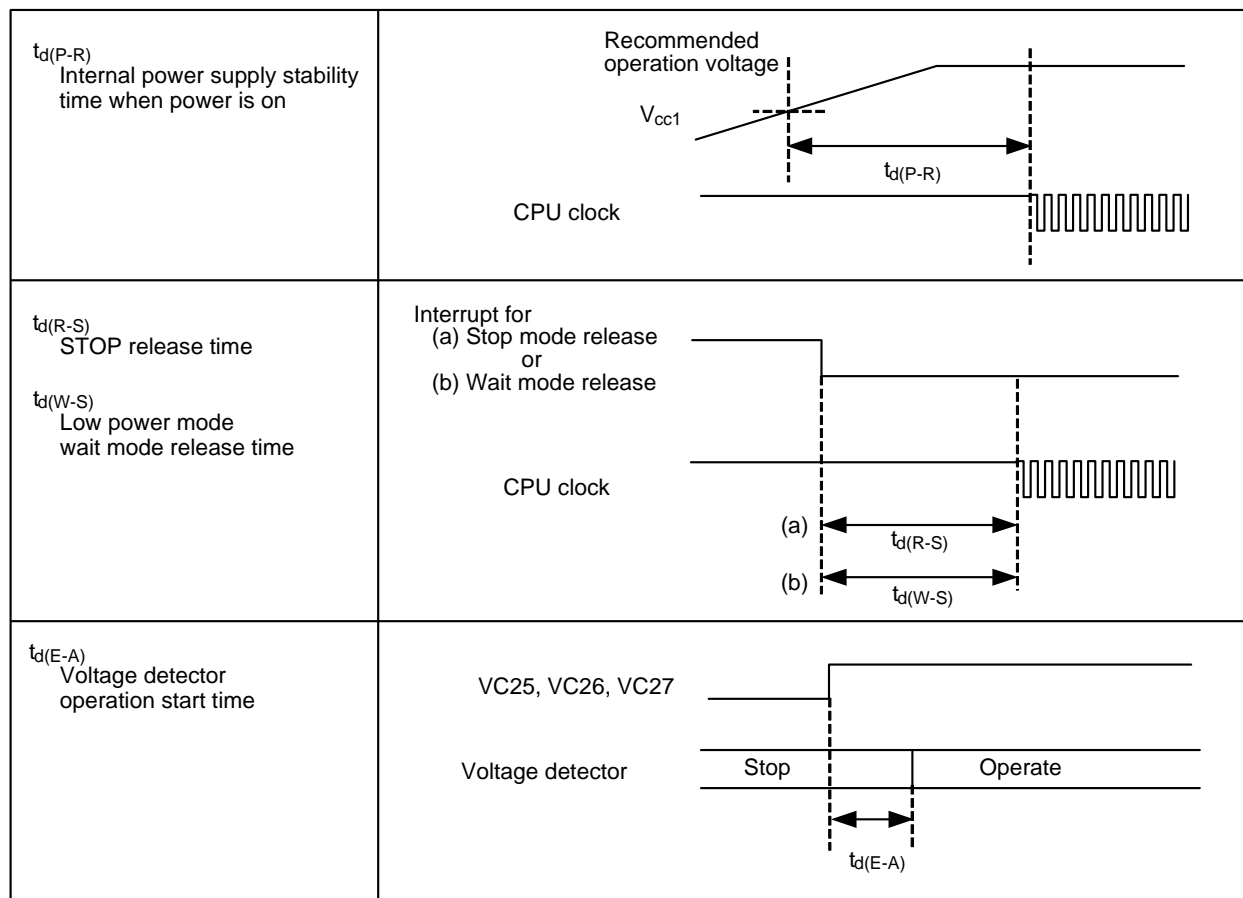


Figure 5.6 Power Supply Circuit Timing Diagram

### 5.1.8 Oscillation Circuit Electrical Characteristics

**Table 5.17 40 MHz On-Chip Oscillator Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$f_{\text{OCO40M}}$	40 MHz on-chip oscillator frequency	Average frequency in a 10 ms period $2.7 \text{ V} \leq V_{\text{CC1}} < 5.5 \text{ V}$	36	40	44	MHz
$t_{\text{su}(f_{\text{OCO40M}})}$	Wait time until 40 MHz on-chip oscillator stabilizes				2	ms

Note:

- $V_{\text{CC1}} = 2.7$  to  $5.5 \text{ V}$ ,  $T_{\text{opr}} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$ , unless otherwise specified.

**Table 5.18 125 kHz On-Chip Oscillator Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$f_{\text{OCO-S}}$	125 kHz on-chip oscillator frequency	Average frequency in a 10 ms period	100	125	150	kHz
$t_{\text{su}(f_{\text{OCO-S}})}$	Wait time until 125 kHz on-chip oscillator stabilizes				20	$\mu\text{s}$

Note:

- $V_{\text{CC1}} = 2.7$  to  $5.5 \text{ V}$ ,  $T_{\text{opr}} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$ , unless otherwise specified.

## 5.2 Electrical Characteristics ( $V_{CC1} = V_{CC2} = 5\text{ V}$ )

### 5.2.1 Electrical Characteristics

$$V_{CC1} = V_{CC2} = 5\text{ V}$$

**Table 5.19 Electrical Characteristics (1) (1, 2)**

Symbol	Parameter		Measuring Condition	Standard			Unit	
				Min.	Typ.	Max.		
$V_{OH}$	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	$I_{OH} = -5\text{ mA}$	$V_{CC1} - 2.0$		$V_{CC1}$	V	
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	$I_{OH} = -5\text{ mA}$	$V_{CC2} - 2.0$		$V_{CC2}$		
$V_{OH}$	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	$I_{OH} = -200\text{ }\mu\text{A}$	$V_{CC1} - 0.3$		$V_{CC1}$	V	
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	$I_{OH} = -200\text{ }\mu\text{A}$	$V_{CC2} - 0.3$		$V_{CC2}$		
$V_{OH}$	High output voltage	XOUT	HIGHPOWER	$I_{OH} = -1\text{ mA}$	$V_{CC1} - 2.0$		$V_{CC1}$	V
			LOWPOWER	$I_{OH} = -0.5\text{ mA}$	$V_{CC1} - 2.0$		$V_{CC1}$	
	High output voltage	XCOUT	HIGHPOWER	With no load applied		2.6		V
			LOWPOWER	With no load applied		2.2		
$V_{OL}$	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7	$I_{OL} = 5\text{ mA}$			2.0	V	
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	$I_{OL} = 5\text{ mA}$			2.0		
$V_{OL}$	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7	$I_{OL} = 200\text{ }\mu\text{A}$			0.45	V	
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	$I_{OL} = 200\text{ }\mu\text{A}$			0.45		
$V_{OL}$	Low output voltage	XOUT	HIGHPOWER	$I_{OL} = 1\text{ mA}$			2.0	V
			LOWPOWER	$I_{OL} = 0.5\text{ mA}$			2.0	
	Low output voltage	XCOUT	HIGHPOWER	With no load applied		0		V
			LOWPOWER	With no load applied		0		

Notes:

1. Referenced to  $V_{CC1} = V_{CC2} = 4.2\text{ to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{opr} = -20\text{ to }85^\circ\text{C}/-40\text{ to }85^\circ\text{C}$  unless otherwise specified.
2. When  $V_{CC1} \neq V_{CC2}$ , refer to 5 V or 3 V standard depending on the voltage.

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

Table 5.20 Electrical Characteristics (2) (1, 2)

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT7, NMI, ADTRG, CTS0 to CTS5, SCL0 to SCL5, SDA0 to SDA5, CLK0 to CLK5, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD5, SD, SCLMM, SDAMM		0.5		2.0	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{\text{RESET}}$		0.5		2.5	V
$I_{IH}$	High input current P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{\text{RESET}}$ , CNVSS	$V_I = 5 \text{ V}$			5.0	$\mu\text{A}$
$I_{IL}$	Low input current P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{\text{RESET}}$ , CNVSS	$V_I = 0 \text{ V}$			-5.0	$\mu\text{A}$
$R_{PULLUP}$	Pull-up resistance P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	$V_I = 0 \text{ V}$	30	50	100	$\text{k}\Omega$
$R_{fXIN}$	Feedback resistance XIN			1.5		$\text{M}\Omega$
$R_{fXCIN}$	Feedback resistance XCIN			8		$\text{M}\Omega$
$V_{RAM}$	RAM retention voltage	In stop mode	1.8			V

## Notes:

1. Referenced to  $V_{CC1} = V_{CC2} = 4.2$  to  $5.5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$  at  $T_{opr} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified.
2. When  $V_{CC1} \neq V_{CC2}$ , refer to 5 V or 3 V standard depending on the voltage.

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

Table 5.21 Electrical Characteristics (3) (1)

Symbol	Parameter	Measuring Condition	Standard			Unit	
			Min.	Typ.	Max.		
I <sub>CC</sub>	Power supply current  In single-chip mode, the output pin are open and other pins are V <sub>SS</sub>	High-speed mode	f <sub>(BCLK)</sub> = 32 MHz XIN = 4MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stop		27.0		mA
			f <sub>(BCLK)</sub> = 32 MHz, A/D conversion <sup>(3)</sup> XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stop		27.7		mA
			f <sub>(BCLK)</sub> = 16 MHz XIN = 16MHz (square wave), 125 kHz on-chip oscillator stop		13.0		mA
		40 MHz on-chip oscillator mode	Main clock stop 40 MHz on-chip oscillator on, no division 125 kHz on-chip oscillator stop		17.0		mA
		125 kHz on-chip oscillator Low-power mode	Main clock stop 40 MHz on-chip oscillator stop 125 kHz on-chip oscillator on, no division FMR22 = 1		500.0		μA
		Low-power mode	f <sub>(BCLK)</sub> = 32 kHz In low-power mode, FMR22 = FMR23 = 1 on flash memory <sup>(2)</sup>		160.0		μA
			f <sub>(BCLK)</sub> = 32 kHz In low-power mode, on RAM <sup>(2)</sup>		45.0		μA
		Wait mode	Main clock stop 40 MHz on-chip oscillator stop 125 kHz on-chip oscillator on Peripheral clock operation T <sub>opr</sub> = 25°C		21.0		μA
			f <sub>(XCIN)</sub> = 32 kHz (oscillation capacity High) 40 MHz on-chip oscillator stop 125 kHz on-chip oscillator stop Peripheral clock operation T <sub>opr</sub> = 25°C		11.0		μA
			f <sub>(XCIN)</sub> = 32 kHz (oscillation capacity Low) 40 MHz on-chip oscillator stop 125 kHz on-chip oscillator stop Peripheral clock operation T <sub>opr</sub> = 25°C		6.0		μA
		Stop mode	Main clock stop 40MHz on-chip oscillator stop 125 kHz on-chip oscillator stop Peripheral clock stop T <sub>opr</sub> = 25°C		2.2		μA

## Notes:

1. Referenced to V<sub>CC1</sub> = V<sub>CC2</sub> = 4.2 to 5.5 V, V<sub>SS</sub> = 0 V at T<sub>opr</sub> = -20 to 85°C/-40 to 85°C, f<sub>(BCLK)</sub> = 32 MHz unless otherwise specified.
2. This indicates the memory in which the program to be executed exists.
3. This applies when using one A/D converter (φAD=25MHz), with the ADSTBY bit for the unused A/D converter set to 0 (A/D operation stopped (standby)).

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

### 5.2.2 Timing Requirements (Peripheral Functions and Others)

( $V_{CC1} = V_{CC2} = 5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , at  $T_{opr} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified)

**Table 5.22 External Clock Input (XIN Input) (1)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c$	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
$t_r$	External clock rise time		9	ns
$t_f$	External clock fall time		9	ns

Note:

- The condition is  $V_{CC1} = V_{CC2} = 3.0$  to  $5.0 \text{ V}$ .

**Table 5.23 Timer A Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input high pulse width	40		ns
$t_{w(TAL)}$	TAiIN input low pulse width	40		ns

**Table 5.24 Timer A Input (Gating Input in Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high pulse width	200		ns
$t_{w(TAL)}$	TAiIN input low pulse width	200		ns

**Table 5.25 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

**Table 5.26 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

**Table 5.27 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

$$V_{CC1} = V_{CC2} = 5\text{ V}$$

**Timing Requirements**

( $V_{CC1} = V_{CC2} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -20\text{ to }85^\circ\text{C}/-40\text{ to }85^\circ\text{C}$  unless otherwise specified)

**Table 5.28 Timer B Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on both edges)	80		ns

**Table 5.29 Timer B Input (Pulse Period Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

**Table 5.30 Timer B Input (Pulse Width Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

**Table 5.31 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high pulse width	100		ns
$t_{w(CKL)}$	CLKi input low pulse width	100		ns
$t_d(C-Q)$	TXDi output delay time		80	ns
$t_h(C-Q)$	TXDi hold time	0		ns
$t_{su}(D-C)$	RXDi input setup time	70		ns
$t_h(C-D)$	RXDi input hold time	90		ns

**Table 5.32 External Interrupt  $\overline{INTi}$  Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	250		ns

**Table 5.33 Reset Input ( $\overline{RESET}$  Input)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{RESET}$ input low pulse width	10		$\mu\text{s}$

$$V_{CC1} = V_{CC2} = 5\text{ V}$$

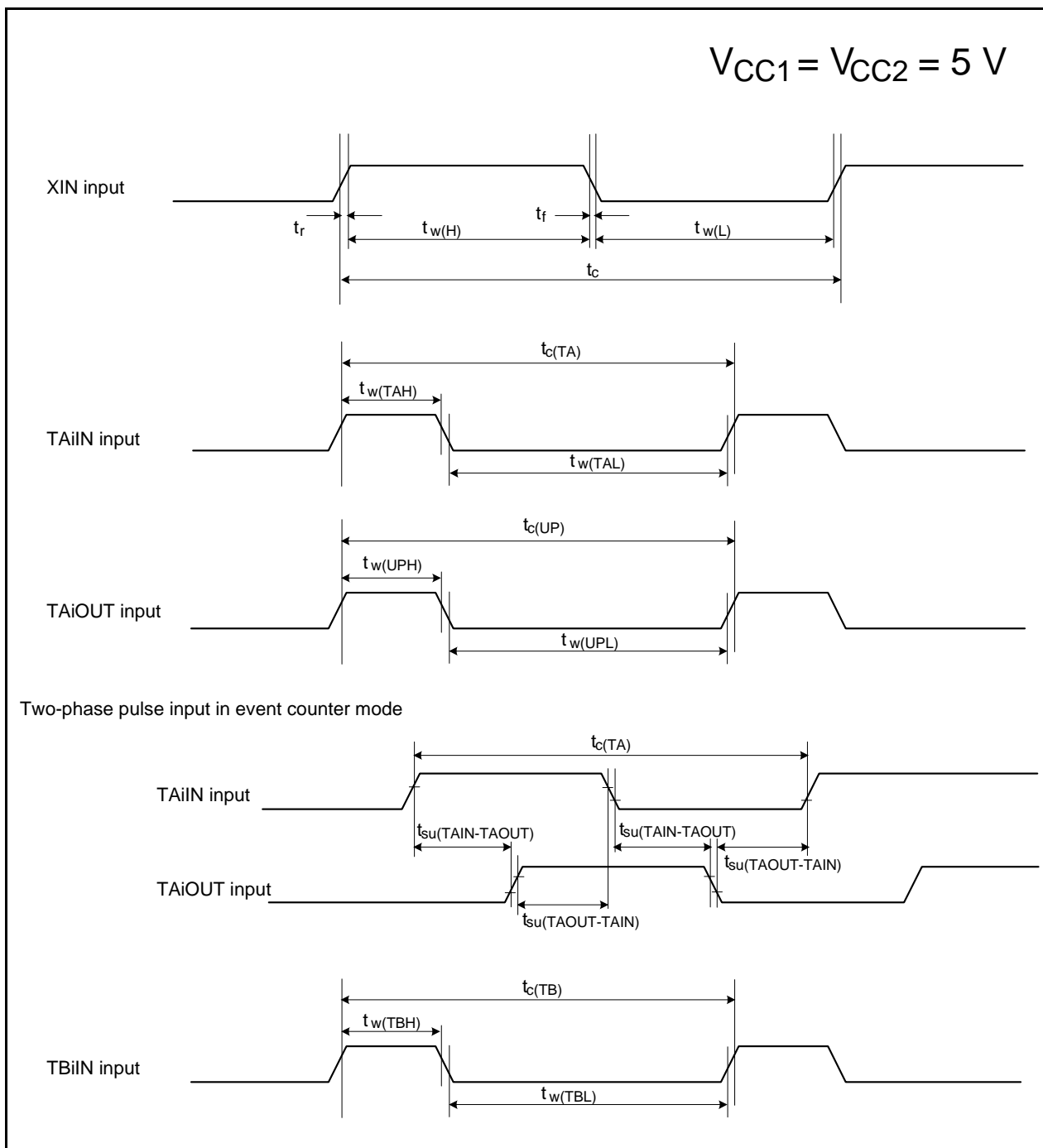


Figure 5.7 Timing Diagram (1)

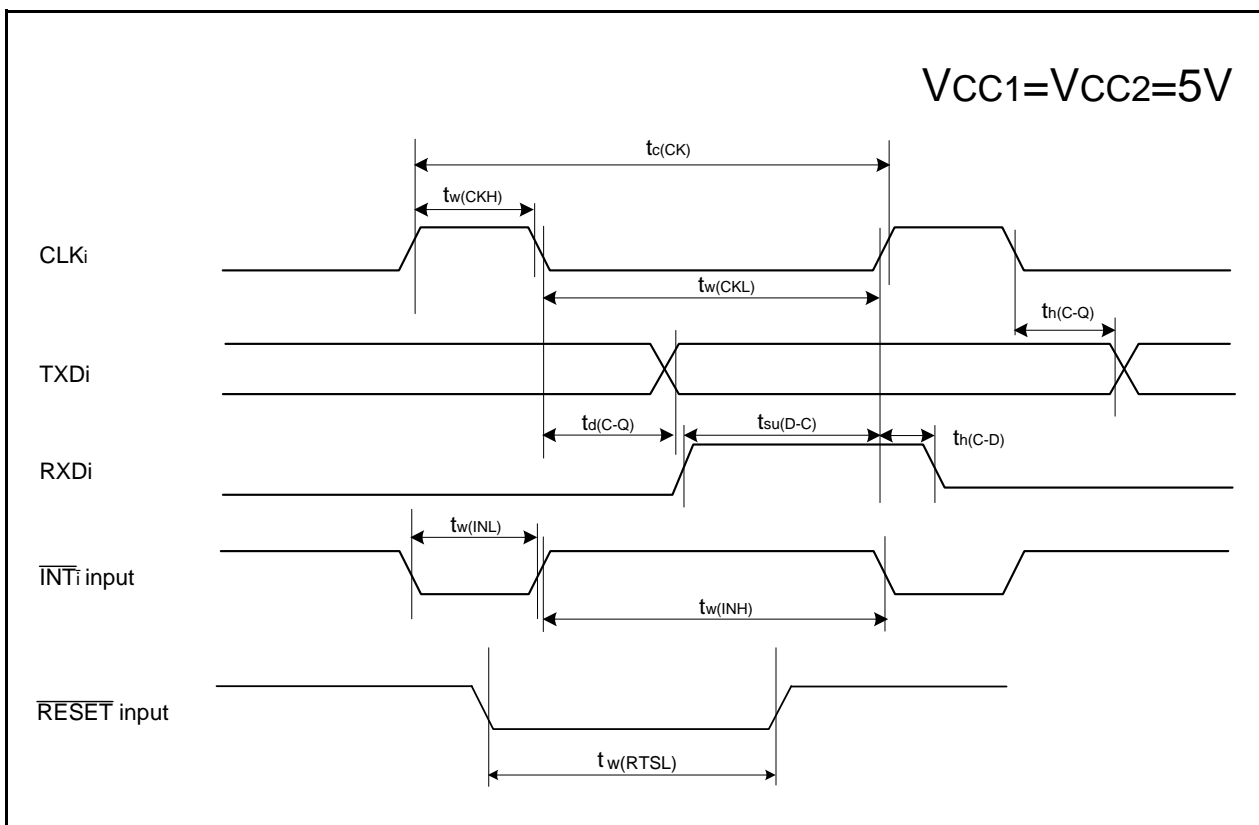


Figure 5.8 Timing Diagram (2)

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

### 5.2.3 Timing Requirements (Memory Expansion Mode and Microprocessor Mode)

( $V_{CC1} = V_{CC2} = 5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , at  $T_{opr} = -20 \text{ to } 85^\circ\text{C}/-40 \text{ to } 85^\circ\text{C}$  unless otherwise specified)

**Table 5.34 Memory Expansion Mode and Microprocessor Mode**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1}(\text{RD-DB})$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2}(\text{RD-DB})$	Data input access time (for setting with 1 to 3 waits)		(Note 2)	ns
$t_{ac3}(\text{RD-DB})$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{su}(\text{DB-RD})$	Data input setup time	40		ns
$t_{su}(\text{RDY-BCLK})$	$\overline{\text{RDY}}$ input setup time	30		ns
$t_{su}(\text{HOLD-BCLK})$	$\overline{\text{HOLD}}$ input setup time	40		ns
$t_h(\text{RD-DB})$	Data input hold time	0		ns
$t_h(\text{BCLK-RDY})$	$\overline{\text{RDY}}$ input hold time	0		ns
$t_h(\text{BCLK-HOLD})$	$\overline{\text{HOLD}}$ input hold time	0		ns

**Notes:**

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(\text{BCLK})}} - 45[\text{ns}]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n + 0.5) \times 10^9}{f_{(\text{BCLK})}} - 45[\text{ns}] \quad n \text{ is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(\text{BCLK})}} - 45[\text{ns}] \quad n \text{ is 2 for 2 waits setting, and 3 for 3 waits setting.}$$

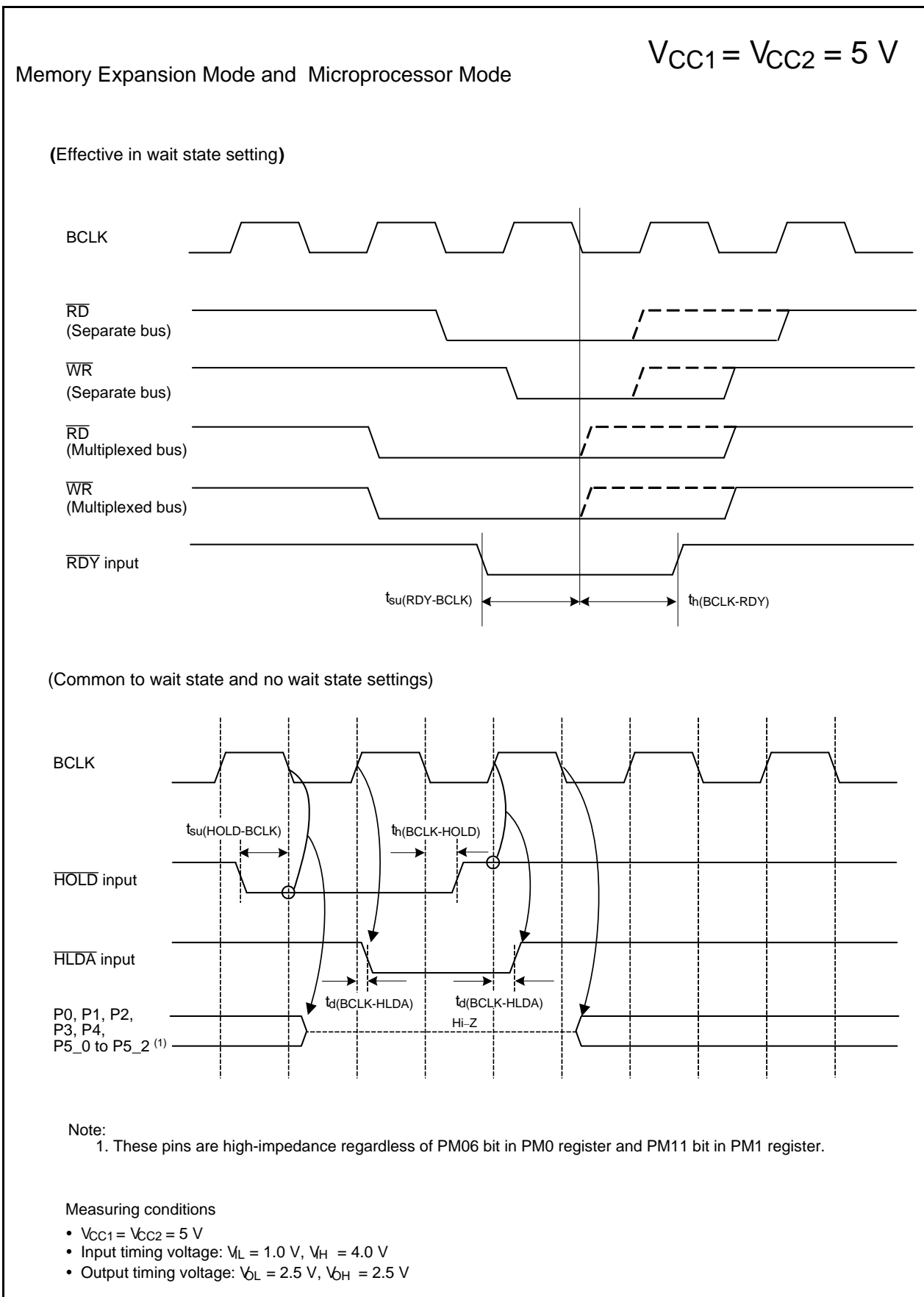


Figure 5.9 Timing Diagram

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

### 5.2.4 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode (in No Wait State Setting))

( $V_{CC1} = V_{CC2} = 5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , at  $T_{opr} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified)

**Table 5.35 Memory Expansion Mode and Microprocessor Mode (in No Wait State Setting)**

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(\text{BCLK-AD})}$	Address output delay time	See Figure 5.10		25	ns
$t_{h(\text{BCLK-AD})}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(\text{RD-AD})}$	Address output hold time (in relation to RD)		0		ns
$t_{h(\text{WR-AD})}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(\text{BCLK-CS})}$	Chip select output delay time			25	ns
$t_{h(\text{BCLK-CS})}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(\text{BCLK-ALE})}$	ALE signal output delay time			15	ns
$t_{h(\text{BCLK-ALE})}$	ALE signal output hold time		-4		ns
$t_{d(\text{BCLK-RD})}$	RD signal output delay time			25	ns
$t_{h(\text{BCLK-RD})}$	RD signal output hold time		0		ns
$t_{d(\text{BCLK-WR})}$	WR signal output delay time			25	ns
$t_{h(\text{BCLK-WR})}$	WR signal output hold time		0		ns
$t_{d(\text{BCLK-DB})}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(\text{BCLK-DB})}$	Data output hold time (in relation to BCLK) <sup>(3)</sup>		0		ns
$t_{d(\text{DB-WR})}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(\text{WR-DB})}$	Data output hold time (in relation to WR) <sup>(3)</sup>		(Note 2)		ns
$t_{d(\text{BCLK-HLDA})}$	HLDA output delay time		40	ns	

**Notes:**

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(\text{BCLK})}} - 40[\text{ns}] \quad f_{(\text{BCLK})} \text{ is } 12.5 \text{ MHz or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(\text{BCLK})}} - 10[\text{ns}]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

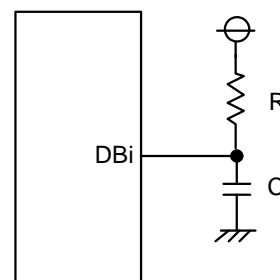
Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$$

by a circuit of the right figure.

For example, when  $V_{OL} = 0.2V_{CC2}$ ,  $C = 30 \text{ pF}$ ,  $R = 1 \text{ k}\Omega$ , hold time of output low level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2}) = 6.7 \text{ ns.}$$



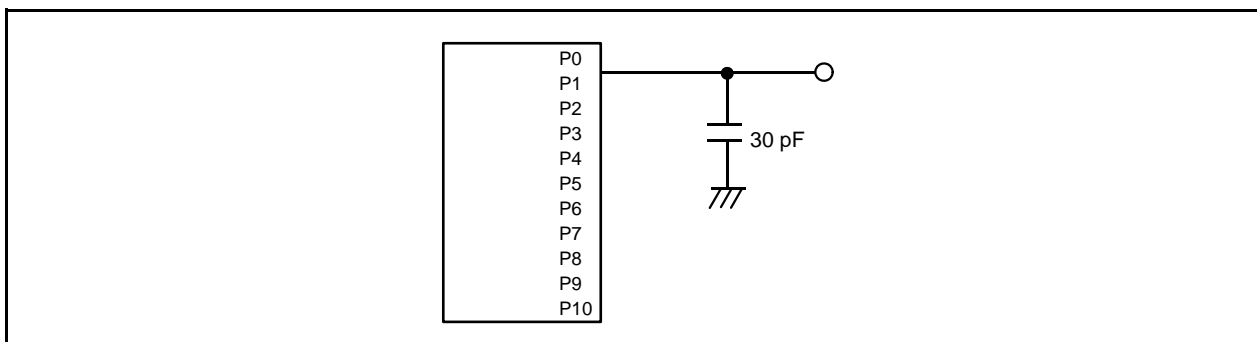


Figure 5.10 Ports P0 to P10 Measurement Circuit

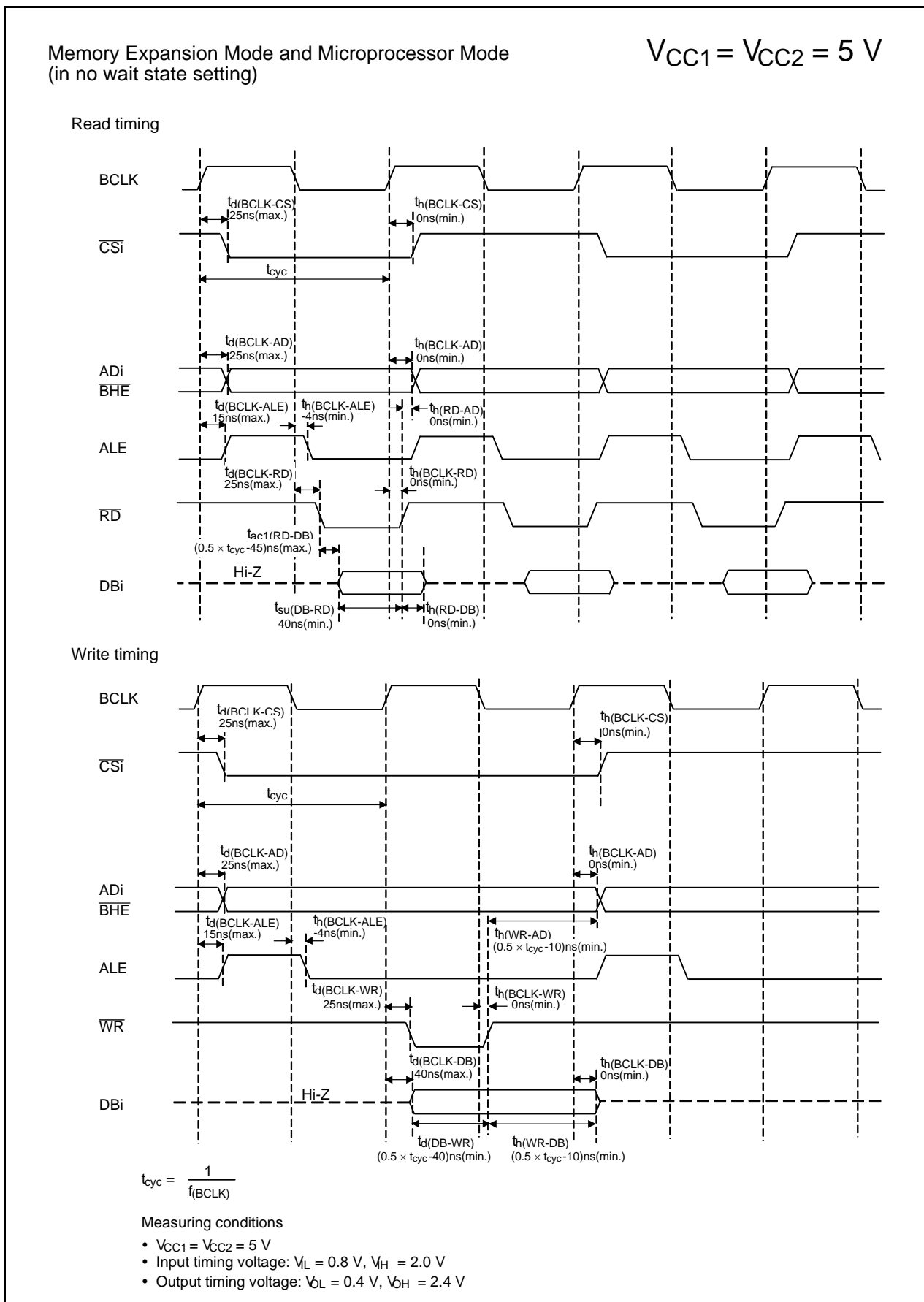


Figure 5.11 Timing Diagram

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

### 5.2.5 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area))

( $V_{CC1} = V_{CC2} = 5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , at  $T_{opr} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified)

**Table 5.36 Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area)**

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.10		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) <sup>(3)</sup>		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) <sup>(3)</sup>		(Note 2)		ns
$t_{d(BCLK-HLDA)}$	HLDA output delay time		40	ns	

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 40 [\text{ns}] \quad \begin{array}{l} n \text{ is } 1 \text{ for } 1 \text{ wait setting, } 2 \text{ for } 2 \text{ waits setting and } 3 \text{ for } 3 \text{ waits setting.} \\ \text{When } n = 1, f_{(BCLK)} \text{ is } 12.5 \text{ MHz or less.} \end{array}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10 [\text{ns}]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$$

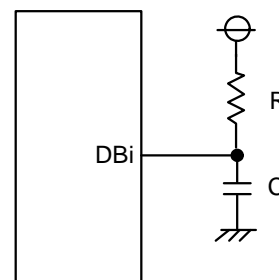
by a circuit of the right figure.

For example, when  $V_{OL} = 0.2V_{CC2}$ ,  $C = 30 \text{ pF}$ ,  $R = 1 \text{ k}\Omega$ ,

hold time of output low level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$$

= 6.7 ns.



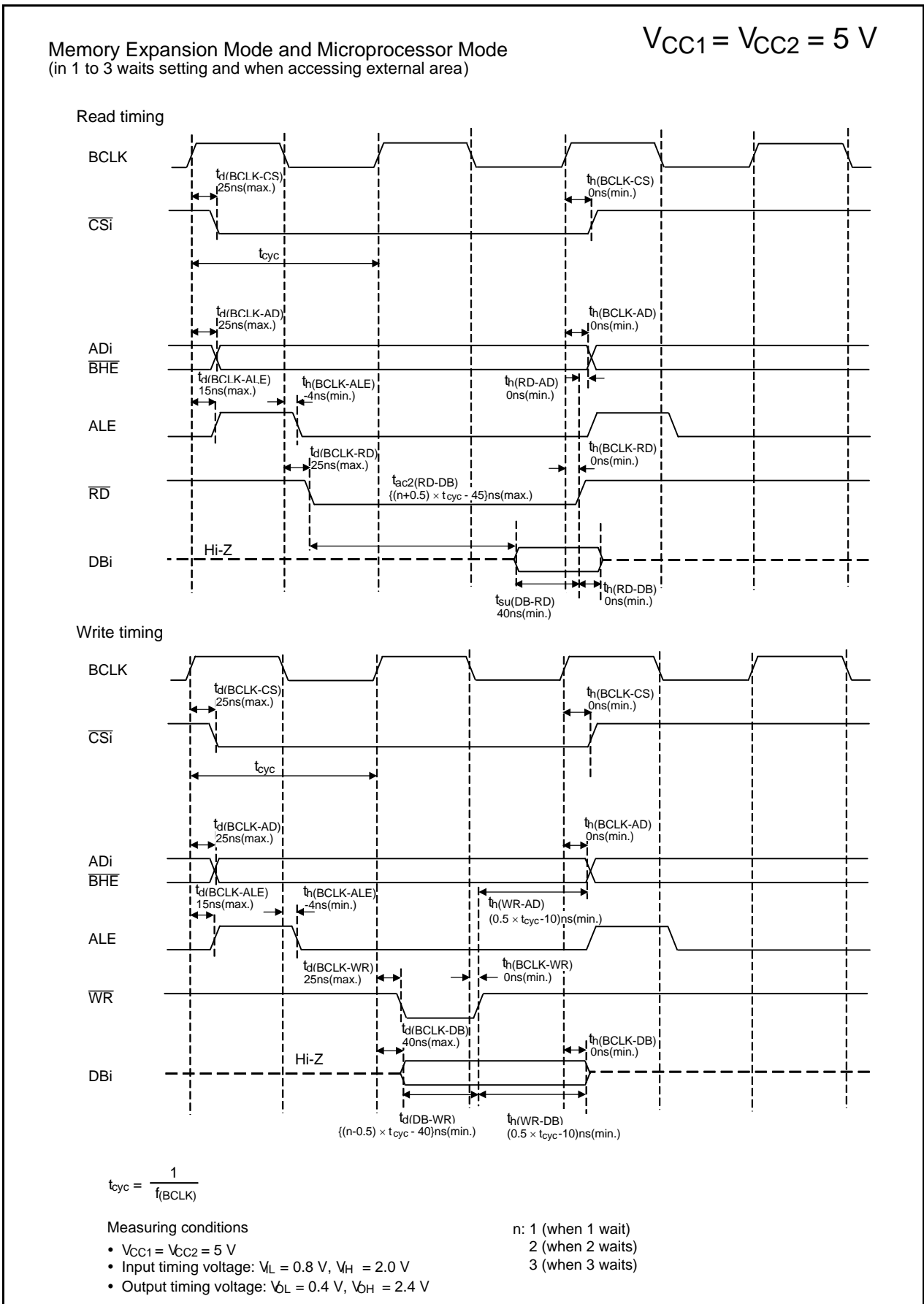


Figure 5.12 Timing Diagram

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

### 5.2.6 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode (in 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus))

( $V_{CC1} = V_{CC2} = 5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , at  $T_{opr} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified)

**Table 5.37 Memory Expansion Mode and Microprocessor Mode (in 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus) (5)**

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.10		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{h(RD-CS)}$	Chip select output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time			40	ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (in relation to BCLK)			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (in relation to BCLK)		-4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (in relation to Address)		(Note 3)		ns
$t_{h(AD-ALE)}$	ALE signal output hold time (in relation to Address)	(Note 4)		ns	
$t_{d(AD-RD)}$	RD signal output delay from the end of address	0		ns	
$t_{d(AD-WR)}$	WR signal output delay from the end of address	0		ns	
$t_{dz(RD-AD)}$	Address output floating start time		8	ns	

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10 [\text{ns}]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 40 [\text{ns}] \quad n \text{ is 2 for 2-wait setting, 3 for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 25 [\text{ns}]$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 15 [\text{ns}]$$

5. When using multiplex bus, set  $f_{(BCLK)}$  12.5 MHz or less.

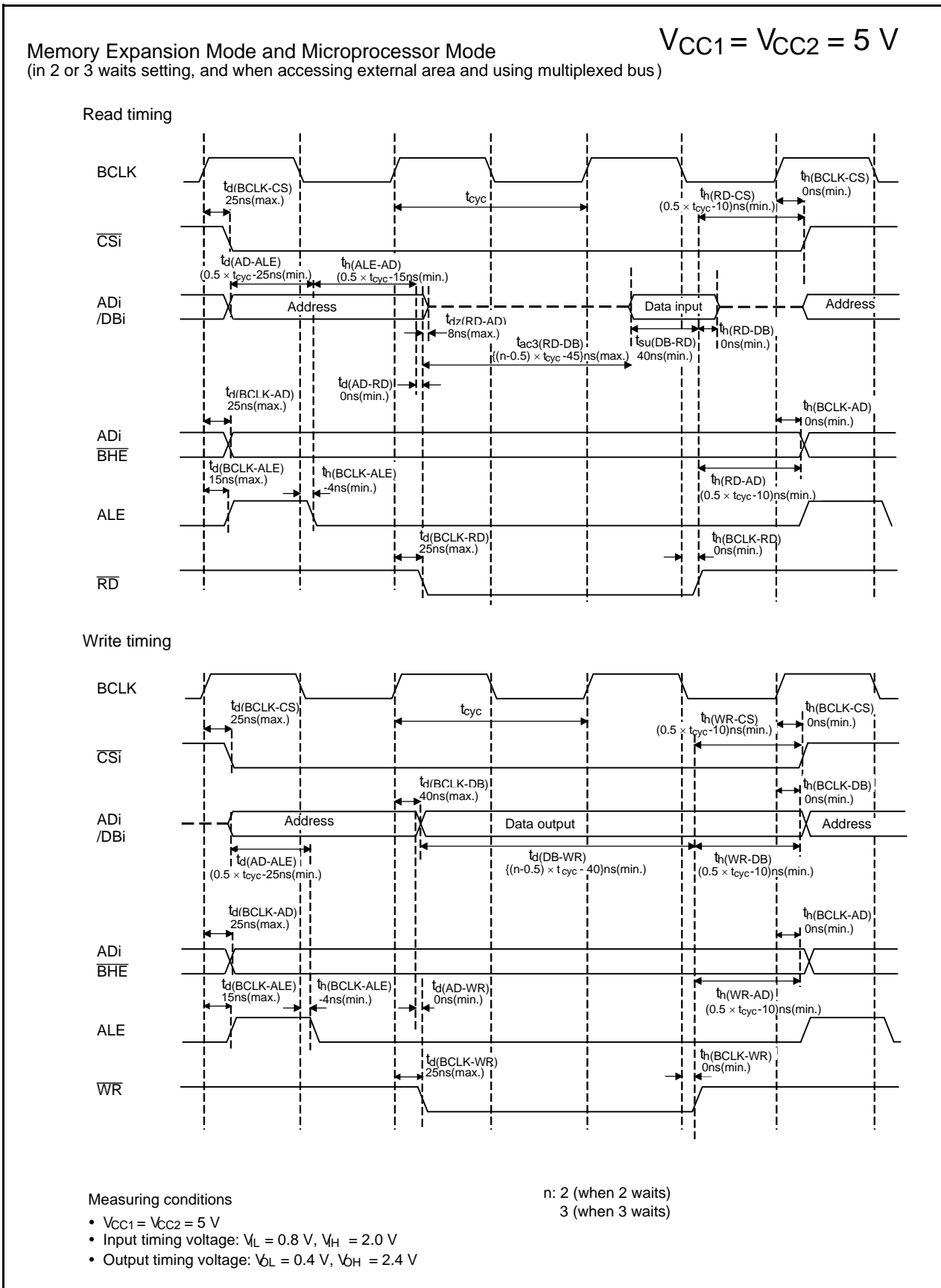


Figure 5.13 Timing Diagram

### 5.3 Electrical Characteristics ( $V_{CC1} = V_{CC2} = 3\text{ V}$ )

#### 5.3.1 Electrical Characteristics

$$V_{CC1} = V_{CC2} = 3\text{ V}$$

Table 5.38 Electrical Characteristics (1) (1, 2)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
$V_{OH}$	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	$I_{OH} = -1\text{ mA}$	$V_{CC1} - 0.5$		$V_{CC1}$	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	$I_{OH} = -1\text{ mA}$	$V_{CC2} - 0.5$		$V_{CC2}$	
$V_{OH}$	High output voltage	XOUT	HIGHPOWER	$I_{OH} = -0.1\text{ mA}$	$V_{CC1} - 0.5$	$V_{CC1}$	V
			LOWPOWER	$I_{OH} = -50\text{ }\mu\text{A}$	$V_{CC1} - 0.5$	$V_{CC1}$	
	High output voltage	XCOUT	HIGHPOWER	With no load applied		2.6	V
			LOWPOWER	With no load applied		2.2	
$V_{OL}$	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7	$I_{OL} = 1\text{ mA}$			0.5	V
			$I_{OL} = 1\text{ mA}$			0.5	
$V_{OL}$	Low output voltage	XOUT	HIGHPOWER	$I_{OL} = 0.1\text{ mA}$		0.5	V
			LOWPOWER	$I_{OL} = 50\text{ }\mu\text{A}$		0.5	
	Low output voltage	XCOUT	HIGHPOWER	With no load applied		0	V
			LOWPOWER	With no load applied		0	
$V_{T+}-V_{T-}$	Hysteresis	$\overline{HOLD}$ , $\overline{RDY}$ , TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT7, $\overline{NMI}$ , ADTRG, CTS0 to CTS5, SCL0 to SCL5, SDA0 to SDA5, CLK0 to CLK5, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD5, SD, SCLMM, SDAMM		0.2		1.0	V
$V_{T+}-V_{T-}$	Hysteresis	$\overline{RESET}$		0.2		1.8	V
$I_{IH}$	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$ , CNVSS	$V_1 = 3\text{ V}$			4.0	$\mu\text{A}$

Notes:

1. Referenced to  $V_{CC1} = V_{CC2} = 2.7$  to  $3.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{opr} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified.
2. When  $V_{CC1} \neq V_{CC2}$ , refer to 5 V or 3 V standard depending on the voltage.

**Table 5.39 Electrical Characteristics (2) (1, 2)**

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$I_{IL}$	Low input current P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS	$V_I = 0\text{ V}$			-4.0	$\mu\text{A}$
$R_{PULLUP}$	Pull-up resistance P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	$V_I = 0\text{ V}$	50	80	150	$\text{k}\Omega$
$R_{fXIN}$	Feedback resistance XIN			3.0		$\text{M}\Omega$
$R_{fXCIN}$	Feedback resistance XCIN			16		$\text{M}\Omega$
$V_{RAM}$	RAM retention voltage	In stop mode	1.8			V

## Notes:

1. Referenced to  $V_{CC1} = V_{CC2} = 2.7$  to  $3.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{opr} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified.
2. When  $V_{CC1} \neq V_{CC2}$ , refer to 5 V or 3 V standard depending on the voltage.

$$V_{CC1} = V_{CC2} = 3 \text{ V}$$

Table 5.40 Electrical Characteristics (3) (1)

Symbol	Parameter	Measuring Condition	Standard			Unit	
			Min.	Typ.	Max.		
I <sub>CC</sub>	Power supply current  In single-chip mode, the output pin are open and other pins are V <sub>SS</sub>	High-speed mode	f <sub>(BCLK)</sub> = 32 MHz XIN = 4MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stop		27.0		mA
			f <sub>(BCLK)</sub> = 32 MHz, A/D conversion <sup>(3)</sup> XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stop		27.7		mA
			f <sub>(BCLK)</sub> = 16 MHz XIN = 16MHz (square wave), 125 kHz on-chip oscillator stop		13.0		mA
		40 MHz on-chip oscillator mode	Main clock stop 40 MHz on-chip oscillator on, no division 125 kHz on-chip oscillator stop		17.0		mA
		125 kHz on-chip oscillator Low-power mode	Main clock stop 40 MHz on-chip oscillator stop 125 kHz on-chip oscillator on, no division FMR22 = 1		450.0		μA
		Low-power mode	f <sub>(BCLK)</sub> = 32 kHz In low-power mode, FMR22 = FMR23 = 1 on flash memory <sup>(2)</sup>		160.0		μA
			f <sub>(BCLK)</sub> = 32 kHz In low-power mode, on RAM <sup>(2)</sup>		40.0		μA
		Wait mode	Main clock stop 40 MHz on-chip oscillator stop 125 kHz on-chip oscillator on Peripheral clock operation T <sub>opr</sub> = 25°C		20.0		μA
			f <sub>(XCIN)</sub> = 32 kHz (oscillation capacity High) 40 MHz on-chip oscillator stop 125 kHz on-chip oscillator stop Peripheral clock operation T <sub>opr</sub> = 25°C		8.0		μA
			f <sub>(XCIN)</sub> = 32 kHz (oscillation capacity Low) 40 MHz on-chip oscillator stop 125 kHz on-chip oscillator stop Peripheral clock operation T <sub>opr</sub> = 25°C		6.0		μA
Stop mode	Main clock stop 40 MHz on-chip oscillator stop 125 kHz on-chip oscillator stop Peripheral clock stop T <sub>opr</sub> = 25°C		2.0		μA		

## Notes:

1. Referenced to V<sub>CC1</sub> = V<sub>CC2</sub> = 2.7 to 3.3 V, V<sub>SS</sub> = 0 V at T<sub>opr</sub> = -20 to 85°C/-40 to 85°C, f<sub>(BCLK)</sub> = 32 MHz unless otherwise specified.
2. This indicates the memory in which the program to be executed exists.
3. This applies when using one A/D converter (φ<sub>AD</sub>=25MHz), with the ADSTBY bit for the unused A/D converter set to 0 (A/D operation stopped (standby)).

$$V_{CC1} = V_{CC2} = 3 \text{ V}$$

### 5.3.2 Timing Requirements (Peripheral Functions and Others)

( $V_{CC1} = V_{CC2} = 3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , at  $T_{opr} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified)

**Table 5.41 External Clock Input (XIN Input) (1)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c$	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
$t_r$	External clock rise time		9	ns
$t_f$	External clock fall time		9	ns

Note:

- The condition is  $V_{CC1} = V_{CC2} = 2.7$  to  $3.0 \text{ V}$ .

**Table 5.42 Timer A Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input high pulse width	60		ns
$t_{w(TAL)}$	TAiIN input low pulse width	60		ns

**Table 5.43 Timer A Input (Gating Input in Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input high pulse width	300		ns
$t_{w(TAL)}$	TAiIN input low pulse width	300		ns

**Table 5.44 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

**Table 5.45 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

**Table 5.46 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		$\mu\text{s}$
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

$$V_{CC1} = V_{CC2} = 3 V$$

**Timing Requirements**

( $V_{CC1} = V_{CC2} = 3 V$ ,  $V_{SS} = 0 V$ , at  $T_{opr} = -20$  to  $85^{\circ}C$  /  $-40$  to  $85^{\circ}C$  unless otherwise specified)

**Table 5.47 Timer B Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on both edges)	120		ns

**Table 5.48 Timer B Input (Pulse Period Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

**Table 5.49 Timer B Input (Pulse Width Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

**Table 5.50 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input high pulse width	150		ns
$t_{w(CKL)}$	CLKi input low pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXD <sub>i</sub> input setup time	100		ns
$t_{h(C-D)}$	RXD <sub>i</sub> input hold time	90		ns

**Table 5.51 External Interrupt  $\overline{INTi}$  Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	380		ns

**Table 5.52 Reset Input ( $\overline{RESET}$  Input)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{RESET}$ input low pulse width	10		$\mu s$

$$V_{CC1} = V_{CC2} = 3\text{ V}$$

**Timing Requirements**

( $V_{CC1} = V_{CC2} = 3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -20\text{ to }85^\circ\text{C}/-40\text{ to }85^\circ\text{C}$  unless otherwise specified)

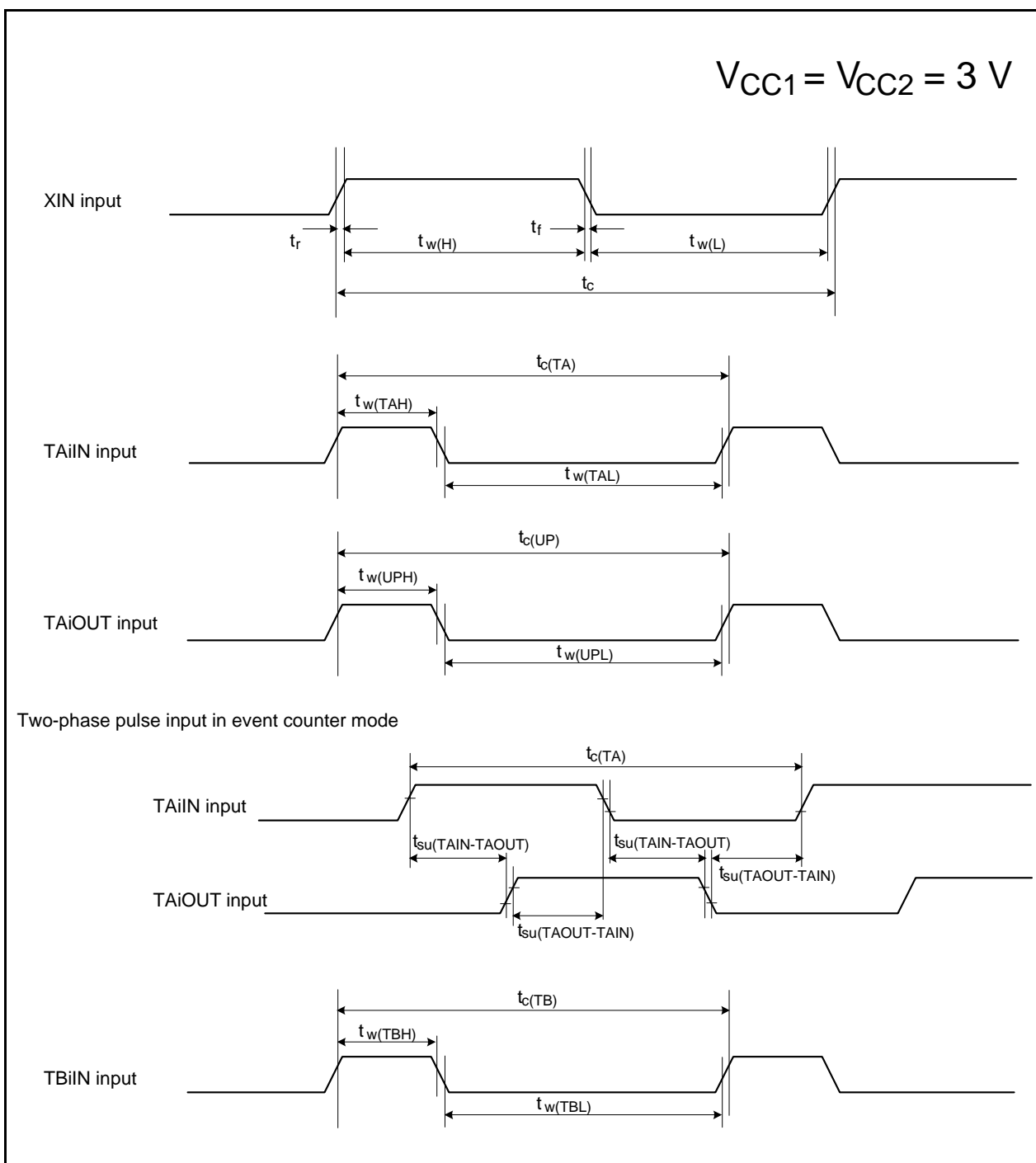


Figure 5.14 Timing Diagram (1)

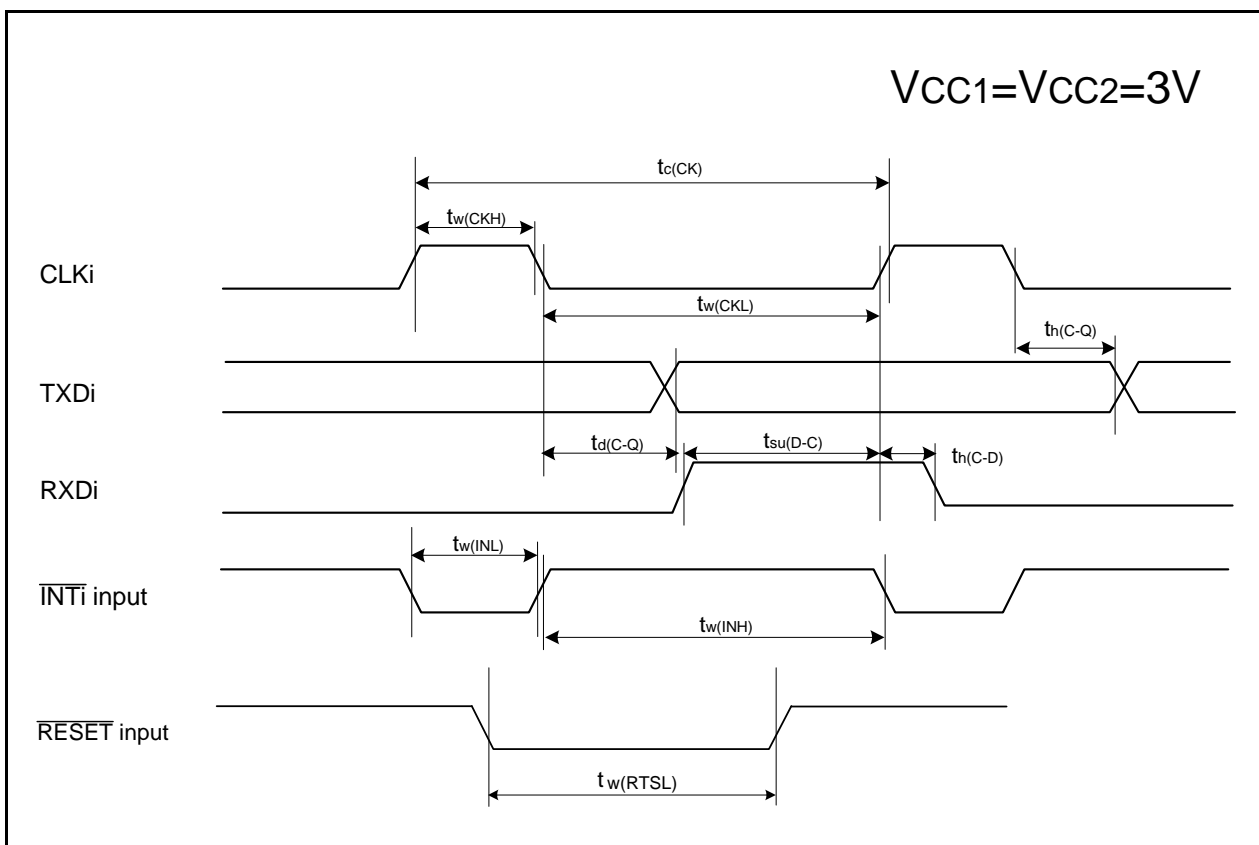


Figure 5.15 Timing Diagram (2)

$$V_{CC1} = V_{CC2} = 3 \text{ V}$$

### 5.3.3 Timing Requirements (Memory Expansion Mode and Microprocessor Mode)

( $V_{CC1} = V_{CC2} = 3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , at  $T_{opr} = -20$  to  $85^{\circ}\text{C}/-40$  to  $85^{\circ}\text{C}$  unless otherwise specified)

**Table 5.53 Memory Expansion Mode and Microprocessor Mode**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1}(\text{RD-DB})$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2}(\text{RD-DB})$	Data input access time (for setting with wait)		(Note 2)	ns
$t_{ac3}(\text{RD-DB})$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{su}(\text{DB-RD})$	Data input setup time	50		ns
$t_{su}(\text{RDY-BCLK})$	$\overline{\text{RDY}}$ input setup time	40		ns
$t_{su}(\text{HOLD-BCLK})$	$\overline{\text{HOLD}}$ input setup time	50		ns
$t_h(\text{RD-DB})$	Data input hold time	0		ns
$t_h(\text{BCLK-RDY})$	$\overline{\text{RDY}}$ input hold time	0		ns
$t_h(\text{BCLK-HOLD})$	$\overline{\text{HOLD}}$ input hold time	0		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(\text{BCLK})}} - 60[\text{ns}]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n + 0.5) \times 10^9}{f_{(\text{BCLK})}} - 60[\text{ns}] \quad n \text{ is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(\text{BCLK})}} - 60[\text{ns}] \quad n \text{ is 2 for 2 waits setting, 3 for 3 waits setting.}$$

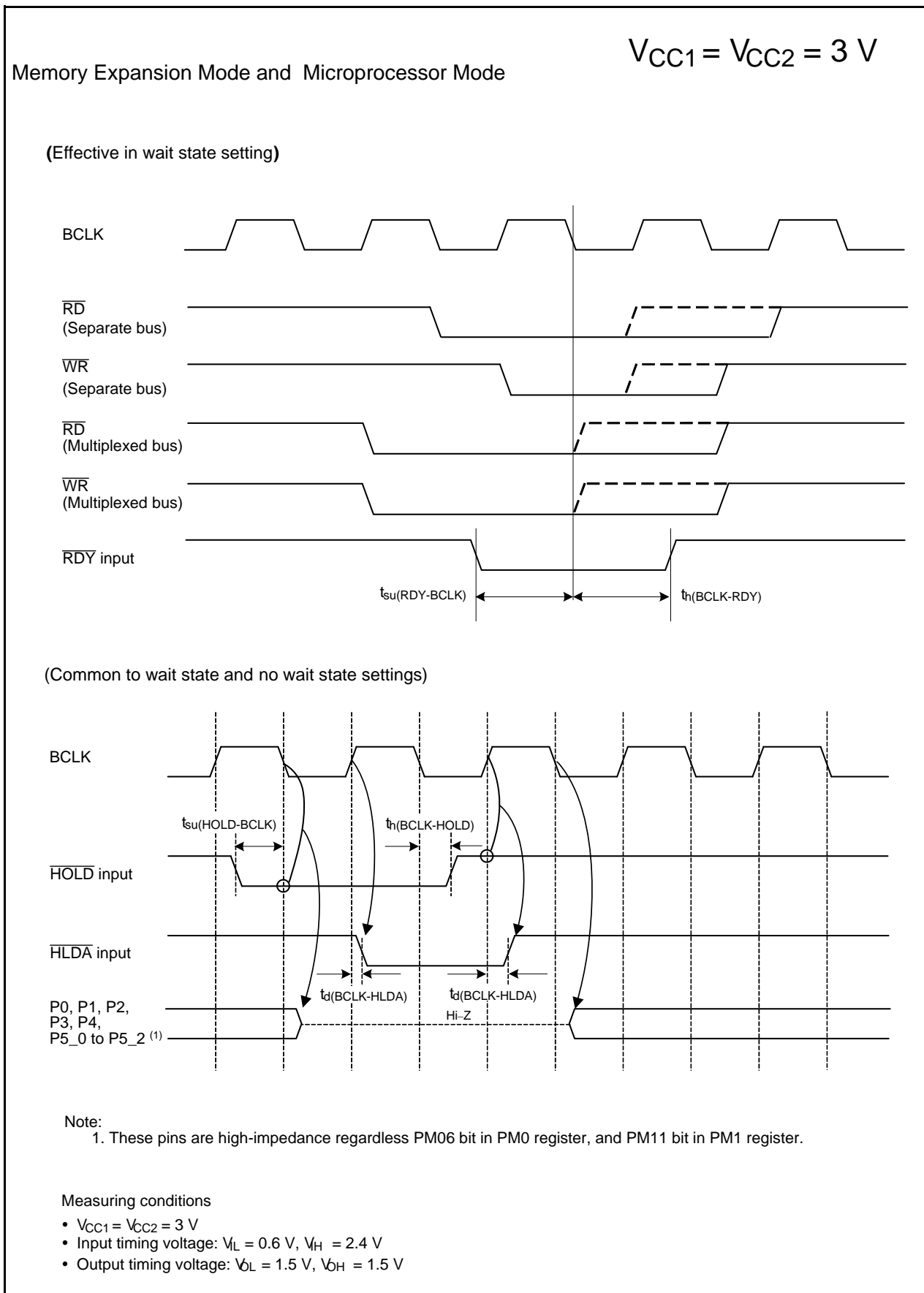


Figure 5.16 Timing Diagram

$$V_{CC1} = V_{CC2} = 3 \text{ V}$$

### 5.3.4 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode (in No Wait State Setting))

( $V_{CC1} = V_{CC2} = 3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , at  $T_{opr} = -20$  to  $85^\circ\text{C}/-40$  to  $85^\circ\text{C}$  unless otherwise specified)

**Table 5.54 Memory Expansion and Microprocessor Modes (in No Wait State Setting)**

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.17		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) <sup>(3)</sup>		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) <sup>(3)</sup>		(Note 2)		ns
$t_{d(BCLK-HLDA)}$	HLDA output delay time			40	ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40[\text{ns}] \quad f_{(BCLK)} \text{ is } 12.5 \text{ MHz or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[\text{ns}]$$

This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

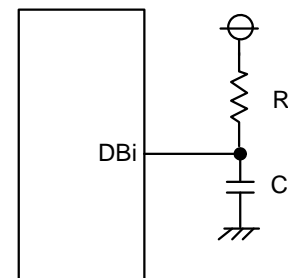
$$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$$

by a circuit of the right figure.

For example, when  $V_{OL} = 0.2V_{CC2}$ ,  $C = 30 \text{ pF}$ ,  $R = 1 \text{ k}\Omega$ ,

hold time of output low level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2}) = 6.7 \text{ ns.}$$



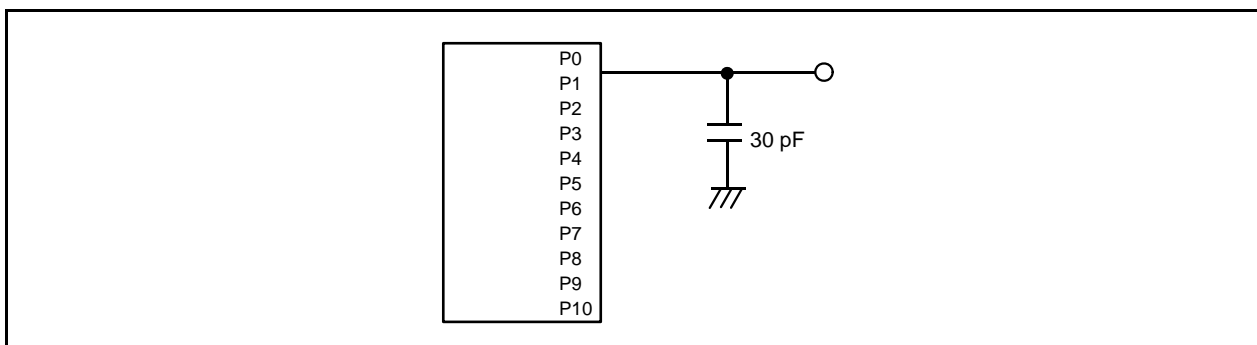


Figure 5.17 Ports P0 to P10 Measurement Circuit

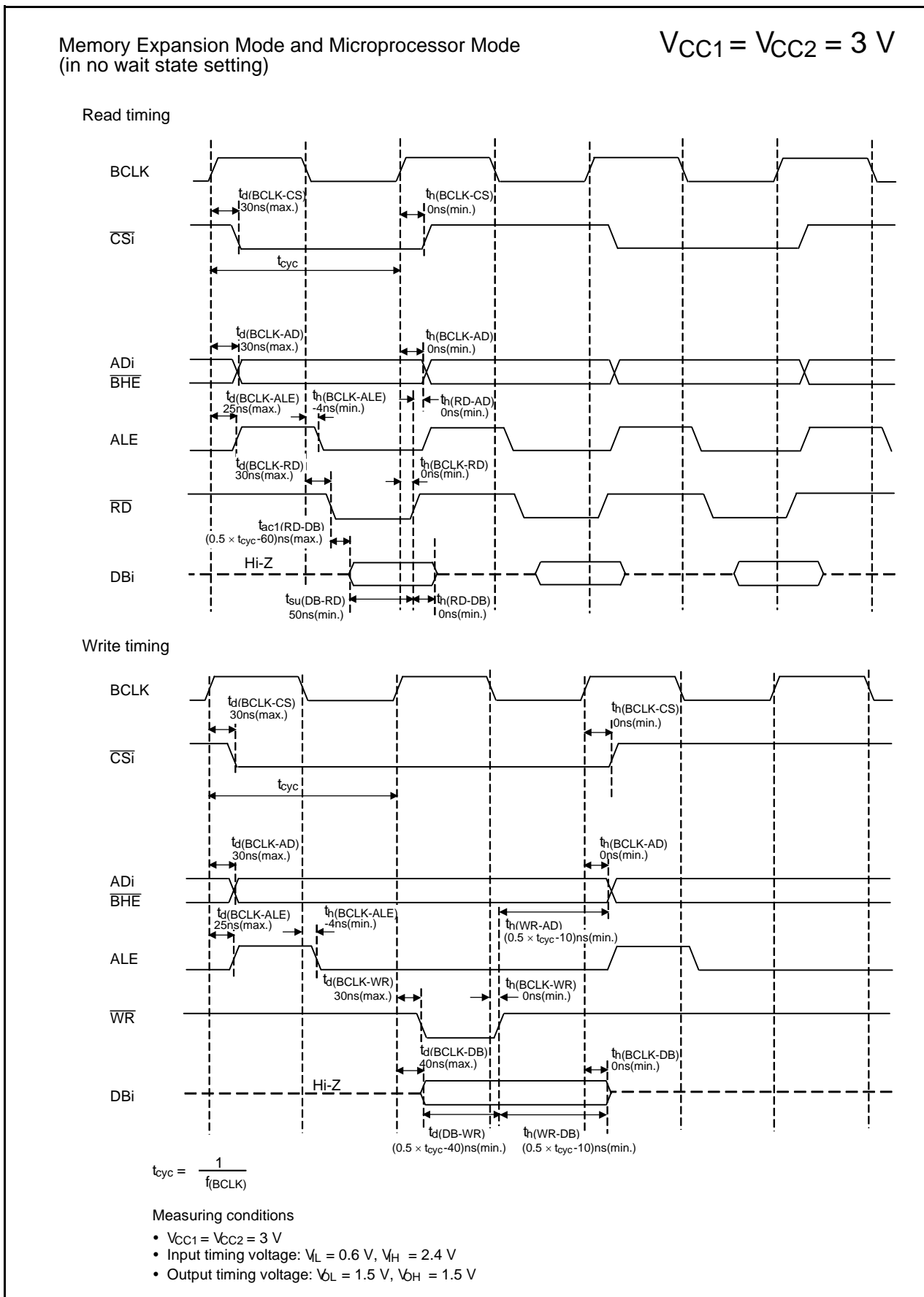


Figure 5.18 Timing Diagram

$$V_{CC1} = V_{CC2} = 3 \text{ V}$$

### 5.3.5 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area))

( $V_{CC1} = V_{CC2} = 3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , at  $T_{opr} = -20 \text{ to } 85^\circ\text{C}/-40 \text{ to } 85^\circ\text{C}$  unless otherwise specified)

**Table 5.55 Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area)**

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.17		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) <sup>(3)</sup>		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) <sup>(3)</sup>		(Note 2)		ns
$t_{d(BCLK-HLDA)}$	HLDA output delay time			40	ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f_{(BCLK)}} - 40[\text{ns}] \quad \begin{array}{l} n \text{ is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.} \\ \text{When } n = 1, f_{(BCLK)} \text{ is 12.5 MHz or less.} \end{array}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[\text{ns}]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.  
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

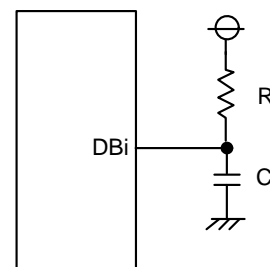
Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$$

by a circuit of the right figure.

For example, when  $V_{OL} = 0.2V_{CC2}$ ,  $C = 30 \text{ pF}$ ,  $R = 1 \text{ k}\Omega$ , hold time of output low level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2}) = 6.7 \text{ ns.}$$



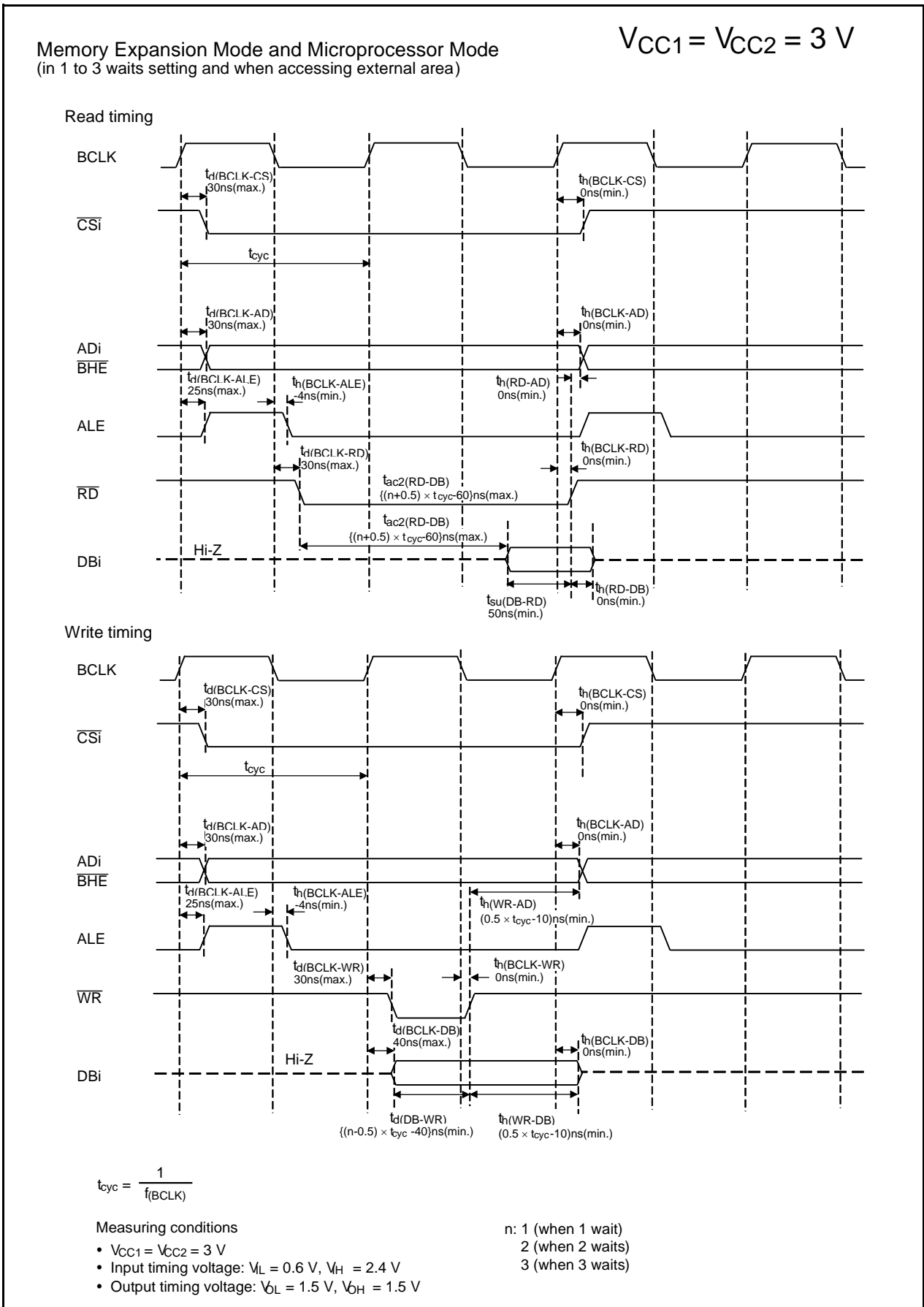


Figure 5.19 Timing Diagram

$$V_{CC1} = V_{CC2} = 3\text{ V}$$

### 5.3.6 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode (in 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus))

( $V_{CC1} = V_{CC2} = 3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -20\text{ to }85^{\circ}\text{C}/-40\text{ to }85^{\circ}\text{C}$  unless otherwise specified)

**Table 5.56 Memory Expansion Mode and Microprocessor Mode (in 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus) (5)**

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.17		50	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			50	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{h(RD-CS)}$	Chip select output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			40	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			40	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			50	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time			40	ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (in relation to BCLK)			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (in relation to BCLK)		-4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (in relation to Address)		(Note 3)		ns
$t_{h(AD-ALE)}$	ALE signal output hold time (in relation to Address)	(Note 4)		ns	
$t_{d(AD-RD)}$	RD signal output delay from the end of address	0		ns	
$t_{d(AD-WR)}$	WR signal output delay from the end of address	0		ns	
$t_{dz(RD-AD)}$	Address output floating start time		8	ns	

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[\text{ns}]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 50[\text{ns}] \quad n \text{ is 2 for 2 waits setting, 3 for 3 waits setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40[\text{ns}]$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 15[\text{ns}]$$

5. When using multiplexed bus, set  $f_{(BCLK)}$  12.5 MHz or less.

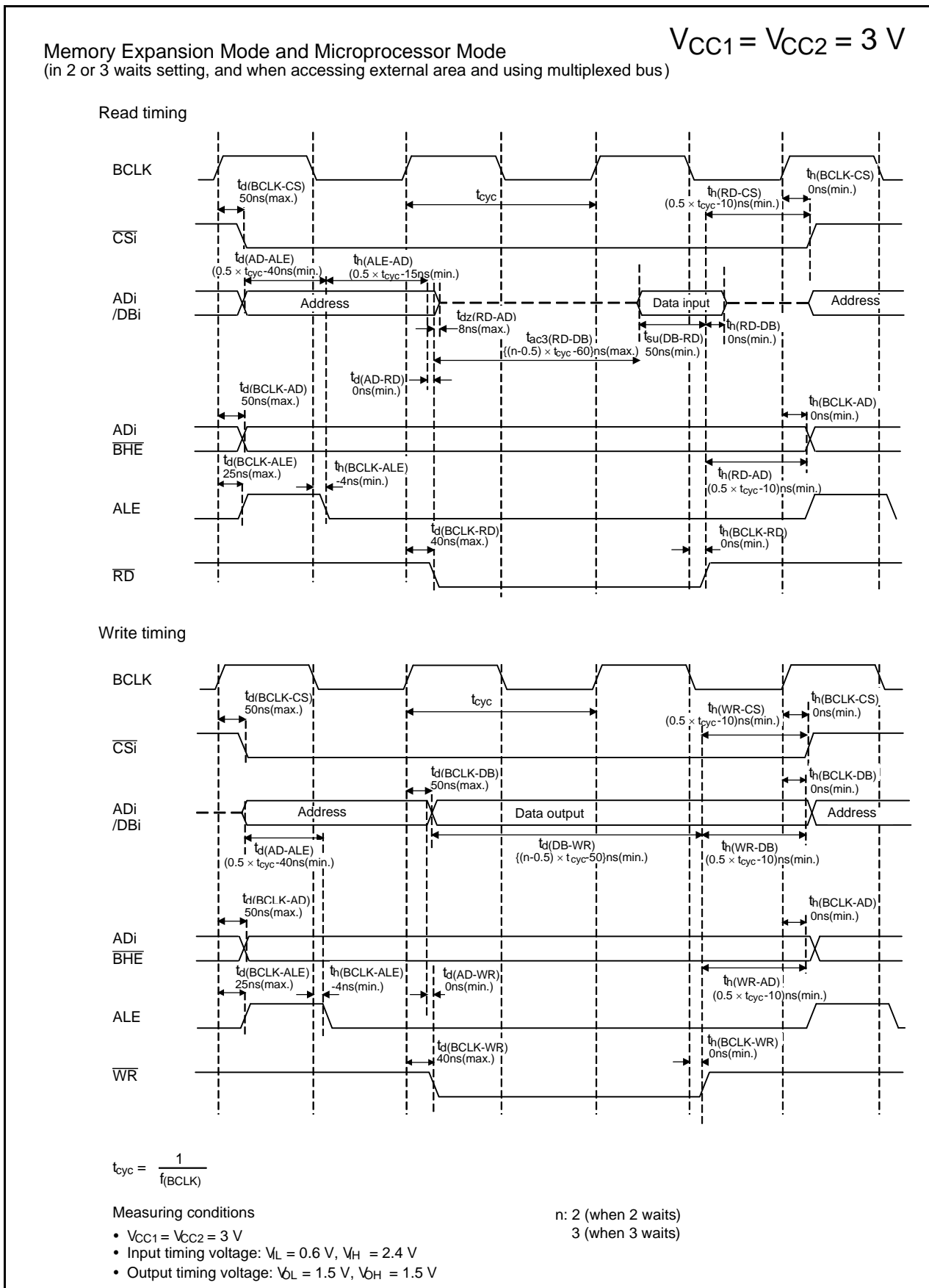
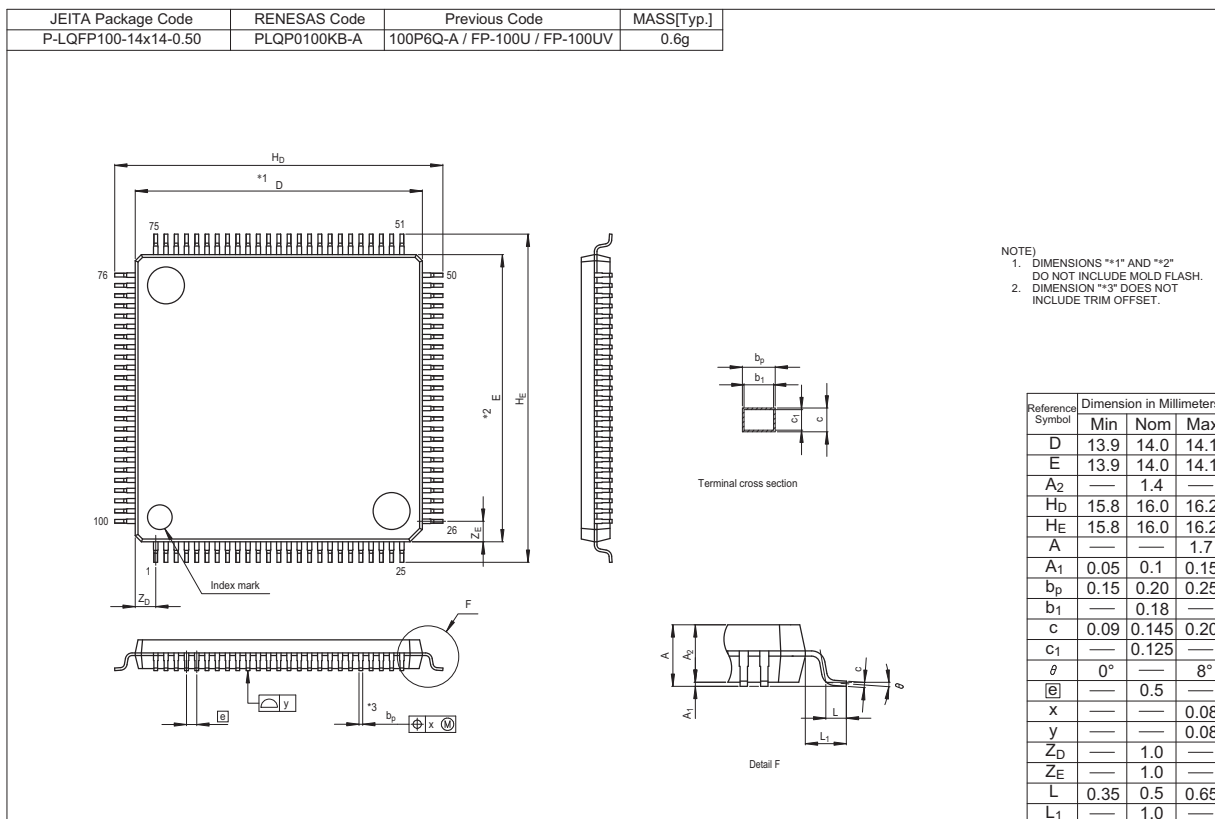
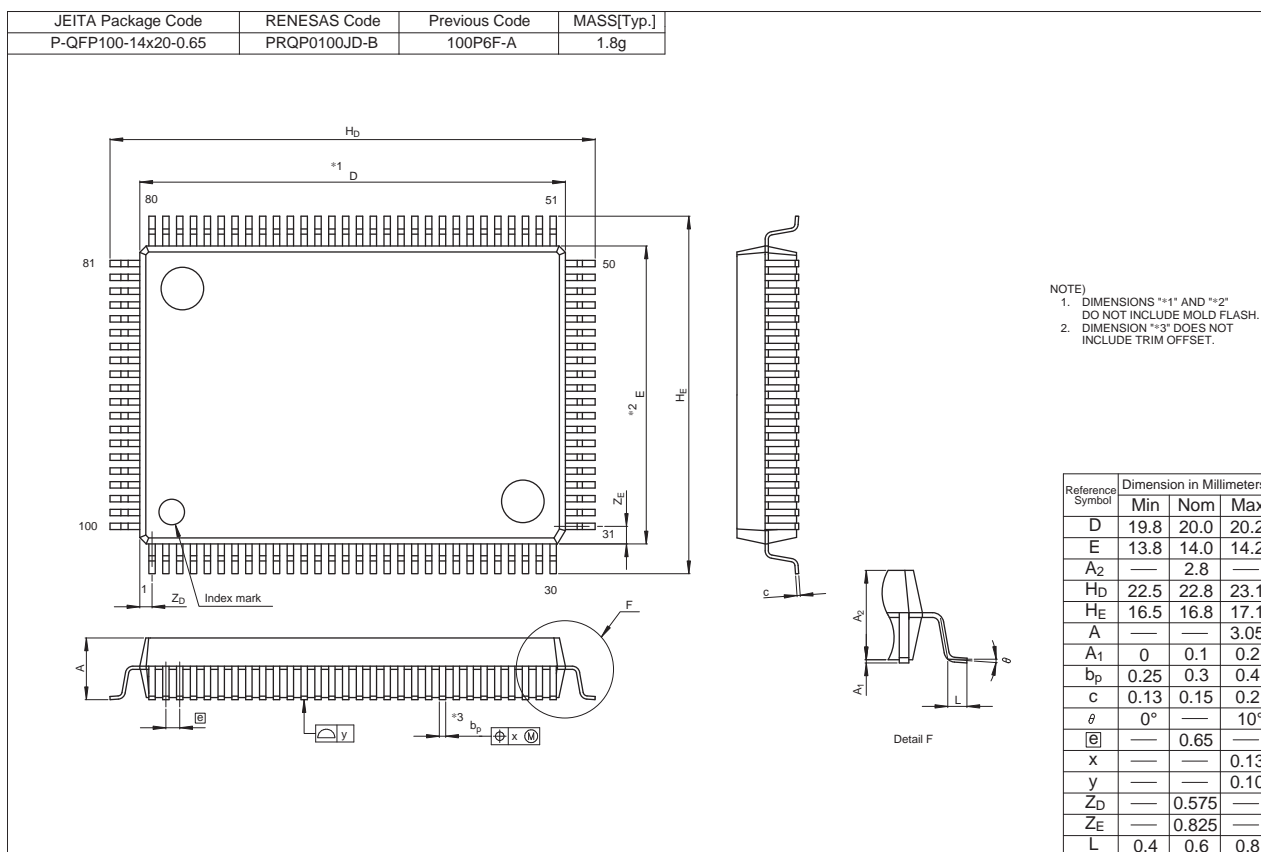


Figure 5.20 Timing Diagram

## Appendix 1. Package Dimensions

The information on the latest package dimensions or packaging may be obtained from “Packages” on the Renesas Technology Web site.





<b>REVISION HISTORY</b>	<b>M16C/6C Group Datasheet</b>
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Rev.	Date	Description	
		Page	Summary
1.00	Jul 15, 2009	-	First Edition issued.

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