Renesas Synergy™ MCU S7G2

S7 Series: High Performance Microcontrollers

Rev.1.00
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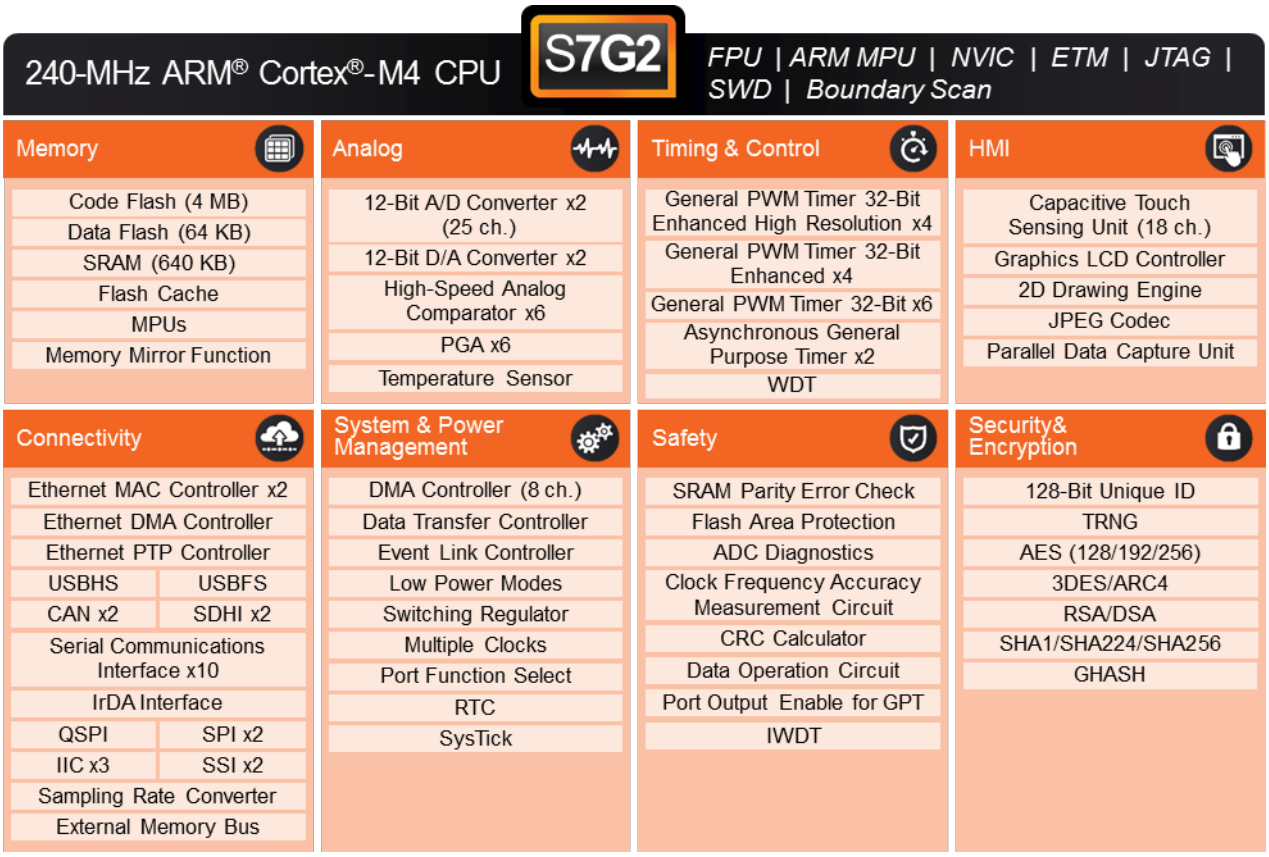
Overview

Leading-performance 240-MHz ARM® Cortex®-M4 microcontroller, up to 4-MB flash memory, 640-KB SRAM, Graphics LCD Controller, 2D Drawing Engine, Capacitive Touch Sensing Unit, Ethernet MAC Controller with IEEE 1588 PTP, USB High-Speed, USB Full-Speed, SDHI, Quad SPI, Security and Safety features, and advanced analog.

Features

- **32-bit ARM® Cortex®-M4 with Floating Point Unit (FPU)**
  - ARM®v7E-M architecture with DSP instruction set
  - Maximum operating frequency: 240 MHz
  - Supports 4-GB address space
  - On-Chip Debugging System: JTAG, SWD, and ETM
  - Boundary scan and ARM® Memory protection unit (MPU)
- **Memory**
  - Up to 4-MB of Code Flash memory (80 MHz zero wait states)
  - Up to 640-KB of SRAM
  - Up to 64-KB of Data Flash (up to 100,000 erase / write cycles)
  - Flash Cache (FCACHE)
  - Memory Protections Units
  - Memory Mirror Function
- **Connectivity**
  - Ethernet MAC Controller (ETHERC) x2
  - Ethernet DMA Controller (EDMAC)
  - Ethernet PTP Controller (EPTPC)
  - USB 2.0 High-Speed Module (USBHS)
    - On-chip transceiver
    - USB battery charge 1.2 version supported
  - USB 2.0 Full-Speed Module (USBFS)
    - On-chip transceiver
  - Serial Communications Interface (SCI) with FIFO x10
  - Serial Peripheral Interface (SPI) x2
  - I2C bus interface (IIC) x3
  - CAN module (CAN) x2
  - Serial Sound Interface (SSI) x2
  - SD/MMC Host Interface (SDHI) x2
  - Quad Serial Peripheral Interface (QSPI)
  - IrDA Interface
  - Sampling Rate Converter (SRC)
  - External Memory Bus
    - 8- and 16-bit address width
    - SDRAM support
- **Analog**
  - 12-Bit A/D Converter (ADC12) with 3 sample and hold circuit each, x2
  - 12-Bit D/A Converter (DAC12) x2
  - High-Speed Analog Comparator (ACMPHS) x6
  - Programmable Gain Amplifier (PGA) x6
  - Temperature Sensor
- **Timers**
  - General PWM Timer 32-Bit with Enhanced High Resolution (GPT32EH) x4
  - General PWM Timer 32-bit Enhanced (GPT32E) x4
  - General PWM Timer 32-bit (GPT32) x6
  - Asynchronous General Purpose Timer (AGT) 16-bit x2
  - Watchdog Timer (WDT)
- **Safety**
  - SRAM Parity Error Check
  - Flash Area Protection
  - ADC Diagnostics
  - Clock Frequency Accuracy Measurement Circuit (CAC)
  - Cyclic Redundancy Check (CRC) Calculator
  - Data Operation Circuit (DOC)
  - Port Output Enable for GPT (POEG)
  - Independent Watchdog Timer (IWDT)
  - GPIO Readback Level Detection
  - Register Write Protection
  - Main Oscillator Stop Detection
  - Illegal Memory Access
- **System and Power Management**
  - Low power modes
  - Switching regulator
  - Realtime Clock (RTC) with calendar & VBATT support
  - Event Link Controller (ELC)
  - DMA Controller (DMAC) x8
  - Data Transfer Controller (DTC)
  - Key interrupts
  - Power-on reset
  - Low voltage detector with voltage settings
  - SysTick
  - Port Function Select
- **Security and Encryption**
  - AES128/192/256
  - 3DES/ARC4
  - SHA1/SHA224/SHA256
  - GHASH
  - RSA/DSA
  - True Random Number Generator (TRNG)
  - 128-Bit Unique ID
- **Human Machine Interface (HMI)**
  - Graphics LCD Controller (GLCDC)
  - JPEG codec
  - 2D Drawing Engine (DRW)
  - Capacitive Touch Sensing Unit (CTSU)
  - Parallel Data Capture Unit (PDC)
- **Multiple Clock Sources**
  - Main Clock Oscillator (MOSC) (8 to 24 MHz)
  - Sub clock Oscillator (SOSC) (32.768 KHz)
  - High-speed on Chip Oscillator (HOCO) (16/18/20 MHz)
  - Middle_Speed on Chip Oscillator (MOCO) (8MHz)
  - Low-speed on Chip Oscillator (LOCO) (32.768 KHz)
  - Independent Watchdog Timer (OCO) (15 KHz)
  - Clock trim function for HOCO/MOCO/LOCO
  - Clock out support
- **General Purpose I/O Ports**
  - Up to 172 I/O pins
    - Up to 9 CMOS input
    - Up to 163 CMOS inputs/outputs
      - Up to 22 5-V tolerant I/O
      - Up to high-current 24 pins (20 mA)
- **Operating Voltage**
  - VCC: 2.7 V to 3.6 V
- **Operating Temperature and Packages**
  - Ta: -40°C to 85°C
    - LGA145 (7 mm x 7 mm, 0.5 mm)
    - BGA176 (13 mm x 13 mm, 0.8 mm)
    - BGA224 (13 mm x 13 mm, 0.8 mm)
  - Ta: -40°C to 105°C
    - LQFP100 (14 mm x 14 mm, 0.5 mm)
    - LQFP144 (20 mm x 20 mm, 0.5 mm)
    - LQFP176 (24 mm x 24 mm, 0.5 mm)

S7G2 Block Diagram



Note: This block diagram represents the superset S7G2 device.

S7G2 Device Summary

Product		R7FS7G27H2A01CBD	R7FS7G27G2A01CBD	R7FS7G27H2A01CBG	R7FS7G27G2A01CBG	R7FS7G27H3A01CFC	R7FS7G27G3A01CFC
Package		BGA224		BGA176		LQFP176	
Code Flash (KB)		4096	3072	4096	3072	4096	3072
Data Flash (KB)		64	64	64	64	64	64
SRAM (KB)		640	640	640	640	640	640
GPIO	Total	172	172	126	126	126	126
	Input/output	163	163	117	117	117	117
	Input	9	9	9	9	9	9
Connectivity	Ethernet MAC Controller	2	2	2	2	2	2
	Ethernet DMA Controller	1	1	1	1	1	1
	USBHS	1	1	1	1	1	1
	USBFS	1	1	1	1	1	1
	SCI	10	10	10	10	10	10
	SPI	2	2	2	2	2	2
	IIC	3	3	3	3	3	3
	CAN	2	2	2	2	2	2
	SSI	2	2	2	2	2	2
	SDHI	2	2	2	2	2	2
	IrDA interface	1	1	1	1	1	1
	QSPI	1	1	1	1	1	1
	Sample Rate Converter	1	1	1	1	1	1
	External Memory Bus	16/8-bit	16/8-bit	16/8-bit	16/8-bit	16/8-bit	16/8-bit
Analog	12-Bit A/D Converter (No. ch.)	2 (25)	2 (25)	2 (21)	2 (21)	2 (21)	2 (21)
	12-Bit D/A Converter	2	2	2	2	2	2
	High-Speed Analog Comparator	6	6	6	6	6	6
	PGA	6	6	6	6	6	6
	Temperature Sensor	1	1	1	1	1	1
Timing and Control	General PWM Timer 32-Bit Enhanced High Resolution	4	4	4	4	4	4
	General PMW Timer 32-Bit Enhanced	4	4	4	4	4	4
	General PWM Timer 32-Bit	6	6	6	6	6	6
	Asynchronous General Purpose Timer	2	2	2	2	2	2
	WDT	1	1	1	1	1	1
HMI	Graphics LCD Controller	RGB888 RGB565	RGB888 RGB565	RGB888 RGB565	RGB888 RGB565	RGB888 RGB565	RGB888 RGB565
	2D Drawing Engine	1	1	1	1	1	1
	JPEG CODEC	1	1	1	1	1	1
	Parallel Data Capture	1	1	1	1	1	1
	Capacitive Touch Sensing Unit	18	18	12	12	12	12
System and Power Management	DMA Controller	8	8	8	8	8	8
	Data Transfer Controller	1	1	1	1	1	1
	Event Link Controller	1	1	1	1	1	1
	Switching Regulator	1	1	1	1	1	1
	Port Function Select	1	1	1	1	1	1
	RTC	1	1	1	1	1	1
	SysTick	1	1	1	1	1	1
Safety		SRAM Parity Error Check, Flash Area Protection, ADC Diagnostics, Clock Frequency Accuracy Measurement Circuit, Cyclic Redundancy Check Calculator, Data Operation Circuit, Port Output Enable for GPT, Independent Watchdog Timer, GPIO Readback Level Detection, Register Write Protection, Main Oscillator Stop Detection, Illegal Memory Access					
Security and Encryption		AES128/192/256, 3DES/ARC4, SHA1/SHA224/SHA256, GHASH, RSA/DSA, TRNG, 128-Bit Unique ID					
Operating Voltage		2.7 V to 3.6 V					
Operating ambient Temperature (Ta)		-40°C to 85°C		-40°C to 85°C		-40°C to 105°C	

S7G2 Device Summary (continued)

Product		R7FS7G27H2A01CLK	R7FS7G27G2A01CLK	R7FS7G27H3A01CFB	R7FS7G27G3A01CFB	R7FS7G27G3A01CFP
Package		LGA145		LQFP144		LQFP100
Code Flash (KB)		4096	3072	4096	3072	3072
Data Flash (KB)		64	64	64	64	64
SRAM (KB)		640	640	640	640	640
GPIO	Total	104	104	104	104	70
	Input/output	95	95	95	95	61
	Input	9	9	9	9	9
Connectivity	Ethernet MAC Controller	2	2	2	2	1
	Ethernet DMA Controller	1	1	1	1	1
	USBHS	-	-	-	-	-
	USBFS	1	1	1	1	1
	SCI	10	10	10	10	10
	SPI	2	2	2	2	2
	IIC	3	3	3	3	2
	CAN	2	2	2	2	2
	SSI	2	2	2	2	1
	SDHI	2	2	2	2	2
	IrDA interface	1	1	1	1	1
	QSPI	1	1	1	1	1
	Sample Rate Converter	1	1	1	1	1
	External Memory Bus	16/8-bit	16/8-bit	16/8-bit	16/8-bit	8-bit
Analog	12-Bit A/D Converter (No. ch.)	2 (19)	2 (19)	2 (19)	2 (19)	2 (16)
	12-Bit D/A Converter	2	2	2	2	2
	High-Speed Analog Comparator	6	6	6	6	6
	PGA	6	6	6	6	6
	Temperature Sensor	1	1	1	1	1
Timing and Control	General PWM Timer 32-Bit Enhanced High Resolution	4	4	4	4	4
	General PMW Timer 32-Bit Enhanced	4	4	4	4	3
	General PWM Timer 32-Bit	6	6	6	6	6
	Asynchronous General Purpose Timer	2	2	2	2	2
	WDT	1	1	1	1	1
HMI	Graphics LCD Controller	RGB888 RGB565	RGB888 RGB565	RGB888 RGB565	RGB888 RGB565	RGB565
	2D Drawing Engine	1	1	1	1	1
	JPEG CODEC	1	1	1	1	1
	Parallel Data Capture	1	1	1	1	1
	Capacitive Touch Sensing Unit	18	18	18	18	12
System and Power Management	DMA Controller	8	8	8	8	8
	Data Transfer Controller	1	1	1	1	1
	Event Link Controller	1	1	1	1	1
	Switching Regulator	1	1	1	1	1
	Port Function Select	1	1	1	1	1
	RTC	1	1	1	1	1
	SysTick	1	1	1	1	1
Safety		SRAM Parity Error Check, Flash Area Protection, Clock Frequency Accuracy Measurement Circuit CRC Calculator, Data Operation Circuit, Port Output Enable, Independent Watchdog, GPIO Readback Level Detection, Secure Memory Protection Unit, Register Write Protection, Oscillator Stop Detection, Illegal Memory Access				
Security and Encryption		AES128/192/256, 3DES/ARC4, SHA1/SHA224/SHA256, GHASH, RSA/DSA, TRNG, 128-Bit Unique ID				
Operating Voltage		2.7V to 3.6V				
Operating ambient Temperature (Ta)		-40°C to 85°C		-40°C to 105°C		-40°C to 105°C

Peripheral Description

■ 32-bit ARM® Cortex®-M4 with FPU

■ Memory

- **Code Flash**

The on-chip, high-speed Code Flash is used to store the user application. The Code Flash features integrated security protection against illicit tampering with, or reading from, the flash memory. The Code Flash also features a mechanism to protect flash contents from erroneous overwriting. A section of Code Flash can be read while another of section is being programmed. At a minimum, a block of 256 bytes can be programmed in one operation.

- **SRAM**

The on-chip, high-speed SRAM supports single-cycle access for both read and write operations. A section of RAM supports detection of 2-bit errors. A parity bit is added to the rest of the SRAM at the time of writing. The parity bit is used to perform an even parity check upon reading to detect parity errors. Interrupts can be generated upon 1-bit or 2-bit error and parity error detection.

- **Data Flash**

The on-chip, high-speed Data Flash features integrated security protection against illicit tampering with, or reading from, the flash memory. The Data Flash also features a mechanism to protect the flash contents from erroneous overwriting.

- **Flash Cache**

The Flash Cache provides single cycle access to data and instructions. Flash caches consist of data, instructions, and pre-fetch buffers. The most frequently used data and instructions are cached in the buffers, and they can be accessed by the CPU in a single clock cycle to accelerate the application execution.

■ Connectivity

- **Ethernet MAC Controller (ETHERC)**

The Ethernet MAC controller features two IEEE 802.3 compliant MACs, both of which provide independent Media Independent Interface (MII) and Reduced-MII (RMII) for connection with external PHY (optical, twisted wire, etc.). The controller supports full duplex and data transmission rates of up to 100 Mbps, and it features a dedicated Ethernet DMA controller which is used to transfer data between memory and the MAC without CPU intervention. It also supports Magic Packet detection and Wake-on-LAN functionality for remote activation of peripherals. This functionality is particularly useful in Internet of Things (IoT) applications. A synchronization clock can be generated in compliance with the IEEE 1588 Precision Time Protocol (PTP).

- **USB High-Speed Module (USBHS)**

The USBHS module incorporates an integrated USB 2.0 controller and transceiver that support high-speed, full-speed, and low-speed operation in host, device, and on-the-go (OTG) modes. The high-speed module supports data transfer speeds of up to 480 Mbps, and it also features self-powered and bus-powered operation. End points can be assigned to up to 10 pipes, which are provided in the buffer memory. In the host mode, start of frame (SOF) and packet transmission are automatically scheduled. Programmable intervals for isochronous and interrupt transfers are also supported. Internal pull-up and pull-down resistors for D+ & D- signals lower the overall system cost.

- **USB Full-Speed Module (USBFS)**

The USBFS module incorporates an integrated USB 2.0 controller and transceiver that supports full-speed and low-speed operation in host, device, and on-the-go (OTG) modes. The full-speed module supports data transfer speeds of up to 12 Mbps, and it also features self-powered and bus-powered operation. End points can be assigned to up to 10 pipes, which are provided in the buffer memory. In the host mode, start of frame (SOF) and packet transmission are automatically scheduled. Programmable intervals for isochronous and interrupt transfers are also supported. Internal pull-up and pull-down resistors for D+ & D- signals lower the overall system cost.

- **Serial Communication Interface (SCI)**

The Serial Communication Interface (SCI) can be configured to support any of the following asynchronous and synchronous serial interfaces: the asynchronous interface (UART and asynchronous communications interface adapter (ACIA)), 8-bit clock synchronous interface, simple IIC (master-only), simple SPI (master only), and smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. The data transfer speed can be configured using an on-chip baud rate generator.

- **Serial Peripheral Interface (SPI)**

The Serial Peripheral Interface (SPI) provides a high-speed, synchronous, serial communication interface for full-duplex, short range communication. The SPI module can be configured for operation in multi-master, single-master, slave, 3-wire, and 4-wire modes. The SPI also features operation in transmit-only and loopback modes. The SPI is capable of detecting errors on underrun, overrun, parity, and mode faults.

- **I2C Bus Interface (IIC)**

The Inter-IC Communication (IIC) peripheral provides asynchronous bi-directional data transfer through a two-wire multi-master, serial, single-ended bus. The IIC module supports operation in legacy IIC mode and in System Management Bus (SMBus) v2.0 mode. The module can be operated as a single-master or multi-master transmitter and receiver, and as a slave transmitter and receiver. In addition to 7-bit and 10-bit address formats, it also supports match detection for Slave, General Call, Device ID, and SMBus host addresses. For higher transmission rates, the IIC module supports Fast-mode Plus. The IIC module includes a bus hanging timeout feature that is particularly useful when the slave holds clock low for an unexpectedly long period of time.

- **CAN Controller (CAN)**

The Controller Area Network (CAN) peripheral provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically noisy applications. The CAN interface complies with the ISO 11898-1 (CAN2.0A/CAN2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported.

- **Serial Sound Interface (SSI)**

The Serial Sound Interface (SSI) peripheral provides functionality for interfacing digital audio devices in order to transmit PCM audio data over a serial bus with the microcontroller. The SSI supports an audio clock frequency of up to 50 MHz, and it can be operated as a slave or master receiver/transmitter/transceiver to suit a variety of applications. The SSI includes 8-stage FIFO buffers in the receiver and transmitter, and it supports interrupt- and DMA-driven data reception and transmission.

- **SD/MMC Host Interface (SDHI)**

The Secure Digital Host Interface and MultiMediaCard (SDHI) peripheral provide the functionality needed to connect a variety of external memory cards. The SDHI interface supports both 1-bit and 4-bit buses for connecting SC, SDHC, and SDXC SD memory cards. The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC4.51 device access.

- **Quad Serial Peripheral Interface (QSPI)**

The Quad Serial Peripheral Interface support 4-bit multiplexed communication and up to four times the bandwidth of a serial peripheral interface (SPI). The address width can be configured from 8 bits to 32 bits. Several features including timing adjustment, ROM read instructions (read, fast read, fast read dual output, fast read quad output), and other ROM instructions (erase, write, ID read, power-down control) are supported to enable faster and easier access to external serial ROMs.

- **IrDA Interface**

The Infrared Data (IrDA) interface enables wireless infrared serial communication by encoding and decoding the transmit (TX) and receive (RX) signals from the serial communication interface (SCI). Connecting the encoded and decoded signals to an infrared transceiver implements a wireless communication in compliance with the IrDA 1.0 standard. Data transfer can start at 9600 bps and the transfer rate can be changed by the software whenever necessary. The infrared receive and transmit pins are multiplexed with the SCI receive and transmit pins.

- **External Memory Bus**

The External Memory Bus allows the high-speed MCU bus master to access external slaves such as external memory and peripherals. The bus arbitrates requests for bus mastership on the external address space and external bus control registers on the CPU bus and on other bus masters. External address space is divided into eight chip select (CS) areas and an SDRAM area. Bus width (8 or 16 bit) can be separately configured for each of the nine areas. Additionally, endian mode can be specified for each area.

Advanced Analog

- **12-Bit A/D Converter (ADC12)**

The 12-Bit A/D Converter (ADC12) features a 12-bit, SAR ADC which can be used to convert analog voltages from up to 25 multiplexed analog inputs (23 simultaneous inputs), an internal temperature sensor, and an internal reference voltage. The ADC12 can be operated in single-scan mode, continuous arbitrary mode, and group scan mode, each providing different levels of flexibility to meet the requirements of a large number of applications. The input signals can be sampled in single-ended mode and differential mode. The ADC conversion can be triggered from internal event signals, the PWM, the timer, and the temperature sensor. It can also be triggered from software or an external trigger input.

- **12-Bit D/A Converter (DAC12)**

The 12-Bit D/A Converter (DAC12) converts discrete time, digital amplitude signals into a continuous time, continuous signal. The DAC12 also features an integrated output current amplifier that can be used to drive external loads with high enough current. Additionally, the DAC12 can be configured to operate in-sync or out-of-sync with the ADC. This capability is particularly useful to control the timing of inrush current generated by the DAC and to prevent degradation of the ADC conversation accuracy due to interference.

- **High-Speed Analog Comparator (ACMPHS)**

The High-Speed Analog Comparator (ACMPHS) can compare a test voltage with a reference voltage and provide a digital output based on the result of the conversion. Both the test signal and the reference voltage signal can be provided to the comparator from internal sources (such as output of the DAC or internal reference voltage) and external sources. Such flexibility is beneficial in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring ADC conversion.

- **Programmable Gain Amplifier (PGA)**

The Programmable Gain Amplifier (PGA) can amplify small signals before they are applied to an ADC. The PGA can amplify single input signals and differential signals, reference voltage is generated by the on-chip DAC. The bias voltage can be 50% and 60% of AVCC in differential input mode. In single input mode, the amplifier gain can be one of fifteen values (2, 2.5, 2.667, 2.857, 3.077, 3.333, 3.636, 4, 4.444, 5, 5.714, 6.667, 8, 10, or 13.33). In differential input mode, the amplifier gain can be one of four values (1.5, 2.333, 4, or 5.667).

- **Temperature Sensor**

The on-chip Temperature Sensor can predict and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC for conversion and further use by the end application.

Timers

- **General PWM Timer 32-Bit Enhanced High Resolution (GPT32EH)**

Each instance of the General PWM Timer 32-Bit Enhanced High Resolution (GPT32EH) features four independent timers, which have up to 260 ps of resolution when used with the picosecond delay function. Each timer operates on an independent clock. The timers can be operated in five different modes: counter, compare match, phase counting, input capture, and pulse width measurement (PWM). Multiple internal events or any of four external trigger inputs can be used to start, stop and clear the counter. Additionally, the GPT32EH can be used to trigger ADC conversion. For traditional motor control applications, the timer can be used automatically to insert dead time, and for high-speed, brushless DC motor applications, the timer can be used with an integrated 3-phase PWM generator to generate control signals.

- **General PWM Timer 32-Bit Enhanced (GPT32E)**

Each instance of the General PWM Timer 32-Bit Enhanced (GPT32E) features four independent timers. Each timer operates on an independent clock. The timers can be operated in five different modes: counter, compare match, phase counting, input capture, and pulse width measurement (PWM). Multiple internal events or any of four external trigger inputs can be used to start, stop and clear the counter. Additionally, GPT32E can be used to trigger ADC conversion. For traditional motor control applications, the timer can be used automatically to insert dead time, and for high-speed, brushless DC motor applications, the timer can be used with an integrated 3-phase PWM generator to generate control signals.

- **General PWM Timer 32-Bit (GPT32)**

The General PWM Timer 32-Bit (GPT32) features a set of highly configurable, 32-bit general purpose timers. This timer also has the enhanced capability to generate PWM waveform, PWM delay, perform pulse width measurement and capture inputs using up and down counters. Counter start, stop, and clear operations can be triggered by multiple internal events or by several external inputs. GPT32 has the flexibility to select clock sources independently for each channel. GPT32 can insert dead time during complimentary PWM operations and also generate A/D converter start triggers.

- **Asynchronous General Purpose Timer (AGT)**

The 16-bit Asynchronous General Purpose Timer (AGT) generates configurable output pulses, measures the pulse width and period of an external signal, and counts external events. AGT can be operated in five different modes: timer, pulse output, event counter, pulse width measurement, and pulse period measurement—each of which provides flexibility and capability to perform a variety of counting functions. AGT can be operated using a number of different clock sources such as a peripheral clock, a low-speed on-chip oscillator, and an underflow signal of the timer.

- **Watchdog Timer (WDT)**

The Watchdog Timer consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The WDT can reset the MCU or generate a non-maskable interrupt upon timer underflow. This feature is particularly useful for returning the MCU to a known state as a failsafe mechanism when the system runs out of control. The WDT can be triggered automatically upon reset, underflow, or refresh error, or by refreshing the count value in the registers.

■ Safety

- **SRAM Parity Error Check**

The SRAM Parity Error Check provides functionality to check SRAM for parity errors upon reading. The error check function appends a parity bit to an 8-bit word in SRAM at the time of writing, and it then performs an even parity check at the time of reading. Depending on the result of the parity check, an interrupt or system reset can be asserted. This feature is particularly useful for applications that require compliance with the IEC 60730 Safety Standard for Household Appliances.

- **Flash Area Protection**

Flash Area Protection provides the functionality to write-protect an area within the Code Flash to prevent undesired self-programming. The start block and end block addresses of the write-protect window can be configured in the boot mode, the self-programming mode, and the debugger mode. The Flash Area Protection feature can be enabled only during self-programming in single-chip mode per block basis. This feature is particularly suitable for applications that require compliance with the IEC 60730 Safety Standard for Household Appliances.

- **ADC Diagnostics**

ADC Diagnostics consist of multiple techniques for early detection of erroneous or improper operation of the ADC. These techniques help improve the reliability and quality of a product and they are particularly useful for meeting requirements of the IEC 60730 Safety Standard for Household Appliances. ADC diagnostics diagnose sample-and-hold circuits and input multiplexers by applying known reference voltages to input channels in a controlled manner. Input disconnect detection assist features can be used to detect an input disconnection by means of controlled charging and discharging of the input circuits. Integrated functionality to pre-charge (pull up) and discharge (pull down) the sample-and-hold capacitor eliminates the need for an external discharging path and components, thus reducing system complexity, bill of material (BOM) costs, and PCB footprint. Additionally, an external voltage reference check can be performed to detect unusual variation in the external reference voltage, and the data registers can be cleared automatically to prevent repeated “previous” value readings when, in the absence of a trigger, the ADC is not converting signals.

- **Clock Frequency Accuracy Measurement Circuit (CAC)**

The Clock Frequency Accuracy Measurement Circuit (CAC) is used to check the system clock frequency with a reference clock signal by counting the number of pulses of the clock to be measured (system clock) and comparing that number to the reference clock. The reference clock can be provided externally through a GPIO pin or internally from a variety of on-chip oscillators. Event signals can be generated in case of clock mismatch. This feature is particularly useful in implementing a failsafe mechanism for home and industrial automation applications.

- **CRC Calculator**

The CRC Calculator feature generates cyclic redundancy check codes to detect errors in the data in the CRC data register. CRC codes can be generated for any desired 8-bit or 32-bit data, and the CRC is executed in parallel on 8 bits or 32 bits. The bit order of the CRC calculation result can be switched for LSB-first or MSB-first communication. Additionally, a variety of CRC generation polynomials are available to the user. Snoop functionality allows for monitoring reads from and writes to specific addresses. This functionality is useful in applications that require CRC code to be generated automatically in certain events; for example, in monitoring writes to the serial transmit buffer and reads from the serial receive buffer.

- **Data Operation Circuit (DOC)**

The Data Operation Circuit (DOC) peripheral can perform 16-bit addition, subtraction, and comparison without CPU intervention. It is particularly useful in reducing CPU load while performing tests on large sections of the memory. Multiple event signals can be generated depending on the result of the data operation. The DOC is suitable for meeting requirements of the IEC 60730 Safety Standard for Household Appliances.

- **Port Output Enable for GPT (POEG)**

The Port Output Enable for GPT (POEG) feature can be used to disable timer output pins in response to several events in order to implement safety mechanisms. The output pins can be disabled upon detecting a change in the result of the comparator output, a dead time error from the timer, a rising edge or high level of GPIO pins, an oscillator stop, or a software setting. This feature is particularly suitable for applications that require compliance with the IEC 60730 Safety Standard for Household Appliances.

- **Independent Watchdog (IWDT)**

The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt upon timer underflow. Because the timer operates using an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a failsafe mechanism when the system runs out of control. The IWDT can be triggered automatically upon reset, underflow, or refresh error, or by refreshing the count value in the registers.

- **GPIO Readback Level Detection**

The GPIO Readback Level Detection feature can be used to read back the data written to GPIO pins when they are driven high or low. The input and output values written to and read back from the GPIO port control register can be compared to detect any abnormality with the GPIO connections (for example, external shorts to ground or supply voltage). This feature is particularly useful for applications that require compliance with the IEC 60730 Safety Standard for Household Appliances.

- **Memory Protection Unit (MPU)**

The MCU incorporate memory protection functionalities provided by the four memory protection units: Bus Master MPU, Bus Slave MPU and ARM MPU. The Bus Master MPU monitors the address of bus master access to the memory space. Access control can be set for up to 32 regions and access to each region can be monitored. When access to a protected region is detected, the Bus Master MPU generates an internal reset or a non-maskable interrupt. The Bus Slave MPU checks the access to the Bus Slave Function such as Flash or SRAM. The Bus Slave MPU has a separate protection register for each bus master and can protect access individually. If the access to the protected region is detected, the Bus Slave MPU generates an internal reset or a non-maskable interrupt. The ARM MPU has been implemented as the ARM® Cortex®-M architecture details which can be found on the ARM® website.

- **Register Write Protection**

System and power management registers can be register write protected to secure sensitive hardware configurations. Protect bits can be used to write-protect clock generation and control registers, low power mode control registers, software reset registers, and low voltage detect registers. When SFRs are write-protected, only register writes are protected; register reads are performed normally. This feature is particularly useful for applications that require compliance with the IEC 60730 Safety Standard for Household Appliances.

- **Main Oscillator Stop Detection**

The Main Oscillator Stop Detection feature can detect malfunctioning of the main clock oscillator and provide an alternative clock from the on-chip oscillator (MOCO) as the system clock. An oscillation stop detection interrupt request can be generated upon oscillator stop detection. The stop detection can also be sent to the Port Output Enable for GPT (POEG) peripheral to disable timer output pins to implement safety mechanisms.

- **Illegal Memory Access**

The Illegal Memory Access feature provides a mechanism to generate an interrupt any time the CPU illegally accesses the default memory map. Such instances include accessing areas in which memory is not allocated. This MCU also incorporates a CPU stack pointer monitor that detects underflows and overflows of the stack pointers. These include the monitor for the SP_main and SP_process, stack pointers. When a stack pointer underflow or overflow is detected, the CPU stack pointer monitor generates an internal reset or a non-maskable interrupt.

System and Power Management

- **Low Power Modes**

The low power modes provides operational flexibility to dramatically reduce current consumption. In applications that do not require the CPU to run code, the snooze feature allows certain peripherals to operate while the CPU and other peripherals remain disabled. Independent wake-up signals are provided for the data acquisition and data transmission peripherals. While the device is in low power snooze, sub-system clock settings are retained.

- **Switching Regulator**

The microcontrollers feature an integrated, low-quiescent DC-DC buck convertor and a low-dropout linear voltage regulator to supply power to the core, memory subsystem, and other digital peripherals. The power rail for these peripherals can be switched between the DC-DC buck convertor and the linear regulator depending on the overall current requirement for a wide range of operating conditions. Using the DC-DC buck convertor reduces the power dissipated in the device and increases efficiency for high-load currents as compared to using a linear regulator. Additionally, low quiescent current consumption results in extended operating time for battery-powered end applications.

- **Realtime Clock (RTC)**

The 32-bit RTC can be used to keep an accurate track of time. The RTC can be operated in calendar count mode and in binary count mode. In calendar count mode, it keeps track of time in years, months, days, dates, minutes, and seconds, and it supports automatic adjustment for the leap year. In binary count mode, the RTC maintains only the count value, which is useful for tracking a calendar other than Gregorian calendar. The RTC operates on one 128-Hz clock, which can be provided from an external crystal or an internal low-frequency oscillator. Additionally, there are three input pins that can be used to capture the time from the RTC.

- **Event Link Controller (ELC)**

The Event Link Controller (ELC) peripheral enables direct interaction between different peripherals without CPU intervention. This controller routes source event signals generated by peripherals to event inputs of other peripherals, thereby allowing direct signaling from one peripheral to another. The ELC also makes it possible to handle a large number of event signals with a limited number of available interrupt vectors. Additionally, the event signals can activate a peripheral for a desired operation—for example, start/stop/clear timer, up/down counting, trigger ADC and DAC conversion, and change state of GPIO—and issue an interrupt to the CPU. Almost every peripheral is capable of generating event signals.

- **DMA Controller (DMAC)**

The Direct Memory Access Controller (DMAC) peripheral can transfer data between memory and peripherals, or between two peripherals without CPU intervention. The DMA Controller supports multiple data transfer channels, each with its own priority, and can transfer up to 64 MB of data. The DMA Controller can operate in normal transfer mode, repeat transfer mode, and block transfer mode, each of which provides flexible operation to suit a variety of use cases. The data transfer unit size can be 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits), and a single block of data can consist of up to 1024 units. The activation source for each of the sources can be selected independently.

- **Data Transfer Controller (DTC)**

The Data Transfer Controller (DTC) peripheral can be used to transfer data between memory and registers without CPU intervention. It can be operated in normal transfer mode, repeat transfer mode, and block transfer mode, each of which provides flexible operation to suit a variety of use cases. The data transfer unit size can be 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits), and a single block of data can consist of up to 256 units.

- **Port Function Select (PFS)**

Most digital IO pins are multiplexed among different peripherals; that is, many peripherals have their signals mapped to different pin groups. The Port Function Select peripheral controls routing and assignment of multiple digital signals from different peripherals to different IO pins. This functionality provides design flexibility to simplify PCB layout and to optimize system performance. It also enables easier migration to different MCU products within the same product family without requiring a significant effort in redesigning the PCB.

Security and Encryption

The security and encryption block features several security features and National Institute of Standards and Technology (NIST)-compliant, primitive cryptographic algorithms for various network communication applications. These features and algorithms can be used to perform authentication and secure channel communication between the microcontroller and an external communication device or network, and also to encrypt confidential and sensitive data for storage in the microcontroller. The security and encryption block also features high-throughput and low-power hardware accelerators to enable authentication and to meet secure communication requirements for most network applications.

Each microcontroller has a 128-bit unique identification word programmed in it which can be used to generate secure firmware keys using a variety of encryption algorithms. The security and encryption block incorporates a high-throughput, true random number generator (TRNG) that can generate random numbers with high entropy for use as a seed to other deterministic random number generators (such as NIST SP800-90A DRBG). Several hashing functions are also supported (SHA1/SHA224/SHA256/GHASH).

In addition, the security and encryption block supports several NIST-compliant symmetric algorithms for data exchange. The data transmitter and receiver uses the symmetric keys. Advanced Encryption Standard (128/192/256-bit), Data Encryption Standard 3DES and Alleged RC4 (ARC4) algorithms are supported.

Lastly, the security and encryption block also supports several NIST-compliant asymmetric algorithms for data exchange. The data transmitter and receiver uses the asymmetric keys. Rivest, Shamir and Adleman (RSA), Digital Signal Algorithm (DSA) are supported.

Human Machine Interface (HMI)

- **Graphics LCD Controller (GLCDC)**

The highly configurable, integrated Graphics LCD Controller can drive a variety of color TFT LCD screens. The controller reads image data from system memory, displays it on an LCD screen, and frees up the CPU for other processing tasks. It is capable of generating control signals from internal vertical synchronization and horizontal synchronization signals, and it can output image data in a format (serial and up to 24-bit parallel) compatible with the number of LCD screens. The graphics controller can be used to superimpose two drawing planes and one background plane, and also to perform alpha-blending, dither correction, brightness and contrast correction, and gamma correction on the image data. Low current consumption makes this controller suitable for handheld and battery-operated commercial and home applications.

- **JPEG Codec**

The on-chip JPEG engine performs high-speed image data compression and decoding of JPEG image data. The JPEG engine conforms to the JPEG baseline decompression standard, JPEG Part 2, ISO-IEC 10918-2. It supports compression and multiple pixel formats for decompression, and it provides four Huffman tables—two for AC coefficients and two for DC coefficients—which are used for error management during decompression. The JPEG engine is particularly useful in displaying JPEG images in low-cost HMI applications.

- **2D Drawing Engine (DRW)**

The 2D Drawing Engine (DRW) provides functionality to update the frame buffer with graphical content to be displayed on the LCD screen while reducing the CPU load. This feature supports a variety of 2D graphic primitives such as lines, polygons, circles, ellipses, and quadratic Bezier curves along with custom geometries. The DRW can be used to perform alpha-blending, anti-aliasing, outlining, texture mapping, and transformation. It also supports BitBLT (bit boundary block transfer), which allows two bitmaps to be combined, and it can be used to perform fill, copy, rotate, scale, alpha blending, color conversion, bilinear filtering, and similar operations.

- **Capacitive Touch Sensing Unit (CTSU)**

The Capacitive Touch Sensing Unit module enables detection of touch by measuring the change in parasitic electrostatic capacitance of the sensing electrode. The change in electrostatic capacitance of an electrode is detected using either a self-capacitance or mutual-capacitance method. Self-capacitance supports operation in single scan and

multi-scan modes. The capacitive touch module provides a cost-effective way to replace mechanical buttons and sliders with appealing, exciting, and durable touch interfaces for a variety of industrial and home applications.

- **Parallel Data Capture Unit (PDC)**

The Parallel Data Capture Unit can transfer parallel data (such as image output) from external I/O devices (such as cameras and image scanners) to the MCU's SRAM or external address space (such as SDRAM) via the on-chip DMA controller or Data Transfer Controller. The Parallel Data Capture Unit can capture a wide range of parallel data: 1 to 4095 lines in the vertical direction and 4 to 4095 bytes in the horizontal direction. The camera interface can also generate a 1–30-MHz external transfer clock. It allows monitoring of VSYNC and HSYNC signals as well as error detection while receiving data so that software control can be applied.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HALII Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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