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April 1st, 2010
Renesas Electronics Corporation

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M62301SP/FP

10 to 12-bit 4-ch Integrating A/D Converter

REJ03D0861-0300

Rev.3.00

Mar 25, 2008

Description

M62301 semiconductor integrated circuit forms an integrating A/D converter, being connected to a microcomputer unit. By using selection signals and counter clock signals from the unit, a 10 to 12-bit A/D converter can be created at a low cost.

The integration time and resolution can be set at the users option by changing external parameters. In addition, the built-in circuit offset, delay time and temperature fluctuation are adjustable, enabling a wide range of applications. M62301 has a 3 input decoder circuit, high-precision reference voltage (1.22 V) generator, current supply and comparator for integration, and voltage-monitoring reset circuit for a 5 V power supply. It is also equipped with girdling to prevent current leak from integration capacitor.

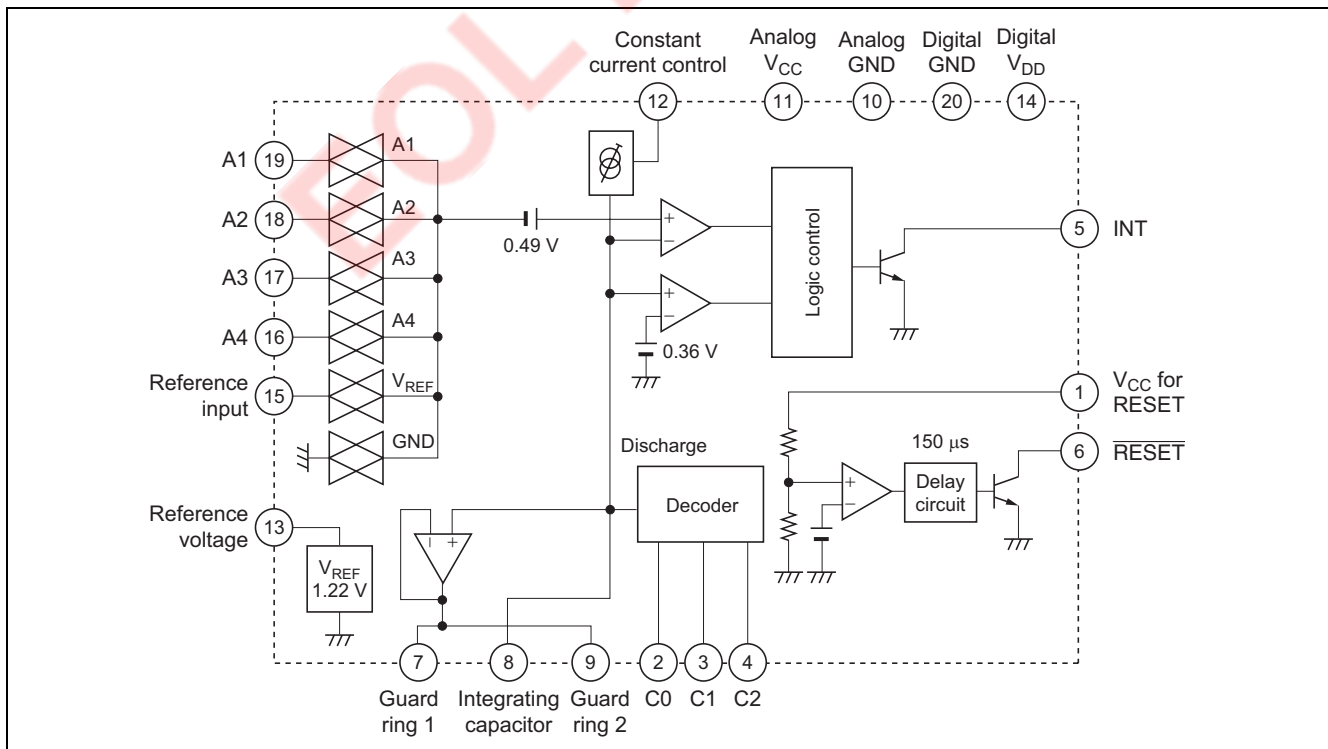
Features

- Separate power supplies for analog section and digital section.
- Low power dissipation: 2 mA (Typ)
(1 mA for A/D conversion and the other 1 mA for reset)
- Linear error: $\pm 0.02\%$ (Typ)
- Conversion time: 526 $\mu\text{s}/\text{ch}$ (Typ)
- Built-in system reset: 4.45 V (Typ)

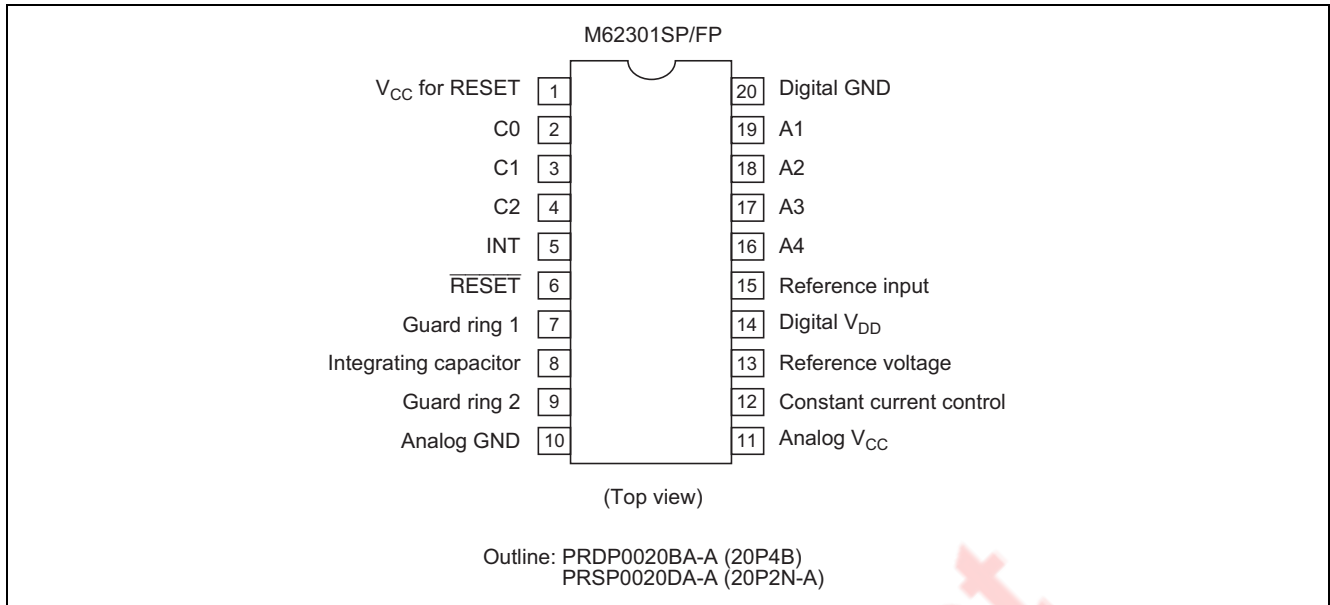
Application

High-precision control systems such as temperature control and speed control

Block Diagram



Pin Arrangement



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Ratings	Unit
Analog section supply voltage	V_{CC}	15	V
Digital section supply voltage	V_{DD}	8	V
Digital input voltage	V_{ID}	-0.3 to $V_{DD} + 0.3$	V
Analog input voltage	V_{IA}	-0.3 to $V_{DD} + 0.3$	V
INT output current	I_{OINT}	6	mA
Reset output current	I_{ORE}	6	mA
INT output withstand voltage	V_{INT}	15	V
Reset output withstand voltage	V_{RESET}	15	V
Reset supply voltage	V_{RE}	6	V
Power dissipation	P_d	990 (P) / 660 (FP)	mW
Thermal derating	K_θ	9.9 (P) / 6.6 (FP)	mW/ $^\circ\text{C}$
Operating temperature	T_{opr}	-20 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}	-40 to +125	$^\circ\text{C}$

Recommended Operating Conditions

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Limits			Unit
		Min	Typ	Max	
Analog section supply voltage	V _{CC}	4.5	8.0	12.0	V
Digital section supply voltage	V _{DD}	4.5	5.0	5.5	V
Analog input voltage range (I _I = 50 μA)	V _{IA}	0	—	No more than (V _{CC} – 2.5 V) and V _{DD} * ¹	V
Reference input voltage (I _I = 50 μA)	V _{IR}	1	—	No more than (V _{CC} – 2.5 V) and V _{DD} * ¹	V
Integration capacity	C _I	300	—	22000	pF
Resistance to determine charge current	R _I	6	—	60	kΩ
Output current	I _O	—	—	4	mA

Note: 1. Maximum analog input voltage is less than the difference between V_{CC} – 2.5 V as well as V_{DD}.

$$\text{Charging current } I_I = \frac{V_{REF}}{R_I}$$

Electrical Characteristics

(V_{CC} = 5.0 V, V_{DD} = 5.0 V, Ta = 25°C, unless otherwise noted)

	Item	Symbol	Limits			Unit	Test Conditions
			Min	Typ	Max		
A/D Converter	Supply current	I _{CC}	—	1.0	2.0	mA	
	Analog input voltage range	V _{IA}	0	—	2.5	V	I _I = 100 μA
					2.2		I _I = 200 μA
	Reference input voltage	V _{REF}	1.17	1.22	1.27	V	I _{REF} = ±5 μA C _{REF} = 4700 pF
	Permissible current inflow at reference voltage	I _{REF+}	—	—	50	μA	
		I _{REF-}	—	—	-10		
	Conversion error	E _C	—	0.05	0.1	%/FSR	R _I = 24 kΩ* ¹
	Linear error	E _L	—	0.02	0.09	%/FSR	R _I = 24 kΩ* ²
	Conversion time	T _T	—	526	—	μs	V _{IA} = 2.5 V, C _I = 0.01 μF R _I = 24 kΩ
	Discharge time	T _{di}	—	3	17	μs	V ₍₈₎ = 3 V → 0.3 V C _I = 4700 pF
	Analog input current	I _B	—	-0.35	-3.5	μA	
	Digital input "H" level	V _{IH}	3.5	—	—	V	
	Digital input "L" level	V _{IL}	—	—	0.8	V	
INT output "L" level	V _{LINT}	—	0.1	0.4	V	I _{OL} = 1 mA	
INT output leak current	I _{OHINT}	—	—	1	μA	V ₍₅₎ = 15 V	
Reset Section	Detection voltage	V _{DET}	4.30	4.45	4.60	V	
	Hysteresis voltage	ΔV _{DET}	30	50	80	mV	
	Delay time	T _{DE}	75	150	300	μs	
	Reset output "L" level	V _{LRE}	—	0.1	0.4	V	I _{OL} = 1 mA
	Reset output leak current	I _{OHRE}	—	—	1	μA	V ₍₆₎ = 15 V
	Supply current	I _{RE}	—	1.0	2.0	mA	V _{RE} = 5 V
	Limit operating voltage	V _{OPL}	—	0.75	1.0	V	R _L = 2.2 kΩ, V _{LRE} ≤ 0.4 V
—			0.6	0.8		R _L = 100 kΩ, V _{LRE} ≤ 0.4 V	

Notes: 1. Conversion error; Deviation from the line that links the "0" scale point (mode 0) and reference scale point (mode 3. V_{FSR} = 2.5 V). Associated with all channels.

2. Linear error; Deviation from the line that links the 0 V input point and 2.5 V input point on a given channel.

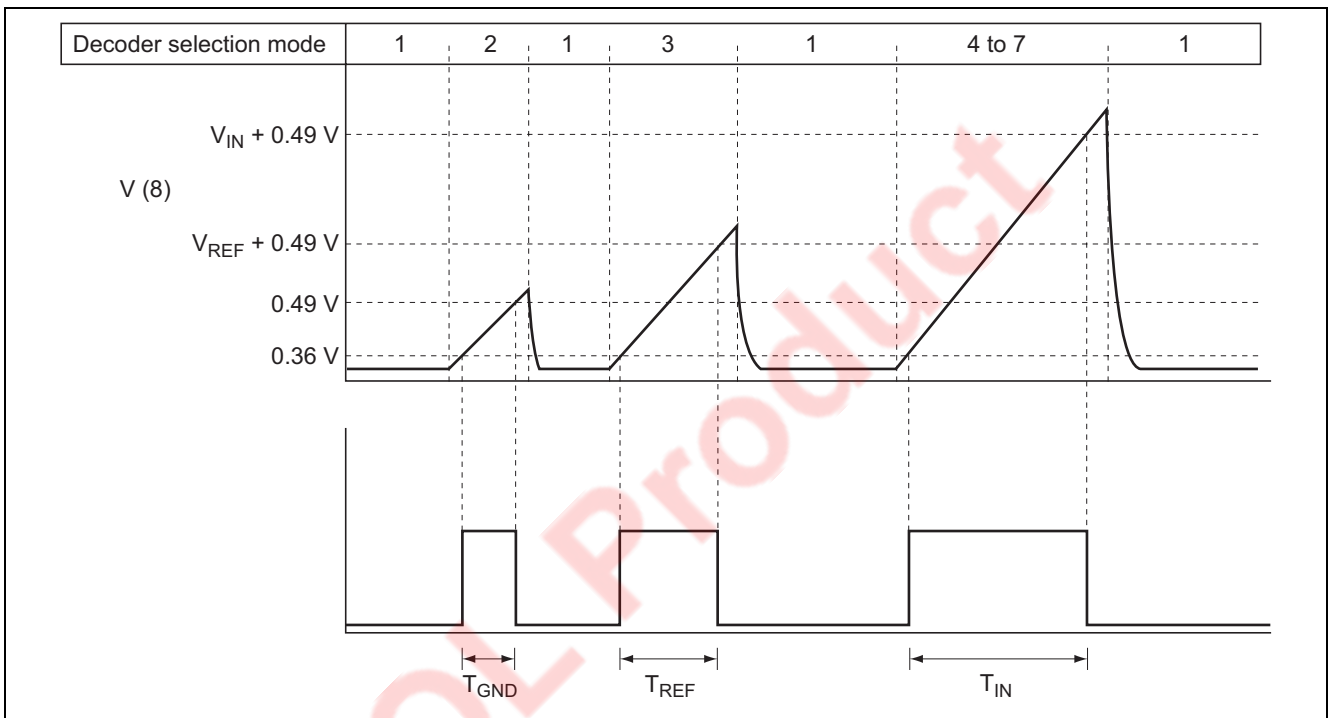
Operating Description

(1) Decoder

Based on digital inputs to C0, C1, C2, the analog switch is set to on, and the input of "0" scale (GND input), input of reference scale (reference voltage input), input to A1-A4, or discharge from integration capacitor (C_I) is performed. None of these operations is performed when the "mode 8" input is given:

Mode	1	2	3	4	5	6	7	8
C0	0	1	0	1	0	1	0	1
C1	0	0	1	1	0	0	1	1
C2	0	0	0	0	1	1	1	1
	Discharge	GND	V_{REF}	A1	A2	A3	A4	—

(2) A/D conversion



Multiplexer first selects V_{GND} , obtaining minimum pulse T_{GND} . It then selects V_{REF} , obtaining reference pulse T_{REF} . Input is selected next, obtaining input pulse T_{IN} . V_{IN} is obtained by deducting T_{GND} , as the offset, from T_{REF} and T_{IN} .

$$V_{IN} = V_{REF} \cdot \frac{T_{IN} - T_G}{T_{REF} - T_G}$$

By measuring voltage at the maximum input for approximately 500 μ s under the counter clock of 8 MHz, resolution of approximately 12 bits can be obtained;

$$\frac{500 \mu\text{s}}{125 \text{ ns}} \approx 2^{12}$$

Note: To ensure discharge from capacitor C_I , the decoder input as in the above diagram should stay in mode 1 at least for the period calculated above: $T_{di} = (C_I \times \frac{V_{I\text{Amax}} + 0.49}{1 \text{ mA}})$

It is not necessary to measure T_{GND} , and T_{REF} for each channel.

(3) Constant current control

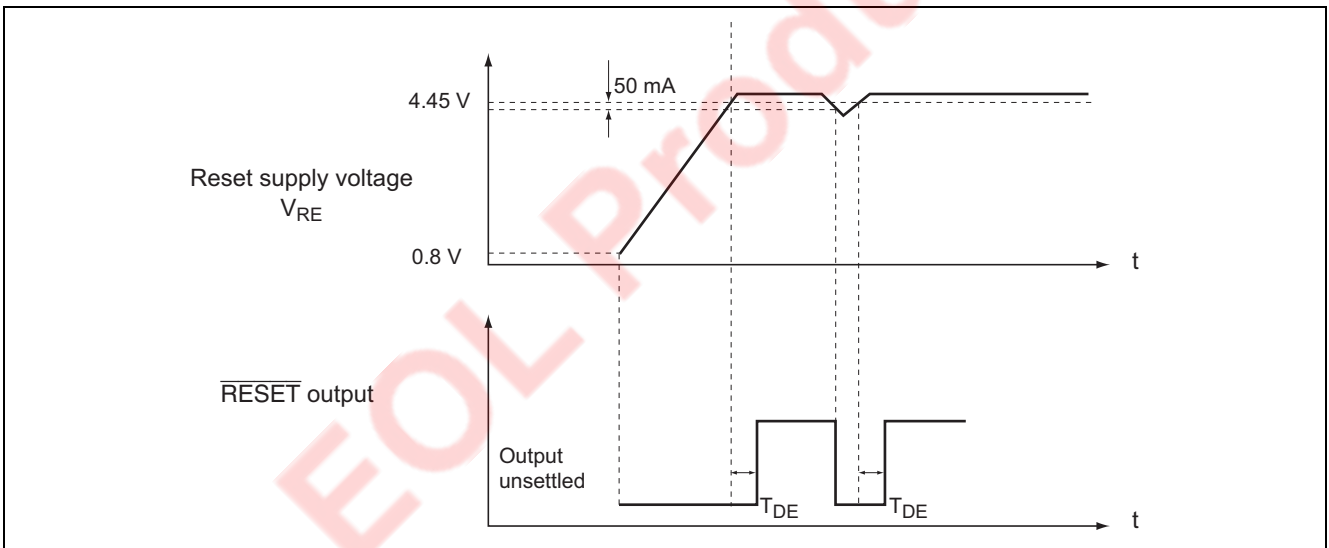
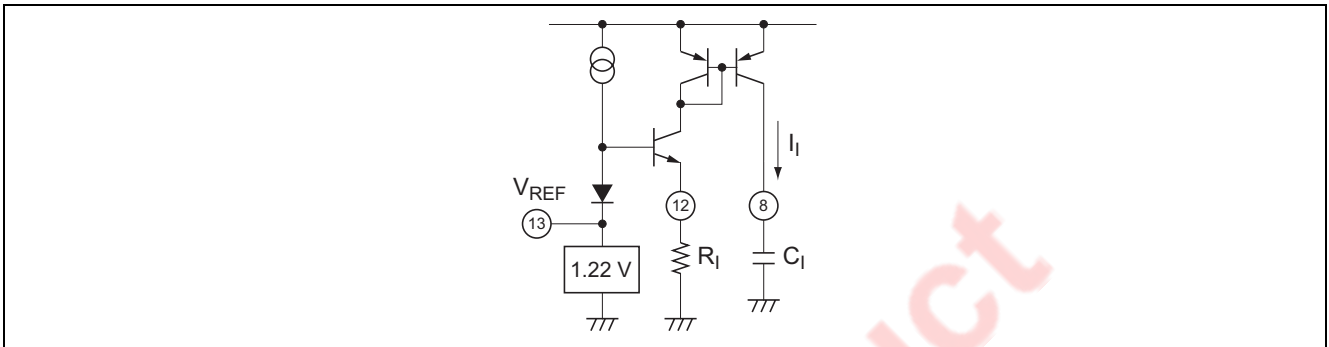
Integrating current I_I can be obtained based on the reference voltage (1.22 V) by the built-in high-precision generator and resistance R_I .

$$I_I = \frac{1.22}{R_I} \quad (\text{A}) \quad \dots\dots\dots (1)$$

Integration time T_I can be calculated as follows;

$$T_I = (V_{IN} + 0.49) \frac{C_I}{I_I} \quad \dots\dots\dots (2)$$

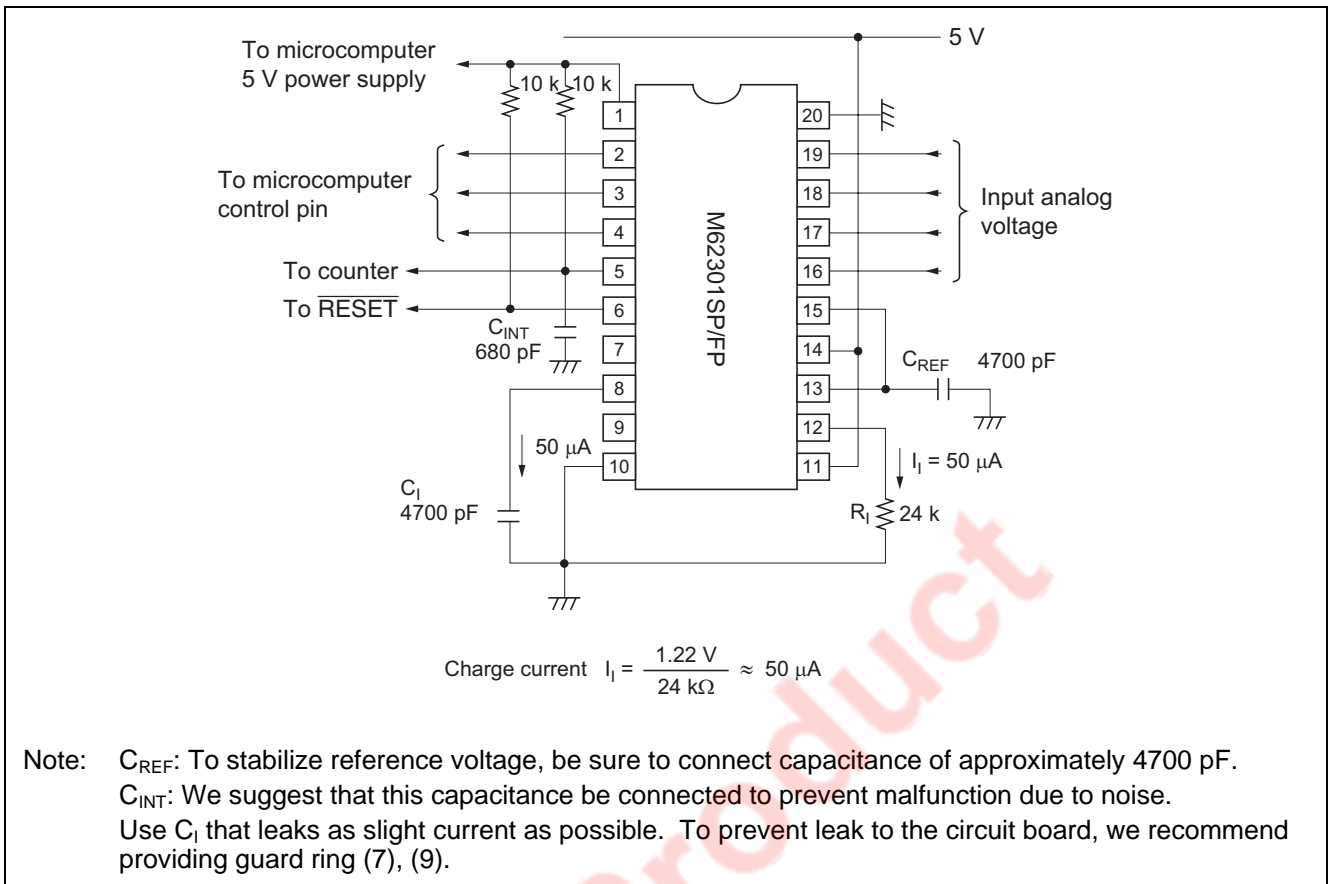
However, parameters such as built-in comparator offset voltage, analog switch offset, voltage leak current and delay time are not counted.



When voltage applied to pin V_{RE} becomes less than 4.45 V, the $\overline{\text{RESET}}$ output status becomes "L". If voltage increases over 4.50 V, the RESET status becomes "H" within 150 μs .

Application Suggestion

1. 4-channel 11-bit A/D converter system



Resolution depends on the number of microcomputer counter clock pulses that are generated while the INT output status is "high" at the maximum input voltage 2.5 V ($V_{CC} - 2.5 \text{ V}$).

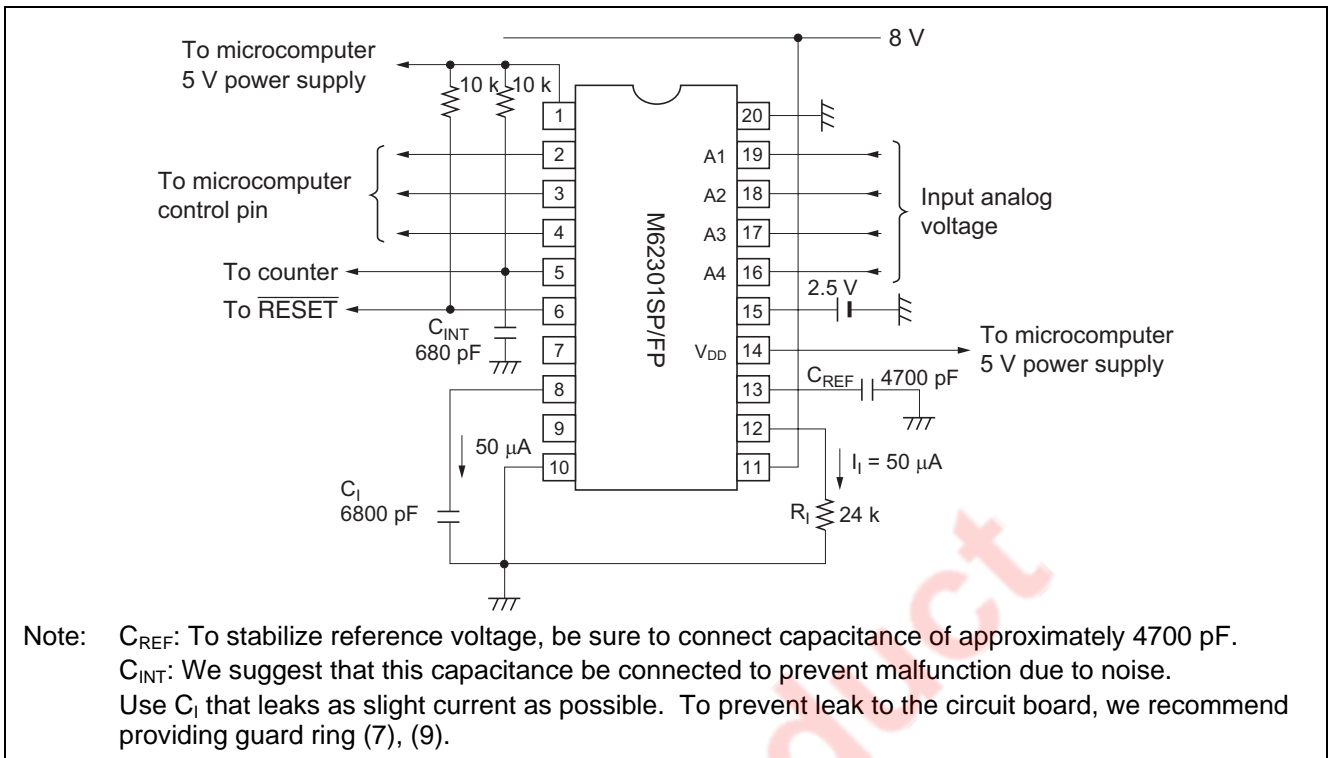
When the microcomputer counter clock frequency is 8 MHz, the resolution can be calculated by using the constant calculated above, as follows;

$$\frac{4700 \text{ pF} \times \frac{(2.5 + 0.13)}{50 \mu\text{A}}}{\frac{1}{8 \text{ M}}} \approx 2^{11}$$

Therefore, the resolution of this system is approximately 11 bits.

2. 4-channel 12-bit A/D converter system

Separate power supplies to analog section and digital section, analog input voltage range mode wider up to V_{DD} , external reference voltage for integration.



Because separate power supplies are provided for the analog and digital sections, the M62301 has two supply voltages V_{CC} and V_{DD} , enabling a wide analog input voltage range V_{IA} . The upper limit of the range is required to be no more than the difference between $V_{CC} - 2.5$ V as well as V_{DD} , therefore, the analog input voltage range in this application is 0 V to 5 V.

When the counter clock frequency is 8 MHz, resolution is;

$$\frac{6800 \text{ pF} \times \frac{(5 + 0.13)}{50 \text{ } \mu\text{A}}}{\frac{1}{8 \text{ M}}} \approx 2^{12}$$

An A/D converter system with resolution of approximately 12 bits can be formed.

Recommended operational settings according to clock frequency, resolution, and time required for discharge (decoder mode 1)

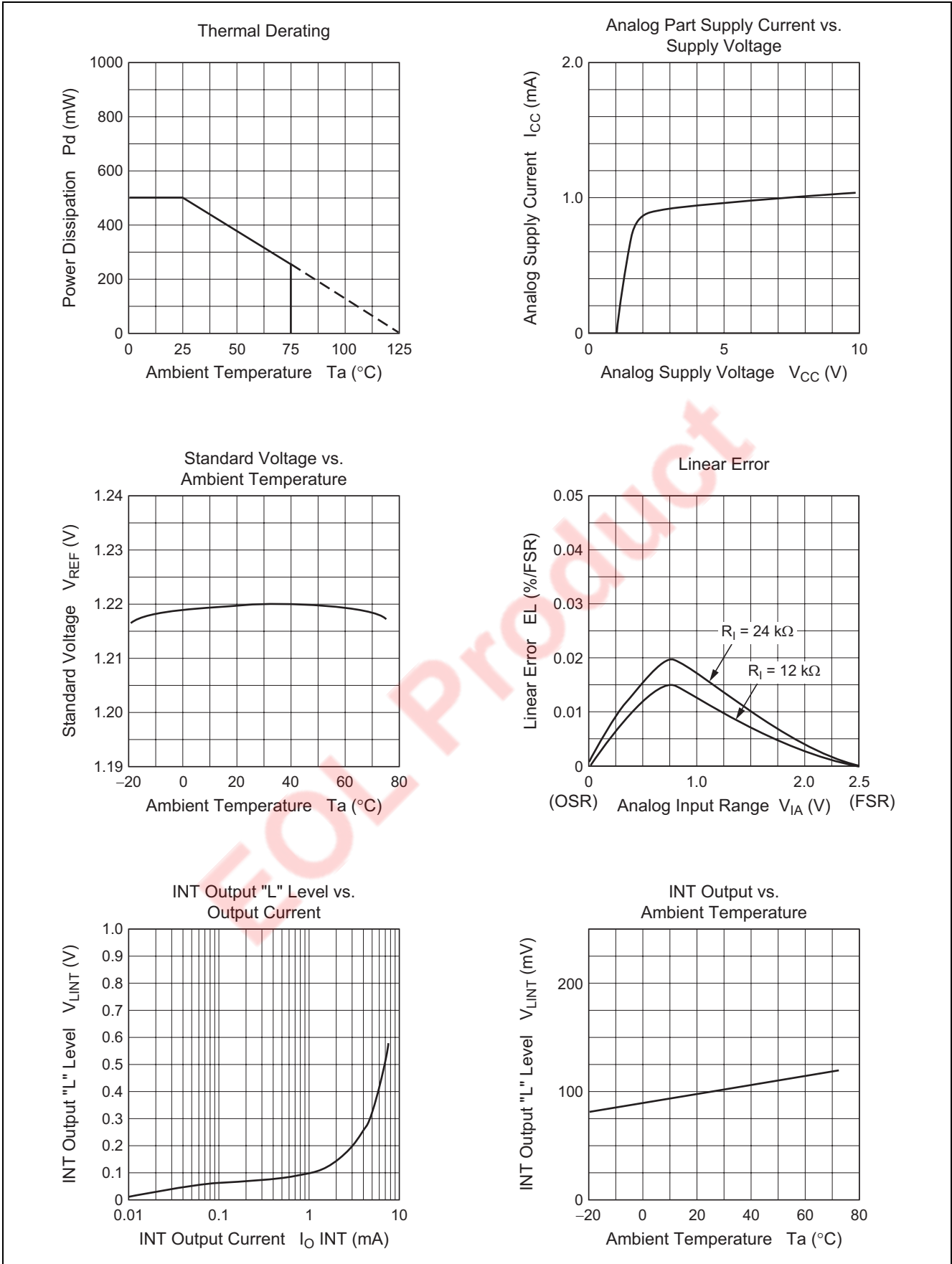
Counter Clock	Resolution	Change Current I _I (μA)	Resistance to Determine Constant Current R _I (kΩ)	Integration Capacitance C _I	Discharge Time T _{di} (μs)
8 MHz	10-bit	50	24	1400 pF	7.7
		100	12	2800 pF	15.4
	11-bit	50	24	2800 pF	15.4
		100	12	5600 pF	30.7
	12-bit	50	24	5600 pF	30.7
		100	12	12000 pF	65.9
16 MHz	10-bit	50	24	700 pF	3.9
		100	12	1400 pF	7.7
	11-bit	50	24	1400 pF	7.7
		100	12	2800 pF	15.4
	12-bit	50	24	2800 pF	15.4
		100	12	5600 pF	30.7

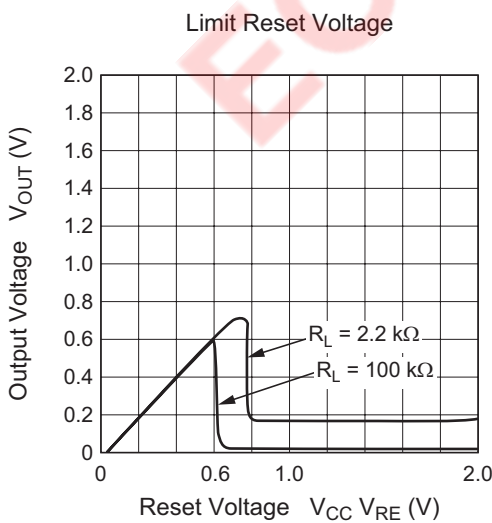
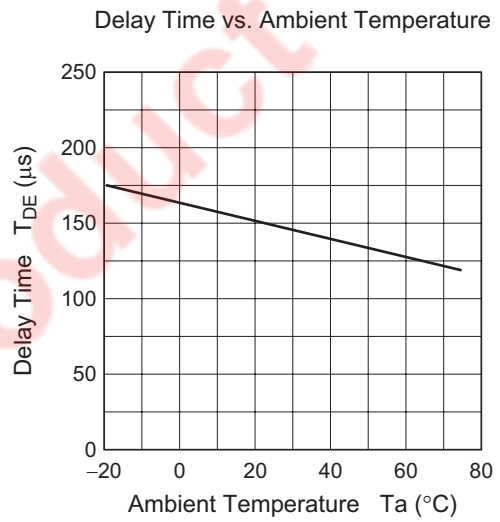
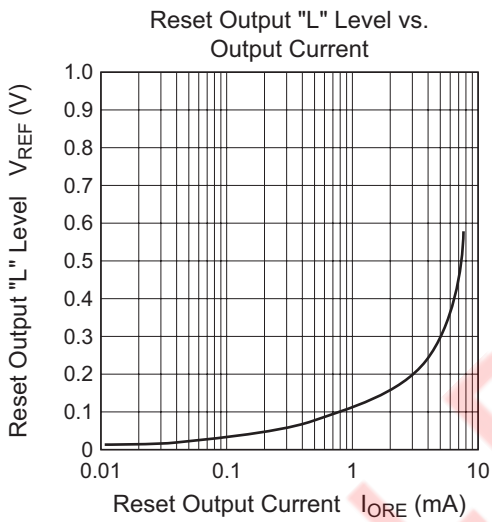
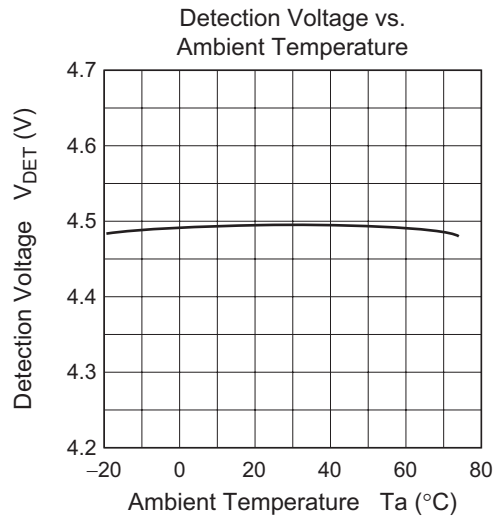
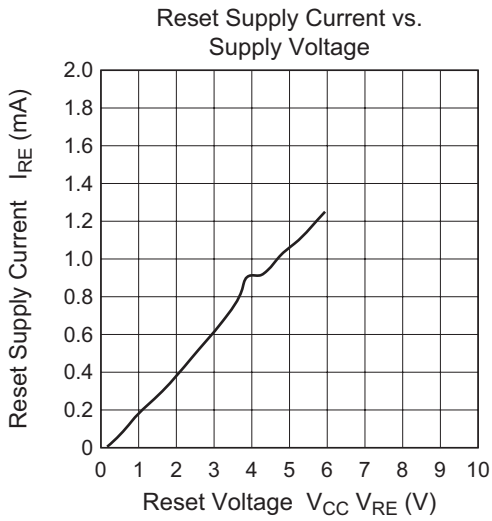
Note: 1. Discharge time $T_{di} = (C_I \times \frac{(V_{I_{max}} + 0.49)}{1 \text{ mA}})$

The values in this table apply when $V_{I_{max}}$ is 5 V.

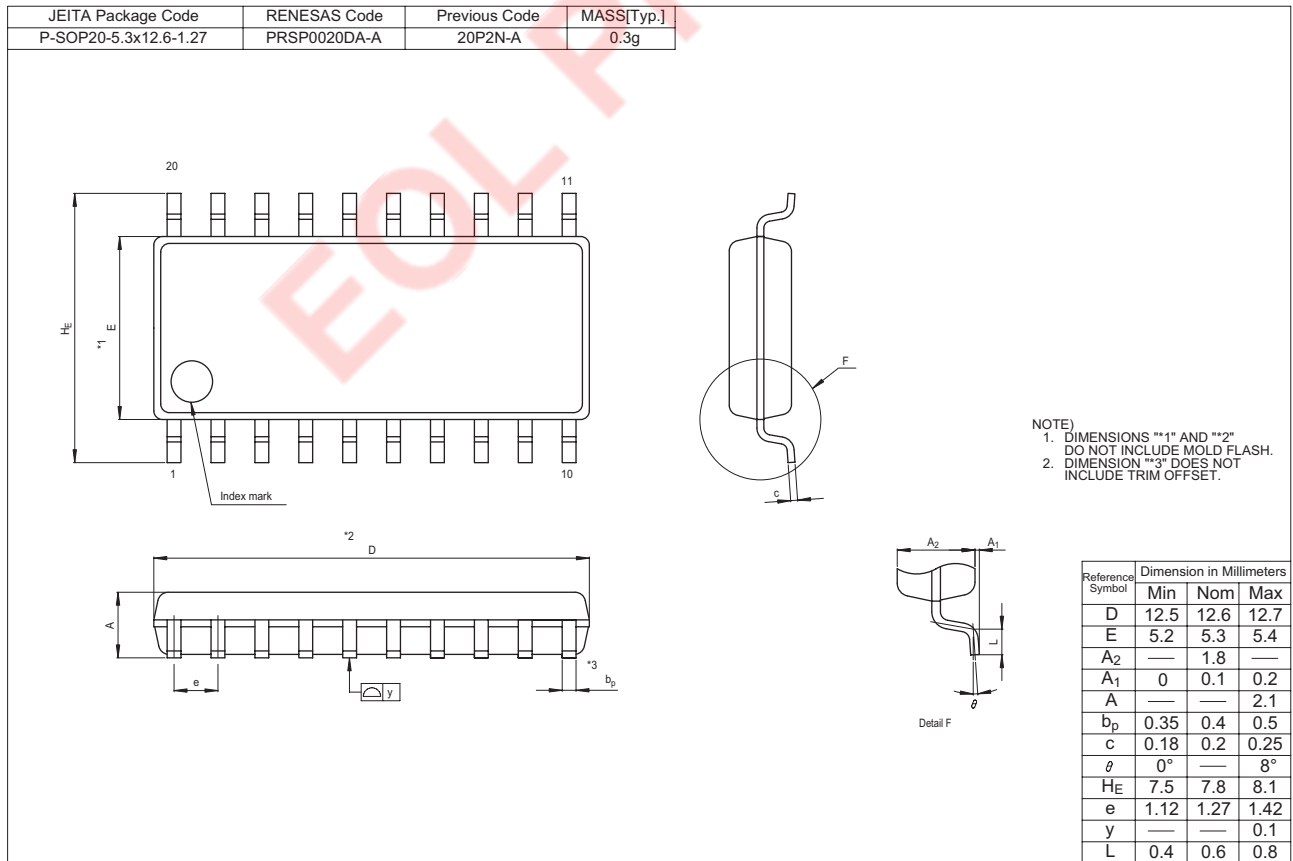
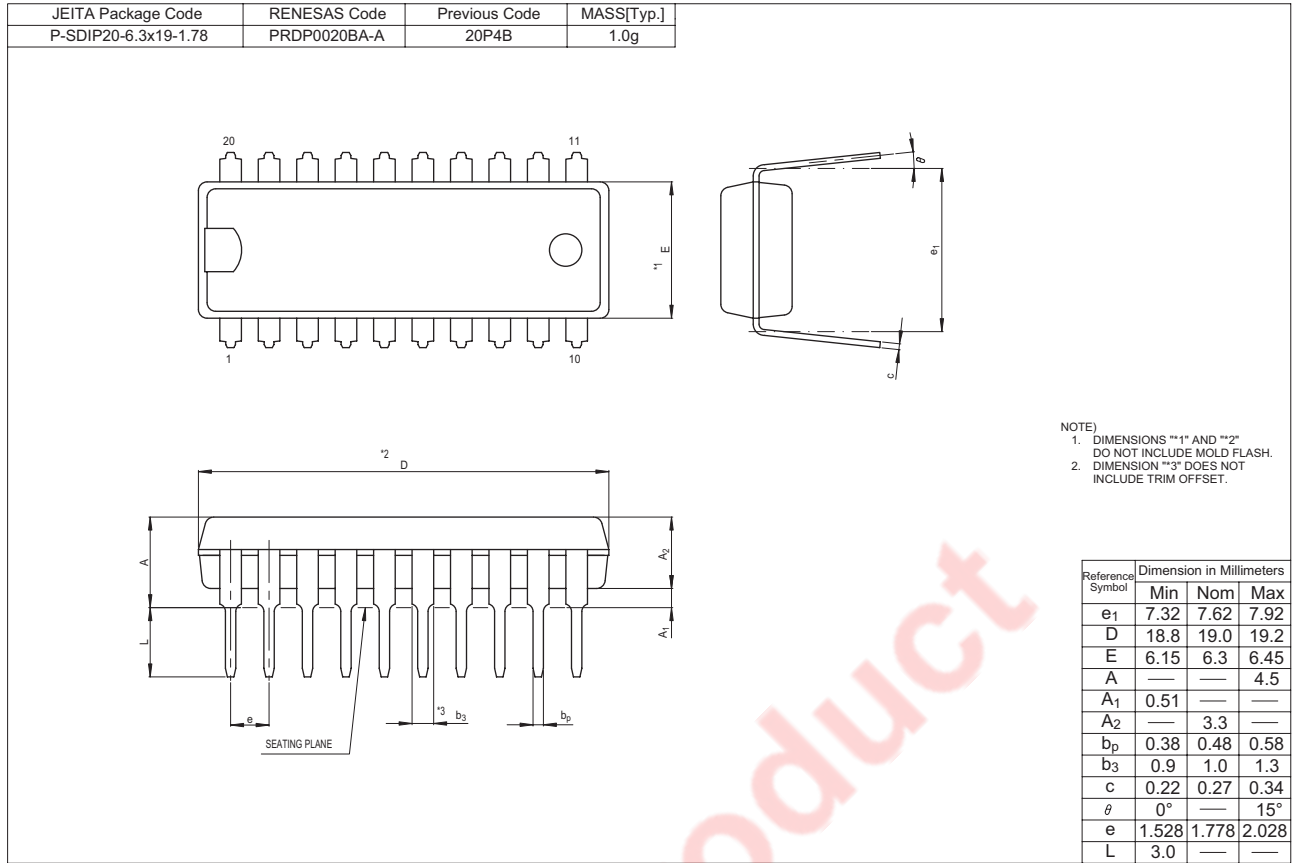
EOL Product

Typical Characteristics





Package Dimensions



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