1. Overview

1.1 Introduction

The R-Car M2-W is an SOC that features the basic functions for next-generation car navigation systems.

The R-Car M2-W includes:

- Two 1.5-GHz ARM Cortex™-A15 MPCore™ cores,
- SuperH™ RISC Engine (optional),
- Memory controller for DDR3-SDRAM (DDR3-1600) with 32 bits × two channels,
- Two- and three-dimensional graphics engines,
- Video processing unit,
- Sound processing unit,
- SD card host interface,
- USB3.0 and USB2.0 interfaces,
- PCI Express interface,
- Serial ATA interface, and
- CAN interface.

Also, a full implementation of the extremely expandable and Internal AXI bus has been adopted for the R-Car M2-W.

This bus structure is optimized for maximum system performance, leading to the realization of high-performance and cost-effective premium in-vehicle infotainment systems.

Notes: 1. ARM is a registered trademark and Cortex is a trademark of ARM Limited. All other brands or product names are the property of their respective holders.
2. For items listed as "optional", contact your local Renesas sales representative.

1.2 System Configuration Diagram

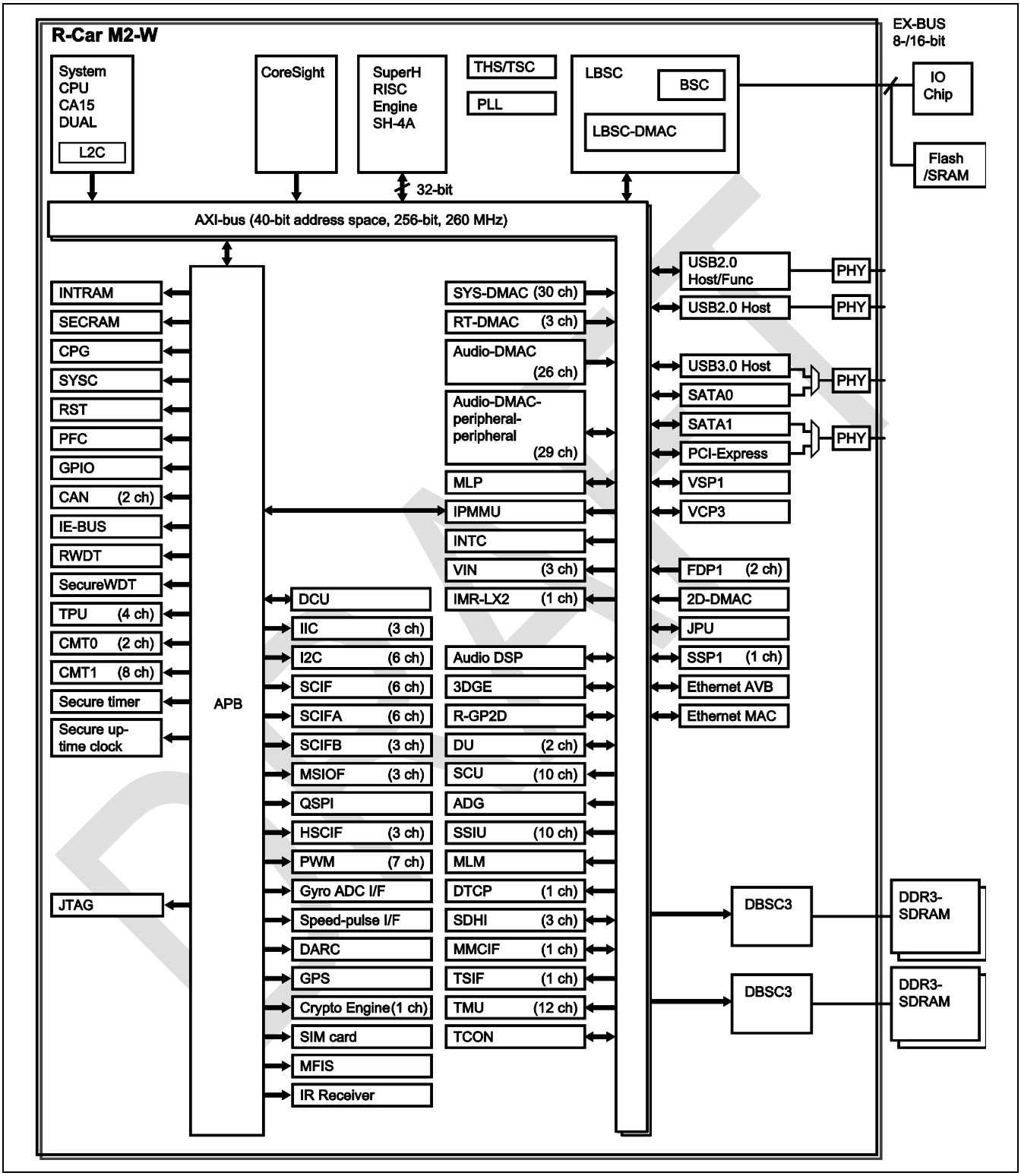


Figure 1.1 R-Car M2-W System Configuration

1.3 List of Specifications

1.3.1 ARM Core

Item	Description
System CPU CA15	• ARM Cortex-A15 Dual MPCore 1.5 GHz • L1 I/D cache 32/32 Kbytes, L2 cache 1 Mbyte • NEON™/VFPv4 supported • Security extension supported
ARM debugger (CoreSight)	• CoreSight system compliant • JTAG/SWD I/F supported • CoreSight PTM-A15 supported (each CPU) • CoreSight ETR 16 Kbytes for program flow trace • CoreSight ETR 4 Kbytes for system trace

1.3.2 SuperH RISC Engine (Optional)

Item	Description
SH-4A	• SH-4A architecture • Maximum frequency: 780 MHz
User debugging interface (H-UDI)	• Single channel • JTAG interface (TCK, TMS, TRST#, TDI, and TDO) • E10A emulator support • Realtime branch trace

1.3.3 CPU Core Peripherals

Item	Description
Operating clock pulse generation circuit (CPG)	• Generates the clocks from external clock (EXTAL1). — Maximum CA15 clock: 1.5 GHz — Maximum AXI-bus clock: 260 MHz — Maximum SDRAM bus clock: 800 MHz (DDR3-1600), 666 MHz (DDR3-1333) — Maximum media clock: 260 MHz — Maximum peripheral clock (HPϕ): 130 MHz • System-CPU shut down mode control supported • Module-standby mode supported • Includes module reset registers to control reset operation of individual on-chip peripheral modules
System controller (SYSC)	• Shuts down and restores power to target modules. Target modules: — Cortex-A15 (with independent shutting down of CPUs 0, 1, and SCU+L2$)*1 — 3DGE*2 — SH-4A Notes: 1. SCU and L2$ are treated as one power-domain. When CPU is working, SCU+L2$ can't be powered off. 2. Although 3DGE is a target of power-shutdown, version/revision is different from H1's 3DGE. Please refer to 3DGE's specification.
Reset (RST)	• Includes one reset-signal external output port for external modules • Includes Boot Address Register etc.
Pin function controller (PFC)	• Setting multiplexed pin functions for LSI pins Function of the R-Car M2-W pin selectable by setting the registers in the PFC module. • Module selection Enable and disable the functions of R-Car M2-W LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module. • Pull-up control for each LSI pin On/off of the pull-up resistor on each LSI pin can be controlled by setting the registers in the PFC module. • Control of SDIO functions SDIO functions, including the driving ability of pins for the SDIF, can be controlled by setting registers of the PFC.
General-purpose I/O (GPIO)	• General-purpose I/O ports: 244 • Supports GPIO interrupts.
Thermal sensor (THS/TSC)	• Single channel of thermal sensor • Programmable 4 temperature level for the sensor, to indicate the temperature level • Selectable operation (Interrupt/Reset) when the temperature reaches programmed

1.3.4 External Bus Module

Item	Description
Local bus state controller (LBSC)	• EX-BUS interface: max. 16-bit bus • Frequency: 65 MHz • External area divided into several areas and managed — Allocation to space of area 0, area 1, and area 6 or allocation to space of area 0 only is selected at startup time. — Area 0 supports 128-Mbyte memory space (startup mode). — Space of area 6 is divided into up to six areas (capacity of each area variable) and managed — I/F settings, bus width settings, and wait state insertion are possible for each area • SRAM interface — Wait states can be inserted through register settings — Period of waiting is set in cycle unit, and the maximum value is 15. — EX_WAIT pin can be used for wait state insertion — Connectable bus widths: 16 bits or 8 bits • Burst ROM interface — Wait states can be inserted through register settings — Number of bursts can be set through register settings — Connectable bus widths: 16 bits or 8 bits • Byte-control SRAM interface (available with areas 1 and 6 only) — Byte-control SRAM interface — Wait states can be inserted through register settings — EX_WAIT pin can be used for wait state insertion — Connectable bus widths: 16 bits or 8 bits • ATA interface (two ports) — Wait states can be inserted through register settings — Supports PIO modes 0 through 4 — Supports multi-word modes 0 through 2 — Supports Ultra DMA modes 0 through 4 (Ultra ATA66) — Ready timeout detection (detection time (ns) = EX-BUS operating frequency (ns) × 100 clock cycles) • Supports external buffer enable/direction control

Item	Description
LBSC-DMAC	• Three channels • Address space: Physical address space • Transfer direction: Peripheral to memory (AXI-bus), memory (AXI-bus) to peripheral • Data packing for peripheral read data: Memory write data length is selectable as transfer data length to memory side. • Transfer data length: Peripheral (APB-bus) side: 1, 2, 4 bytes Memory (AXI-bus) side: 4 or 16 (channel 2), 32 (channel 0 and 1) bytes • Transfer burst length: 1, 8 (transfer with a burst length of 8 supported only for LBSCDMAC00, 01) • Number of transfers — Maximum number of transfers: 16 M (16,777,216 transfers), 64M (67,108,864 transfers), (64 M transfers supported only for LBSC-DMAC00) — Minimum number of transfers: One • Address mode: Dual address mode • Transfer modes: Single transfer mode, continuous transfer mode • Transfer end interrupt: Occurs at the end of the number of transfers specified in the register
External bus controller for DDR3-SDRAM (DBSC3)	• Two channels (32-bit bus mode) or single channel (64-bit bus mode) • DDR3-SDRAM/DDR3L-SDRAM can be connected directly. • Memory size: Up to 8 Gbytes (8-Gbit memory × 8) • Data bus width: 32 bits × 2 or 64 bits × 1 • Auto-refresh/self-refresh/partial array self-refresh supported • Deep-power-down mode supported • Auto precharge mode/bank active mode • DDR back up supported (only 32-bit × 1 backup)
Memory connections	DDR3-SDRAM compliant to JEDEC JESD79-3E Supports from 512-Mbit to 8-Gbit memory unit configurations 32-bit DDR3-1600 (four units with 8-bit width) 32-bit DDR3L-1600 (four units with 8-bit width)

1.3.5 Internal Bus Module

Item	Description
AXI-bus	• On-chip main bus — Bus protocol : AXI3 with QoS control — Frequency: 260 MHz — Bus width: 256 bits/128 bits • On-chip CPU & GPU main bus — Corelink™ CCI-400 Cache Coherent Interconnect - r0p3 — Bus protocol: AMBA4® ACE™ and ACE-Lite™ — Frequency: 520 MHz — Bus width: 128 bits
Direct memory access controller for system (SYS-DMAC)	• 30 channels for ARM domain • Address space: 4 Gbytes on architecture • Data transfer length: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, 32 bytes and 64 bytes • Maximum number of transfer times: 16,777,216 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
Realtime direct memory access controller (RT-DMAC)	• Three channels for the realtime domain • Address space: 4 GBytes on architecture • Data transfer length: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, 32 bytes and 64 bytes • Maximum number of transfer times: 16,777,216 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)

Item	Description	
Direct memory access controller for Audio (Audio-DMAC)	• 26 channels for Audio domain • Address space: 4 Gbytes on architecture • Data transfer length: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, 32 bytes and 64 bytes • Maximum number of transfer times: 16,777,216 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)	
Direct memory access controller (Audio-DMAC-Peripheral-Peripheral)	Audio-DMAC (for transfer from Peripheral to Peripheral) • 29 channels for audio domain • Data transfer length: longword (4 bytes) • Transfer count: Transfer count is not specified (DMA transfer is made from the transfer-start to transfer-stop settings.) • Transfer request: Selectable from on-chip audio peripheral module request • Priority: round-robin mode • Interrupt request: not supports interrupt request to CPU at the end of data transfer	
IPMMU	An IPMMU is a memory management unit (MMU) which provides address translation and access protection functionalities to processing units and interconnect networks.	
Interrupt controller (INTC)	INTC-SYS	— 10 interrupt pins which can detect external interrupts — Fall/rise/high level/low level detection is selectable — On-chip peripheral interrupts: Priority can be specified for each module — Max. 384 shared peripheral interrupts supported — 16 software interrupts that have been generated and 6 private peripheral interrupts supported — 32-level priority selectable — Trust Zone supported
	INTC-RT (interrupt controller for the realtime domain)	— 10 interrupt pins which can detect external interrupts — Fall/rise/high level/low level detection is selectable — On-chip peripheral interrupts: Priority can be specified for each module — Max. 384 peripheral interrupts supported
Multifunctional interface (MFIS)	• Interrupt generation between SYS domain and RT domain • Fifteen external source bits for controlling 32-K types of interrupts • Lock function for exclusive access supported	

1.3.6 Local Memory

Item	Description
INTRAM	• RAM0 of 72 Kbytes • RAM1 of 4 Kbytes
SECRAM	• RAM of 256 Kbytes

1.3.7 Graphics Units

Item	Description	
3D graphics engine (3DGE)	• Imagination Technologies PowerVR SGX544MP2 • Max. Freq. 520 MHz • Most comprehensive IP core family and roadmap in the industry • USSE2 delivers twice the peak floating point and instruction throughput of Series5 USSE • YCbCr and color space accelerators for improved performance • Upgraded PowerVR Series5XT shader-driven tile-based deferred rendering (TBDR) architecture • Support for all industry standard mobile and desktop graphics APIs and operating systems	
Graphics engine basic functions (R-GP2D)	Maximum operating clock frequency	AXI: 260 MHz APB: 65 MHz
	Drawing functions	Four-vertex surface drawing, polygon drawing, line drawing, highly-functional thick line drawing, anti-aliasing, BitBLT with raster operations/α blending, α blended lines
	Coordinate transformation functions	4 × 4 matrix operations + perspective W-division performed
	Color display	8-bit index, RGB565, ARGB1555, ARGB8888
	Screen coordinates	• X direction: 0 to 4095 • Y direction: 0 to 4095
	Register settings	• Current point setting [MOVE/RMOVE] • Local offset setting [LCOFS/RLCOFS] • Specific address mapped register setting [WPR] • Local coordinates conversion offset setting [RGTOFS]
	Sequence control	• Vsync wait [VBKEM] • Jump [JUMP] • Subroutine [GOSUB] (nesting level: 1, 8)
	Anti-aliased fonts	8 bits/pixel color format, anti-aliased font drawing
	Multiple source blending with α map reference values	Supports 8 bits/pixel color format α maps
	Thick line customizing	Borders at which thickness direction is switched can be set [BDS], jaggy reduction [WLM]
	New anti-aliased line	Anti-aliasing for vertical, horizontal and 45-degree oblique lines is possible. [NAA]
	Loop function	Draws a closed figure by connecting the start and end points. [LOOP]

Item	Description	
Display unit (DU)	Display channel	Two independently controllable channels
	Screen size and number of composite planes	• Maximum screen size: 4095 × 2047 • Number of planes specifiable: 8 planes Note that possibility number of combined display depends on DCLK; 1-plane @DCLK > 75 MHz 2-plane @75 MHz ≥ DCLK > 38 MHz 3-plane @38 MHz ≥ DCLK
	CRT scanning method	Non-interlaced, interlaced sync, interlaced sync & video
	Synchronization method	Master, TV sync
	Internal color palette	Includes four color palette planes which can display 256 of 260 thousands colors at the same time.
	Digital RGB	• One output channel • Output on rising and falling edges of the synchronizing signal (resolution for the same display) • 8-bit precision for each RGB color
	Blending ratio settings	Number of color palette planes with blending ratio: 4
	Dot clock	Switchable between external input and internal clock
	Color management	• γ correction, gain correction • Applies correction of color (skin color adjustment and color correction set in memory) in terms of color phase, brightness, and chromaticity for a specified range of colors or for the full range of colors
	Interface	• LVDS output: Four lanes × single channel (two lanes × 2) • RGB888 × 1
	LVDS interface (1ch)	• Output: compliant with TIA/EIA-644; five pairs of differential output (four pairs of data and one pair of clock) • Operating frequency: Dotclk 148.5 MHz • Selectable 8 output formats
De-compression unit (DCU)	• De-compression to row picture data from compressed data by Run-length method • Input data format: Compressed data by Run-Length method (ARGB8888, RGB888, RGB565, RGBA4444, RGBA5551, and A8) • Output data format: Row data (ARGB8888, RGB888, RGB565, RGBA4444, RGBA5551, and A8) • 2 interrupt sources: Conversion finished, and Check sum error • Including DMAC (DCU_DMAC)	
Timing controller (TCON)	Modulate the various timing signal for LCD panel driver with RGB parallel output interface.	

Item	Description	
Video input (VIN)	Input data format	• 8-, 10-, or 12-bit YCbCr422 (CbYCrY format) • 16-bit YCbCr422 (8-bit (Y) + 8-bit (CbCr) format) • 20-bit YCbCr422 (10-bit (Y) + 10-bit (CbCr) format) • 24-bit YCbCr422 (12-bit (Y) + 12-bit (CbCr) format) • 18-bit RGB666 • 24-bit RGB888
	Clipping function	Up to 2048 × 2048
	Horizontal scaling	Uses a 9-tap multi-phase filter. Up to two times, but only scaling down is possible for HD1080i or HD720P data.
	Vertical scaling	Scaling by linear interpolation Up to three times, but only scaling down is possible for HD1080i or HD720P data.
	Output format	RGB-565, ARGB-1555, YCbCr422, RGB888 (for channels 0 and 1), YC separation, and extraction of the Y component
IMR-LX2	• Pixel pipelines internally operate at the 260-MHz clock frequency (pixels are generated and distortion is corrected at one pixel per cycle). • Reads data from the external memory or from the path directly connected to VIN and outputs data in which distortion was corrected to the external memory. • Access to the AXI-Bus is at the 260-MHz clock frequency. • Image data format: 16 bpp (YCbCr422 (Y: 8 bpp, 10 bpp, CbCr: 8 bpp))	

1.3.8 Video Processing

Item	Description
Video signal processor 1 (VSP1)	The VSP1 is the successor IP of Renesas' VIO6-IP series, and has the following features. (1) Supports various data formats and conversion — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying (2) Full HD video processing — Up and down scaling with arbitrary scaling ratio — Super resolution processing — Blending of four picture layers and raster operations (ROPs) (3) Full HD picture quality/color correction with 1D/3D look up table (LUT) — Dynamic γ correction and gain correction — Correction of color (to adjust skin tones or colors in memory) — Hue, brightness, and saturation adjustment — 1D histogram (4) Direct connection to display module — Display unit (DU) supported

Item	Description
Video processing unit (VCP3)	The VCP3 is a multi-codec module which provides encoding and decoding capabilities on the basis of multiple video coding schemes, e.g., H.264/AVC, MPEG-4, MPEG-2 and VC-1. This IP (Intellectual Property) is a multi codec that processes the frame or each field by controlling software for VCP3 executed on host CPU. The VCP3 has the following features: • Support for multiple codecs — H.264/MPEG-4 AVC HP (High Profile) and MVC SHP (Stereo High Profile) encoding and decoding — H.262/MPEG-2 MP (Main Profile) decoding — MPEG-4 ASP (Advanced Simple Profile) decoding — VC-1 SP/MP/AP (Simple, Main, Advanced Profile) decoding — H.263 Baseline decoding — VP8 decoding • Support for HDTV resolutions — 1920 pixels × 1080 lines × 60 frames/second × single channel — Maximum performance will change with securable bus bandwidth. • Data handling on a picture-by-picture basis — Encodes/decodes data one picture (frame or field) at a time. • High picture quality — Supports the H.264 high-efficiency coding tools (CABAC, 8 × 8 frequency conversion, and quantization matrix). — High-efficiency motion vector detection by a combination of discrete search and trace search — Highly efficient real-time intra-prediction by Prediction from Original Image (POI) — Optimal-mode selection by Rate-Distortion (RD) cost evaluation — Picture quality control based on activity analysis results which match visual models • Low power dissipation — Dynamically disables the clocks for the entire VCP3. — Dynamically disables the clocks for individual submodules. • Includes its own dedicated 64-KByte cache Use the middleware from Renesas to handle VCP3 functions if these are required.
Fine display processor 1 (FDP1)	The FDP1 is the de-interlacing module which converts the interlaced video to progressive video, and has the following features. (1) Supports various data formats — Input: YCbCr444/422/420 — Output: YCbCr444/422/420 and RGB/αRGB (2) Full HD video processing performance (3) High image quality de-interlacing algorithm — Motion adaptive de-interlacing — Accurate still detection — Diagonal line interpolation (DLI)

Item	Description
Image extraction direct memory access controller (2D-DMAC)	• Supports conversion between various RGB formats. • Image extraction function: Capable of extracting an image and storing it as a separate image in the RAM. • Image rotation/reversal function: Reverses an image vertically/horizontally or rotates it by 90°/270°. • Simple scaling function: Capable of scaling an image two times in the X or Y direction. • Format conversion • Supports conversion from RGB to RGB and from YCbCr to YCbCr.
JPEG processing unit (JPU)	The JPU is an IP module that encodes and decodes the JPEG image. • Conforming specification: JPEG baseline • Operating precision: Conforming to JPEG Part 2, ISO-IEC10918-2 • Color format: YCbCr 4:2:2 or YCbCr 4:2:0 • Quantization tables: Four tables • Huffman tables: Four tables (two AC tables and two DC tables) • Target markers: Start of image (SOI), start of frame type 0 (SOF0), start of scan (SOS), define quantization tables (DQT), define Huffman tables (DHT), define restart interval (DRI), restart (RSTm), and end of image (EOI) • Image data rate: Maximum 260 Mbytes/sec (at 130-MHz operation) • Image rotation (by 90°, 180°, or 270°) can be performed in the encoding process. • Processable image size: — Maximum 8000 (horizontal) × 8000 (vertical) pixels, — Minimum 16 (horizontal) × 16 (vertical) pixels — Image is processed in 4-pixel units.
Stream processor 1 (SSP1) (optional)	• TS/PS input interface • Single serial input • MULTI2/DVB-CSA/DES/3-DES/AES128 descrambler included • System time clock correction • Bit rate: Up to 66 Mbps • Use the middleware from Renesas to handle SSP1 functions if these are required.

1.3.9 Sound Interface

Item	Description
Audio DSP (ADSP)	• On-chip Audio-DSP (Dual MACs can operate as 32 × 16-bit / 24 × 24-bit) • 32-bit RISC architecture with 7-stage pipeline • 24-bit audio processing instructions • Dual-issue, static super-scalar VLIW • I-cache: 16 Kbytes, D-cache: 64 Kbytes

Item	Description	
Sampling rate converter unit (SCU)	Overall specification	• Includes ten SRC modules — Supports the quality suitable for audio sound (THD+N -132dB): six modules — Supports the quality suitable for voice sound (THD+N -96dB): four modules • The SRC module is capable of correcting phase change and delay (timing jitter) generated during data transfer over external memories or external devices. • The channel count conversion unit (CTU), mixer (MIX), and digital mute and volume function (DVC) can be used on two fixed output channels.
	Sampling rate conversion (SRC)	• Capable of asynchronous sampling rate conversion • Supports resolutions up to 24 bits • Two kinds of filter type for SRC. — Supports the quality suitable for audio sound (THD+N -132dB): Realized the filter by passband -1dB@0.4575FS, cutoff -18dB@0.5FS. — Supports the quality suitable for voice sound (THD+N -96dB): Realized the filter by passband -1dB@0.4561FS, cutoff -72dB@0.5FS (Characteristics of each filter is written in the equivalent/up-sampling cases). • Automatically generates antialiasing filter coefficients • For monaural to eight-channel sound sources
	Channel count conversion unit (CTU)	• Downmixing and splitter functions — Conversion of eight input channels into four output channels — Conversion of six input channels into two output channels — Conversion of two input channels into four sets of two output channels — Conversion of one input channel into eight sets of one output channel — No conversion
	Mixer (MIX)	• Mixing (adds) two to four sources into one • Ratio for adding sources is selectable • Ratio is dynamically changeable • Mixing with volume ramp is available (ramp period is selectable)
	Digital volume and mute function (DVC)	• Volume control function including digital volume, volume ramp, and zero-crossing mute • The digital volume function is specified by a 24-bit fixed-point value within the range from 0 to 8 times (mute, or -120 to 18 dB) • The volume ramp function can be used for soft mute, fade-in, fade-out, or desired volume adjustment • The volume ramp period can be changed within the sampling range from the 0th to 23rd power of 2 • The zero-crossing mute function silences the sound at the zero-crossing point of the audio data

Item	Description	
Serial sound interface unit (SSIU)	Overall specification	• Includes ten SSI modules functioning as interfaces with external devices. — Supports short and long formats — Supports TDM format (six modules of ten modules can be used for this function) • Up to four independent stereo sound sources in a TDM format can be distributed to each course within SoC. Up to four independent stereo sound sources in SoC can be combined output in TDM format.
	Serial sound interface (SSI)	• Operating mode: non-compressed mode (Not support compressed mode) • Supports versatile serial audio formats (I2S/left justified/right justified) • Supports master/slave functions • Programmable word clock, bit clock generation functions • Multichannel format functions (up to four channels) • Supports 8-/16-/18-/20-/22-/24-/32-bit data formats • Supports TDM mode • Supports WS continue mode • The DMA controller or interrupts control the transfer of data to and from the SSI module. • Supports short and long frames for monaural data (valid data lengths are 8 and 16 bits) • Up to nine independent clock signals can be input.
MediaLB+ (MLP)	MOST interface	• Media Local Bus (MediaLB) — MediaLB 6-pin/3-pin interface (Not support MediaLB 5-pin interface) — Up to 300-Mbps data transfer rate is supported. • Synchronous transfer • Asynchronous transfer • Isochronous transfer • Control transfer • 6-pin interface and 3-pin interface do not operate simultaneously.
MLP local memory (MLM)	Buffer memory for MLP	
Digital transmission content protection (DTCP) (optional)	• Authentication and Key Exchange (AKE) and protection of contents are possible. • Two lines are simultaneously possible. • Support MOST DTCP	
Audio clock generator (ADG)	Selection or division of audio clock signals	

1.3.10 Storage

Item	Description
USB2.0 host & function module (USB2.0)	• Two channels (Host only 1 channel/Host-Function 1 channel selected)* • PHY integrated • USB Host (EHCI/OHCI) 2LINK • Compliance with USB2.0 • USB Function 1LINK • Compliance with USB2.0 (High-Speed) • Interrupt request • Internal dedicated DMA Note: * A USB2.0 PHY is used as USB3.0 host HS/FS. USB2.0: Two channels (HS/FS/LS) / USB2.0 + USB3.0: Single channel (SS/HS/FS)
USB 3.0 host module (USB3.0)	• USB 3.0 host 1 ch* • Supports SS/HS/FS/LS. xHCI • Not support FUNCTION and OTG Note: * A USB2.0 PHY is used as USB3.0 HOST HS/FS. USB2.0: Two channels (HS/FS/LS) / USB2.0 + USB3.0: Single channel (SS/HS/FS)
Serial-ATA	• Serial ATA Standard Rev.3.1 supported • 3.0-Gbps (Gen2) transfer rate supported — Single-channel PHY for USB3.0 and SATA (channel 0) — Single-channel PHY for PCIEC and SATA (channel 1)
SD host interface (SDHI)	• Three channels — Interface 0: Support SDR104 class transfer rate at max. 97.5 Mbytes/s@ 195 MHz, and SDXC. Does not support CPRM. — Interfaces 1 and 2: Support CPRM, SDR50 class transfer rate at max. 48 Mbytes/s@ 97.5 MHz, and SDXC. • Supports SD memory/SDIO interface (1-/4-bit SD buses). • Error check function: CRC7 (command/response), CRC16 (data) • Card detection function • Supports write protection • SD-binding function — Compliant with Content Protection for Recordable Media Specification in revision 0.92 of the SD-Binding Part of the SD Memory Card Book • SD-SD content protection — Compliant with Content Protection for Recordable Media Specification in revision 0.92 of the SD-SD part of the SD Memory Card Book
Multi-media card interface (MMCIF)	• Single channel • MMC 4.41 base • eMMC controllable • Data bus: 1/4/8-bit MMC mode (not support SPI mode) • Support block transfer (not support stream transfer) • Block size in multi-block transfer: 512 bytes

1.3.11 Network

Item	Description
CAN interface (CAN)	• Two channels • Supports CAN specification 2.0B • ISO-11898-1 compliant • Maximum bit rate: 1 Mbps • Message box — Normal mode: 32 receive-only mailboxes and 32 mailboxes for transmission/reception — FIFO mode: 32 receive-only mailboxes and 24 mailboxes for transmission/reception, 4-stage FIFO for transmission, and 4-stage FIFO for reception • Reception — Data frame and remote frame can be received. — Selectable receiving ID format — Selectable overwrite mode (message overwritten) or overrun mode (message discarded) • Acceptance filter — Mask can be enabled or disabled for each mailbox. • Transmission — Data frame and remote frame can be transmitted. — Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) — Selectable ID priority mode or mailbox number priority mode • Sleep mode for reducing power consumption
IE-BUS	• IEBus protocol control (layer 2) • Half-duplex asynchronous communication • Multi-master method • Broadcast communication function • Two modes with different transfer rates available — Mode 0: Approximately 4.1 kbps (at 6.29-MHz operation), maximum transfer of 16 Bytes/frame — Mode 1: Approximately 18 kbps (at 6.29-MHz operation), maximum transfer of 32 Bytes/frame • 32-Byte built-in data transmit and receive buffers • Continuous transmission and reception up to 32 Bytes, or the maximum number of Bytes to be transferred of mode 1. • External driver/receiver • IEBus clock: 6.29-MHz Note: IEBus is a trademark of Renesas Electronics Corp.
PCI-Express Controller (PCIEC)	• PCI Express Base Specification Revision 2.0 • Single channel • PHY integrated
Ethernet AVB	• Supports IEEE802.1BA, IEEE802.1AS, IEEE802.1Qav and IEEE1722 functions • Supports transfer at 1000 Mbps and 100 Mbps • Magic packet detection • Supports Reception Filtering to separate streaming frames from different sources • Supports interface conforming to IEEE802.3 PHY GMII (Gigabit Media Independent Interface) and MII (Media Independent Interface)

Item	Description
Ethernet MAC	• IEEE802.3u MAC (Ether) function • Supports transfer at 10 and 100 Mbps • Flow control conforming to IEEE802.3x or back pressure system • Supports interface conforming to IEEE802.3u • Magic packet detection • Includes DMAC • Supports RMII (Reduced Media Independent Interface)

1.3.12 Timer

Item	Description
Watchdog timer (RWDT)	• Internal 16-bit watchdog timer operated by RCLK • Programmable overflow time-period: more than 1 hour count capable
Secure WDT (optional)	• Internal 16-bit watchdog timer • Programmable overflow time period: maximum 1[h]: initial counter value 180[s]
Timer pulse unit (TPU)	• 4-channels • 16-bit timers • Each channel outputs PWM
Compare match timer 0 (CMT0)	• 32-bit timer, two channels (16 bits/32 bits can be selected) • Source clock: RCLK clock • Compare match function provided • Interrupt requests
Compare match timer 1 (CMT1)	• 48-bit timer, eight channels (16 bits/32 bits/48 bits can be selected) • Source clock: RCLK/system clock • Compare match function provided • Interrupt requests
Secure timer (optional)	• 32-bit timer, single channel (16 bits/32 bits can be selected) • Compare match function provided • Interrupt requests
Secure up-time clock (optional)	• Internal 32-bit timer • Programmable overflow time period: maximum 24 hours
Timer unit (TMU)	• 4 sets of 3-channel 32-bit timer • Auto-reload type 32-bit down counter • Internal prescaler • Interrupt request • Two channels for input capture

1.3.13 Peripheral Module

Item	Description
Crypto engine (optional)	• Single channel • PKA engine (Diffie-Hellman, RSA) • Hash engine (SHA1, SHA-256, MD5) • Bulk encryption engine (DES, 3DES, AES) • Internal RAM for crypto engine
I2C bus interface (IIC)	• Single channel for DVFS (open drain type IO buffer) • Two channels for general purpose • Supports single master transmission/reception • Interrupt request • DMAC request
Multi-master I2C bus interface (I2C)	• Five channels for 3.3-V LVTTL buffers and single channel for GPS external device (Open drain type IO buffer) • Philips I2C bus interface method supported • Master/slave functions • Multi-master functions • Transfer rate up to 400 kbps supported • Programmable clock generation from the system clock
Serial communication interface with FIFO (SCIFA)	• Six channels • Internal 64-byte transmit/receive FIFOs • High-speed UART • Internal prescaler • Clock synchronous serial communications possible • Support edge selection function • Interrupt request, DMAC request and DMA multi-Byte transfer supported • Asynchronous mode (modem control is enabled) • Clock synchronous mode
Serial communication interface with FIFO (SCIFB)	• Three channels • Internal 256-byte transmit/receive FIFOs • High-speed UART • Internal prescaler • Clock synchronous serial communications possible • Support edge selection function • Interrupt request, DMAC request and DMA multi-Byte transfer supported • Asynchronous mode (modem control is enabled) • Clock synchronous mode

Item	Description	
Serial communication interface with FIFO (SCIF)	Overall specification	• Six channels • Asynchronous, clock-synchronized modes • Asynchronous serial communication mode The SCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). There is a choice of eight serial data transfer formats. — Data length: 7 bits or 8 bits — Stop bits: 1 bit or 2 bits — Parity: Even/odd/none — Receive error detection: Parity, framing, and overrun errors — Break detection: A break is detected when a framing error lasts for more than 1 frame length at space 0 (low level). When a framing error occurs, a break can also be detected by reading the RX pin level directly from the serial port register (SCSPTR). • Clock synchronous serial communication mode The SCIF performs serial data communication synchronized with a clock. This feature enables serial data communication with other LSIs that support synchronous communication. There is a single serial data communication format for clock synchronous serial communication. — Data length: 8 bits — Receive error detection: Overrun errors • Full-duplex communication capability The SCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 16-stage FIFO buffer structure, enabling continuous serial data transmission and reception. • On-chip baud rate generator, enabling any bit rate to be selected The SCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock. • Eight interrupt sources The SCIF has eight types of interrupt sources: receive-data-ready, receive-FIFO-data-full, break, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out and enables any of them to be requested independently. • DMA data transfer When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • In asynchronous mode, a receive data ready (DR) or a timeout error (TO) can be detected during reception.

Item	Description
Clock-synchronized serial interface with FIFO (MSIOF)	• Three channels • Max. speed: 26 Mbps • Internal 64-byte transmit FIFOs/internal 256-byte receive FIFOs • Supports master and slave modes • Internal prescaler • Supports serial formats: IIS, SPI (master and slave modes) • Interrupt request, DMAC request
QSPI	• Single/Dual/Quad-SPI: serial slave transfer enabled • Supports master mode • SPICLK clock rate: 1 to 4080 in master mode; Max. 78 MHz
High-speed serial communication interface with FIFO (HSCIF)	• Three channels • Asynchronous serial communication mode • Capable of full-duplex communication • On-chip baud rate generator, enabling any bit rate to be selected • Eight interrupt sources • DMA data transfer • Modem control functions (HRTS and HCTS) are stored. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • A receive data ready (DR) or a timeout error (TO) can be detected during reception.
PWM timer (PWM)	• Seven channels • High-level width (10 bits) of PWM output can be set. • High-level periods (10 bits) of PWM can be set. • Periods in the range from two to 2^{24} × 1024 cycles of the Pϕ clock can be set. • Continuous pulse or single pulse output selectable
Gyro ADC I/F	• Controls the interface with a 12-bit or 16-bit A/D converter for gyroscopic sensors. • Applies parallel conversion to the serial data input from the A/D converter and stores the converted data in registers. • Connectable device (switchable by setting the mode select register) • MB88101A (FUJITSU), ADCS7476(TI), AD7476 (Analog Devices), or MAX1162 (Maxim) • Realtime data or 100-ms data (data added every 10 ms ten times) can be selected.
Speed-pulse I/F	• 16-bit speed pulse counter • Internal noise filter (low-pass filter) removes chattering and bounce from speed pulses. • The pulse width to be filtered out by the noise filter is selectable by the user. Passing all pulses without filtering can also be selected. • Two types of pulse count register are provided: one for indicating the count in realtime and another for latching the count every 100 ms. • Five types of pulse width measurement registers are provided: two for the elapsed time, one for the pulse width, and two for the observation period. • Counts are incremented in synchronization with the rising edge of the speed pulse.
TSIF	• Single channel • Serial data input • Support for TS data transfer by DMA auto request • Acquisition of TS packets Filters 67 kinds of PIDs (Packet ID) in total (The PID values of PAT and CAT packets are fixed. For PCR, video, and audio packets, the PID values are predefined).

Item	Description
IR Receiver (IR)	• Auto detection of a reader • Built-in circuit for synchronization protection (noise malfunction prevention) during the detection of a reader • Up to 64 bits of a code are receivable per frame. • Capable of receiving a maximum of two frames of code
FM multiplex demodulator (DARC) (optional)	Functions for receiving FM multiplex broadcasting data in the DARC format Clock: 8.192 MHz ± 200 ppm (VICS) Features: • Automatic error correction achieved by using on-chip frame memory • Continuous reading of one-frame data possible during 250 ms after the second horizontal correction interrupt • On-chip descrambler for VICS • Two reception channels (main and sub channels) provided • Fully automated simultaneous reception of two channels. — Two packets of data receivable at a time — During simultaneous data reception, control other than tuner selection (notification by an interrupt) and reading of received data (interrupt) is unnecessary. • Number of synchronization protection steps settable • On-chip error correction circuit • On-chip CRC check circuit for hierarchies 4 and 2 • Compatible with the international standard frame formats A, B, and C • Reception interrupt function after the first horizontal error correction according to the specified SI (service identification) • Timing interrupts that occur in synchronization with frames: two channels

Item	Description	
GPS (optional)	GPS reception performance	• Received channels: Multiple (maximum 16 satellites) • Received frequency: 1575.42 MHz (GPS/Galileo L1 signal) • Sensitivity of reception (GPS) — Acquisition level: -148 dBm — Tracking level: -163 dBm
	GPS positioning performance	• Positioning method: All-in-view positioning • Positioning interval: 1 Hz • Positioning accuracy [Conditions: open sky, stationary state] GPS/Galileo common positioning — Position: 4 m 2drms (target) Single-GPS positioning — Position: 10 m 2drms (SA off, HDOP ≤ 1.5) — Speed: 0.04 m/s. rms (SA off, HDOP ≤ 1.5) — Direction: 0.35 degree or less (SA off, 60 km/h speed, HDOP ≤ 1.5) • TTFF (Time to First Fix) [Conditions: open sky, stationary state] — Hot start: 2 seconds (typ.); ephemeris provided, latest almanac — Warm start: 32 seconds (typ.), 3 seconds (min., target); ephemeris not provided, latest almanac — Cold start: 35 seconds (typ.); ephemeris not provided, almanac not provided • Re-acquisition time [Conditions: open sky, stationary state, for interruptions of 5 seconds or less]: 3 seconds (typ.) • Positioning limits — Longitude and latitude: Global — Height: -100 m to 6000 m — Speed: 300 km/h or less (200 km/h or less for recovery from interruptions) — Acceleration: Less than 9.8 m/s^2 — Support for rollover: Depends on the week number at which product implementation starts (the valid period is until 1023 weeks after that week). Notes: 1. The above-mentioned performance is only guaranteed when the specified RF-IC (i.e. the recommended circuit) is in use. 2. The hardware already supports Galileo and quasi-zenith satellites; for use with GPS in the future, the program on the host side will require modifications.
	GLONASS function	
Boot Function (BOOT)	• System startup with selectable boot mode at power-on reset • Program downloaded to internal memory (LRAM) • Autorun function for the downloaded program	

1.3.14 Special Edition Modules (Restricted)

Item	Description
SIMcard (optional)	• ISO/IEC7816-3 (Identification Card) supported • Asynchronous half-duplex character transmission protocol • Data length of 8 bits • Bitrate can be selected: the clock generated by the internal baud rate generator. • Generates and checks a parity bit • Four interrupt sources Notice: Use the middleware from Renesas to handle SIMcard interfaces if these are required.

1.3.15 Others

Item	Description
JTAG	JTAG interface for CoreSight, SH-4A and DSP
Process	28-nm Si-CMOS
Package	FC-BGA2727-831

1.4 Power Supply Voltages and Temperature Range

- Power supply voltage (typ.)
  1.8 V: (ETM, SD, MMC, SATA, PCI Express, USB3.0, LVCMOS I/F, Xtal, JTAG, Trace and RST)
  1.03 V: (core)
  1.5 V: (DDR3-I/O SSTL mode: DDR3)
  1.35V: (DDR3-I/O SSTL mode: DDR3L)
  3.3 V: (Others)

- Temperature range
  Tc = –40°C to +105°C
  Ta = –40°C to +85°C

2. Area Map

See section 2, Area Map in the R-Car Series, 2nd Generation User's Manual: Hardware.

3. Pin Assignment

Non disclosure agreement (NDA) is required for documentation.

Please contact a Renesas Electronics sales representative.

4. Pin Multiplexing

Non disclosure agreement (NDA) is required for documentation.

Please contact a Renesas Electronics sales representative.

5. Pin Function Controller (PFC)

5.1 Overview

The pin function controller (PFC) is a module that consists of registers for selecting the function of the multiplexed pins and controlling the pull-up resistor on each LSI pin.

5.1.1 Features

- Register access through the APB bus interface
- Setting multiplexed pin functions for LSI pins

  Function of the R-Car M2-W pin selectable by setting the registers in the PFC module

  (The function of the LSI pin can be selected by the GPIO/peripheral function select registers 0 to 7 (GPSR0 to GPSR7) and peripheral function select registers 0 to 16 (IPSR0 to IPSR16) in the PFC module. For details, see sections 5.3.2, GPIO/Peripheral Function Select Register 0 (GPSR0) through 5.3.26, Peripheral Function Select Register 16 (IPSR16).)
- Module selection

  Enable and disable the functions of R-Car M2-W LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module.

  (Selection is handled by the module select register (MOD_SEL), module select register 2 (MOD_SEL2), module select register 3 (MOD_SEL3) and module register4 (MOD_SEL4). For details, see sections 5.3.27, Module Select Register (MOD_SEL), through 5.3.30, Module Select Register 4 (MOD_SEL4).
- Pull-up control for each LSI pin.

  On/off of the pull-up or pull-down resistors on each LSI pin can be controlled by setting the registers in the PFC module.

  (The pull-up or pull-down resistors on each LSI pin can be turned on or off individually by setting the LSI pin pull-up/down control registers 0 to 7 (PUPR0 to PUPR7) in the PFC module. For details, see sections 5.3.31, LSI Pin Pull-Up Control Register 0 (PUPR0) through 5.3.38, LSI Pin Pull-Up Control Register 7 (PUPR7).)
- Control of IO functions, including SSP1, SDHI, IRQ, DU, Ethernet, ADG, SSI and LBSC.

  SDIO functions, including the driving ability, POC of pins, can be controlled by setting registers of the PFC module. For details, see sections 5.3.39, SD Control Register 0 (IOCTRL0) through 5.3.44, IIC3 (DVFS) and TDBG IO Cell Control Register (IOCTRL7).

  DDR3 GPIO function can also be selected by setting registers of the PFC. For details, see sections 5.3.45, DDR3 General Port IO Enable Register (DDR3GPEN) through 5.3.48, DDR3 General Port Input Data Register (DDR3GPID).

5.2 Register Configuration

All the registers in the PFC are mapped into the APB bus space. Table 5.1 shows the configuration of the registers provided in the PFC. For details on the registers of the PFC, see section 5.3, Register Description.

Table 5.1 Configuration of Registers in PFC

Name	Abbr.	R/W	Initial Value	Address	Access Size	Condition
LSI multiplexed pin setting mask register	PMMR	R/W	H'0000 0000	H'E606 0000	32	—
GPIO/peripheral function select register 0	GPSR0	R/W	H'FFFF FFFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)	H'E606 0004	32	—
GPIO/peripheral function select register 1	GPSR1	R/W	H'00EC 0FFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000), or H'00EC 0FFF (in power-on reset)	H'E606 0008	32	—
GPIO/peripheral function select register 2	GPSR2	R/W	H'0000 0000	H'E606 000C	32	—
GPIO/peripheral function select register 3	GPSR3	R/W	H'0000 0000	H'E606 0010	32	—
GPIO/peripheral function select register 4	GPSR4	R/W	H'0000 0000	H'E606 0014	32	—
GPIO/peripheral function select register 5	GPSR5	R/W	H'0000 0000	H'E606 0018	32	—
GPIO/peripheral function select register 6	GPSR6	R/W	H'4000 0000	H'E606 001C	32	—
GPIO/peripheral function select register 7	GPSR7	R/W	H'0380 0000	H'E606 0074	32	—
Peripheral function select register 0	IPSR0	R/W	H'0000 0000	H'E606 0020	32	—
Peripheral function select register 1	IPSR1	R/W	H'0000 0000	H'E606 0024	32	—
Peripheral function select register 2	IPSR2	R/W	H'0000 0000	H'E606 0028	32	—
Peripheral function select register 3	IPSR3	R/W	H'0000 0000	H'E606 002C	32	—
Peripheral function select register 4	IPSR4	R/W	H'0000 0000	H'E606 0030	32	—
Peripheral function select register 5	IPSR5	R/W	H'0000 0000	H'E606 0034	32	—
Peripheral function select register 6	IPSR6	R/W	H'0000 0000	H'E606 0038	32	—
Peripheral function select register 7	IPSR7	R/W	H'0000 0000	H'E606 003C	32	—

Name	Abbr.	R/W	Initial Value	Address	Access Size	Condition
Peripheral function select register 8	IPSR8	R/W	H'0000 0000	H'E606 0040	32	—
Peripheral function select register 9	IPSR9	R/W	H'0000 0000	H'E606 0044	32	—
Peripheral function select register 10	IPSR10	R/W	H'0000 0000	H'E606 0048	32	—
Peripheral function select register 11	IPSR11	R/W	H'0000 0000	H'E606 004C	32	—
Peripheral function select register 12	IPSR12	R/W	H'0000 0000	H'E606 0050	32	—
Peripheral function select register 13	IPSR13	R/W	H'0000 0000	H'E606 0054	32	—
Peripheral function select register 14	IPSR14	R/W	H'0000 0000	H'E606 0058	32	—
Peripheral function select register 15	IPSR15	R/W	H'0000 0000	H'E606 005C	32	—
Peripheral function select register 16	IPSR16	R/W	H'0000 0000	H'E606 0160	32	—
Module select register	MOD_SEL	R/W	H'0000 0000	H'E606 0090	32	—
Module select register 2	MOD_SEL2	R/W	H'0000 0000	H'E606 0094	32	—
Module select register 3	MOD_SEL3	R/W	H'0000 0000	H'E606 0098	32	—
Module select register 4	MOD_SEL4	R/W	H'0000 0000	H'E606 009C	32	—
LSI pin pull-up control register 0	PUPR0	R/W	H'D87F FFFF	H'E606 0100	32	—
LSI pin pull-up control register 1	PUPR1	R/W	H'EC8B7DC6	H'E606 0104	32	—
LSI pin pull-up control register 2	PUPR2	R/W	H'DE61 F3FF	H'E606 0108	32	—
LSI pin pull-up control register 3	PUPR3	R/W	H'DFFF FFFF	H'E606 010C	32	—
LSI pin pull-up control register 4	PUPR4	R/W	H'FFFF FF27	H'E606 0110	32	—
LSI pin pull-up control register 5	PUPR5	R/W	H'FFFF FFE1	H'E606 0114	32	—
LSI pin pull-up control register 6	PUPR6	R/W	H'F000 000F	H'E606 0118	32	—
LSI pin pull-up control register 7	PUPR7	R/W	H'015C 0FF3	H'E606 011C	32	—
SD control register 0	IOCTRL0	R/W	H'8000 FFFF	H'E606 0060	32	—
SD control register 1	IOCTRL1	R/W	H'FFFF FFFF	H'E606 0064	32	—
TDSEL control register 4	IOCTRL4	R/W	H'0000 0000	H'E606 0084	32	—
TDSEL control register 5	IOCTRL5	R/W	H'0000 0000	H'E606 0088	32	—
POC control register	IOCTRL6	R/W	H'FFFF FFFF	H'E606 008C	32	—
IIC3 (DVFS) and TDBG IO cell control register	IOCTRL7	R/W	H'0000 0000	H'E606 0070	32	—
DDR3 general port io enable register	DDR3GPEN	R/W	H'0000_0000	H'E606 0240	32	—
DDR3 general port output enable register	DDR3GPOE	R/W	H'0000_0000	H'E606 0244	32	—

Name	Abbr.	R/W	Initial Value	Address	Access Size	Condition
DDR3 general port output data register	DDR3GPOD	R/W	H'0000_0000	H'E606 0248	32	—
DDR3 general port input data register	DDR3GPID	R	H'XXXX_XXX0	H'E606 024C	32	—

5.3 Register Description

[Legend]

Initial value:	Register value after a reset
:	Undefined value
R/W:	Readable/writable. The written value can be read.
R:	Read-only. The write value should always be 0.
R/WC0:	Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.
R/WC1:	Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.
W:	Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.
—/W:	Write-only. The read value is undefined.

All the bits are active high unless otherwise specified, and deactivated on reset.

All access to registers is made in longword units.

The write value to a reserved bit should always be 0.

5.3.1 LSI Multiplexed Pin Setting Mask Register (PMMR)

Function: PMMR enables/disables writing to the multiplexed pin setting registers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PMPM															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PMPM															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PMPM[31:0]	H'0000 0000	R/W	Multiplexed Pin Setting Mask Writing a value to any register from among the GPIO/peripheral function select registers GPSR0 to GPSR7, peripheral function select registers IPSR0 to IPSR16, module select registers MOD_SEL, MOD_SEL2, MOD_SEL3 and MOD_SEL4, IO cell control registers IOCTRL0, IOCTRL1 and IOCTRL4 to IOCTRL7 is enabled by writing the inverse of the value to this register.

Note: This register must be set before setting each of the GPIO/peripheral function select registers GPSR0 to GPSR7, peripheral function select registers IPSR0 to IPSR16, module select registers MOD_SEL, MOD_SEL2, MOD_SEL3 and MOD_SEL4, IO cell control registers IOCTRL0, IOCTRL1 and IOCTRL4 to IOCTRL7.

5.3.2 GPIO/Peripheral Function Select Register 0 (GPSR0)

Function: GPSR0 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP0 [31]	GP0 [30]	GP0 [29]	GP0 [28]	GP0 [27]	GP0 [26]	GP0 [25]	GP0 [24]	GP0 [23]	GP0 [22]	GP0 [21]	GP0 [20]	GP0 [19]	GP0 [18]	GP0 [17]	GP0 [16]
Initial value:	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP0 [15]	GP0 [14]	GP0 [13]	GP0 [12]	GP0 [11]	GP0 [10]	GP0 [9]	GP0 [8]	GP0 [7]	GP0 [6]	GP0 [5]	GP0 [4]	GP0 [3]	GP0 [2]	GP0 [1]	GP0 [0]
Initial value:	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP0[31:0]	H'FFFF FFFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000 or power-on reset)	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP0[0]	GP-0-0	Peripheral function selected by IP0[0]
GP0[1]	GP-0-1	Peripheral function selected by IP0[1]
GP0[2]	GP-0-2	Peripheral function selected by IP0[2]
GP0[3]	GP-0-3	Peripheral function selected by IP0[3]
GP0[4]	GP-0-4	Peripheral function selected by IP0[4]
GP0[5]	GP-0-5	Peripheral function selected by IP0[5]
GP0[6]	GP-0-6	Peripheral function selected by IP0[6]
GP0[7]	GP-0-7	Peripheral function selected by IP0[7]
GP0[8]	GP-0-8	Peripheral function selected by IP0[8]
GP0[9]	GP-0-9	Peripheral function selected by IP0[9]
GP0[10]	GP-0-10	Peripheral function selected by IP0[10]
GP0[11]	GP-0-11	Peripheral function selected by IP0[11]
GP0[12]	GP-0-12	Peripheral function selected by IP0[12]
GP0[13]	GP-0-13	Peripheral function selected by IP0[13]
GP0[14]	GP-0-14	Peripheral function selected by IP0[14]
GP0[15]	GP-0-15	Peripheral function selected by IP0[15]
GP0[16]	GP-0-16	Peripheral function selected by IP0[18:16]
GP0[17]	GP-0-17	Peripheral function selected by IP0[20:19]
GP0[18]	GP-0-18	Peripheral function selected by IP0[22:21]
GP0[19]	GP-0-19	Peripheral function selected by IP0[24:23]
GP0[20]	GP-0-20	Peripheral function selected by IP0[26:25]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP0[21]	GP-0-21	Peripheral function selected by IP0[28:27]
GP0[22]	GP-0-22	Peripheral function selected by IP0[30:29]
GP0[23]	GP-0-23	Peripheral function selected by IP1[1:0]
GP0[24]	GP-0-24	Peripheral function selected by IP1[3:2]
GP0[25]	GP-0-25	Peripheral function selected by IP1[5:4]
GP0[26]	GP-0-26	Peripheral function selected by IP1[7:6]
GP0[27]	GP-0-27	Peripheral function selected by IP1[10:8]
GP0[28]	GP-0-28	Peripheral function selected by IP1[13:11]
GP0[29]	GP-0-29	Peripheral function selected by IP1[16:14]
GP0[30]	GP-0-30	Peripheral function selected by IP1[19:17]
GP0[31]	GP-0-31	Peripheral function selected by IP1[22:20]

5.3.3 GPIO/Peripheral Function Select Register 1 (GPSR1)

Function: GPSR1 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP1 [31]	GP1 [30]	GP1 [29]	GP1 [28]	GP1 [27]	GP1 [26]	GP1 [25]	GP1 [24]	GP1 [23]	GP1 [22]	GP1 [21]	GP1 [20]	GP1 [19]	GP1 [18]	GP1 [17]	GP1 [16]
Initial value:	0	0	0	0	0	0	0	0	1/0	1/0	1/0	0	1/0	1/0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP1 [15]	GP1 [14]	GP1 [13]	GP1 [12]	GP1 [11]	GP1 [10]	GP1 [9]	GP1 [8]	GP1 [7]	GP1 [6]	GP1 [5]	GP1 [4]	GP1 [3]	GP1 [2]	GP1 [1]	GP1 [0]
Initial value:	0	0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP1[31:0]	H'00EC 0FFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000), or H'00EC 0FFF (in power-on reset)	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP1[0]	GP-1-0	Peripheral function selected by IP1[25:23]
GP1[1]	GP-1-1	Peripheral function selected by IP1[28:26]
GP1[2]	GP-1-2	Peripheral function selected by IP1[31:29]
GP1[3]	GP-1-3	Peripheral function selected by IP2[2:0]
GP1[4]	GP-1-4	Peripheral function selected by IP2[4:3]
GP1[5]	GP-1-5	Peripheral function selected by IP2[6:5]
GP1[6]	GP-1-6	Peripheral function selected by IP2[9:7]
GP1[7]	GP-1-7	Peripheral function selected by IP2[12:10]
GP1[8]	GP-1-8	Peripheral function selected by IP2[15:13]
GP1[9]	GP-1-9	Peripheral function selected by IP2[18:16]
GP1[10]	GP-1-10	Peripheral function selected by IP2[20:19]
GP1[11]	GP-1-11	Peripheral function selected by IP2[22:21]
GP1[12]	GP-1-12	EX_CS0#
GP1[13]	GP-1-13	Peripheral function selected by IP2[24:23]
GP1[14]	GP-1-14	Peripheral function selected by IP2[26:25]
GP1[15]	GP-1-15	Peripheral function selected by IP2[29:27]
GP1[16]	GP-1-16	Peripheral function selected by IP3[2:0]
GP1[17]	GP-1-17	Peripheral function selected by IP3[5:3]
GP1[18]	GP-1-18	Peripheral function selected by IP3[8:6]
GP1[19]	GP-1-19	RD#
GP1[20]	GP-1-20	Peripheral function selected by IP3[11:9]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP1[21]	GP-1-21	Peripheral function selected by IP3[13:12]
GP1[22]	GP-1-22	Peripheral function selected by IP3[15:14]
GP1[23]	GP-1-23	Peripheral function selected by IP3[17:16]
GP1[24]	GP-1-24	Peripheral function selected by IP3[19:18]
GP1[25]	GP-1-25	Peripheral function selected by IP3[21:20]
GP1[26]	—	—
GP1[27]	—	—
GP1[28]	—	—
GP1[29]	—	—
GP1[30]	—	—
GP1[31]	—	—

5.3.4 GPIO/Peripheral Function Select Register 2 (GPSR2)

Function: GPSR2 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP2 [31]	GP2 [30]	GP2 [29]	GP2 [28]	GP2 [27]	GP2 [26]	GP2 [25]	GP2 [24]	GP2 [23]	GP2 [22]	GP2 [21]	GP2 [20]	GP2 [19]	GP2 [18]	GP2 [17]	GP2 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP2 [15]	GP2 [14]	GP2 [13]	GP2 [12]	GP2 [11]	GP2 [10]	GP2 [9]	GP2 [8]	GP2 [7]	GP2 [6]	GP2 [5]	GP2 [4]	GP2 [3]	GP2 [2]	GP2 [1]	GP2 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP2[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP2[0]	GP-2-0	Peripheral function selected by IP3[27:25]
GP2[1]	GP-2-1	Peripheral function selected by IP3[30:28]
GP2[2]	GP-2-2	Peripheral function selected by IP4[1:0]
GP2[3]	GP-2-3	Peripheral function selected by IP4[4:2]
GP2[4]	GP-2-4	Peripheral function selected by IP4[7:5]
GP2[5]	GP-2-5	Peripheral function selected by IP4[9:8]
GP2[6]	GP-2-6	Peripheral function selected by IP4[12:10]
GP2[7]	GP-2-7	Peripheral function selected by IP4[15:13]
GP2[8]	GP-2-8	Peripheral function selected by IP4[18:16]
GP2[9]	GP-2-9	Peripheral function selected by IP4[19]
GP2[10]	GP-2-10	Peripheral function selected by IP4[20]
GP2[11]	GP-2-11	Peripheral function selected by IP4[21]
GP2[12]	GP-2-12	Peripheral function selected by IP4[23:22]
GP2[13]	GP-2-13	Peripheral function selected by IP4[25:24]
GP2[14]	GP-2-14	Peripheral function selected by IP4[27:26]
GP2[15]	GP-2-15	Peripheral function selected by IP4[30:28]
GP2[16]	GP-2-16	Peripheral function selected by IP5[2:0]
GP2[17]	GP-2-17	Peripheral function selected by IP5[5:3]
GP2[18]	GP-2-18	Peripheral function selected by IP5[8:6]
GP2[19]	GP-2-19	Peripheral function selected by IP5[11:9]
GP2[20]	GP-2-20	Peripheral function selected by IP5[14:12]
GP2[21]	GP-2-21	Peripheral function selected by IP5[16:15]
GP2[22]	GP-2-22	Peripheral function selected by IP5[19:17]
GP2[23]	GP-2-23	Peripheral function selected by IP5[21:20]
GP2[24]	GP-2-24	Peripheral function selected by IP5[23:22]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP2[25]	GP-2-25	Peripheral function selected by IP5[25:24]
GP2[26]	GP-2-26	Peripheral function selected by IP5[28:26]
GP2[27]	GP-2-27	Peripheral function selected by IP5[31:29]
GP2[28]	GP-2-28	AUDIO_CLKA
GP2[29]	GP-2-29	Peripheral function selected by IP6[2:0]
GP2[30]	GP-2-30	Peripheral function selected by IP6[5:3]
GP2[31]	GP-2-31	Peripheral function selected by IP6[7:6]

5.3.5 GPIO/Peripheral Function Select Register 3 (GPSR3)

Function: GPSR3 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP3 [31]	GP3 [30]	GP3 [29]	GP3 [28]	GP3 [27]	GP3 [26]	GP3 [25]	GP3 [24]	GP3 [23]	GP3 [22]	GP3 [21]	GP3 [20]	GP3 [19]	GP3 [18]	GP3 [17]	GP3 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP3 [15]	GP3 [14]	GP3 [13]	GP3 [12]	GP3 [11]	GP3 [10]	GP3 [9]	GP3 [8]	GP3 [7]	GP3 [6]	GP3 [5]	GP3 [4]	GP3 [3]	GP3 [2]	GP3 [1]	GP3 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP3[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP3[0]	GP-3-0	Peripheral function selected by IP7[5:3]
GP3[1]	GP-3-1	Peripheral function selected by IP7[8:6]
GP3[2]	GP-3-2	Peripheral function selected by IP7[10:9]
GP3[3]	GP-3-3	Peripheral function selected by IP7[12:11]
GP3[4]	GP-3-4	Peripheral function selected by IP7[14:13]
GP3[5]	GP-3-5	Peripheral function selected by IP7[16:15]
GP3[6]	GP-3-6	Peripheral function selected by IP7[18:17]
GP3[7]	GP-3-7	Peripheral function selected by IP7[20:19]
GP3[8]	GP-3-8	Peripheral function selected by IP7[23:21]
GP3[9]	GP-3-9	Peripheral function selected by IP7[26:24]
GP3[10]	GP-3-10	Peripheral function selected by IP7[29:27]
GP3[11]	GP-3-11	Peripheral function selected by IP8[2:0]
GP3[12]	GP-3-12	Peripheral function selected by IP8[5:3]
GP3[13]	GP-3-13	Peripheral function selected by IP8[8:6]
GP3[14]	GP-3-14	Peripheral function selected by IP8[11:9]
GP3[15]	GP-3-15	Peripheral function selected by IP8[14:12]
GP3[16]	GP-3-16	Peripheral function selected by IP8[17:15]
GP3[17]	GP-3-17	Peripheral function selected by IP8[20:18]
GP3[18]	GP-3-18	Peripheral function selected by IP8[23:21]
GP3[19]	GP-3-19	Peripheral function selected by IP8[25:24]
GP3[20]	GP-3-20	Peripheral function selected by IP8[27:26]
GP3[21]	GP-3-21	Peripheral function selected by IP8[30:28]
GP3[22]	GP-3-22	Peripheral function selected by IP9[2:0]
GP3[23]	GP-3-23	Peripheral function selected by IP9[5:3]
GP3[24]	GP-3-24	Peripheral function selected by IP9[6]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP3[25]	GP-3-25	Peripheral function selected by IP9[7]
GP3[26]	GP-3-26	Peripheral function selected by IP9[10:8]
GP3[27]	GP-3-27	Peripheral function selected by IP9[11]
GP3[28]	GP-3-28	Peripheral function selected by IP9[12]
GP3[29]	GP-3-29	Peripheral function selected by IP9[15:13]
GP3[30]	GP-3-30	Peripheral function selected by IP9[16]
GP3[31]	GP-3-31	Peripheral function selected by IP9[18:17]

5.3.6 GPIO/Peripheral Function Select Register 4 (GPSR4)

Function: GPSR4 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP4 [31]	GP4 [30]	GP4 [29]	GP4 [28]	GP4 [27]	GP4 [26]	GP4 [25]	GP4 [24]	GP4 [23]	GP4 [22]	GP4 [21]	GP4 [20]	GP4 [19]	GP4 [18]	GP4 [17]	GP4 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP4 [15]	GP4 [14]	GP4 [13]	GP4 [12]	GP4 [11]	GP4 [10]	GP4 [9]	GP4 [8]	GP4 [7]	GP4 [6]	GP4 [5]	GP4 [4]	GP4 [3]	GP4 [2]	GP4 [1]	GP4 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP4[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP4[0]	GP-4-0	VI0_CLK
GP4[1]	GP-4-1	Peripheral function selected by IP9[20:19]
GP4[2]	GP-4-2	Peripheral function selected by IP9[22:21]
GP4[3]	GP-4-3	Peripheral function selected by IP9[24:23]
GP4[4]	GP-4-4	Peripheral function selected by IP9[26:25]
GP4[5]	GP-4-5	VI0_DATA0_VI0_B0
GP4[6]	GP-4-6	VI0_DATA1_VI0_B1
GP4[7]	GP-4-7	VI0_DATA2_VI0_B2
GP4[8]	GP-4-8	Peripheral function selected by IP9[28:27]
GP4[9]	GP-4-9	VI0_DATA4_VI0_B4
GP4[10]	GP-4-10	VI0_DATA5_VI0_B5
GP4[11]	GP-4-11	VI0_DATA6_VI0_B6
GP4[12]	GP-4-12	VI0_DATA7_VI0_B7
GP4[13]	GP-4-13	Peripheral function selected by IP9[31:29]
GP4[14]	GP-4-14	Peripheral function selected by IP10[2:0]
GP4[15]	GP-4-15	Peripheral function selected by IP10[5:3]
GP4[16]	GP-4-16	Peripheral function selected by IP10[8:6]
GP4[17]	GP-4-17	Peripheral function selected by IP10[11:9]
GP4[18]	GP-4-18	Peripheral function selected by IP10[14:12]
GP4[19]	GP-4-19	Peripheral function selected by IP10[16:15]
GP4[20]	GP-4-20	Peripheral function selected by IP10[18:17]
GP4[21]	GP-4-21	Peripheral function selected by IP10[21:19]
GP4[22]	GP-4-22	Peripheral function selected by IP10[24:22]
GP4[23]	GP-4-23	Peripheral function selected by IP10[26:25]
GP4[24]	GP-4-24	Peripheral function selected by IP10[28:27]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP4[25]	GP-4-25	Peripheral function selected by IP10[31:29]
GP4[26]	GP-4-26	Peripheral function selected by IP11[2:0]
GP4[27]	GP-4-27	Peripheral function selected by IP11[5:3]
GP4[28]	GP-4-28	Peripheral function selected by IP11[8:6]
GP4[29]	GP-4-29	Peripheral function selected by IP15[1:0]
GP4[30]	GP-4-30	Peripheral function selected by IP15[3:2]
GP4[31]	GP-4-31	Peripheral function selected by IP15[5:4]

5.3.7 GPIO/Peripheral Function Select Register 5 (GPSR5)

Function: GPSR5 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP5 [31]	GP5 [30]	GP5 [29]	GP5 [28]	GP5 [27]	GP5 [26]	GP5 [25]	GP5 [24]	GP5 [23]	GP5 [22]	GP5 [21]	GP5 [20]	GP5 [19]	GP5 [18]	GP5 [17]	GP5 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP5 [15]	GP5 [14]	GP5 [13]	GP5 [12]	GP5 [11]	GP5 [10]	GP5 [9]	GP5 [8]	GP5 [7]	GP5 [6]	GP5 [5]	GP5 [4]	GP5 [3]	GP5 [2]	GP5 [1]	GP5 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP5[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP5[0]	GP-5-0	Peripheral function selected by IP11[11:9]
GP5[1]	GP-5-1	Peripheral function selected by IP11[14:12]
GP5[2]	GP-5-2	Peripheral function selected by IP11[16:15]
GP5[3]	GP-5-3	Peripheral function selected by IP11[18:17]
GP5[4]	GP-5-4	Peripheral function selected by IP11[19]
GP5[5]	GP-5-5	Peripheral function selected by IP11[20]
GP5[6]	GP-5-6	Peripheral function selected by IP11[21]
GP5[7]	GP-5-7	Peripheral function selected by IP11[22]
GP5[8]	GP-5-8	Peripheral function selected by IP11[23]
GP5[9]	GP-5-9	Peripheral function selected by IP11[24]
GP5[10]	GP-5-10	Peripheral function selected by IP11[25]
GP5[11]	GP-5-11	Peripheral function selected by IP11[26]
GP5[12]	GP-5-12	Peripheral function selected by IP11[27]
GP5[13]	GP-5-13	Peripheral function selected by IP11[29:28]
GP5[14]	GP-5-14	Peripheral function selected by IP11[31:30]
GP5[15]	GP-5-15	Peripheral function selected by IP12[1:0]
GP5[16]	GP-5-16	Peripheral function selected by IP12[3:2]
GP5[17]	GP-5-17	Peripheral function selected by IP12[6:4]
GP5[18]	GP-5-18	Peripheral function selected by IP12[9:7]
GP5[19]	GP-5-19	Peripheral function selected by IP12[12:10]
GP5[20]	GP-5-20	Peripheral function selected by IP12[15:13]
GP5[21]	GP-5-21	Peripheral function selected by IP12[17:16]
GP5[22]	GP-5-22	Peripheral function selected by IP12[19:18]
GP5[23]	GP-5-23	Peripheral function selected by IP12[21:20]
GP5[24]	GP-5-24	Peripheral function selected by IP12[23:22]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP5[25]	GP-5-25	Peripheral function selected by IP12[26:24]
GP5[26]	GP-5-26	Peripheral function selected by IP12[29:27]
GP5[27]	GP-5-27	Peripheral function selected by IP13[2:0]
GP5[28]	GP-5-28	Peripheral function selected by IP13[4:3]
GP5[29]	GP-5-29	Peripheral function selected by IP13[6:5]
GP5[30]	GP-5-30	Peripheral function selected by IP13[9:7]
GP5[31]	GP-5-31	Peripheral function selected by IP3[24:22]

5.3.8 GPIO/Peripheral Function Select Register 6 (GPSR6)

Function: GPSR6 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP6 [31]	GP6 [30]	GP6 [29]	GP6 [28]	GP6 [27]	GP6 [26]	GP6 [25]	GP6 [24]	GP6 [23]	GP6 [22]	GP6 [21]	GP6 [20]	GP6 [19]	GP6 [18]	GP6 [17]	GP6 [16]
Initial value:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP6 [15]	GP6 [14]	GP6 [13]	GP6 [12]	GP6 [11]	GP6 [10]	GP6 [9]	GP6 [8]	GP6 [7]	GP6 [6]	GP6 [5]	GP6 [4]	GP6 [3]	GP6 [2]	GP6 [1]	GP6 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP6[31:0]	H'4000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP6[0]	GP-6-0	Peripheral function selected by IP13[10]
GP6[1]	GP-6-1	Peripheral function selected by IP13[11]
GP6[2]	GP-6-2	Peripheral function selected by IP13[12]
GP6[3]	GP-6-3	Peripheral function selected by IP13[13]
GP6[4]	GP-6-4	Peripheral function selected by IP13[14]
GP6[5]	GP-6-5	Peripheral function selected by IP13[15]
GP6[6]	GP-6-6	Peripheral function selected by IP13[18:16]
GP6[7]	GP-6-7	Peripheral function selected by IP13[21:19]
GP6[8]	GP-6-8	SD2_CLK
GP6[9]	GP-6-9	Peripheral function selected by IP13[22]
GP6[10]	GP-6-10	Peripheral function selected by IP13[24:23]
GP6[11]	GP-6-11	Peripheral function selected by IP13[25]
GP6[12]	GP-6-12	Peripheral function selected by IP13[26]
GP6[13]	GP-6-13	Peripheral function selected by IP13[27]
GP6[14]	GP-6-14	Peripheral function selected by IP13[30:28]
GP6[15]	GP-6-15	Peripheral function selected by IP14[1:0]
GP6[16]	GP-6-16	Peripheral function selected by IP14[2]
GP6[17]	GP-6-17	Peripheral function selected by IP14[3]
GP6[18]	GP-6-18	Peripheral function selected by IP14[4]
GP6[19]	GP-6-19	Peripheral function selected by IP14[5]
GP6[20]	GP-6-20	Peripheral function selected by IP14[6]
GP6[21]	GP-6-21	Peripheral function selected by IP14[7]
GP6[22]	GP-6-22	Peripheral function selected by IP14[10:8]
GP6[23]	GP-6-23	Peripheral function selected by IP14[13:11]
GP6[24]	GP-6-24	Peripheral function selected by IP14[16:14]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP6[25]	GP-6-25	Peripheral function selected by IP14[19:17]
GP6[26]	GP-6-26	Peripheral function selected by IP14[22:20]
GP6[27]	GP-6-27	Peripheral function selected by IP14[25:23]
GP6[28]	GP-6-28	Peripheral function selected by IP14[28:26]
GP6[29]	GP-6-29	Peripheral function selected by IP14[31:29]
GP6[30]	GP-6-30	USB1_OVC
GP6[31]	GP-6-31	DU0_DOTCLKIN

5.3.9 GPIO/Peripheral Function Select Register 7 (GPSR7)

Function: GPSR7 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP7 [31]	GP7 [30]	GP7 [29]	GP7 [28]	GP7 [27]	GP7 [26]	GP7 [25]	GP7 [24]	GP7 [23]	GP7 [22]	GP7 [21]	GP7 [20]	GP7 [19]	GP7 [18]	GP7 [17]	GP7 [16]
Initial value:	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP7 [15]	GP7 [14]	GP7 [13]	GP7 [12]	GP7 [11]	GP7 [10]	GP7 [9]	GP7 [8]	GP7 [7]	GP7 [6]	GP7 [5]	GP7 [4]	GP7 [3]	GP7 [2]	GP7 [1]	GP7 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP7[31:0]	H'0380 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP7[0]	GP-7-0	Peripheral function selected by IP15[17:15]
GP7[1]	GP-7-1	Peripheral function selected by IP15[20:18]
GP7[2]	GP-7-2	Peripheral function selected by IP15[23:21]
GP7[3]	GP-7-3	Peripheral function selected by IP15[26:24]
GP7[4]	GP-7-4	Peripheral function selected by IP15[29:27]
GP7[5]	GP-7-5	Peripheral function selected by IP16[2:0]
GP7[6]	GP-7-6	Peripheral function selected by IP16[5:3]
GP7[7]	GP-7-7	Peripheral function selected by IP16[7:6]
GP7[8]	GP-7-8	Peripheral function selected by IP16[9:8]
GP7[9]	GP-7-9	Peripheral function selected by IP16[11:10]
GP7[10]	GP-7-10	Peripheral function selected by IP6[9:8]
GP7[11]	GP-7-11	Peripheral function selected by IP6[11:10]
GP7[12]	GP-7-12	Peripheral function selected by IP6[13:12]
GP7[13]	GP-7-13	Peripheral function selected by IP6[15:14]
GP7[14]	GP-7-14	Peripheral function selected by IP6[18:16]
GP7[15]	GP-7-15	Peripheral function selected by IP6[20:19]
GP7[16]	GP-7-16	Peripheral function selected by IP6[23:21]
GP7[17]	GP-7-17	Peripheral function selected by IP6[26:24]
GP7[18]	GP-7-18	Peripheral function selected by IP6[29:27]
GP7[19]	GP-7-19	Peripheral function selected by IP7[2:0]
GP7[20]	GP-7-20	Peripheral function selected by IP15[8:6]
GP7[21]	GP-7-21	Peripheral function selected by IP15[11:9]
GP7[22]	GP-7-22	Peripheral function selected by IP15[14:12]
GP7[23]	GP-7-23	USB0_PWEN
GP7[24]	GP-7-24	USB0_OVC

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP7[25]	GP-7-25	USB1_PWEN
GP7[26]	GP-7-26	—
GP7[27]	GP-7-27	—
GP7[28]	GP-7-28	—
GP7[29]	GP-7-29	—
GP7[30]	GP-7-30	—
GP7[31]	GP-7-31	—

5.3.10 Peripheral Function Select Register 0 (IPSR0)

Function: IPSR0 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP0 [30]	IP0 [29]	IP0 [28]	IP0 [27]	IP0 [26]	IP0 [25]	IP0 [24]	IP0 [23]	IP0 [22]	IP0 [21]	IP0 [20]	IP0 [19]	IP0 [18]	IP0 [17]	IP0 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP0 [15]	IP0 [14]	IP0 [13]	IP0 [12]	IP0 [11]	IP0 [10]	IP0 [9]	IP0 [8]	IP0 [7]	IP0 [6]	IP0 [5]	IP0 [4]	IP0 [3]	IP0 [2]	IP0 [1]	IP0 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP0[0]	D0	—	—	—	—	—	—
IP0[1]	D1	—	—	—	—	—	—
IP0[2]	D2	—	—	—	—	—	—
IP0[3]	D3	—	—	—	—	—	—
IP0[4]	D4	—	—	—	—	—	—
IP0[5]	D5	—	—	—	—	—	—
IP0[6]	D6	—	—	—	—	—	—
IP0[7]	D7	—	—	—	—	—	—
IP0[8]	D8	—	—	—	—	—	—
IP0[9]	D9	—	—	—	—	—	—
IP0[10]	D10	—	—	—	—	—	—
IP0[11]	D11	—	—	—	—	—	—
IP0[12]	D12	—	—	—	—	—	—
IP0[13]	D13	—	—	—	—	—	—
IP0[14]	D14	—	—	—	—	—	—
IP0[15]	D15	—	—	—	—	—	—
IP0[18:16]	A0	ATAWR0#_C	MSIOF0_SCK_B	I2C0_SCL_C	PWM2_B	—	—
IP0[20:19]	A1	MSIOF0_SYNC_B	—	—	—	—	—
IP0[22:21]	A2	MSIOF0_SS1_B	—	—	—	—	—
IP0[24:23]	A3	MSIOF0_SS2_B	—	—	—	—	—
IP0[26:25]	A4	MSIOF0_TXD_B	—	—	—	—	—
IP0[28:27]	A5	MSIOF0_RXD_B	—	—	—	—	—
IP0[30:29]	A6	MSIOF1_SCK	—	—	—	—	—

Legend: — Setting prohibited

5.3.11 Peripheral Function Select Register 1 (IPSR1)

Function: IPSR1 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP1 [31]	IP1 [30]	IP1 [29]	IP1 [28]	IP1 [27]	IP1 [26]	IP1 [25]	IP1 [24]	IP1 [23]	IP1 [22]	IP1 [21]	IP1 [20]	IP1 [19]	IP1 [18]	IP1 [17]	IP1 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP1 [15]	IP1 [14]	IP1 [13]	IP1 [12]	IP1 [11]	IP1 [10]	IP1 [9]	IP1 [8]	IP1 [7]	IP1 [6]	IP1 [5]	IP1 [4]	IP1 [3]	IP1 [2]	IP1 [1]	IP1 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP1[1:0]	A7	MSIOF1_SYNC	—	—	—	—	—	—
IP1[3:2]	A8	MSIOF1_SS1	I2C0_SCL	—	—	—	—	—
IP1[5:4]	A9	MSIOF1_SS2	I2C0_SDA	—	—	—	—	—
IP1[7:6]	A10	MSIOF1_TXD	—	MSIOF1_TXD_D	—	—	—	—
IP1[10:8]	A11	MSIOF1_RXD	I2C3_SCL_D	MSIOF1_RXD_D	—	—	—	—
IP1[13:11]	A12	FMCLK	I2C3_SDA_D	MSIOF1_SCK_D	—	—	—	—
IP1[16:14]	A13	ATAG0#_C	BPFCLK	MSIOF1_SS1_D	—	—	—	—
IP1[19:17]	A14	ATADIR0#_C	FMIN	FMIN_C	MSIOF1_SYNC_D	—	—	—
IP1[22:20]	A15	BPFCLK_C	—	—	—	—	—	—
IP1[25:23]	A16	DREQ2_B	FMCLK_C	—	SCIFA1_SCK_B	—	—	—
IP1[28:26]	A17	DACK2_B	—	I2C0_SDA_C	—	—	—	—
IP1[31:29]	A18	DREQ1	SCIFA1_RXD_C	—	SCIFB1_RXD_C	—	—	—

Legend: — Setting prohibited

5.3.12 Peripheral Function Select Register 2 (IPSR2)

Function: IPSR2 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP2 [29]	IP2 [28]	IP2 [27]	IP2 [26]	IP2 [25]	IP2 [24]	IP2 [23]	IP2 [22]	IP2 [21]	IP2 [20]	IP2 [19]	IP2 [18]	IP2 [17]	IP2 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP2 [15]	IP2 [14]	IP2 [13]	IP2 [12]	IP2 [11]	IP2 [10]	IP2 [9]	IP2 [8]	IP2 [7]	IP2 [6]	IP2 [5]	IP2 [4]	IP2 [3]	IP2 [2]	IP2 [1]	IP2 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP2[2:0]	A19	DACK1	SCIFA1_TXD_C	—	SCIFB1_TXD_C	—	SCIFB1_SCK_B	—	—
IP2[4:3]	A20	SPCLK	—	—	—	—	—	—	—
IP2[6:5]	A21	ATAWR0#_B	MOSI_IO0	—	—	—	—	—	—
IP2[9:7]	A22	MISO_IO1	FMCLK_B	TX0	SCIFA0_TXD	—	—	—	—
IP2[12:10]	A23	IO2	BPFCLK_B	RX0	SCIFA0_RXD	—	—	—	—
IP2[15:13]	A24	DREQ2	IO3	TX1	SCIFA1_TXD	—	—	—	—
IP2[18:16]	A25	DACK2	SSL	DREQ1_C	RX1	SCIFA1_RXD	—	—	—
IP2[20:19]	CS0#	ATAG0#_B	I2C1_SCL	—	—	—	—	—	—
IP2[22:21]	CS1#/A26	ATADIR0#_B	I2C1_SDA	—	—	—	—	—	—
IP2[24:23]	EX_CS1#	MSIOF2_SCK	-	—	—	—	—	—	—
IP2[26:25]	EX_CS2#	ATAWR0#	MSIOF2_SYNC	—	—	—	—	—	—
IP2[29:27]	EX_CS3#	ATADIR0#	MSIOF2_TXD	ATAG0#	—	EX_WAIT1	—	—	—

Legend: — Setting prohibited

5.3.13 Peripheral Function Select Register 3 (IPSR3)

Function: IPSR3 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP3 [30]	IP3 [29]	IP3 [28]	IP3 [27]	IP3 [26]	IP3 [25]	IP3 [24]	IP3 [23]	IP3 [22]	IP3 [21]	IP3 [20]	IP3 [19]	IP3 [18]	IP3 [17]	IP3 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP3 [15]	IP3 [14]	IP3 [13]	IP3 [12]	IP3 [11]	IP3 [10]	IP3 [9]	IP3 [8]	IP3 [7]	IP3 [6]	IP3 [5]	IP3 [4]	IP3 [3]	IP3 [2]	IP3 [1]	IP3 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP3[2:0]	EX_CS4#	ATARD0#	MSIOF2_RXD	—	EX_WAIT2	—	—	—	—
IP3[5:3]	EX_CS5#	ATACS00#	MSIOF2_SS1	HRX1_B	SCIFB1_RXD_B	PWM1	TPU_TO1	—	—
IP3[8:6]	BS#	ATACS10#	MSIOF2_SS2	HTX1_B	SCIFB1_TXD_B	PWM2	TPU_TO2	—	—
IP3[11:9]	RD/WR#	HRX2_B\HRX2_D	FMIN_B	SCIFB0_RXD_B	DREQ1_D	—	—	—	—
IP3[13:12]	WE0#	HCTS2#_B	SCIFB0_TXD_B	—	—	—	—	—	—
IP3[15:14]	WE1#	ATARD0#_B	HTX2_B	SCIFB0_RTS#_B	—	—	—	—	—
IP3[17:16]	EX_WAIT0	HRTS2#_B	SCIFB0_CTS#_B	—	—	—	—	—	—
IP3[19:18]	DREQ0	PWM3	TPU_TO3	—	—	—	—	—	—
IP3[21:20]	DACK0	DRACK0	REMOCON	—	—	—	—	—	—
IP3[24:22]	SPEEDIN	—	HSCK0_C	HSCK2_C	SCIFB0_SCK_B	SCIFB2_SCK_B	DREQ2_C	HTX2_D	-
IP3[27:25]	SSI_SCK0129	HRX0_C	HRX2_C	SCIFB0_RXD_C	SCIFB2_RXD_C	—	—	—	—
IP3[30:28]	SSI_WS0129	HTX0_C	HTX2_C	SCIFB0_TXD_C	SCIFB2_TXD_C	—	—	—	—

Legend: — Setting prohibited

5.3.14 Peripheral Function Select Register 4 (IPSR4)

Function: IPSR4 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP4 [30]	IP4 [29]	IP4 [28]	IP4 [27]	IP4 [26]	IP4 [25]	IP4 [24]	IP4 [23]	IP4 [22]	IP4 [21]	IP4 [20]	IP4 [19]	IP4 [18]	IP4 [17]	IP4 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP4 [15]	IP4 [14]	IP4 [13]	IP4 [12]	IP4 [11]	IP4 [10]	IP4 [9]	IP4 [8]	IP4 [7]	IP4 [6]	IP4 [5]	IP4 [4]	IP4 [3]	IP4 [2]	IP4 [1]	IP4 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP4[1:0]	SSI_SDATA0	I2C0_SCL_B	IIC0_SCL_B	MSIOF2_SCK_C	—	—	—	—
IP4[4:2]	SSI_SCK1	I2C0_SDA_B	IIC0_SDA_B	MSIOF2_SYNC_C	GLO_I0_D	—	—	—
IP4[7:5]	SSI_WS1	I2C1_SCL_B	IIC1_SCL_B	MSIOF2_TXD_C	GLO_I1_D	—	—	—
IP4[9:8]	SSI_SDATA1	I2C1_SDA_B	IIC1_SDA_B	MSIOF2_RXD_C	—	—	—	—
IP4[12:10]	SSI_SCK2	I2C2_SCL	GPS_CLK_B	GLO_Q0_D	HSCK1_E	—	—	—
IP4[15:13]	SSI_WS2	I2C2_SDA	GPS_SIGN_B	RX2_E	GLO_Q1_D	HCTS1#_E	—	—
IP4[18:16]	SSI_SDATA2	GPS_MAG_B	TX2_E	HRTS1#_E	—	—	—	—
IP4[19]	SSI_SCK34	—	—	—	—	—	—	—
IP4[20]	SSI_WS34	—	—	—	—	—	—	—
IP4[21]	SSI_SDATA3	—	—	—	—	—	—	—
IP4[23:22]	SSI_SCK4	GLO_SS_D	—	—	—	—	—	—
IP4[25:24]	SSI_WS4	GLO_RFON_D	—	—	—	—	—	—
IP4[27:26]	SSI_SDATA4	MSIOF2_SCK_D	—	—	—	—	—	—
IP4[30:28]	SSI_SCK5	MSIOF1_SCK_C	TS_SDATA0	GLO_I0	MSIOF2_SYNC_D	VI1_R2_B	—	—

Legend: — Setting prohibited

5.3.15 Peripheral Function Select Register 5 (IPSR5)

Function: IPSR5 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP5 [31]	IP5 [30]	IP5 [29]	IP5 [28]	IP5 [27]	IP5 [26]	IP5 [25]	IP5 [24]	IP5 [23]	IP5 [22]	IP5 [21]	IP5 [20]	IP5 [19]	IP5 [18]	IP5 [17]	IP5 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP5 [15]	IP5 [14]	IP5 [13]	IP5 [12]	IP5 [11]	IP5 [10]	IP5 [9]	IP5 [8]	IP5 [7]	IP5 [6]	IP5 [5]	IP5 [4]	IP5 [3]	IP5 [2]	IP5 [1]	IP5 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP5[2:0]	SSI_WS5	MSIOF1_SYNC_C	TS_SCK0	GLO_I1	MSIOF2_TXD_D	VI1_R3_B	—	—
IP5[5:3]	SSI_SDATA5	MSIOF1_TXD_C	TS_SDEN0	GLO_Q0	MSIOF2_SS1_D	VI1_R4_B	—	—
IP5[8:6]	SSI_SCK6	MSIOF1_RXD_C	TS_SPSYNC0	GLO_Q1	MSIOF2_RXD_D	VI1_R5_B	—	—
IP5[11:9]	SSI_WS6	GLO_SCLK	MSIOF2_SS2_D	VI1_R6_B	—	—	—	—
IP5[14:12]	SSI_SDATA6	STP_IVCXO27_0_B	GLO_SDATA	VI1_R7_B	—	—	—	—
IP5[16:15]	SSI_SCK78	STP_ISCLK_0_B	GLO_SS	—	—	—	—	—
IP5[19:17]	SSI_WS78	TX0_D	STP_ISD_0_B	GLO_RFON	—	—	—	—
IP5[21:20]	SSI_SDATA7	RX0_D	STP_ISEN_0_B	—	—	—	—	—
IP5[23:22]	SSI_SDATA8	TX1_D	STP_ISSYNC_0_B	—	—	—	—	—
IP5[25:24]	SSI_SCK9	RX1_D	GLO_SCLK_D	—	—	—	—	—
IP5[28:26]	SSI_WS9	TX3_D	CAN0_TX_D	GLO_SDATA_D	—	—	—	—
IP5[31:29]	SSI_SDATA9	RX3_D	CAN0_RX_D	—	—	—	—	—

Legend: — Setting prohibited

5.3.16 Peripheral Function Select Register 6 (IPSR6)

Function: IPSR6 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP6 [29]	IP6 [28]	IP6 [27]	IP6 [26]	IP6 [25]	IP6 [24]	IP6 [23]	IP6 [22]	IP6 [21]	IP6 [20]	IP6 [19]	IP6 [18]	IP6 [17]	IP6 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP6 [15]	IP6 [14]	IP6 [13]	IP6 [12]	IP6 [11]	IP6 [10]	IP6 [9]	IP6 [8]	IP6 [7]	IP6 [6]	IP6 [5]	IP6 [4]	IP6 [3]	IP6 [2]	IP6 [1]	IP6 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP6[2:0]	AUDIO_CLKB	STP_OPWM_0_B	MSIOF1_SCK_B	SCIF_CLK	DVC_MUTE	BPFCLK_E	—	—
IP6[5:3]	AUDIO_CLKC	SCIFB0_SCK_C	MSIOF1_SYNC_B	RX2	SCIFA2_RXD	FMIN_E	—	—
IP6[7:6]	AUDIO_CLKOUT	MSIOF1_SS1_B	TX2	SCIFA2_TXD	—	—	—	—
IP6[9:8]	IRQ0	SCIFB1_RXD_D	—	—	—	—	—	—
IP6[11:10]	IRQ1	SCIFB1_SCK_C	—	—	—	—	—	—
IP6[13:12]	IRQ2	SCIFB1_TXD_D	—	—	—	—	—	—
IP6[15:14]	IRQ3	I2C4_SCL_C	MSIOF2_TXD_E	—	—	—	—	—
IP6[18:16]	IRQ4	HRX1_C/HRX1_E	I2C4_SDA_C	MSIOF2_RXD_E	—	—	—	—
IP6[20:19]	IRQ5	HTX1_C/HTX1_E	I2C1_SCL_E	MSIOF2_SCK_E	—	—	—	—
IP6[23:21]	IRQ6	HSCK1_C	MSIOF1_SS2_B	I2C1_SDA_E	MSIOF2_SYNC_E	—	—	—
IP6[26:24]	IRQ7	HCTS1#_C	MSIOF1_TXD_B	GPS_CLK_C	GPS_CLK_D	—	—	—
IP6[29:27]	IRQ8	HRTS1#_C	MSIOF1_RXD_B	GPS_SIGN_C	GPS_SIGN_D	—	—	—

Legend: — Setting prohibited

5.3.17 Peripheral Function Select Register 7 (IPSR7)

Function: IPSR7 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP7 [29]	IP7 [28]	IP7 [27]	IP7 [26]	IP7 [25]	IP7 [24]	IP7 [23]	IP7 [22]	IP7 [21]	IP7 [20]	IP7 [19]	IP7 [18]	IP7 [17]	IP7 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP7 [15]	IP7 [14]	IP7 [13]	IP7 [12]	IP7 [11]	IP7 [10]	IP7 [9]	IP7 [8]	IP7 [7]	IP7 [6]	IP7 [5]	IP7 [4]	IP7 [3]	IP7 [2]	IP7 [1]	IP7 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP7[2:0]	IRQ9	DU1_DOTCLKIN_B	CAN_CLK_D	GPS_MAG_C	SCIF_CLK_B	GPS_MAG_D	—
IP7[5:3]	DU1_DR0	LCDOUT0	VI1_DATA0_B	TX0_B	SCIFA0_TXD_B	MSIOF2_SCK_B	—
IP7[8:6]	DU1_DR1	LCDOUT1	VI1_DATA1_B	RX0_B	SCIFA0_RXD_B	MSIOF2_SYNC_B	—
IP7[10:9]	DU1_DR2	LCDOUT2	SSI_SCK0129_B	—	—	—	—
IP7[12:11]	DU1_DR3	LCDOUT3	SSI_WS0129_B	—	—	—	—
IP7[14:13]	DU1_DR4	LCDOUT4	SSI_SDATA0_B	—	—	—	—
IP7[16:15]	DU1_DR5	LCDOUT5	SSI_SCK1_B	—	—	—	—
IP7[18:17]	DU1_DR6	LCDOUT6	SSI_WS1_B	—	—	—	—
IP7[20:19]	DU1_DR7	LCDOUT7	SSI_SDATA1_B	—	—	—	—
IP7[23:21]	DU1_DG0	LCDOUT8	VI1_DATA2_B	TX1_B	SCIFA1_TXD_B	MSIOF2_SS1_B	—
IP7[26:24]	DU1_DG1	LCDOUT9	VI1_DATA3_B	RX1_B	SCIFA1_RXD_B	MSIOF2_SS2_B	—
IP7[29:27]	DU1_DG2	LCDOUT10	VI1_DATA4_B	SCIF1_SCK_B	SCIFA1_SCK	SSI_SCK78_B	—

Legend: — Setting prohibited

5.3.18 Peripheral Function Select Register 8 (IPSR8)

Function: IPSR8 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP8 [30]	IP8 [29]	IP8 [28]	IP8 [27]	IP8 [26]	IP8 [25]	IP8 [24]	IP8 [23]	IP8 [22]	IP8 [21]	IP8 [20]	IP8 [19]	IP8 [18]	IP8 [17]	IP8 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP8 [15]	IP8 [14]	IP8 [13]	IP8 [12]	IP8 [11]	IP8 [10]	IP8 [9]	IP8 [8]	IP8 [7]	IP8 [6]	IP8 [5]	IP8 [4]	IP8 [3]	IP8 [2]	IP8 [1]	IP8 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP8[2:0]	DU1_DG3	LCDOUT11	VI1_DATA5_B	—	SSI_WS78_B	—	—
IP8[5:3]	DU1_DG4	LCDOUT12	VI1_DATA6_B	HRX0_B	SCIFB2_RXD_B	SSI_SDATA7_B	—
IP8[8:6]	DU1_DG5	LCDOUT13	VI1_DATA7_B	HCTS0#_B	SCIFB2_TXD_B	SSI_SDATA8_B	—
IP8[11:9]	DU1_DG6	LCDOUT14	HRTS0#_B	SCIFB2_CTS#_B	SSI_SCK9_B	—	—
IP8[14:12]	DU1_DG7	LCDOUT15	HTX0_B	SCIFB2_RTS#_B	SSI_WS9_B	—	—
IP8[17:15]	DU1_DB0	LCDOUT16	VI1_CLK_B	TX2_B	SCIFA2_TXD_B	MSIOF2_TXD_B	—
IP8[20:18]	DU1_DB1	LCDOUT17	VI1_HSYNC#_B	RX2_B	SCIFA2_RXD_B	MSIOF2_RXD_B	—
IP8[23:21]	DU1_DB2	LCDOUT18	VI1_VSYNC#_B	SCIF2_SCK_B	SCIFA2_SCK	SSI_SDATA9_B	—
IP8[25:24]	DU1_DB3	LCDOUT19	VI1_CLKENB_B	—	—	—	—
IP8[27:26]	DU1_DB4	LCDOUT20	VI1_FIELD_B	CAN1_RX	—	—	—
IP8[30:28]	DU1_DB5	LCDOUT21	TX3	SCIFA3_TXD	CAN1_TX	—	—

Legend: — Setting prohibited

5.3.19 Peripheral Function Select Register 9 (IPSR9)

Function: IPSR9 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP9 [31]	IP9 [30]	IP9 [29]	IP9 [28]	IP9 [27]	IP9 [26]	IP9 [25]	IP9 [24]	IP9 [23]	IP9 [22]	IP9 [21]	IP9 [20]	IP9 [19]	IP9 [18]	IP9 [17]	IP9 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP9 [15]	IP9 [14]	IP9 [13]	IP9 [12]	IP9 [11]	IP9 [10]	IP9 [9]	IP9 [8]	IP9 [7]	IP9 [6]	IP9 [5]	IP9 [4]	IP9 [3]	IP9 [2]	IP9 [1]	IP9 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP9[2:0]	DU1_DB6	LCDOUT22	I2C3_SCL_C	RX3	SCIFA3_RXD	—	—	—
IP9[5:3]	DU1_DB7	LCDOUT23	I2C3_SDA_C	SCIF3_SCK	SCIFA3_SCK	—	—	—
IP9[6]	DU1_DOTCLKIN	QSTVA_QVS	—	—	—	—	—	—
IP9[7]	DU1_DOTCLKOUT0	QCLK	—	—	—	—	—	—
IP9[10:8]	DU1_DOTCLKOUT1	QSTVB_QVE	CAN0_TX	TX3_B	I2C2_SCL_B	PWM4	—	—
IP9[11]	DU1_EXHSYNC_DU1_HSYNC	QSTH_QHS	—	—	—	—	—	—
IP9[12]	DU1_EXVSYNC_DU1_VSYNC	QSTB_QHE	—	—	—	—	—	—
IP9[15:13]	DU1_EXODDF_DU1_ODDF_DISP_CDE	QCPV_QDE	CAN0_RX	RX3_B	I2C2_SDA_B	—	—	—
IP9[16]	DU1_DISP	QPOLA	—	—	—	—	—	—
IP9[18:17]	DU1_CDE	QPOLB	PWM4_B	—	—	—	—	—
IP9[20:19]	VI0_CLKENB	TX4	SCIFA4_TXD	TS_SDATA0_D	—	—	—	—
IP9[22:21]	VI0_FIELD	RX4	SCIFA4_RXD	TS_SCK0_D	—	—	—	—
IP9[24:23]	VI0_HSYNC#	TX5	SCIFA5_TXD	TS_SDEN0_D	—	—	—	—
IP9[26:25]	VI0_VSYNC#	RX5	SCIFA5_RXD	TS_SPSYNC0_D	—	—	—	—
IP9[28:27]	VI0_DATA3_VI0_B3	SCIF3_SCK_B	SCIFA3_SCK_B	—	—	—	—	—
IP9[31:29]	VI0_G0	IIC1_SCL	STP_IVCXO27_0_C	I2C4_SCL	HCTS2#	SCIFB2_CTS#	ATAWR1#	—

Legend: — Setting prohibited

5.3.20 Peripheral Function Select Register 10 (IPSR10)

Function: IPSR10 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP10 [31]	IP10 [30]	IP10 [29]	IP10 [28]	IP10 [27]	IP10 [26]	IP10 [25]	IP10 [24]	IP10 [23]	IP10 [22]	IP10 [21]	IP10 [20]	IP10 [19]	IP10 [18]	IP10 [17]	IP10 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP10 [15]	IP10 [14]	IP10 [13]	IP10 [12]	IP10 [11]	IP10 [10]	IP10 [9]	IP10 [8]	IP10 [7]	IP10 [6]	IP10 [5]	IP10 [4]	IP10 [3]	IP10 [2]	IP10 [1]	IP10 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP10[2:0]	VI0_G1	IIC1_SDA	STP_ISCLK_0_C	I2C4_SDA	HRTS2#	SCIFB2_RTS#	ATADIR1#	—
IP10[5:3]	VI0_G2	VI2_HSYNC#	STP_ISD_0_C	I2C3_SCL_B	HSCK2	SCIFB2_SCK	ATARD1#	—
IP10[8:6]	VI0_G3	VI2_VSYNC#	STP_ISEN_0_C	I2C3_SDA_B	HRX2	SCIFB2_RXD	ATACS01#	—
IP10[11:9]	VI0_G4	VI2_CLKENB	STP_ISSYNC_0_C	HTX2	SCIFB2_TXD	SCIFB0_SCK_D	—	—
IP10[14:12]	VI0_G5	VI2_FIELD	STP_OPWM_0_C	FMCLK_D	CAN0_TX_E	HTX1_D	SCIFB0_TXD_D	—
IP10[16:15]	VI0_G6	VI2_CLK	BPFCLK_D	—	—	—	—	—
IP10[18:17]	VI0_G7	VI2_DATA0	FMIN_D	—	—	—	—	—
IP10[21:19]	VI0_R0	VI2_DATA1	GLO_I0_B	TS_SDATA0_C	ATACS11#	—	—	—
IP10[24:22]	VI0_R1	VI2_DATA2	GLO_I1_B	TS_SCK0_C	ATAG1#	—	—	—
IP10[26:25]	VI0_R2	VI2_DATA3	GLO_Q0_B	TS_SDEN0_C	—	—	—	—
IP10[28:27]	VI0_R3	VI2_DATA4	GLO_Q1_B	TS_SPSYNC0_C	—	—	—	—
IP10[31:29]	VI0_R4	VI2_DATA5	GLO_SCLK_B	TX0_C	I2C1_SCL_D	—	—	—

Legend: — Setting prohibited

5.3.21 Peripheral Function Select Register 11 (IPSR11)

Function: IPSR11 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP11 [31]	IP11 [30]	IP11 [29]	IP11 [28]	IP11 [27]	IP11 [26]	IP11 [25]	IP11 [24]	IP11 [23]	IP11 [22]	IP11 [21]	IP11 [20]	IP11 [19]	IP11 [18]	IP11 [17]	IP11 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP11 [15]	IP11 [14]	IP11 [13]	IP11 [12]	IP11 [11]	IP11 [10]	IP11 [9]	IP11 [8]	IP11 [7]	IP11 [6]	IP11 [5]	IP11 [4]	IP11 [3]	IP11 [2]	IP11 [1]	IP11 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP11[2:0]	VI0_R5	VI2_DATA6	GLO_SDATA_B	RX0_C	I2C1_SDA_D	—	—	—
IP11[5:3]	VI0_R6	VI2_DATA7	GLO_SS_B	TX1_C	I2C4_SCL_B	—	—	—
IP11[8:6]	VI0_R7	GLO_RFON_B	RX1_C	CAN0_RX_E	I2C4_SDA_B	HRX1_D	SCIFB0_RXD_D	-
IP11[11:9]	VI1_HSYNC#	AVB_RXD0	TS_SDATA0_B	TX4_B	SCIFA4_TXD_B	—	—	—
IP11[14:12]	VI1_VSYNC#	AVB_RXD1	TS_SCK0_B	RX4_B	SCIFA4_RXD_B	—	—	—
IP11[16:15]	VI1_CLKENB	AVB_RXD2	TS_SDEN0_B	—	—	—	—	—
IP11[18:17]	VI1_FIELD	AVB_RXD3	TS_SPSYNC0_B	—	—	—	—	—
IP11[19]	VI1_CLK	AVB_RXD4	—	—	—	—	—	—
IP11[20]	VI1_DATA0	AVB_RXD5	—	—	—	—	—	—
IP11[21]	VI1_DATA1	AVB_RXD6	—	—	—	—	—	—
IP11[22]	VI1_DATA2	AVB_RXD7	—	—	—	—	—	—
IP11[23]	VI1_DATA3	AVB_RX_ER	—	—	—	—	—	—
IP11[24]	VI1_DATA4	AVB_MDIO	—	—	—	—	—	—
IP11[25]	VI1_DATA5	AVB_RX_DV	—	—	—	—	—	—
IP11[26]	VI1_DATA6	AVB_MAGIC	—	—	—	—	—	—
IP11[27]	VI1_DATA7	AVB_MDC	—	—	—	—	—	—
IP11[29:28]	ETH_MDIO	AVB_RX_CLK	I2C2_SCL_C	—	—	—	—	—
IP11[31:30]	ETH_CRS_DV	AVB_LINK	I2C2_SDA_C	—	—	—	—	—

Legend: — Setting prohibited

5.3.22 Peripheral Function Select Register 12 (IPSR12)

Function: IPSR12 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP12 [29]	IP12 [28]	IP12 [27]	IP12 [26]	IP12 [25]	IP12 [24]	IP12 [23]	IP12 [22]	IP12 [21]	IP12 [20]	IP12 [19]	IP12 [18]	IP12 [17]	IP12 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP12 [15]	IP12 [14]	IP12 [13]	IP12 [12]	IP12 [11]	IP12 [10]	IP12 [9]	IP12 [8]	IP12 [7]	IP12 [6]	IP12 [5]	IP12 [4]	IP12 [3]	IP12 [2]	IP12 [1]	IP12 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Others (Set Value = H'5 to H'F)
IP12[1:0]	ETH_RX_ER	AVB_CRS	I2C3_SCL	IIC0_SCL	—	—
IP12[3:2]	ETH_RXD0	AVB_PHY_INT	I2C3_SDA	IIC0_SDA	—	—
IP12[6:4]	ETH_RXD1	AVB_GTXREFCLK	CAN0_TX_C	I2C2_SCL_D	MSIOF1_RXD_E	—
IP12[9:7]	ETH_LINK	AVB_TXD0	CAN0_RX_C	I2C2_SDA_D	MSIOF1_SCK_E	—
IP12[12:10]	ETH_REFCLK	AVB_TXD1	SCIFA3_RXD_B	CAN1_RX_C	MSIOF1_SYNC_E	—
IP12[15:13]	ETH_TXD1	AVB_TXD2	SCIFA3_TXD_B	CAN1_TX_C	MSIOF1_TXD_E	—
IP12[17:16]	ETH_TX_EN	AVB_TXD3	TCLK1_B	CAN_CLK_B	—	—
IP12[19:18]	ETH_MAGIC	AVB_TXD4	IETX_C	—	—	—
IP12[21:20]	ETH_TXD0	AVB_TXD5	IECLK_C	—	—	—
IP12[23:22]	ETH_MDC	AVB_TXD6	IERX_C	—	—	—
IP12[26:24]	STP_IVCXO27_0	AVB_TXD7	SCIFB2_TXD_D	ADIDATA_B	MSIOF0_SYNC_C	—
IP12[29:27]	STP_ISCLK_0	AVB_TX_EN	SCIFB2_RXD_D	ADICS_SAMP_B	MSIOF0_SCK_C	—

Legend: — Setting prohibited

5.3.23 Peripheral Function Select Register 13 (IPSR13)

Function: IPSR13 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP13 [30]	IP13 [29]	IP13 [28]	IP13 [27]	IP13 [26]	IP13 [25]	IP13 [24]	IP13 [23]	IP13 [22]	IP13 [21]	IP13 [20]	IP13 [19]	IP13 [18]	IP13 [17]	IP13 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP13 [15]	IP13 [14]	IP13 [13]	IP13 [12]	IP13 [11]	IP13 [10]	IP13 [9]	IP13 [8]	IP13 [7]	IP13 [6]	IP13 [5]	IP13 [4]	IP13 [3]	IP13 [2]	IP13 [1]	IP13 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP13[2:0]	STP_ISD_0	AVB_TX_ER	SCIFB2_SCK_C	ADICLK_B	MSIOF0_SS1_C	—	—	—	—
IP13[4:3]	STP_ISEN_0	AVB_TX_CLK	ADICHS0_B	MSIOF0_SS2_C	—	—	—	—	—
IP13[6:5]	STP_ISSYNC_0	AVB_COL	ADICHS1_B	MSIOF0_RXD_C	—	—	—	—	—
IP13[9:7]	STP_OPWM_0	AVB_GTX_CLK	PWM0_B	ADICHS2_B	MSIOF0_TXD_C	—	—	—	—
IP13[10]	SD0_CLK	SPCLK_B	—	—	—	—	—	—	—
IP13[11]	SD0_CMD	MOSI_IO0_B	—	—	—	—	—	—	—
IP13[12]	SD0_DATA0	MISO_IO1_B	—	—	—	—	—	—	—
IP13[13]	SD0_DATA1	IO2_B	—	—	—	—	—	—	—
IP13[14]	SD0_DATA2	IO3_B	—	—	—	—	—	—	—
IP13[15]	SD0_DATA3	SSL_B	—	—	—	—	—	—	—
IP13[18:16]	SD0_CD	MMC_D6_B	SIM0_RST_B	CAN0_RX_F	SCIFA5_TXD_B	TX3_C			—
IP13[21:19]	SD0_WP	MMC_D7_B	SIM0_D_B	CAN0_TX_F	SCIFA5_RXD_B	RX3_C			—
IP13[22]	SD2_CMD	REMOCON_B	—	—	—	—	—	—	—
IP13[24:23]	SD2_DATA0	SPEEDIN_B	—	—	—	—	—	—	—
IP13[25]	SD2_DATA1	IETX_B	—	—	—	—	—	—	—
IP13[26]	SD2_DATA2	IECLK_B	—	—	—	—	—	—	—
IP13[27]	SD2_DATA3	IERX_B	—	—	—	—	—	—	—
IP13[30:28]	SD2_CD	PWM0	TPU_TO0	I2C1_SCL_C		—	—	—	—

Legend: — Setting prohibited

5.3.24 Peripheral Function Select Register 14 (IPSR14)

Function: IPSR14 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP14 [31]	IP14 [30]	IP14 [29]	IP14 [28]	IP14 [27]	IP14 [26]	IP14 [25]	IP14 [24]	IP14 [23]	IP14 [22]	IP14 [21]	IP14 [20]	IP14 [19]	IP14 [18]	IP14 [17]	IP14 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP14 [15]	IP14 [14]	IP14 [13]	IP14 [12]	IP14 [11]	IP14 [10]	IP14 [9]	IP14 [8]	IP14 [7]	IP14 [6]	IP14 [5]	IP14 [4]	IP14 [3]	IP14 [2]	IP14 [1]	IP14 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP14[1:0]	SD2_WP	PWM1_B	I2C1_SDA_C	—	—	—	—	—
IP14[2]	SD3_CLK	MMC_CLK	—	—	—	—	—	—
IP14[3]	SD3_CMD	MMC_CMD	—	—	—	—	—	—
IP14[4]	SD3_DATA0	MMC_D0	—	—	—	—	—	—
IP14[5]	SD3_DATA1	MMC_D1	—	—	—	—	—	—
IP14[6]	SD3_DATA2	MMC_D2	—	—	—	—	—	—
IP14[7]	SD3_DATA3	MMC_D3	—	—	—	—	—	—
IP14[10:8]	SD3_CD	MMC_D4	IIC1_SCL_C	TX5_B	SCIFA5_TXD_C	—	—	—
IP14[13:11]	SD3_WP	MMC_D5	IIC1_SDA_C	RX5_B	SCIFA5_RXD_C	—	—	—
IP14[16:14]	MSIOF0_SCK	RX2_C	ADIDATA	—	VI1_CLK_C	VI1_G0_B	—	—
IP14[19:17]	MSIOF0_SYNC	TX2_C	ADICS_SAMP	—	VI1_CLKENB_C	VI1_G1_B	—	—
IP14[22:20]	MSIOF0_TXD	ADICLK	—	VI1_FIELD_C	VI1_G2_B	—	—	—
IP14[25:23]	MSIOF0_RXD	ADICHS0	—	VI1_DATA0_C	VI1_G3_B	—	—	—
IP14[28:26]	MSIOF0_SS1	MMC_D6	ADICHS1	TX0_E	VI1_HSYNC#_C	IIC0_SCL_C	VI1_G4_B	—
IP14[31:29]	MSIOF0_SS2	MMC_D7	ADICHS2	RX0_E	VI1_VSYNC#_C	IIC0_SDA_C	VI1_G5_B	—

Legend: — Setting prohibited

5.3.25 Peripheral Function Select Register 15 (IPSR15)

Function: IPSR15 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP15 [29]	IP15 [28]	IP15 [27]	IP15 [26]	IP15 [25]	IP15 [24]	IP15 [23]	IP15 [22]	IP15 [21]	IP15 [20]	IP15 [19]	IP15 [18]	IP15 [17]	IP15 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP15 [15]	IP15 [14]	IP15 [13]	IP15 [12]	IP15 [11]	IP15 [10]	IP15 [9]	IP15 [8]	IP15 [7]	IP15 [6]	IP15 [5]	IP15 [4]	IP15 [3]	IP15 [2]	IP15 [1]	IP15 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP15[1:0]	SIM0_RST	IETX	CAN1_TX_D	—	—	—	—	—
IP15[3:2]	SIM0_CLK	IECLK	CAN_CLK_C	—	—	—	—	—
IP15[5:4]	SIM0_D	IERX	CAN1_RX_D	—	—	—	—	—
IP15[8:6]	GPS_CLK	DU1_DOTCLKIN_C	AUDIO_CLKB_B	PWM5_B	SCIFA3_TXD_C	—	—	—
IP15[11:9]	GPS_SIGN	TX4_C	SCIFA4_TXD_C	PWM5	VI1_G6_B	SCIFA3_RXD_C	—	—
IP15[14:12]	GPS_MAG	RX4_C	SCIFA4_RXD_C	PWM6	VI1_G7_B	SCIFA3_SCK_C	—	—
IP15[17:15]	HCTS0#	SCIFB0_CTS#	—	GLO_I0_C	TCLK1	VI1_DATA1_C	—	—
IP15[20:18]	HRTS0#	SCIFB0_RTS#	—	GLO_I1_C	VI1_DATA2_C	—	—	—
IP15[23:21]	HSCK0	SCIFB0_SCK	—	GLO_Q0_C	CAN_CLK	TCLK2	VI1_DATA3_C	—
IP15[26:24]	HRX0	SCIFB0_RXD	—	GLO_Q1_C	CAN0_RX_B	VI1_DATA4_C	—	—
IP15[29:27]	HTX0	SCIFB0_TXD	—	GLO_SCLK_C	CAN0_TX_B	VI1_DATA5_C	—	—

Legend: — Setting prohibited

5.3.26 Peripheral Function Select Register 16 (IPSR16)

Function: IPSR16 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	IP16 [11]	IP16 [10]	IP16 [9]	IP16 [8]	IP16 [7]	IP16 [6]	IP16 [5]	IP16 [4]	IP16 [3]	IP16 [2]	IP16 [1]	IP16 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Others (Set Value = H'5 to H'F)
IP16[2:0]	HRX1	SCIFB1_RXD	VI1_R0_B	GLO_SDATA_C	VI1_DATA6_C	—
IP16[5:3]	HTX1	SCIFB1_TXD	VI1_R1_B	GLO_SS_C	VI1_DATA7_C	—
IP16[7:6]	HSCK1	SCIFB1_SCK	MLB_CK	GLO_RFON_C	—	—
IP16[9:8]	HCTS1#	SCIFB1_CTS#	MLB_SIG	CAN1_TX_B	—	—
IP16[11:10]	HRTS1#	SCIFB1_RTS#	MLB_DAT	CAN1_RX_B	—	—

Legend: — Setting prohibited

Table 5.2 shows the correspondence between the function signals and the bit settings in the GPIO/peripheral function select registers and peripheral function selecting registers.

Table 5.2 Correspondence between Function Signals and Register Bit Settings

GPIO	Peripheral-Module-(GP-Set-Value-=-1)								GPIO/ Peripheral -Function- Selecting- Bit	Peripheral- Function- Selecting- Bit
	Function-Selected-by-IP-Bits									
(GP-Set-Value-=-0)	Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)		
GP-0-0	D0	—	—	—	—	—	—	—	GP0[0]	IP0[0]
GP-0-1	D1	—	—	—	—	—	—	—	GP0[1]	IP0[1]
GP-0-2	D2	—	—	—	—	—	—	—	GP0[2]	IP0[2]
GP-0-3	D3	—	—	—	—	—	—	—	GP0[3]	IP0[3]
GP-0-4	D4	—	—	—	—	—	—	—	GP0[4]	IP0[4]
GP-0-5	D5	—	—	—	—	—	—	—	GP0[5]	IP0[5]
GP-0-6	D6	—	—	—	—	—	—	—	GP0[6]	IP0[6]
GP-0-7	D7	—	—	—	—	—	—	—	GP0[7]	IP0[7]
GP-0-8	D8	—	—	—	—	—	—	—	GP0[8]	IP0[8]
GP-0-9	D9	—	—	—	—	—	—	—	GP0[9]	IP0[9]
GP-0-10	D10	—	—	—	—	—	—	—	GP0[10]	IP0[10]
GP-0-11	D11	—	—	—	—	—	—	—	GP0[11]	IP0[11]
GP-0-12	D12	—	—	—	—	—	—	—	GP0[12]	IP0[12]
GP-0-13	D13	—	—	—	—	—	—	—	GP0[13]	IP0[13]
GP-0-14	D14	—	—	—	—	—	—	—	GP0[14]	IP0[14]
GP-0-15	D15	—	—	—	—	—	—	—	GP0[15]	IP0[15]
GP-0-16	A0	ATAWR0#_C	MSIOF0_SCK_B	I2C0_SCL_C	PWM2_B	—	—	—	GP0[16]	IP0[18:16]
GP-0-17	A1	MSIOF0_SYNC_B	—	—	—	—	—	—	GP0[17]	IP0[20:19]
GP-0-18	A2	MSIOF0_SS1_B	—	—	—	—	—	—	GP0[18]	IP0[22:21]
GP-0-19	A3	MSIOF0_SS2_B	—	—	—	—	—	—	GP0[19]	IP0[24:23]
GP-0-20	A4	MSIOF0_TXD_B	—	—	—	—	—	—	GP0[20]	IP0[26:25]
GP-0-21	A5	MSIOF0_RXD_B	—	—	—	—	—	—	GP0[21]	IP0[28:27]
GP-0-22	A6	MSIOF1_SCK	—	—	—	—	—	—	GP0[22]	IP0[30:29]
GP-0-23	A7	MSIOF1_SYNC	—	—	—	—	—	—	GP0[23]	IP1[1:0]
GP-0-24	A8	MSIOF1_SS1	I2C0_SCL	—	—	—	—	—	GP0[24]	IP1[3:2]
GP-0-25	A9	MSIOF1_SS2	I2C0_SDA	—	—	—	—	—	GP0[25]	IP1[5:4]
GP-0-26	A10	MSIOF1_TXD	—	MSIOF1_TXD_D	—	—	—	—	GP0[26]	IP1[7:6]
GP-0-27	A11	MSIOF1_RXD	I2C3_SCL_D	MSIOF1_RXD_D	—	—	—	—	GP0[27]	IP1[10:8]
GP-0-28	A12	FMCLK	I2C3_SDA_D	MSIOF1_SCK_D	—	—	—	—	GP0[28]	IP1[13:11]
GP-0-29	A13	ATAG0#_C	BPFCLK	MSIOF1_SS1_D	—	—	—	—	GP0[29]	IP1[16:14]
GP-0-30	A14	ATADIR0#_C	FMIN	FMIN_C	MSIOF1_SYNC_D	—	—	—	GP0[30]	IP1[19:17]
GP-0-31	A15	BPFCLK_C	—	—	—	—	—	—	GP0[31]	IP1[22:20]
GP-1-0	A16	DREQ2_B	FMCLK_C	—	SCIFA1_SCK_B	—	—	—	GP1[0]	IP1[25:23]
GP-1-1	A17	DACK2_B	—	I2C0_SDA_C	—	—	—	—	GP1[1]	IP1[28:26]
GP-1-2	A18	DREQ1	SCIFA1_RXD_C	—	SCIFB1_RXD_C	—	—	—	GP1[2]	IP1[31:29]
GP-1-3	A19	DACK1	SCIFA1_TXD_C	—	SCIFB1_TXD_C	—	SCIFB1_SCK_B	—	GP1[3]	IP2[2:0]
GP-1-4	A20	SPCLK	—	—	—	—	—	—	GP1[4]	IP2[4:3]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral-Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP-1-5	A21	ATAWR0#_B	MOSI_IO0	—	—	—	—	—	GP1[5]	IP2[6:5]
GP-1-6	A22	MISO_IO1	FMCLK_B	TX0	SCIFA0_TXD	—	—	—	GP1[6]	IP2[9:7]
GP-1-7	A23	IO2	BPFCLK_B	RX0	SCIFA0_RXD	—	—	—	GP1[7]	IP2[12:10]
GP-1-8	A24	DREQ2	IO3	TX1	SCIFA1_TXD	—	—	—	GP1[8]	IP2[15:13]
GP-1-9	A25	DACK2	SSL	DREQ1_C	RX1	SCIFA1_RXD	—	—	GP1[9]	IP2[18:16]
GP-1-10	CS0#	ATAG0#_B	I2C1_SCL	—	—	—	—	—	GP1[10]	IP2[20:19]
GP-1-11	CS1#/A26	ATADIR0#_B	I2C1_SDA	—	—	—	—	—	GP1[11]	IP2[22:21]
GP-1-12	EX_CS0#	—	—	—	—	—	—	—	GP1[12]	—
GP-1-13	EX_CS1#	MSIOF2_SCK	—	—	—	—	—	—	GP1[13]	IP2[24:23]
GP-1-14	EX_CS2#	ATAWR0#	MSIOF2_SYNC	—	—	—	—	—	GP1[14]	IP2[26:25]
GP-1-15	EX_CS3#	ATADIR0#	MSIOF2_TXD	ATAG0#	—	EX_WAIT1	—	—	GP1[15]	IP2[29:27]
GP-1-16	EX_CS4#	ATARD0#	MSIOF2_RXD	—	EX_WAIT2	—	—	—	GP1[16]	IP3[2:0]
GP-1-17	EX_CS5#	ATACS00#	MSIOF2_SS1	HRX1_B	SCIFB1_RXD_B	PWM1	TPU_TO1	—	GP1[17]	IP3[5:3]
GP-1-18	BS#	ATACS10#	MSIOF2_SS2	HTX1_B	SCIFB1_TXD_B	PWM2	TPU_TO2	—	GP1[18]	IP3[8:6]
GP-1-19	RD#	—	—	—	—	—	—	—	GP1[19]	—
GP-1-20	RD/WR#	HRX2_B\HRX2_D	FMIN_B	SCIFB0_RXD_B	DREQ1_D	—	—	—	GP1[20]	IP3[11:9]
GP-1-21	WE0#	HCTS2#_B	SCIFB0_TXD_B	—	—	—	—	—	GP1[21]	IP3[13:12]
GP-1-22	WE1#	ATARD0#_B	HTX2_B	SCIFB0_RTS#_B	—	—	—	—	GP1[22]	IP3[15:14]
GP-1-23	EX_WAIT0	HRTS2#_B	SCIFB0_CTS#_B	—	—	—	—	—	GP1[23]	IP3[17:16]
GP-1-24	DREQ0	PWM3	TPU_TO3	—	—	—	—	—	GP1[24]	IP3[19:18]
GP-1-25	DACK0	DRACK0	REMOCON	—	—	—	—	—	GP1[25]	IP3[21:20]
GP-2-0	SSI_SCK0129	HRX0_C	HRX2_C	SCIFB0_RXD_C	SCIFB2_RXD_C	—	—	—	GP2[0]	IP3[27:25]
GP-2-1	SSI_WS0129	HTX0_C	HTX2_C	SCIFB0_TXD_C	SCIFB2_TXD_C	—	—	—	GP2[1]	IP3[30:28]
GP-2-2	SSI_SDATA0	I2C0_SCL_B	IIC0_SCL_B	MSIOF2_SCK_C	—	—	—	—	GP2[2]	IP4[1:0]
GP-2-3	SSI_SCK1	I2C0_SDA_B	IIC0_SDA_B	MSIOF2_SYNC_C	GLO_I0_D	—	—	—	GP2[3]	IP4[4:2]
GP-2-4	SSI_WS1	I2C1_SCL_B	IIC1_SCL_B	MSIOF2_TXD_C	GLO_I1_D	—	—	—	GP2[4]	IP4[7:5]
GP-2-5	SSI_SDATA1	I2C1_SDA_B	IIC1_SDA_B	MSIOF2_RXD_C	—	—	—	—	GP2[5]	IP4[9:8]
GP-2-6	SSI_SCK2	I2C2_SCL	GPS_CLK_B	GLO_Q0_D	HSCK1_E	—	—	—	GP2[6]	IP4[12:10]
GP-2-7	SSI_WS2	I2C2_SDA	GPS_SIGN_B	RX2_E	GLO_Q1_D	HCTS1#_E	—	—	GP2[7]	IP4[15:13]
GP-2-8	SSI_SDATA2	GPS_MAG_B	TX2_E	HRTS1#_E	—	—	—	—	GP2[8]	IP4[18:16]
GP-2-9	SSI_SCK34	—	—	—	—	—	—	—	GP2[9]	IP4[19]
GP-2-10	SSI_WS34	—	—	—	—	—	—	—	GP2[10]	IP4[20]
GP-2-11	SSI_SDATA3	—	—	—	—	—	—	—	GP2[11]	IP4[21]
GP-2-12	SSI_SCK4	GLO_SS_D	—	—	—	—	—	—	GP2[12]	IP4[23:22]
GP-2-13	SSI_WS4	GLO_RFON_D	—	—	—	—	—	—	GP2[13]	IP4[25:24]
GP-2-14	SSI_SDATA4	MSIOF2_SCK_D	—	—	—	—	—	—	GP2[14]	IP4[27:26]
GP-2-15	SSI_SCK5	MSIOF1_SCK_C	TS_SDATA0	GLO_I0	MSIOF2_SYNC_D	VI1_R2_B	—	—	GP2[15]	IP4[30:28]
GP-2-16	SSI_WS5	MSIOF1_SYNC_C	TS_SCK0	GLO_I1	MSIOF2_TXD_D	VI1_R3_B	—	—	GP2[16]	IP5[2:0]
GP-2-17	SSI_SDATA5	MSIOF1_TXD_C	TS_SDEN0	GLO_Q0	MSIOF2_SS1_D	VI1_R4_B	—	—	GP2[17]	IP5[5:3]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral -Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP-2-18	SSI_SCK6	MSIOF1_RXD_C	TS_SPSYNC0	GLO_Q1	MSIOF2_RXD_D	VI1_R5_B	—	—	GP2[18]	IP5[8:6]
GP-2-19	SSI_WS6	GLO_SCLK	MSIOF2_SS2_D	VI1_R6_B	—	—	—	—	GP2[19]	IP5[11:9]
GP-2-20	SSI_SDATA6	STP_IVCXO27_0_B	GLO_SDATA	VI1_R7_B	—	—	—	—	GP2[20]	IP5[14:12]
GP-2-21	SSI_SCK78	STP_ISCLK_0_B	GLO_SS	—	—	—	—	—	GP2[21]	IP5[16:15]
GP-2-22	SSI_WS78	TX0_D	STP_ISD_0_B	GLO_RFON	—	—	—	—	GP2[22]	IP5[19:17]
GP-2-23	SSI_SDATA7	RX0_D	STP_ISEN_0_B	—	—	—	—	—	GP2[23]	IP5[21:20]
GP-2-24	SSI_SDATA8	TX1_D	STP_ISSYNC_0_B	—	—	—	—	—	GP2[24]	IP5[23:22]
GP-2-25	SSI_SCK9	RX1_D	GLO_SCLK_D	—	—	—	—	—	GP2[25]	IP5[25:24]
GP-2-26	SSI_WS9	TX3_D	CAN0_TX_D	GLO_SDATA_D	—	—	—	—	GP2[26]	IP5[28:26]
GP-2-27	SSI_SDATA9	RX3_D	CAN0_RX_D	—	—	—	—	—	GP2[27]	IP5[31:29]
GP-2-28	AUDIO_CLKA	—	—	—	—	—	—	—	GP2[28]	-
GP-2-29	AUDIO_CLKB	STP_OPWM_0_B	MSIOF1_SCK_B	SCIF_CLK	—	BPFCLK_E	—	—	GP2[29]	IP6[2:0]
GP-2-30	AUDIO_CLKC	SCIFB0_SCK_C	MSIOF1_SYNC_B	RX2	SCIFA2_RXD	FMIN_E	—	—	GP2[30]	IP6[5:3]
GP-2-31	AUDIO_CLKOUT	MSIOF1_SS1_B	TX2	SCIFA2_TXD	—	—	—	—	GP2[31]	IP6[7:6]
GP-3-0	DU1_DR0	LCDOUT0	VI1_DATA0_B	TX0_B	SCIFA0_TXD_B	MSIOF2_SCK_B	—	—	GP3[0]	IP7[5:3]
GP-3-1	DU1_DR1	LCDOUT1	VI1_DATA1_B	RX0_B	SCIFA0_RXD_B	MSIOF2_SYNC_B	—	—	GP3[1]	IP7[8:6]
GP-3-2	DU1_DR2	LCDOUT2	SSI_SCK0129_B	—	—	—	—	—	GP3[2]	IP7[10:9]
GP-3-3	DU1_DR3	LCDOUT3	SSI_WS0129_B	—	—	—	—	—	GP3[3]	IP7[12:11]
GP-3-4	DU1_DR4	LCDOUT4	SSI_SDATA0_B	—	—	—	—	—	GP3[4]	IP7[14:13]
GP-3-5	DU1_DR5	LCDOUT5	SSI_SCK1_B	—	—	—	—	—	GP3[5]	IP7[16:15]
GP-3-6	DU1_DR6	LCDOUT6	SSI_WS1_B	—	—	—	—	—	GP3[6]	IP7[18:17]
GP-3-7	DU1_DR7	LCDOUT7	SSI_SDATA1_B	—	—	—	—	—	GP3[7]	IP7[20:19]
GP-3-8	DU1_DG0	LCDOUT8	VI1_DATA2_B	TX1_B	SCIFA1_TXD_B	MSIOF2_SS1_B	—	—	GP3[8]	IP7[23:21]
GP-3-9	DU1_DG1	LCDOUT9	VI1_DATA3_B	RX1_B	SCIFA1_RXD_B	MSIOF2_SS2_B	—	—	GP3[9]	IP7[26:24]
GP-3-10	DU1_DG2	LCDOUT10	VI1_DATA4_B	SCIF1_SCK_B	SCIFA1_SCK	SSI_SCK78_B	—	—	GP3[10]	IP7[29:27]
GP-3-11	DU1_DG3	LCDOUT11	VI1_DATA5_B	—	SSI_WS78_B	—	—	—	GP3[11]	IP8[2:0]
GP-3-12	DU1_DG4	LCDOUT12	VI1_DATA6_B	HRX0_B	SCIFB2_RXD_B	SSI_SDATA7_B	—	—	GP3[12]	IP8[5:3]
GP-3-13	DU1_DG5	LCDOUT13	VI1_DATA7_B	HCTS0#_B	SCIFB2_TXD_B	SSI_SDATA8_B	—	—	GP3[13]	IP8[8:6]
GP-3-14	DU1_DG6	LCDOUT14	HRTS0#_B	SCIFB2_CTS#_B	SSI_SCK9_B	—	—	—	GP3[14]	IP8[11:9]
GP-3-15	DU1_DG7	LCDOUT15	HTX0_B	SCIFB2_RTS#_B	SSI_WS9_B	—	—	—	GP3[15]	IP8[14:12]
GP-3-16	DU1_DB0	LCDOUT16	VI1_CLK_B	TX2_B	SCIFA2_TXD_B	MSIOF2_TXD_B	—	—	GP3[16]	IP8[17:15]
GP-3-17	DU1_DB1	LCDOUT17	VI1_HSYNC#_B	RX2_B	SCIFA2_RXD_B	MSIOF2_RXD_B	—	—	GP3[17]	IP8[20:18]
GP-3-18	DU1_DB2	LCDOUT18	VI1_VSYNC#_B	SCIF2_SCK_B	SCIFA2_SCK	SSI_SDATA9_B	—	—	GP3[18]	IP8[23:21]
GP-3-19	DU1_DB3	LCDOUT19	VI1_CLKENB_B	—	—	—	—	—	GP3[19]	IP8[25:24]
GP-3-20	DU1_DB4	LCDOUT20	VI1_FIELD_B	CAN1_RX	—	—	—	—	GP3[20]	IP8[27:26]
GP-3-21	DU1_DB5	LCDOUT21	TX3	SCIFA3_TXD	CAN1_TX	—	—	—	GP3[21]	IP8[30:28]
GP-3-22	DU1_DB6	LCDOUT22	I2C3_SCL_C	RX3	SCIFA3_RXD	—	—	—	GP3[22]	IP9[2:0]
GP-3-23	DU1_DB7	LCDOUT23	I2C3_SDA_C	SCIF3_SCK	SCIFA3_SCK	—	—	—	GP3[23]	IP9[5:3]
GP-3-24	DU1_DOTCLKIN	QSTVA_QVS	—	—	—	—	—	—	GP3[24]	IP9[6]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral-Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP-3-25	DU1_DOTCLKOUT0	QCLK	—	—	—	—	—	—	GP3[25]	IP9[7]
GP-3-26	DU1_DOTCLKOUT1	QSTVB_QVE	CAN0_TX	TX3_B	I2C2_SCL_B	PWM4	—	—	GP3[26]	IP9[10:8]
GP-3-27	DU1_EXHSYNC_DU1_HSYNC	QSTH_QHS	—	—	—	—	—	—	GP3[27]	IP9[11]
GP-3-28	DU1_EXVSYNC_DU1_VSYNC	QSTB_QHE	—	—	—	—	—	—	GP3[28]	IP9[12]
GP-3-29	DU1_EXODDF_DU1_ODDF_DISP_CDE	QCPV_QDE	CAN0_RX	RX3_B	I2C2_SDA_B	—	—	—	GP3[29]	IP9[15:13]
GP-3-30	DU1_DISP	QPOLA	—	—	—	—	—	—	GP3[30]	IP9[16]
GP-3-31	DU1_CDE	QPOLB	PWM4_B	—	—	—	—	—	GP3[31]	IP9[18:17]
GP-4-0	VI0_CLK	—	—	—	—	—	—	—	GP4[0]	—
GP-4-1	VI0_CLKENB	TX4	SCIFA4_TXD	TS_SDATA0_D	—	—	—	—	GP4[1]	IP9[20:19]
GP-4-2	VI0_FIELD	RX4	SCIFA4_RXD	TS_SCK0_D	—	—	—	—	GP4[2]	IP9[22:21]
GP-4-3	VI0_HSYNC#	TX5	SCIFA5_TXD	TS_SDEN0_D	—	—	—	—	GP4[3]	IP9[24:23]
GP-4-4	VI0_VSYNC#	RX5	SCIFA5_RXD	TS_SPSYNC0_D	—	—	—	—	GP4[4]	IP9[26:25]
GP-4-5	VI0_DATA0_VI0_B0	—	—	—	—	—	—	—	GP4[5]	—
GP-4-6	VI0_DATA1_VI0_B1	—	—	—	—	—	—	—	GP4[6]	—
GP-4-7	VI0_DATA2_VI0_B2	—	—	—	—	—	—	—	GP4[7]	—
GP-4-8	VI0_DATA3_VI0_B3	SCIF3_SCK_B	SCIFA3_SCK_B	—	—	—	—	—	GP4[8]	IP9[28:27]
GP-4-9	VI0_DATA4_VI0_B4	—	—	—	—	—	—	—	GP4[9]	—
GP-4-10	VI0_DATA5_VI0_B5	—	—	—	—	—	—	—	GP4[10]	—
GP-4-11	VI0_DATA6_VI0_B6	—	—	—	—	—	—	—	GP4[11]	—
GP-4-12	VI0_DATA7_VI0_B7	—	—	—	—	—	—	—	GP4[12]	—
GP-4-13	VI0_G0	IIC1_SCL	STP_IVCXO27_0_C	I2C4_SCL	HCTS2#	SCIFB2_CTS#	ATAWR1#	—	GP4[13]	IP9[31:29]
GP-4-14	VI0_G1	IIC1_SDA	STP_ISCLK_0_C	I2C4_SDA	HRTS2#	SCIFB2_RTS#	ATADIR1#	—	GP4[14]	IP10[2:0]
GP-4-15	VI0_G2	VI2_HSYNC#	STP_ISD_0_C	I2C3_SCL_B	HSCK2	SCIFB2_SCK	ATARD1#	—	GP4[15]	IP10[5:3]
GP-4-16	VI0_G3	VI2_VSYNC#	STP_ISEN_0_C	I2C3_SDA_B	HRX2	SCIFB2_RXD	ATACS01#	—	GP4[16]	IP10[8:6]
GP-4-17	VI0_G4	VI2_CLKENB	STP_ISSYNC_0_C	HTX2	SCIFB2_TXD	SCIFB0_SCK_D	—	—	GP4[17]	IP10[11:9]
GP-4-18	VI0_G5	VI2_FIELD	STP_OPWM_0_C	FMCLK_D	CAN0_TX_E	HTX1_D	SCIFB0_TXD_D	—	GP4[18]	IP10[14:12]
GP-4-19	VI0_G6	VI2_CLK	BPFCLK_D	—	—	—	—	—	GP4[19]	IP10[16:15]
GP-4-20	VI0_G7	VI2_DATA0	FMIN_D	—	—	—	—	—	GP4[20]	IP10[18:17]
GP-4-21	VI0_R0	VI2_DATA1	GLO_I0_B	TS_SDATA0_C	ATACS11#	—	—	—	GP4[21]	IP10[21:19]
GP-4-22	VI0_R1	VI2_DATA2	GLO_I1_B	TS_SCK0_C	ATAG1#	—	—	—	GP4[22]	IP10[24:22]
GP-4-23	VI0_R2	VI2_DATA3	GLO_Q0_B	TS_SDEN0_C	—	—	—	—	GP4[23]	IP10[26:25]
GP-4-24	VI0_R3	VI2_DATA4	GLO_Q1_B	TS_SPSYNC0_C	—	—	—	—	GP4[24]	IP10[28:27]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral -Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP-4-25	VI0_R4	VI2_DATA5	GLO_SCLK_B	TX0_C	I2C1_SCL_D	—	—	—	GP4[25]	IP10[31:29]
GP-4-26	VI0_R5	VI2_DATA6	GLO_SDATA_B	RX0_C	I2C1_SDA_D	—	—	—	GP4[26]	IP11[2:0]
GP-4-27	VI0_R6	VI2_DATA7	GLO_SS_B	TX1_C	I2C4_SCL_B	—	—	—	GP4[27]	IP11[5:3]
GP-4-28	VI0_R7	GLO_RFON_B	RX1_C	CAN0_RX_E	I2C4_SDA_B	HRX1_D	SCIFB0_RXD_D	—	GP4[28]	IP11[8:6]
GP-4-29	SIM0_RST	IETX	CAN1_TX_D	—	—	—	—	—	GP4[29]	IP15[1:0]
GP-4-30	SIM0_CLK	IECLK	CAN_CLK_C	—	—	—	—	—	GP4[30]	IP15[3:2]
GP-4-31	SIM0_D	IERX	CAN1_RX_D	—	—	—	—	—	GP4[31]	IP15[5:4]
GP-5-0	VI1_HSYNC#	AVB_RXD0	TS_SDATA0_B	TX4_B	SCIFA4_TXD_B	—	—	—	GP5[0]	IP11[11:9]
GP-5-1	VI1_VSYNC#	AVB_RXD1	TS_SCK0_B	RX4_B	SCIFA4_RXD_B	—	—	—	GP5[1]	IP11[14:12]
GP-5-2	VI1_CLKENB	AVB_RXD2	TS_SDEN0_B	—	—	—	—	—	GP5[2]	IP11[16:15]
GP-5-3	VI1_FIELD	AVB_RXD3	TS_SPSYNC0_B	—	—	—	—	—	GP5[3]	IP11[18:17]
GP-5-4	VI1_CLK	AVB_RXD4	—	—	—	—	—	—	GP5[4]	IP11[19]
GP-5-5	VI1_DATA0	AVB_RXD5	—	—	—	—	—	—	GP5[5]	IP11[20]
GP-5-6	VI1_DATA1	AVB_RXD6	—	—	—	—	—	—	GP5[6]	IP11[21]
GP-5-7	VI1_DATA2	AVB_RXD7	—	—	—	—	—	—	GP5[7]	IP11[22]
GP-5-8	VI1_DATA3	AVB_RX_ER	—	—	—	—	—	—	GP5[8]	IP11[23]
GP-5-9	VI1_DATA4	AVB_MDIO	—	—	—	—	—	—	GP5[9]	IP11[24]
GP-5-10	VI1_DATA5	AVB_RX_DV	—	—	—	—	—	—	GP5[10]	IP11[25]
GP-5-11	VI1_DATA6	AVB_MAGIC	—	—	—	—	—	—	GP5[11]	IP11[26]
GP-5-12	VI1_DATA7	AVB_MDC	—	—	—	—	—	—	GP5[12]	IP11[27]
GP-5-13	ETH_MDIO	AVB_RX_CLK	I2C2_SCL_C	—	—	—	—	—	GP5[13]	IP11[29:28]
GP-5-14	ETH_CRS_DV	AVB_LINK	I2C2_SDA_C	—	—	—	—	—	GP5[14]	IP11[31:30]
GP-5-15	ETH_RX_ER	AVB_CRS	I2C3_SCL	IIC0_SCL	—	—	—	—	GP5[15]	IP12[1:0]
GP-5-16	ETH_RXD0	AVB_PHY_INT	I2C3_SDA	IIC0_SDA	—	—	—	—	GP5[16]	IP12[3:2]
GP-5-17	ETH_RXD1	AVB_GTXREFCLK	CAN0_TX_C	I2C2_SCL_D	MSIOF1_RXD_E	—	—	—	GP5[17]	IP12[6:4]
GP-5-18	ETH_LINK	AVB_TXD0	CAN0_RX_C	I2C2_SDA_D	MSIOF1_SCK_E	—	—	—	GP5[18]	IP12[9:7]
GP-5-19	ETH_REFCLK	AVB_TXD1	SCIFA3_RXD_B	CAN1_RX_C	MSIOF1_SYNC_E	—	—	—	GP5[19]	IP12[12:10]
GP-5-20	ETH_TXD1	AVB_TXD2	SCIFA3_TXD_B	CAN1_TX_C	MSIOF1_TXD_E	—	—	—	GP5[20]	IP12[15:13]
GP-5-21	ETH_TX_EN	AVB_TXD3	TCLK1_B	CAN_CLK_B	—	—	—	—	GP5[21]	IP12[17:16]
GP-5-22	ETH_MAGIC	AVB_TXD4	IETX_C	—	—	—	—	—	GP5[22]	IP12[19:18]
GP-5-23	ETH_TXD0	AVB_TXD5	IECLK_C	—	—	—	—	—	GP5[23]	IP12[21:20]
GP-5-24	ETH_MDC	AVB_TXD6	IERX_C	—	—	—	—	—	GP5[24]	IP12[23:22]
GP-5-25	STP_IVCXO27_0	AVB_TXD7	SCIFB2_TXD_D	ADIDATA_B	MSIOF0_SYNC_C	—	—	—	GP5[25]	IP12[26:24]
GP-5-26	STP_ISCLK_0	AVB_TX_EN	SCIFB2_RXD_D	ADICS_SAMP_B	MSIOF0_SCK_C	—	—	—	GP5[26]	IP12[29:27]
GP-5-27	STP_ISD_0	AVB_TX_ER	SCIFB2_SCK_C	ADICLK_B	MSIOF0_SS1_C	—	—	—	GP5[27]	IP13[2:0]
GP-5-28	STP_ISEN_0	AVB_TX_CLK	ADICHS0_B	MSIOF0_SS2_C	—	—	—	—	GP5[28]	IP13[4:3]
GP-5-29	STP_ISSYNC_0	AVB_COL	ADICHS1_B	MSIOF0_RXD_C	—	—	—	—	GP5[29]	IP13[6:5]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral-Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP-5-30	STP_OPWM_0	AVB_GTX_CLK	PWM0_B	ADICHS2_B	MSIOF0_TXD_C	—	—	—	GP5[30]	IP13[9:7]
GP-5-31	SPEEDIN	—	HSCK0_C	HSCK2_C	SCIFB0_SCK_B	SCIFB2_SCK_B	DREQ2_C	HTX2_D	GP5[31]	IP3[24:22]
GP-6-0	SD0_CLK	SPCLK_B	—	—	—	—	—	—	GP6[0]	IP13[10]
GP-6-1	SD0_CMD	MOSI_IO0_B	—	—	—	—	—	—	GP6[1]	IP13[11]
GP-6-2	SD0_DATA0	MISO_IO1_B	—	—	—	—	—	—	GP6[2]	IP13[12]
GP-6-3	SD0_DATA1	IO2_B	—	—	—	—	—	—	GP6[3]	IP13[13]
GP-6-4	SD0_DATA2	IO3_B	—	—	—	—	—	—	GP6[4]	IP13[14]
GP-6-5	SD0_DATA3	SSL_B	—	—	—	—	—	—	GP6[5]	IP13[15]
GP-6-6	SD0_CD	MMC_D6_B	SIM0_RST_B	CAN0_RX_F	SCIFA5_TXD_B	TX3_C	—	—	GP6[6]	IP13[18:16]
GP-6-7	SD0_WP	MMC_D7_B	SIM0_D_B	CAN0_TX_F	SCIFA5_RXD_B	RX3_C	—	—	GP6[7]	IP13[21:19]
GP-6-8	SD2_CLK	—	—	—	—	—	—	—	GP6[8]	-
GP-6-9	SD2_CMD	REMOCON_B	—	—	—	—	—	—	GP6[9]	IP13[22]
GP-6-10	SD2_DATA0	SPEEDIN_B	—	—	—	—	—	—	GP6[10]	IP13[24:23]
GP-6-11	SD2_DATA1	IETX_B	—	—	—	—	—	—	GP6[11]	IP13[25]
GP-6-12	SD2_DATA2	IECLK_B	—	—	—	—	—	—	GP6[12]	IP13[26]
GP-6-13	SD2_DATA3	IERX_B	—	—	—	—	—	—	GP6[13]	IP13[27]
GP-6-14	SD2_CD	PWM0	TPU_TO0	I2C1_SCL_C	—	—	—	—	GP6[14]	IP13[30:28]
GP-6-15	SD2_WP	PWM1_B	I2C1_SDA_C	—	—	—	—	—	GP6[15]	IP14[1:0]
GP-6-16	SD3_CLK	MMC_CLK	—	—	—	—	—	—	GP6[16]	IP14[2]
GP-6-17	SD3_CMD	MMC_CMD	—	—	—	—	—	—	GP6[17]	IP14[3]
GP-6-18	SD3_DATA0	MMC_D0	—	—	—	—	—	—	GP6[18]	IP14[4]
GP-6-19	SD3_DATA1	MMC_D1	—	—	—	—	—	—	GP6[19]	IP14[5]
GP-6-20	SD3_DATA2	MMC_D2	—	—	—	—	—	—	GP6[20]	IP14[6]
GP-6-21	SD3_DATA3	MMC_D3	—	—	—	—	—	—	GP6[21]	IP14[7]
GP-6-22	SD3_CD	MMC_D4	IIC1_SCL_C	TX5_B	SCIFA5_TXD_C	—	—	—	GP6[22]	IP14[10:8]
GP-6-23	SD3_WP	MMC_D5	IIC1_SDA_C	RX5_B	SCIFA5_RXD_C	—	—	—	GP6[23]	IP14[13:11]
GP-6-24	MSIOF0_SCK	RX2_C	ADIDATA	—	VI1_CLK_C	VI1_G0_B	—	—	GP6[24]	IP14[16:14]
GP-6-25	MSIOF0_SYNC	TX2_C	ADICS_SAMP	—	VI1_CLKENB_C	VI1_G1_B	—	—	GP6[25]	IP14[19:17]
GP-6-26	MSIOF0_TXD	ADICLK	—	VI1_FIELD_C	VI1_G2_B	—	—	—	GP6[26]	IP14[22:20]
GP-6-27	MSIOF0_RXD	ADICHS0	—	VI1_DATA0_C	VI1_G3_B	—	—	—	GP6[27]	IP14[25:23]
GP-6-28	MSIOF0_SS1	MMC_D6	ADICHS1	TX0_E	VI1_HSYNC#_C	IIC0_SCL_C	VI1_G4_B	—	GP6[28]	IP14[28:26]
GP-6-29	MSIOF0_SS2	MMC_D7	ADICHS2	RX0_E	VI1_VSYNC#_C	IIC0_SDA_C	VI1_G5_B	—	GP6[29]	IP14[31:29]
GP-6-30	USB1_OVC	—	—	—	—	—	—	—	GP6[30]	—
GP-6-31	DU0_DOTCLKIN	—	—	—	—	—	—	—	GP6[31]	—
GP-7-0	HCTS0#	SCIFB0_CTS#	—	GLO_I0_C	TCLK1	VI1_DATA1_C	—	—	GP7[0]	IP15[17:15]
GP-7-1	HRTS0#	SCIFB0_RTS#	—	GLO_I1_C	VI1_DATA2_C	—	—	—	GP7[1]	IP15[20:18]
GP-7-2	HSCK0	SCIFB0_SCK	—	GLO_Q0_C	CAN_CLK	TCLK2	VI1_DATA3_C	—	GP7[2]	IP15[23:21]
GP-7-3	HRX0	SCIFB0_RXD	—	GLO_Q1_C	CAN0_RX_B	VI1_DATA4_C	—	—	GP7[3]	IP15[26:24]
GP-7-4	HTX0	SCIFB0_TXD	—	GLO_SCLK_C	CAN0_TX_B	VI1_DATA5_C	—	—	GP7[4]	IP15[29:27]
GP-7-5	HRX1	SCIFB1_RXD	VI1_R0_B	GLO_SDATA_C	VI1_DATA6_C	—	—	—	GP7[5]	IP16[2:0]
GP-7-6	HTX1	SCIFB1_TXD	VI1_R1_B	GLO_SS_C	VI1_DATA7_C	—	—	—	GP7[6]	IP16[5:3]
GP-7-7	HSCK1	SCIFB1_SCK	MLB_CK	GLO_RFON_C	—	—	—	—	GP7[7]	IP16[7:6]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits								GPIO/ Peripheral-Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
	Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)		
GP-7-8	HCTS1#	SCIFB1_CTS#	MLB_SIG	CAN1_TX_B	—	—	—	—	GP7[8]	IP16[9:8]
GP-7-9	HRTS1#	SCIFB1_RTS#	MLB_DAT	CAN1_RX_B	—	—	—	—	GP7[9]	IP16[11:10]
GP-7-10	IRQ0	SCIFB1_RXD_D	—	—	—	—	—	—	GP7[10]	IP6[9:8]
GP-7-11	IRQ1	SCIFB1_SCK_C	—	—	—	—	—	—	GP7[11]	IP6[11:10]
GP-7-12	IRQ2	SCIFB1_TXD_D	—	—	—	—	—	—	GP7[12]	IP6[13:12]
GP-7-13	IRQ3	I2C4_SCL_C	MSIOF2_TXD_E	—	—	—	—	—	GP7[13]	IP6[15:14]
GP-7-14	IRQ4	HRX1_C\HRX1_E	I2C4_SDA_C	MSIOF2_RXD_E	—	—	—	—	GP7[14]	IP6[18:16]
GP-7-15	IRQ5	HTX1_C\HTX1_E	I2C1_SCL_E	MSIOF2_SCK_E	—	—	—	—	GP7[15]	IP6[20:19]
GP-7-16	IRQ6	HSCK1_C	MSIOF1_SS2_B	I2C1_SDA_E	MSIOF2_SYNC_E	—	—	—	GP7[16]	IP6[23:21]
GP-7-17	IRQ7	HCTS1#_C	MSIOF1_TXD_B	GPS_CLK_C	GPS_CLK_D	—	—	—	GP7[17]	IP6[26:24]
GP-7-18	IRQ8	HRTS1#_C	MSIOF1_RXD_B	GPS_SIGN_C	GPS_SIGN_D	—	—	—	GP7[18]	IP6[29:27]
GP-7-19	IRQ9	DU1_DOTCLKIN_B	CAN_CLK_D	GPS_MAG_C	SCIF_CLK_B	GPS_MAG_D	—	—	GP7[19]	IP7[2:0]
GP-7-20	GPS_CLK	DU1_DOTCLKIN_C	AUDIO_CLKB_B	PWM5_B	SCIFA3_TXD_C	—	—	—	GP7[20]	IP15[8:6]
GP-7-21	GPS_SIGN	TX4_C	SCIFA4_TXD_C	PWM5	VI1_G6_B	SCIFA3_RXD_C	—	—	GP7[21]	IP15[11:9]
GP-7-22	GPS_MAG	RX4_C	SCIFA4_RXD_C	PWM6	VI1_G7_B	SCIFA3_SCK_C	—	—	GP7[22]	IP15[14:12]
GP-7-23	USB0_PWEN	—	—	—	—	—	—	—	GP7[23]	—
GP-7-24	USB0_OVC	—	—	—	—	—	—	—	GP7[24]	—
GP-7-25	USB1_PWEN	—	—	—	—	—	—	—	GP7[25]	—

Legend: — Setting prohibited

5.3.27 Module Select Register (MOD_SEL)

Function: MOD_SEL selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the SCIF, HSCIF, SSI, QSPI, VI , TMU, LBSC, TSIF and MSIOF are assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups. When ssi7 and ssi8 (in MOD_SEL2 register) are to be used simultaneously, the values of sel_ssi7 and sel_ssi8 must be the same so that the selected pins belong to the same group. If this is not the case, correct operation is not guaranteed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	sel_ scif1_1	sel_ scif1_0	sel_ scifb_1	sel_ scifb_0	sel_ scifb2_1	sel_ scifb2_0	sel_ scifb1_2	sel_ scifb1_1	sel_ scifb1_0	sel_ scifa1_1	sel_ scifa1_0	sel_ ssi9	sel_ scfa	sel_qsp	sel_ ssi7_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_ hscif1_2	sel_ hscif1_1	sel_ hscif1_0	—	—	sel_ vi1_1	sel_ vi1_0	—	—	sel_ tmu1	sel_ lbs_1	sel_ lbs_0	sel_ tsif0_1	sel_ tsif0_0	sel_ sof0_1	sel_ sof0_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 1 * (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_scif1 [1:0]	RX1 of the A25 pin TX1 of the A24 pin	—	RX1_B of the DU1_DG1 pin TX1_B of the DU1_DG0 pin	RX1_C of the VI0_R7 pin TX1_C of the VI0_R6 pin	RX1_D of the SSI_SCK9 pin TX1_D of the SSI_SDATA8 pin	—
sel_scifb [1:0]	SCIFB0_CTS# of the HCTS0# pin SCIFB0_RTS# of the HRTS0# pin SCIFB0_RXD of the HRX0 pin SCIFB0_SCK of the HSCK0 pin SCIFB0_TXD of the HTX0 pin	—	SCIFB0_CTS#_B of the EX_WAIT0 pin SCIFB0_RTS#_B of the WE1# pin SCIFB0_RXD_B of the RD_WR# pin SCIFB0_SCK_B of the SPEEDIN pin SCIFB0_TXD_B of the WE0# pin	SCIFB0_RXD_C of the SSI_SCK0129 pin SCIFB0_SCK_C of the AUDIO_CLKC pin SCIFB0_TXD_C of the SSI_WS0129 pin	SCIFB0_RXD_D of the VI0_R7 pin SCIFB0_SCK_D of the VI0_G4 pin SCIFB0_TXD_D of the VI0_G5 pin	—
sel_scifb2 [1:0]	SCIFB2_CTS# of the VI0_G0 pin SCIFB2_RTS# of the VI0_G1 pin SCIFB2_RXD of the VI0_G3 pin SCIFB2_SCK of the VI0_G2 pin SCIFB2_TXD of the VI0_G4 pin	—	SCIFB2_CTS#_B of the DU1_DG6 pin SCIFB2_RTS#_B of the DU1_DG7 pin SCIFB2_RXD_B of the DU1_DG4 pin SCIFB2_SCK_B of the SPEEDIN pin SCIFB2_TXD_B of the DU1_DG5 pin	SCIFB2_RXD_C of the SSI_SCK0129 pin SCIFB2_SCK_C of the STP_ISD_0 pin SCIFB2_TXD_C of the SSI_WS0129 pin	SCIFB2_RXD_D of the STP_ISCLK_0 pin SCIFB2_TXD_D of the STP_IVCXO27_0 pin	—
sel_scifb1 [2:0]	SCIFB1_RXD of the HRX1 pin SCIFB1_SCK of the HSCK1 pin SCIFB1_TXD of the HTX1 pin	SCIFB1_SCK_B of the A19 pin SCIFB1_RXD of the HRX1 pin SCIFB1_TXD of the HTX1 pin	SCIFB1_RXD_B of the EX_CS5# pin SCIFB1_SCK_B of the A19 pin SCIFB1_TXD_B of the BS# pin	SCIFB1_RXD_C of the A18 pin SCIFB1_SCK_C of the IRQ1 pin SCIFB1_TXD_C of the A19 pin	SCIFB1_RXD_D of the IRQ0 pin SCIFB1_TXD_D of the IRQ2 pin	—

Bit Name	Function 1 (Set Value = H'0)	Function 1 * (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_scifa1 [1:0]	SCIFA1_RXD of the A25 pin SCIFA1_SCK of the DU1_DG2 pin SCIFA1_TXD of the A24 pin	—	SCIFA1_RXD_B of the DU1_DG1 pin SCIFA1_SCK_B of the A16 pin SCIFA1_TXD_B of the DU1_DG0 pin	SCIFA1_RXD_C of the A18 pin SCIFA1_TXD_C of the A19 pin	—	—
sel_ssi9	SSI_SCK9 of the SSI_SCK9 pin SSI_SDATA9 of the SSI_SDATA9 pin SSI_WS9 of the SSI_WS9 pin	—	SSI_SCK9_B of the DU1_DG6 pin SSI_SDATA9_B of the DU1_DB2 pin SSI_WS9_B of the DU1_DG7 pin	—	—	—
sel_scfa	SCIFA0_RXD of the A23 pin SCIFA0_TXD of the A22 pin	—	SCIFA0_RXD_B of the DU1_DR1 pin SCIFA0_TXD_B of the DU1_DR0 pin	—	—	—
sel_qsp	IO2 of the A23 pin IO3 of the A24 pin MISO_IO1 of the A22 pin MOSI_IO0 of the A21 pin SPCLK of the A20 pin SSL of the A25 pin	—	IO2_B of the SD0_DATA1 pin IO3_B of the SD0_DATA2 pin MISO_IO1_B of the SD0_DATA0 pin MOSI_IO0_B of the SD0_CMD pin SPCLK_B of the SD0_CLK pin SSL_B of the SD0_DATA3 pin	—	—	—
sel_ssi7	SSI_SCK78 of the SSI_SCK78 pin SSI_SDATA7 of the SSI_SDATA7 pin SSI_WS78 of the SSI_WS78 pin	—	SSI_SCK78_B of the DU1_DG2 pin SSI_SDATA7_B of the DU1_DG4 pin SSI_WS78_B of the DU1_DG3 pin	—	—	—
sel_hscif1 [2:0]	HCTS1# of the HCTS1# pin HRTS1# of the HRTS1# pin HRX1 of the HRX1 pin HSCK1 of the HSCK1 pin HTX1 of the HTX1 pin	—	HRX1_B of the EX_CS5# pin HTX1_B of the BS# pin	HCTS1#_C of the IRQ7 pin HRTS1#_C of the IRQ8 pin HRX1_C of the IRQ4 pin HSCK1_C of the IRQ6 pin HTX1_C of the IRQ5 pin	HRX1_D of the VI0_R7 pin HTX1_D of the VI0_G5 pin	HCTS1#_E of the SSI_WS2 pin HRTS1#_E of the SSI_SDATA2 pin HRX1_E of the IRQ4 pin HSCK1_E of the SSI_SCK2 pin HTX1_E of the IRQ5 pin
sel_vi1[1:0]	VI1_CLKENB of the VI1_CLKENB pin VI1_CLK of the VI1_CLK pin VI1_DATA0 of the VI1_DATA0 pin VI1_DATA1 of the VI1_DATA1 pin VI1_DATA2 of the VI1_DATA2 pin VI1_DATA3 of the VI1_DATA3 pin VI1_DATA4 of the VI1_DATA4 pin VI1_DATA5 of the VI1_DATA5 pin VI1_DATA6 of the VI1_DATA6 pin VI1_DATA7 of the VI1_DATA7 pin VI1_FIELD of the VI1_FIELD pin VI1_HSYNC# of the VI1_HSYNC# pin VI1_VSYNC# of the VI1_VSYNC# pin	—	VI1_CLK_B of the DU1_DB0 pin VI1_CLKENB_B of the DU1_DB3 pin VI1_DATA0_B of the DU1_DR0 pin VI1_DATA1_B of the DU1_DR1 pin VI1_DATA2_B of the DU1_DG0 pin VI1_DATA3_B of the DU1_DG1 pin VI1_DATA4_B of the DU1_DG2 pin VI1_DATA5_B of the DU1_DG3 pin VI1_DATA6_B of the DU1_DG4 pin VI1_DATA7_B of the DU1_DG5 pin VI1_FIELD_B of the DU1_DB4 pin VI1_HSYNC#_B of the DU1_DB1 pin VI1_VSYNC#_B of the DU1_DB2 pin	VI1_CLK_C of the MSIOF0_SCK pin VI1_CLKENB_C of the MSIOF0_SYNC pin VI1_DATA0_C of the MSIOF0_RXD pin VI1_DATA1_C of the HCTS0# pin VI1_DATA2_C of the HRTS0# pin VI1_DATA3_C of the HSCK0 pin VI1_DATA4_C of the HRX0 pin VI1_DATA5_C of the HTX0 pin VI1_DATA6_C of the HRX1 pin VI1_DATA7_C of the HTX1 pin VI1_FIELD_C of the MSIOF0_TXD pin VI1_HSYNC#_C of the MSIOF0_SS1 pin VI1_VSYNC#_C of the MSIOF0_SS2 pin	—	—
sel_tmu1	TCLK1 of the HCTS0# pin	—	TCLK1_B of the ETH_TX_EN pin	—	—	—

Bit Name	Function 1 (Set Value = H'0)	Function 1 * (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_lbs[1:0]	ATADIR0# of the EX_CS3# pin ATAG0# of the EX_CS3# pin ATARD0# of the EX_CS4# pin ATAWR0# of the EX_CS2# pin DACK2 of the A25 pin DREQ1 of the A18 pin DREQ2 of the A24 pin	—	ATADIR0#_B of the CS1#/A26 pin ATAG0#_B of the CS0# pin ATARD0#_B of the WE1# pin ATAWR0#_B of the A21 pin DACK2_B of the A17 pin DREQ1_D of the RD_WR# pin DREQ2_B of the A16 pin	ATADIR0#_C of the A14 pin ATAG0#_C of the A13 pin ATAWR0#_C of the A0 pin DREQ1_C of the A25 pin DREQ2_C of the SPEEDIN pin	DREQ1_D of the RD_WR# pin DREQ2 of the A24 pin	—
sel_tsif0 [1:0]	TS_SCK0 of the SSI_WS5 pin TS_SDATA0 of the SSI_SCK5 pin TS_SDEN0 of the SSI_SDATA5 pin TS_SPSYNC0 of the SSI_SCK6 pin	—	TS_SCK0_B of the VI1_VSYNC# pin TS_SDATA0_B of the VI1_HSYNC# pin TS_SDEN0_B of the VI1_CLKENB pin TS_SPSYNC0_B of the VI1_FIELD pin	TS_SCK0_C of the VI0_R1 pin TS_SDATA0_C of the VI0_R0 pin TS_SDEN0_C of the VI0_R2 pin TS_SPSYNC0_C of the VI0_R3 pin	TS_SCK0_D of the VI0_FIELD pin TS_SDATA0_D of the VI0_CLKENB pin TS_SDEN0_D of the VI0_HSYNC# pin TS_SPSYNC0_D of the VI0_VSYNC# pin	—
sel_sof0 [1:0]	MSIOF0_RXD of the MSIOF0_RXD pin MSIOF0_SCK of the MSIOF0_SCK pin MSIOF0_SS1 of the MSIOF0_SS1 pin MSIOF0_SS2 of the MSIOF0_SS2 pin MSIOF0_SYNC of the MSIOF0_SYNC pin MSIOF0_TXD of the MSIOF0_TXD pin	—	MSIOF0_RXD_B of the A5 pin MSIOF0_SCK_B of the A0 pin MSIOF0_SS1_B of the A2 pin MSIOF0_SS2_B of the A3 pin MSIOF0_SYNC_B of the A1 pin MSIOF0_TXD_B of the A4 pin	MSIOF0_RXD_C of the STP_ISSYNC_0 pin MSIOF0_SCK_C of the STP_ISCLK_0 pin MSIOF0_SS1_C of the STP_ISD_0 pin MSIOF0_SS2_C of the STP_ISEN_0 pin MSIOF0_SYNC_C of the STP_IVCXO27_0 pin MSIOF0_TXD_C of the STP_OPWM_0 pin	—	—

Legend: – Setting prohibited

Note: * Using SCIFB1_SCK_B is regardless of value of the bit sel_scifb1[2:0].

5.3.28 Module Select Register 2 (MOD_SEL2)

Function: MOD_SEL2 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the SCIF, RCAN, ADG, FM-VICS, GPS, SIM and SSI is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. When ssi8 and ssi7 (in MOD_SEL register) are to be used simultaneously, the values of sel_ssi8 and sel_ssi7 must be the same so that the selected pins belong to the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	sel_ scif0_2	sel_ scif0_1	sel_ scif0_0	—	sel_scif	sel_ can0_2	sel_ can0_1	sel_ can0_0	sel_ can1_1	sel_ can1_0	—	sel_ scifa2_0	sel_ scif4_1	sel_ scif4_0	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_ adg_0	sel_ fm_2	sel_ fm_1	sel_ fm_0	sel_ scifa5_1	sel_ scifa5_0	—	sel_ gps_1	sel_ gps_0	sel_ scifa4_1	sel_ scifa4_0	sel_ scifa3_1	sel_ scifa3_0	sel_ sim_0	—	sel_ ssi8_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)
sel_scif0[2:0]	RX0 of the A23 pin TX0 of the A22 pin	RX0_B of the DU1_DR1 pin TX0_B of the DU1_DR0 pin	RX0_C of the VI0_R5 pin TX0_C of the VI0_R4 pin	RX0_D of the SSI_SDATA7 pin TX0_D of the SSI_WS78 pin	RX0_E of the MSIOF0_SS2 pin TX0_E of the MSIOF0_SS1 pin	—
sel_scif	SCIF_CLK of the AUDIO_CLKB pin	SCIF_CLK_B of the IRQ9 pin	—	—	—	—
sel_can0[2:0]	CAN0_RX of the DU1_EXODDF_ DU1_ODDF_DISP_CD E pin CAN0_TX of the DU1_DOTCLKOUT1 pin	CAN0_RX_B of the HRX0 pin CAN0_TX_B of the HTX0 pin	CAN0_RX_C of the ETH_LINK pin CAN0_TX_C of the ETH_RXD1 pin	CAN0_RX_D of the SSI_SDATA9 pin CAN0_TX_D of the SSI_WS9 pin	CAN0_RX_E of the VI0_R7 pin CAN0_TX_E of the VI0_G5 pin	CAN0_RX_F of the SD0_CD pin CAN0_TX_F of the SD0_WP pin
sel_can1[1:0]	CAN1_RX of the DU1_DB4 pin CAN1_TX of the DU1_DB5 pin	CAN1_RX_B of the HRTS1# pin CAN1_TX_B of the HCTS1# pin	CAN1_RX_C of the ETH_REFCLK pin CAN1_TX_C of the ETH_TXD1 pin	CAN1_RX_D of the SIM0_D pin CAN1_TX_D of the SIM0_RST pin	—	—
sel_scifa2	SCIFA2_RXD of the AUDIO_CLKC pin SCIFA2_TXD of the AUDIO_CLKOUT pin	SCIFA2_SCK of the DU1_DB2 pin * SCIFA2_RXD_B of the DU1_DB1 pin SCIFA2_TXD_B of the DU1_DB0 pin	—	—	—	—
sel_scif4[1:0]	RX4 of the VI0_FIELD pin TX4 of the VI0_CLKENB pin	RX4_B of the VI1_VSYNC# pin TX4_B of the VI1_HSYNC# pin	RX4_C of the GPS_MAG pin TX4_C of the GPS_SIGN pin	—	—	—
sel_adg	AUDIO_CLKB of the AUDIO_CLKB pin	AUDIO_CLKB_B of the GPS_CLK pin	—	—	—	—

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)
sel_fm[2:0]	BPFCLK of the A13 pin FMCLK of the A12 pin FMIN of the A14 pin	BPFCLK_B of the A23 pin FMCLK_B of the A22 pin FMIN_B of the RD_WR# pin	BPFCLK_C of the A15 pin FMCLK_C of the A16 pin FMIN_C of the A14 pin	BPFCLK_D of the VI0_G6 pin FMCLK_D of the VI0_G5 pin FMIN_D of the VI0_G7 pin	BPFCLK_E of the AUDIO_CLKB pin FMIN_E of the pin AUDIO_CLKC	—
sel_scifa5 [1:0]	SCIFA5_RXD of the VI0_VSYNC# pin SCIFA5_TXD of the VI0_HSYNC# pin	SCIFA5_RXD_B of the SD0_WP pin SCIFA5_TXD_B of the SD0_CD pin	SCIFA5_RXD_C of the SD3_WP pin SCIFA5_TXD_C of the SD3_CD pin	—	—	—
sel_gps[1:0]	GLO_I0 of the SSI_SCK5 pin GLO_I1 of the SSI_WS5 pin GLO_Q0 of the SSI_SDATA5 pin GLO_Q1 of the SSI_SCK6 pin GLO_RFON of the SSI_WS78 pin GLO_SCLK of the SSI_WS6 pin GLO_SDATA of the SSI_SDATA6 pin GLO_SS of the SSI_SCK78 pin GPS_CLK of the GPS_CLK pin GPS_MAG of the GPS_MAG pin GPS_SIGN of the GPS_SIGN pin	GLO_I0_B of the VI0_R0 pin GLO_I1_B of the VI0_R1 pin GLO_Q0_B of the VI0_R2 pin GLO_Q1_B of the VI0_R3 pin GLO_RFON_B of the VI0_R7 pin GLO_SCLK_B of the VI0_R4 pin GLO_SDATA_B of the VI0_R5 pin GLO_SS_B of the VI0_R6 pin GPS_CLK_B of the SSI_SCK2 pin GPS_MAG_B of the SSI_SDATA2 pin GPS_SIGN_B of the SSI_WS2 pin	GLO_I0_C of the HCTS0# pin GLO_I1_C of the HRTS0# pin GLO_Q0_C of the HSCK0 pin GLO_Q1_C of the HRX0 pin GLO_RFON_C of the HSCK1 pin GLO_SCLK_C of the HTX0 pin GLO_SDATA_C of the HRX1 pin GLO_SS_C of the HTX1 pin GPS_CLK_C of the IRQ7 pin GPS_MAG_C of the IRQ9 pin GPS_SIGN_C of the IRQ8 pin	GLO_I0_D of the SSI_SCK1 pin GLO_I1_D of the SSI_WS1 pin GLO_Q0_D of the SSI_SCK2 pin GLO_Q1_D of the SSI_WS2 pin GLO_RFON_D of the SSI_WS4 pin GLO_SCLK_D of the SSI_SCK9 pin GLO_SDATA_D of the SSI_WS9 pin GLO_SS_D of the SSI_SCK4 pin GPS_CLK_D of the IRQ7 pin GPS_MAG_D of the IRQ9 pin GPS_SIGN_D of the IRQ8 pin	—	—
sel_scifa4 [1:0]	SCIFA4_RXD of the VI0_FIELD pin SCIFA4_TXD of the VI0_CLKENB pin	SCIFA4_RXD_B of the VI1_VSYNC# pin SCIFA4_TXD_B of the VI1_HSYNC# pin	SCIFA4_RXD_C of the GPS_MAG pin SCIFA4_TXD_C of the GPS_SIGN pin	—	—	—
sel_scifa3 [1:0]	SCIFA3_RXD of the DU1_DB6 pin SCIFA3_SCK of the DU1_DB7 pin SCIFA3_TXD of the DU1_DB5 pin	SCIFA3_RXD_B of the ETH_REFCLK pin SCIFA3_SCK_B of the VI0_DATA3_VI0_B3 pin SCIFA3_TXD_B of the ETH_TXD1 pin	SCIFA3_RXD_C of the GPS_SIGN pin SCIFA3_SCK_C of the GPS_MAG pin SCIFA3_TXD_C of the GPS_CLK pin	—	—	—
sel_sim	SIM0_RST of the SIM0_RST pin SIM0_D of the SIM0_D pin	SIM0_RST_B of the SD0_CD pin SIM0_D_B of the SD0_WP pin	—	—	—	—
sel_ssi8	SSI_SDATA8 of the SSI_SDATA8 pin	SSI_SDATA8_B of the DU1_DG5 pin	—	—	—	—

Legend: – Setting prohibited

Note: * Using SCIFA2_SCK is regardless of value of the bit sel_scifa2.

5.3.29 Module Select Register 3 (MOD_SEL3)

Function: MOD_SEL3 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the SCIF, RCAN, I2C, IIC, IEBUS and MMC is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. When ssi8 (in MOD_SEL2 register) and ssi7 (in MOD_SEL register) are to be used simultaneously, the values of sel_ssi8 and sel_ssi7 must be the same so that the selected pins belong to the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	sel_ hscif2_1	sel_ hscif2_0	sel_can clk_1	sel_can clk_0	sel_ iic1_1	sel_ iic1_0	sel_ iic0_1	sel_ iic0_0	sel_ i2c4_1	sel_ i2c4_0	sel_ i2c3_1	sel_ i2c3_0	sel_ scif3_1	sel_ scif3_0	sel_ ieb_1	sel_ ieb_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_ mmc	sel_ scif5	—	—	sel_ i2c2_1	sel_ i2c2_0	sel_ i2c1_2	sel_ i2c1_1	sel_ i2c1_0	sel_ i2c0_1	sel_ i2c0_0	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_hscif2[1:0]	HCTS2# of the VI0_G0 pin HRTS2# of the VI0_G1 pin HRX2 of the VI0_G3 pin HSCK2 of the VI0_G2 pin HTX2 of the VI0_G4 pin	HCTS2#_B of the WE0# pin HRTS2#_B of the EX_WAIT0 pin HRX2_B of the RD_WR# pin HTX2_B of the WE1# pin	HRX2_C of the SSI_SCK0129 pin HSCK2_C of the SPEEDIN pin HTX2_C of the SSI_WS0129 pin	HTX2_D of the SPEEDIN pin HRX2_D of the RD_WR# pin	—
sel_canclk[1:0]	CAN_CLK of the HSCK0 pin	CAN_CLK_B of the ETH_TX_EN pin	CAN_CLK_C of the SIM0_CLK pin	CAN_CLK_D of the IRQ9 pin	—
sel_iic1[1:0] (iic8)	IIC1_SCL of the VI0_G0 pin IIC1_SDA of the VI0_G1 pin	IIC1_SCL_B of the SSI_WS1 pin IIC1_SDA_B of the SSI_SDATA1 pin	IIC1_SCL_C of the SD3_CD pin IIC1_SDA_C of the SD3_WP pin	—	—
sel_iic0[1:0] (iic7)	IIC0_SCL of the ETH_RX_ER pin IIC0_SDA of the ETH_RXD0 pin	IIC0_SCL_B of the SSI_SDATA0 pin IIC0_SDA_B of the SSI_SCK1 pin	IIC0_SCL_C of the MSIOF0_SS1 pin IIC0_SDA_C of the MSIOF0_SS2 pin	—	—
sel_i2c4[1:0]	I2C4_SCL of the VI0_G0 pin I2C4_SDA of the VI0_G1 pin	I2C4_SCL_B of the VI0_R6 pin I2C4_SDA_B of the VI0_R7 pin	I2C4_SCL_C of the IRQ3 pin I2C4_SDA_C of the IRQ4 pin	—	—
sel_i2c3[1:0]	I2C3_SCL of the ETH_RX_ER pin I2C3_SDA of the ETH_RXD0 pin	I2C3_SCL_B of the VI0_G2 pin I2C3_SDA_B of the VI0_G3 pin	I2C3_SCL_C of the DU1_DB6 pin I2C3_SDA_C of the DU1_DB7 pin	I2C3_SCL_D of the A11 pin I2C3_SDA_D of the A12 pin	—
sel_scif3[1:0]	RX3 of the DU1_DB6 pin SCIF3_SCK of the DU1_DB7 pin TX3 of the DU1_DB5 pin	RX3_B of the DU1_EXODDF_ DU1_ODDF_DISP_CDE pin SCIF3_SCK_B of the VI0_DATA3_VI0_B3 pin TX3_B of the DU1_DOTCLKOUT1 pin	RX3_C of the SD0_WP pin TX3_C of the SD0_CD pin	RX3_D of the SSI_SDATA9 pin TX3_D of the SSI_WS9 pin	—
sel_ieb[1:0]	IECLK of the SIM0_CLK pin IERX of the SIM0_D pin IETX of the SIM0_RST pin	IECLK_B of the SD2_DATA2 pin IERX_B of the SD2_DATA3 pin IETX_B of the SD2_DATA1 pin	IECLK_C of the ETH_TXD0 pin IERX_C of the ETH_MDC pin IETX_C of the ETH_MAGIC pin	—	—

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_mmc	MMC_D6 of the MSIOF0_SS1 pin MMC_D7 of the MSIOF0_SS2 pin	MMC_D6_B of the SD0_CD pin MMC_D7_B of the SD0_WP pin	—	—	—
sel_scif5	RX5 of the VI0_VSYNC# pin TX5 of the VI0_HSYNC# pin	RX5_B of the SD3_WP pin TX5_B of the SD3_CD pin	—	—	—
sel_i2c2[1:0]	I2C2_SCL of the SSI_SCK2 pin I2C2_SDA of the SSI_WS2 pin	I2C2_SCL_B of the DU1_DOTCLKOUT1 pin I2C2_SDA_B of the DU1_EXODDF_ DU1_ODDF_DISP_CDE pin	I2C2_SCL_C of the ETH_MDIO pin I2C2_SDA_C of the ETH_CRS_DV pin	I2C2_SCL_D of the ETH_RXD1 pin I2C2_SDA_D of the ETH_LINK pin	—
sel_i2c1[2:0]	I2C1_SCL of the CS0# pin I2C1_SDA of the CS1#/A26 pin	I2C1_SCL_B of the SSI_WS1 pin I2C1_SDA_B of the SSI_SDATA1 pin	I2C1_SCL_C of the SD2_CD pin I2C1_SDA_C of the SD2_WP pin	I2C1_SCL_D of the VI0_R4 pin I2C1_SDA_D of the VI0_R5 pin	I2C1_SCL_E of the IRQ5 pin I2C1_SDA_E of the IRQ6 pin
sel_i2c0[1:0]	I2C0_SCL of the A8 pin I2C0_SDA of the A9 pin	I2C0_SCL_B of the SSI_SDATA0 pin I2C0_SDA_B of the SSI_SCK1 pin	I2C0_SCL_C of the A0 pin I2C0_SDA_C of the A17 pin	—	—

Legend: – Setting prohibited

5.3.30 Module Select Register 4 (MOD_SEL4)

Function: MOD_SEL4 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the MSIOF, HSCIF, DU, GYRO-ADC, SSI, SSP and IR Receiver is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	sel_sof1_2	sel_sof1_1	sel_sof1_0	sel_hscif0_	sel_hscif0_	sel_dis_1	sel_dis_0	—	sel_rad	sel_rcn	sel_rsp	sel_scif2_2	sel_scif2_1	sel_scif2_0	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	sel_sof2_2	sel_sof2_1	sel_sof2_0	—	sel_ssi1	sel_ssi0	sel_ssp_1	sel_ssp_0	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_sof1[2:0]	MSIOF1_RXD of the A11 pin MSIOF1_SCK of the A6 pin MSIOF1_SS1 of the A8 pin MSIOF1_SS2 of the A9 pin MSIOF1_SYNC of the A7 pin MSIOF1_TXD of the A10 pin	MSIOF1_RXD_B of the IRQ8 pin MSIOF1_SCK_B of the AUDIO_CLKB pin MSIOF1_SS1_B of the AUDIO_CLKOUT pin MSIOF1_SS2_B of the IRQ6 pin MSIOF1_SYNC_B of the AUDIO_CLKC pin MSIOF1_TXD_B of the IRQ7 pin	MSIOF1_RXD_C of the SSI_SCK6 pin MSIOF1_SCK_C of the SSI_SCK5 pin MSIOF1_SYNC_C of the SSI_WS5 pin MSIOF1_TXD_C of the SSI_SDATA5 pin	MSIOF1_RXD_D of the A11 pin MSIOF1_SCK_D of the A12 pin MSIOF1_SS1_D of the A13 pin MSIOF1_SYNC_D of the A14 pin MSIOF1_TXD_D of the A10 pin	MSIOF1_RXD_E of the ETH_RXD1 pin MSIOF1_SCK_E of the ETH_LINK pin MSIOF1_SYNC_E of the ETH_REFCLK pin MSIOF1_TXD_E of the ETH_TXD1 pin
sel_hscif0[1:0]	HCTS0# of the HCTS0# pin HRTS0# of the HRTS0# pin HRX0 of the HRX0 pin HSCK0 of the HSCK0 pin HTX0 of the HTX0 pin	HCTS0#_B of the DU1_DG5 pin HRTS0#_B of the DU1_DG6 pin HRX0_B of the DU1_DG4 pin HTX0_B of the DU1_DG7 pin	HRX0_C of the SSI_SCK0129 pin HTX0_C of the SSI_WS0129 pin HSCK0_C of the SPEEDIN pin	—	—
sel_dis[1:0]	DU1_DOTCLKIN of the DU1_DOTCLKIN pin	DU1_DOTCLKIN_B of the IRQ9 pin	DU1_DOTCLKIN_C of the GPS_CLK pin	—	—
sel_rad	ADICHS0 of the MSIOF0_RXD pin ADICHS1 of the MSIOF0_SS1 pin ADICHS2 of the MSIOF0_SS2 pin ADICLK of the MSIOF0_TXD pin ADICS_SAMP of the MSIOF0_SYNC pin ADIDATA of the MSIOF0_SCK pin	ADICHS0_B of the STP_ISEN_0 pin ADICHS1_B of the STP_ISSYNC_0 pin ADICHS2_B of the STP_OPWM_0 pin ADICLK_B of the STP_ISD_0 pin ADICS_SAMP_B of the STP_ISCLK_0 pin ADIDATA_B of the STP_IVCXO27_0 pin	—	—	—
sel_rcn	REMOCON of the DACK0 pin	REMOCON_B of the SD2_CMD pin	—	—	—
sel_rsp	SPEEDIN of the SPEEDIN pin	SPEEDIN_B of the SD2_DATA0 pin	—	—	—
sel_scif2[2:0]	RX2 of the AUDIO_CLKC pin TX2 of the AUDIO_CLKOUT pin	RX2_B of the DU1_DB1 pin TX2_B of the DU1_DB0 pin	RX2_C of the MSIOF0_SCK pin TX2_C of the MSIOF0_SYNC pin	—	RX2_E of the SSI_WS2 pin TX2_E of the SSI_SDATA2 pin

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_sof2[2:0]	MSIOF2_RXD of the EX_CS4# pin MSIOF2_SCK of the EX_CS1# pin MSIOF2_SS1 of the EX_CS5# pin MSIOF2_SS2 of the BS# pin MSIOF2_SYNC of the EX_CS2# pin MSIOF2_TXD of the EX_CS3# pin	MSIOF2_RXD_B of the DU1_DB1 pin MSIOF2_SCK_B of the DU1_DR0 pin MSIOF2_SS1_B of the DU1_DG0 pin MSIOF2_SS2_B of the DU1_DG1 pin MSIOF2_SYNC_B of the DU1_DR1 pin MSIOF2_TXD_B of the DU1_DB0 pin	MSIOF2_RXD_C of the SSI_SDATA1 pin MSIOF2_SCK_C of the SSI_SDATA0 pin MSIOF2_SYNC_C of the SSI_SCK1 pin MSIOF2_TXD_C of the SSI_WS1 pin	MSIOF2_RXD_D of the SSI_SCK6 pin MSIOF2_SCK_D of the SSI_SDATA4 pin MSIOF2_SS1_D of the SSI_SDATA5 pin MSIOF2_SS2_D of the SSI_WS6 pin MSIOF2_SYNC_D of the SSI_SCK5 pin MSIOF2_TXD_D of the SSI_WS5 pin	MSIOF2_RXD_E of the IRQ4 pin MSIOF2_SCK_E of the IRQ5 pin MSIOF2_SYNC_E of the IRQ6 pin MSIOF2_TXD_E of the IRQ3 pin
sel_ssi1	SSI_SCK1 of the SSI_SCK1 pin SSI_SDATA1 of the SSI_SDATA1 pin SSI_WS1 of the SSI_WS1 pin	SSI_SCK1_B of the DU1_DR5 pin SSI_SDATA1_B of the DU1_DR7 pin SSI_WS1_B of the DU1_DR6 pin	—	—	—
sel_ssi0	SSI_SCK0129 of the SSI_SCK0129 pin SSI_SDATA0 of the SSI_SDATA0 pin SSI_WS0129 of the SSI_WS0129 pin	SSI_SCK0129_B of the DU1_DR2 pin SSI_SDATA0_B of the DU1_DR4 pin SSI_WS0129_B of the DU1_DR3 pin	—	—	—
sel_ssp[1:0]	STP_ISCLK_0 of the STP_ISCLK_0 pin STP_ISD_0 of the STP_ISD_0 pin STP_ISEN_0 of the STP_ISEN_0 pin STP_ISSYNC_0 of the STP_ISSYNC_0 pin STP_IVCXO27_0 of the STP_IVCXO27_0 pin STP_OPWM_0 of the STP_OPWM_0 pin	STP_ISCLK_0_B of the SSI_SCK78 pin STP_ISD_0_B of the SSI_WS78 pin STP_ISEN_0_B of the SSI_SDATA7 pin STP_ISSYNC_0_B of the SSI_SDATA8 pin STP_IVCXO27_0_B of the SSI_SDATA6 pin STP_OPWM_0_B of the AUDIO_CLKB pin	STP_ISCLK_0_C of the VI0_G1 pin STP_ISD_0_C of the VI0_G2 pin STP_ISEN_0_C of the VI0_G3 pin STP_ISSYNC_0_C of the VI0_G4 pin STP_IVCXO27_0_C of the VI0_G0 pin STP_OPWM_0_C of the VI0_G5 pin	—	—

Legend: – Setting prohibited

5.3.31 LSI Pin Pull-Up Control Register 0 (PUPR0)

Function: PUPR0 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR0 [31]	PUPR0 [30]	PUPR0 [29]	PUPR0 [28]	PUPR0 [27]	PUPR0 [26]	PUPR0 [25]	PUPR0 [24]	PUPR0 [23]	PUPR0 [22]	PUPR0 [21]	PUPR0 [20]	PUPR0 [19]	PUPR0 [18]	PUPR0 [17]	PUPR0 [16]
Initial value:	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR0 [15]	PUPR0 [14]	PUPR0 [13]	PUPR0 [12]	PUPR0 [11]	PUPR0 [10]	PUPR0 [9]	PUPR0 [8]	PUPR0 [7]	PUPR0 [6]	PUPR0 [5]	PUPR0 [4]	PUPR0 [3]	PUPR0 [2]	PUPR0 [1]	PUPR0 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR0[31:0]	H'D87F FFFF	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR0[31]	A9 pin is pulled up
PUPR0[30]	A8 pin is pulled up
PUPR0[29]	A7 pin is pulled up
PUPR0[28]	A6 pin is pulled up
PUPR0[27]	A5 pin is pulled up
PUPR0[26]	A4 pin is pulled up
PUPR0[25]	A3 pin is pulled up
PUPR0[24]	A2 pin is pulled up
PUPR0[23]	A1 pin is pulled up
PUPR0[22]	A0 pin is pulled up
PUPR0[21]	D15 pin is pulled up
PUPR0[20]	D14 pin is pulled up
PUPR0[19]	D13 pin is pulled up
PUPR0[18]	D12 pin is pulled up
PUPR0[17]	D11 pin is pulled up
PUPR0[16]	D10 pin is pulled up
PUPR0[15]	D9 pin is pulled up
PUPR0[14]	D8 pin is pulled up
PUPR0[13]	D7 pin is pulled up
PUPR0[12]	D6 pin is pulled up
PUPR0[11]	D5 pin is pulled up
PUPR0[10]	D4 pin is pulled up
PUPR0[9]	D3 pin is pulled up
PUPR0[8]	D2 pin is pulled up
PUPR0[7]	D1 pin is pulled up

Bit Name	Set Value = 1
PUPR0[6]	D0 pin is pulled up
PUPR0[5]	DU0_DOTCLKIN pin is pulled up
PUPR0[4]	A24 pin is pulled up
PUPR0[3]	A23 pin is pulled up
PUPR0[2]	A22 pin is pulled up
PUPR0[1]	A21 pin is pulled up
PUPR0[0]	A20 pin is pulled up

5.3.32 LSI Pin Pull-Up Control Register 1 (PUPR1)

Function: PUPR1 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR1 [31]	PUPR1 [30]	PUPR1 [29]	PUPR1 [28]	PUPR1 [27]	PUPR1 [26]	PUPR1 [25]	PUPR1 [24]	PUPR1 [23]	PUPR1 [22]	PUPR1 [21]	PUPR1 [20]	PUPR1 [19]	PUPR1 [18]	PUPR1 [17]	PUPR1 [16]
Initial value:	1	1	1	0	1	1	0	0	1	0	0	0	1	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR1 [15]	PUPR1 [14]	PUPR1 [13]	PUPR1 [12]	PUPR1 [11]	PUPR1 [10]	PUPR1 [9]	PUPR1 [8]	PUPR1 [7]	PUPR1 [6]	PUPR1 [5]	PUPR1 [4]	PUPR1 [3]	PUPR1 [2]	PUPR1 [1]	PUPR1 [0]
Initial value:	0	1	1	1	1	1	0	1	1	1	0	0	0	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR1[31:0]	H'EC8B 7DC6	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR1[31]	SSI_WS0129 pin is pulled up
PUPR1[30]	SSI_SCK0129 pin is pulled up
PUPR1[29]	SPEEDIN pin is pulled up
PUPR1[28]	DACK0 pin is pulled up
PUPR1[27]	DREQ0 pin is pulled up
PUPR1[26]	EX_WAIT0 pin is pulled up
PUPR1[25]	WE1# pin is pulled up
PUPR1[24]	WE0# pin is pulled up
PUPR1[23]	RD/WR# pin is pulled up
PUPR1[22]	RD# pin is pulled up
PUPR1[21]	BS# pin is pulled up
PUPR1[20]	EX_CS5# pin is pulled up
PUPR1[19]	EX_CS4# pin is pulled up
PUPR1[18]	EX_CS3# pin is pulled up
PUPR1[17]	EX_CS2# pin is pulled up
PUPR1[16]	EX_CS1# pin is pulled up
PUPR1[15]	EX_CS0# pin is pulled up
PUPR1[14]	CS1#/A26 pin is pulled up
PUPR1[13]	TDI pin is pulled up
PUPR1[12]	TMS pin is pulled up
PUPR1[11]	TCK pin is pulled up
PUPR1[10]	TRST# pin is pulled up
PUPR1[9]	A19 pin is pulled up
PUPR1[8]	A18 pin is pulled up
PUPR1[7]	A17 pin is pulled up

Bit Name	Set Value = 1
PUPR1[6]	A16 pin is pulled up
PUPR1[5]	A15 pin is pulled up
PUPR1[4]	A14 pin is pulled up
PUPR1[3]	A13 pin is pulled up
PUPR1[2]	A12 pin is pulled up
PUPR1[1]	A11 pin is pulled up
PUPR1[0]	A10 pin is pulled up

5.3.33 LSI Pin Pull-Up Control Register 2 (PUPR2)

Function: PUPR2 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR2 [31]	PUPR2 [30]	PUPR2 [29]	PUPR2 [28]	PUPR2 [27]	PUPR2 [26]	PUPR2 [25]	PUPR2 [24]	PUPR2 [23]	PUPR2 [22]	PUPR2 [21]	PUPR2 [20]	PUPR2 [19]	PUPR2 [18]	PUPR2 [17]	PUPR2 [16]
Initial value:	1	1	0	1	1	1	1	0	0	1	1	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR2 [15]	PUPR2 [14]	PUPR2 [13]	PUPR2 [12]	PUPR2 [11]	PUPR2 [10]	PUPR2 [9]	PUPR2 [8]	PUPR2 [7]	PUPR2 [6]	PUPR2 [5]	PUPR2 [4]	PUPR2 [3]	PUPR2 [2]	PUPR2 [1]	PUPR2 [0]
Initial value:	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR2[31:0]	H'DE61 F3FF	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR2[31]	IRQ1 pin is pulled up
PUPR2[30]	IRQ0 pin is pulled up
PUPR2[29]	AUDIO_CLKOUT pin is pulled up
PUPR2[28]	AUDIO_CLKC pin is pulled up
PUPR2[27]	AUDIO_CLKB pin is pulled up
PUPR2[26]	AUDIO_CLKA pin is pulled up
PUPR2[25]	SSI_SDATA9 pin is pulled up
PUPR2[24]	SSI_WS9 pin is pulled up
PUPR2[23]	SSI_SCK9 pin is pulled up
PUPR2[22]	SSI_SDATA8 pin is pulled up
PUPR2[21]	SSI_SDATA7 pin is pulled up
PUPR2[20]	SSI_WS78 pin is pulled up
PUPR2[19]	SSI_SCK78 pin is pulled up
PUPR2[18]	SSI_SDATA6 pin is pulled up
PUPR2[17]	SSI_WS6 pin is pulled up
PUPR2[16]	SSI_SCK6 pin is pulled up
PUPR2[15]	SSI_SDATA5 pin is pulled up
PUPR2[14]	SSI_WS5 pin is pulled up
PUPR2[13]	SSI_SCK5 pin is pulled up
PUPR2[12]	SSI_SDATA4 pin is pulled up
PUPR2[11]	SSI_WS4 pin is pulled up
PUPR2[10]	SSI_SCK4 pin is pulled up
PUPR2[9]	SSI_SDATA3 pin is pulled up
PUPR2[8]	SSI_WS34 pin is pulled up
PUPR2[7]	SSI_SCK34 pin is pulled up

Bit Name	Set Value = 1
PUPR2[6]	SSI_SDATA2 pin is pulled up
PUPR2[5]	SSI_WS2 pin is pulled up
PUPR2[4]	SSI_SCK2 pin is pulled up
PUPR2[3]	SSI_SDATA1 pin is pulled up
PUPR2[2]	SSI_WS1 pin is pulled up
PUPR2[1]	SSI_SCK1 pin is pulled up
PUPR2[0]	SSI_SDATA0 pin is pulled up

5.3.34 LSI Pin Pull-Up Control Register 3 (PUPR3)

Function: PUPR3 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR3 [31]	PUPR3 [30]	PUPR3 [29]	PUPR3 [28]	PUPR3 [27]	PUPR3 [26]	PUPR3 [25]	PUPR3 [24]	PUPR3 [23]	PUPR3 [22]	PUPR3 [21]	PUPR3 [20]	PUPR3 [19]	PUPR3 [18]	PUPR3 [17]	PUPR3 [16]
Initial value:	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR3 [15]	PUPR3 [14]	PUPR3 [13]	PUPR3 [12]	PUPR3 [11]	PUPR3 [10]	PUPR3 [9]	PUPR3 [8]	PUPR3 [7]	PUPR3 [6]	PUPR3 [5]	PUPR3 [4]	PUPR3 [3]	PUPR3 [2]	PUPR3 [1]	PUPR3 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR3[31:0]	H'DFFF FFFF	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR3[31]	DU1_DB7
PUPR3[30]	DU1_DB6
PUPR3[29]	DU1_DB5
PUPR3[28]	DU1_DB4 pin is pulled up
PUPR3[27]	DU1_DB3 pin is pulled up
PUPR3[26]	DU1_DB2 pin is pulled up
PUPR3[25]	DU1_DB1 pin is pulled up
PUPR3[24]	DU1_DB0 pin is pulled up
PUPR3[23]	DU1_DG7 pin is pulled up
PUPR3[22]	DU1_DG6 pin is pulled up
PUPR3[21]	DU1_DG5 pin is pulled up
PUPR3[20]	DU1_DG4 pin is pulled up
PUPR3[19]	DU1_DG3 pin is pulled up
PUPR3[18]	DU1_DG2 pin is pulled up
PUPR3[17]	DU1_DG1 pin is pulled up
PUPR3[16]	DU1_DG0 pin is pulled up
PUPR3[15]	DU1_DR7 pin is pulled up
PUPR3[14]	DU1_DR6 pin is pulled up
PUPR3[13]	DU1_DR5 pin is pulled up
PUPR3[12]	DU1_DR4 pin is pulled up
PUPR3[11]	DU1_DR3 pin is pulled up
PUPR3[10]	DU1_DR2 pin is pulled up
PUPR3[9]	DU1_DR1 pin is pulled up
PUPR3[8]	DU1_DR0 pin is pulled up
PUPR3[7]	IRQ9 pin is pulled up

Bit Name	Set Value = 1
PUPR3[6]	IRQ8 pin is pulled up
PUPR3[5]	IRQ7 pin is pulled up
PUPR3[4]	IRQ6 pin is pulled up
PUPR3[3]	IRQ5 pin is pulled up
PUPR3[2]	IRQ4 pin is pulled up
PUPR3[1]	IRQ3 pin is pulled up
PUPR3[0]	IRQ2 pin is pulled up

5.3.35 LSI Pin Pull-Up Control Register 4 (PUPR4)

Function: PUPR4 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR4 [31]	PUPR4 [30]	PUPR4 [29]	PUPR4 [28]	PUPR4 [27]	PUPR4 [26]	PUPR4 [25]	PUPR4 [24]	PUPR4 [23]	PUPR4 [22]	PUPR4 [21]	PUPR4 [20]	PUPR4 [19]	PUPR4 [18]	PUPR4 [17]	PUPR4 [16]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR4 [15]	PUPR4 [14]	PUPR4 [13]	PUPR4 [12]	PUPR4 [11]	PUPR4 [10]	PUPR4 [9]	PUPR4 [8]	PUPR4 [7]	PUPR4 [6]	PUPR4 [5]	PUPR4 [4]	PUPR4 [3]	PUPR4 [2]	PUPR4 [1]	PUPR4 [0]
Initial value:	1	1	1	1	1	1	1	1	0	0	1	0	0	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR4[31:0]	H'FFFF FF27	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR4[31]	VI0_R2 pin is pulled up
PUPR4[30]	VI0_R1 pin is pulled up
PUPR4[29]	VI0_R0 pin is pulled up
PUPR4[28]	VI0_G7 pin is pulled up
PUPR4[27]	VI0_G6 pin is pulled up
PUPR4[26]	VI0_G5 pin is pulled up
PUPR4[25]	VI0_G4 pin is pulled up
PUPR4[24]	VI0_G3 pin is pulled up
PUPR4[23]	VI0_G2 pin is pulled up
PUPR4[22]	VI0_G1 pin is pulled up
PUPR4[21]	VI0_G0 pin is pulled up
PUPR4[20]	VI0_DATA7_VI0_B7 pin is pulled up
PUPR4[19]	VI0_DATA6_VI0_B6 pin is pulled up
PUPR4[18]	VI0_DATA5_VI0_B5 pin is pulled up
PUPR4[17]	VI0_DATA4_VI0_B4 pin is pulled up
PUPR4[16]	VI0_DATA3_VI0_B3 pin is pulled up
PUPR4[15]	VI0_DATA2_VI0_B2 pin is pulled up
PUPR4[14]	VI0_DATA1_VI0_B1 pin is pulled up
PUPR4[13]	VI0_DATA0_VI0_B0 pin is pulled up
PUPR4[12]	VI0_VSYNC# pin is pulled up
PUPR4[11]	VI0_HSYNC# pin is pulled up
PUPR4[10]	VI0_FIELD pin is pulled up
PUPR4[9]	VI0_CLKENB pin is pulled up
PUPR4[8]	VI0_CLK pin is pulled up
PUPR4[7]	DU1_CDE pin is pulled up

Bit Name	Set Value = 1
PUPR4[6]	DU1_DISP pin is pulled up
PUPR4[5]	DU1_EXODDF_DU1_ODDF_DISP_CDE pin is pulled up
PUPR4[4]	DU1_EXVSYNC_DU1_VSYNC pin is pulled up
PUPR4[3]	DU1_EXHSYNC_DU1_HSYNC pin is pulled up
PUPR4[2]	DU1_DOTCLKOUT1 pin is pulled up
PUPR4[1]	DU1_DOTCLKOUT0 pin is pulled up
PUPR4[0]	DU1_DOTCLKIN pin is pulled up

5.3.36 LSI Pin Pull-Up Control Register 5 (PUPR5)

Function: PUPR5 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR5 [31]	PUPR5 [30]	PUPR5 [29]	PUPR5 [28]	PUPR5 [27]	PUPR5 [26]	PUPR5 [25]	PUPR5 [24]	PUPR5 [23]	PUPR5 [22]	PUPR5 [21]	PUPR5 [20]	PUPR5 [19]	PUPR5 [18]	PUPR5 [17]	PUPR5 [16]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR5 [15]	PUPR5 [14]	PUPR5 [13]	PUPR5 [12]	PUPR5 [11]	PUPR5 [10]	PUPR5 [9]	PUPR5 [8]	PUPR5 [7]	PUPR5 [6]	PUPR5 [5]	PUPR5 [4]	PUPR5 [3]	PUPR5 [2]	PUPR5 [1]	PUPR5 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR5[31:0]	H'FFFF FFE1	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR5[31]	STP_ISCLK_0 pin is pulled up
PUPR5[30]	STP_IVCXO27_0 pin is pulled up
PUPR5[29]	ETH_MDC pin is pulled up
PUPR5[28]	ETH_TXD0 pin is pulled up
PUPR5[27]	ETH_MAGIC pin is pulled up
PUPR5[26]	ETH_TX_EN pin is pulled up
PUPR5[25]	ETH_TXD1 pin is pulled up
PUPR5[24]	ETH_REFCLK pin is pulled up
PUPR5[23]	ETH_LINK pin is pulled up
PUPR5[22]	ETH_RXD1 pin is pulled up
PUPR5[21]	ETH_RXD0 pin is pulled up
PUPR5[20]	ETH_RX_ER pin is pulled up
PUPR5[19]	ETH_CRS_DV pin is pulled up
PUPR5[18]	ETH_MDIO pin is pulled up
PUPR5[17]	VI1_DATA7 pin is pulled up
PUPR5[16]	VI1_DATA6 pin is pulled up
PUPR5[15]	VI1_DATA5 pin is pulled up
PUPR5[14]	VI1_DATA4 pin is pulled up
PUPR5[13]	VI1_DATA3 pin is pulled up
PUPR5[12]	VI1_DATA2 pin is pulled up
PUPR5[11]	VI1_DATA1 pin is pulled up
PUPR5[10]	VI1_DATA0 pin is pulled up
PUPR5[9]	VI1_CLK pin is pulled up
PUPR5[8]	VI1_FIELD pin is pulled up
PUPR5[7]	VI1_CLKENB pin is pulled up

Bit Name	Set Value = 1
PUPR5[6]	VI1_VSYNC# pin is pulled up
PUPR5[5]	VI1_HSYNC# pin is pulled up
PUPR5[4]	VI0_R7 pin is pulled up
PUPR5[3]	VI0_R6 pin is pulled up
PUPR5[2]	VI0_R5 pin is pulled up
PUPR5[1]	VI0_R4 pin is pulled up
PUPR5[0]	VI0_R3 pin is pulled up

5.3.37 LSI Pin Pull-Up Control Register 6 (PUPR6)

Function: PUPR6 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR6 [31]	PUPR6 [30]	PUPR6 [29]	PUPR6 [28]	PUPR6 [27]	PUPR6 [26]	PUPR6 [25]	PUPR6 [24]	PUPR6 [23]	PUPR6 [22]	PUPR6 [21]	PUPR6 [20]	PUPR6 [19]	PUPR6 [18]	PUPR6 [17]	PUPR6 [16]
Initial value:	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR6 [15]	PUPR6 [14]	PUPR6 [13]	PUPR6 [12]	PUPR6 [11]	PUPR6 [10]	PUPR6 [9]	PUPR6 [8]	PUPR6 [7]	PUPR6 [6]	PUPR6 [5]	PUPR6 [4]	PUPR6 [3]	PUPR6 [2]	PUPR6 [1]	PUPR6 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR6[31:0]	H'F000 000F	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR6[31]	MSIOF0_RXD pin is pulled up
PUPR6[30]	MSIOF0_TXD pin is pulled up
PUPR6[29]	MSIOF0_SYNC pin is pulled up
PUPR6[28]	MSIOF0_SCK pin is pulled up
PUPR6[27]	SD3_WP pin is pulled up
PUPR6[26]	SD3_CD pin is pulled up
PUPR6[25]	SD3_DATA3 pin is pulled up
PUPR6[24]	SD3_DATA2 pin is pulled up
PUPR6[23]	SD3_DATA1 pin is pulled up
PUPR6[22]	SD3_DATA0 pin is pulled up
PUPR6[21]	SD3_CMD pin is pulled up
PUPR6[20]	SD3_CLK pin is pulled up
PUPR6[19]	SD2_WP pin is pulled up
PUPR6[18]	SD2_CD pin is pulled up
PUPR6[17]	SD2_DATA3 pin is pulled up
PUPR6[16]	SD2_DATA2 pin is pulled up
PUPR6[15]	SD2_DATA1 pin is pulled up
PUPR6[14]	SD2_DATA0 pin is pulled up
PUPR6[13]	SD2_CMD pin is pulled up
PUPR6[12]	SD2_CLK pin is pulled up
PUPR6[11]	SD0_WP pin is pulled up
PUPR6[10]	SD0_CD pin is pulled up
PUPR6[9]	SD0_DATA3 pin is pulled up
PUPR6[8]	SD0_DATA2 pin is pulled up
PUPR6[7]	SD0_DATA1 pin is pulled up

Bit Name	Set Value = 1
PUPR6[6]	SD0_DATA0 pin is pulled up
PUPR6[5]	SD0_CMD pin is pulled up
PUPR6[4]	SD0_CLK pin is pulled up
PUPR6[3]	STP_OPWM_0 pin is pulled up
PUPR6[2]	STP_ISSYNC_0 pin is pulled up
PUPR6[1]	STP_ISEN_0 pin is pulled up
PUPR6[0]	STP_ISD_0 pin is pulled up

5.3.38 LSI Pin Pull-Up Control Register 7 (PUPR7)

Function: PUPR7 performs on/off control of the pull-up/down* resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR7 [31]	PUPR7 [30]	PUPR7 [29]	PUPR7 [28]	PUPR7 [27]	PUPR7 [26]	PUPR7 [25]	PUPR7 [24]	PUPR7 [23]	PUPR7 [22]	PUPR7 [21]	PUPR7 [20]	PUPR7 [19]*	PUPR7 [18]	PUPR7 [17]	PUPR7 [16]
Initial value:	0	0	0	0	0	0	0	1	0	1	0	1	1	1	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR7 [15]	PUPR7 [14]	PUPR7 [13]	PUPR7 [12]	PUPR7 [11]	PUPR7 [10]	PUPR7 [9]	PUPR7 [8]	PUPR7 [7]	PUPR7 [6]	PUPR7 [5]	PUPR7 [4]	PUPR7 [3]	PUPR7 [2]	PUPR7 [1]	PUPR7 [0]
Initial value:	0	0	0	0	1	1	1	1	1	1	1	1	0	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR7[31:0]*	H'015C 0FF3	R/W	Performs individual on/off control of the pull-up/down* resistor provided in each signal pin of the LSI. 0: Pull-up/down function is disabled. 1: Pull-up/down function is enabled.

Note: * Only PUPR7[19] ASEBRK#/ACK pin is available for pull-down function.

Bit Name	Set Value = 1
PUPR7[31]	—
PUPR7[30]	—
PUPR7[29]	—
PUPR7[28]	—
PUPR7[27]	—
PUPR7[26]	AVS2 pin is pulled up
PUPR7[25]	AVS1 pin is pulled up
PUPR7[24]	USB1_OVC pin is pulled up
PUPR7[23]	USB1_PWEN pin is pulled up
PUPR7[22]	USB0_OVC pin is pulled up
PUPR7[21]	USB0_PWEN pin is pulled up
PUPR7[20]	CS0# pin is pulled up
PUPR7[19]	ASEBRK#/ACK is pulled down
PUPR7[18]	A25 pin is pulled up
PUPR7[17]	—
PUPR7[16]	—
PUPR7[15]	—
PUPR7[14]	HTX1 pin is pulled up
PUPR7[13]	HRX1 pin is pulled up
PUPR7[12]	HTX0 pin is pulled up
PUPR7[11]	HRX0 pin is pulled up
PUPR7[10]	HSCK0 pin is pulled up
PUPR7[9]	HRTS0# pin is pulled up
PUPR7[8]	HCTS0# pin is pulled up

Bit Name	Set Value = 1
PUPR7[7]	GPS_MAG pin is pulled up
PUPR7[6]	GPS_SIGN pin is pulled up
PUPR7[5]	GPS_CLK pin is pulled up
PUPR7[4]	SIM0_D pin is pulled up
PUPR7[3]	SIM0_CLK pin is pulled up
PUPR7[2]	SIM0_RST pin is pulled up
PUPR7[1]	MSIOF0_SS2 pin is pulled up
PUPR7[0]	MSIOF0_SS1 pin is pulled up

5.3.39 SD Control Register 0 (IOCTRL0)

Function: IOCTRL0 controls the driving abilities of pins in use for the SSP and SD0 interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	drv2_stpopwm	drv1_stpopwm	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	drv2_sd0wp	drv1_sd0wp	drv2_sd0cd	drv1_sd0cd	drv2_sd0clk	drv1_sd0clk	drv2_sd0cmd	drv1_sd0cmd	drv2_sd0d3	drv1_sd0d3	drv2_sd0d2	drv1_sd0d2	drv2_sd0d1	drv1_sd0d1	drv2_sd0d0	drv1_sd0d0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	drv2_stpopwm	1	R/W	STP_OPWM_0 Setting.
30	drv1_stpopwm	0	R/W	The value of these bits must be 10.
29 to 16	—	All 0	R/W	—
15	drv2_sd0wp	1	R/W	SD0_WP Setting.
14	drv1_sd0wp	1	R/W	The value of these bits must be 11.
13	drv2_sd0cd	1	R/W	SD0_CD Setting.
12	drv1_sd0cd	1	R/W	The value of these bits must be 11.
11	drv2_sd0clk	1	R/W	SD0_CLK Setting.
10	drv1_sd0clk	1	R/W	The value of these bits must be 11.
9	drv2_sd0cmd	1	R/W	SD0_CMD Setting.
8	drv1_sd0cmd	1	R/W	The value of these bits must be 11.
7	drv2_sd0d3	1	R/W	SD0_DATA3 Setting.
6	drv1_sd0d3	1	R/W	The value of these bits must be 11.
5	drv2_sd0d2	1	R/W	SD0_DATA2 Setting.
4	drv1_sd0d2	1	R/W	The value of these bits must be 11.
3	drv2_sd0d1	1	R/W	SD0_DATA1 Setting.
2	drv1_sd0d1	1	R/W	The value of these bits must be 11.
1	drv2_sd0d0	1	R/W	SD0_DATA0 Setting.
0	drv1_sd0d0	1	R/W	The value of these bits must be 11.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.40 SD Control Register 1 (IOCTRL1)

Function: IOCTRL1 controls the driving abilities of pins in use for the SD2 and SD3 interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	drv2_sd2wp	drv1_sd2wp	drv2_sd2cd	drv1_sd2cd	drv2_sd2clk	drv1_sd2clk	drv2_sd2cmd	drv1_sd2cmd	drv2_sd2d3	drv1_sd2d3	drv2_sd2d2	drv1_sd2d2	drv2_sd2d1	drv1_sd2d1	drv2_sd2d0	drv1_sd2d0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	drv2_sd3wp	drv1_sd3wp	drv2_sd3cd	drv1_sd3cd	drv2_sd3clk	drv1_sd3clk	drv2_sd3cmd	drv1_sd3cmd	drv2_sd3d3	drv1_sd3d3	drv2_sd3d2	drv1_sd3d2	drv2_sd3d1	drv1_sd3d1	drv2_sd3d0	drv1_sd3d0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	drv2_sd2wp	1	R/W	SD2_WP Setting.
30	drv1_sd2wp	1	R/W	The value of these bits must be 11.
29	drv2_sd2cd	1	R/W	SD2_CD Setting.
28	drv1_sd2cd	1	R/W	The value of these bits must be 11.
27	drv2_sd2clk	1	R/W	SD2_CLK Setting.
26	drv1_sd2clk	1	R/W	The value of these bits must be 11.
25	drv2_sd2cmd	1	R/W	SD2_CMD Setting.
24	drv1_sd2cmd	1	R/W	The value of these bits must be 11.
23	drv2_sd2d3	1	R/W	SD2_DATA3 Setting.
22	drv1_sd2d3	1	R/W	The value of these bits must be 11.
21	drv2_sd2d2	1	R/W	SD2_DATA2 Setting.
20	drv1_sd2d2	1	R/W	The value of these bits must be 11.
19	drv2_sd2d1	1	R/W	SD2_DATA1 Setting.
18	drv1_sd2d1	1	R/W	The value of these bits must be 11.
17	drv2_sd2d0	1	R/W	SD2_DATA0 Setting.
16	drv1_sd2d0	1	R/W	The value of these bits must be 11.
15	drv2_sd3wp	1	R/W	SD3_WP Setting.
14	drv1_sd3wp	1	R/W	The value of these bits must be 11.
13	drv2_sd3cd	1	R/W	SD3_CD Setting.
12	drv1_sd3cd	1	R/W	The value of these bits must be 11.
11	drv2_sd3clk	1	R/W	SD3_CLK Setting.
10	drv1_sd3clk	1	R/W	The value of these bits must be 11.
9	drv2_sd3cmd	1	R/W	SD3_CMD Setting.
8	drv1_sd3cmd	1	R/W	The value of these bits must be 11.
7	drv2_sd3d3	1	R/W	SD3_DATA3 Setting.
6	drv1_sd3d3	1	R/W	The value of these bits must be 11.
5	drv2_sd3d2	1	R/W	SD3_DATA2 Setting.
4	drv1_sd3d2	1	R/W	The value of these bits must be 11.
3	drv2_sd3d1	1	R/W	SD3_DATA1 Setting.
2	drv1_sd3d1	1	R/W	The value of these bits must be 11.

Bit	Bit Name	Initial Value	R/W	Description
1	drv2_sd3d0	1	R/W	SD3_DATA0 Setting.
0	drv1_sd3d0	1	R/W	The value of these bits must be 11.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.41 TDSEL Control Register 4 (IOCTRL4)

Function: IOCTRL4 controls the delay of returned clock of in pins of IRQ, DU, Ethernet and SSP interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	irq5_tdsel1	irq5_tdsel0	du1dr0_tdsel1	du1dr0_tdsel0	—	—	—	—	—	—	ethlink_tdsel1	ethlink_tdsel0	stpisclk_tdsel1	stpisclk_tdsel0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R/W	—
13	irq5_tdsel1	0	R/W	IRQ5 Setting:
12	irq5_tdsel0	0	R/W	The value of these bits must be 00.
11	du1dr0_tdsel1	0	R/W	DU1_DR0 Setting:
10	du1dr0_tdsel0	0	R/W	The value of these bits must be 00.
9 to 4	—	All 0	R/W	—
3	ethlink_tdsel1	0	R/W	ETH_LINK Setting:
2	ethlink_tdsel0	0	R/W	The value of these bits must be 00.
1	stpisclk_tdsel1	0	R/W	STP_ISCLK_0 Setting:
0	stpisclk_tdsel0	0	R/W	The value of these bits must be 00.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.42 TDSEL Control Register 5 (IOCTRL5)

Function: IOCTRL5 controls the delay of returned clock in pins of SDHI, LBSC, SSI and ADG interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	audio_tdsel1	audio_tdsel0	ssisck5_tdsel1	ssisck5_tdsel0	ssisdat4_tdsel1	ssisdat4_tdsel0	ssisdat0_tdsel1	ssisdat0_tdsel0	excs1_tdsel1	excs1_tdsel0	sd0tdsel1	sd0tdsel0	sd2tdsel1	sd2tdsel0	sd3tdsel1	sd3tdsel0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	a0_tdsel1	a0_tdsel0	—	—	a12_tdsel1	a12_tdsel0	—	—	—	—	—	—	—	—	a6_tdsel1	a6_tdsel0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	audio_tdsel1	0	R/W	AUDIO_CLKB Setting:
30	audio_tdsel0	0	R/W	The setting value of these bits must be 00.
29	ssisck5_tdsel1	0	R/W	SSI_SCK5 Setting:
28	ssisck5_tdsel0	0	R/W	The setting value of these bits must be 00.
27	ssisdat4_tdsel1	0	R/W	SSI_SDATA4 Setting:
26	ssisdat4_tdsel0	0	R/W	The setting value of these bits must be 00.
25	ssisdat0_tdsel1	0	R/W	SSI_SDATA0 Setting:
24	ssisdat0_tdsel0	0	R/W	The setting value of these bits must be 00.
23	excs1_tdsel1	0	R/W	EX_CS1# Setting:
22	excs1_tdsel0	0	R/W	The setting value of these bits must be 00.
21	sd0tdsel1	0	R/W	SD0_CLK Setting 2:
20	sd0tdsel0	0	R/W	The setting value of these bits must be 00.
19	sd2tdsel1	0	R/W	SD2_CLK Setting 2:
18	sd2tdsel0	0	R/W	The setting value of these bits must be 00.
17	sd3tdsel1	0	R/W	SD3_CLK Setting 2:
16	sd3tdsel0	0	R/W	The setting value of these bits must be 00.
15	a0_tdsel1	0	R/W	A0 Setting:
14	a0_tdsel0	0	R/W	The setting value of these bits must be 00.
13, 12	—	All 0	R/W	—
11	a12_tdsel1	0	R/W	A12 Setting:
10	a12_tdsel0	0	R/W	The setting value of these bits must be 00.
9 to 2	—	All 0	R/W	—
1	a6_tdsel1	0	R/W	A6 Setting:
0	a6_tdsel0	0	R/W	The setting value of these bits must be 00.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.43 SD Control Register 6 (IOCTRL6)

Function: IOCTRL6 controls the IO voltage of pins in use for the SD interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	poc_sd 0clk	poc_sd 0cmd	poc_sd 0dat0	poc_sd 0dat1	poc_sd 0dat2	poc_sd 0dat3	poc_sd 0cd	poc_sd 0wp	poc_sd 2clk	poc_sd 2cmd	poc_sd 2dat0	poc_sd 2dat1	poc_sd 2dat2	poc_sd 2dat3	poc_sd 2cd	poc_sd 2wp
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	poc_sd 3clk	poc_sd 3cmd	poc_sd 3dat0	poc_sd 3dat1	poc_sd 3dat2	poc_sd 3dat3	poc_sd 3cd	poc_sd 3wp	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	poc_sd0clk	1	R/W	Selecting IO voltage for the pin SD0_CLK 0: 1.8 V 1: 3.3 V
30	poc_sd0cmd	1	R/W	Selecting IO voltage for the pin SD0_CMD 0: 1.8 V 1: 3.3 V
29	poc_sd0dat0	1	R/W	Selecting IO voltage for the pin SD0_DATA0 0: 1.8 V 1: 3.3 V
28	poc_sd0dat1	1	R/W	Selecting IO voltage for the pin SD0_DATA1 0: 1.8 V 1: 3.3 V
27	poc_sd0dat2	1	R/W	Selecting IO voltage for the pin SD0_ DATA2 0: 1.8 V 1: 3.3 V
26	poc_sd0dat3	1	R/W	Selecting IO voltage for the pin SD0_ DATA3 0: 1.8 V 1: 3.3 V
25	poc_sd0cd	1	R/W	Selecting IO voltage for the pin SD0_CD 0: 1.8 V 1: 3.3 V
24	poc_sd0wp	1	R/W	Selecting IO voltage for the pin SD0_WP 0: 1.8 V 1: 3.3 V
23	poc_sd2clk	1	R/W	Selecting IO voltage for the pin SD2_CLK 0: 1.8 V 1: 3.3 V
22	poc_sd2cmd	1	R/W	Selecting IO voltage for the pin SD2_CMD 0: 1.8 V 1: 3.3 V
21	poc_sd2dat0	1	R/W	Selecting IO voltage for the pin SD2_DATA0 0: 1.8 V 1: 3.3 V

Bit	Bit Name	Initial Value	R/W	Description
20	poc_sd2dat1	1	R/W	Selecting IO voltage for the pin SD2_DATA1 0: 1.8 V 1: 3.3 V
19	poc_sd2dat2	1	R/W	Selecting IO voltage for the pin SD2_DATA2 0: 1.8 V 1: 3.3 V
18	poc_sd2dat3	1	R/W	Selecting IO voltage for the pin SD2_DATA3 0: 1.8 V 1: 3.3 V
17	poc_sd2cd	1	R/W	Selecting IO voltage for the pin SD2_CD 0: 1.8 V 1: 3.3 V
16	poc_sd2wp	1	R/W	Selecting IO voltage for the pin SD2_WP 0: 1.8 V 1: 3.3 V
15	poc_sd3clk	1	R/W	Selecting IO voltage for the pin SD3_CLK 0: 1.8 V 1: 3.3 V
14	poc_sd3cmd	1	R/W	Selecting IO voltage for the pin SD3_CMD 0: 1.8 V 1: 3.3 V
13	poc_sd3dat0	1	R/W	Selecting IO voltage for the pin SD3_DATA0 0: 1.8 V 1: 3.3 V
12	poc_sd3dat1	1	R/W	Selecting IO voltage for the pin SD3_DATA1 0: 1.8 V 1: 3.3 V
11	poc_sd3dat2	1	R/W	Selecting IO voltage for the pin SD3_DATA2 0: 1.8 V 1: 3.3 V
10	poc_sd3dat3	1	R/W	Selecting IO voltage for the pin SD3_DATA3 0: 1.8 V 1: 3.3 V
9	poc_sd3cd	1	R/W	Selecting IO voltage for the pin SD3_CD 0: 1.8 V 1: 3.3 V
8	poc_sd3wp	1	R/W	Selecting IO voltage for the pin SD3_WP 0: 1.8 V 1: 3.3 V
7 to 0	—	All 0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.44 IIC3 (DVFS) and TDBG IO Cell Control Register (IOCTRL7)

Function: IOCTRL controls the driving abilities of pins in use for the IIC and IIC3 (DVFS) interfaces. This register is internal use and reserved; the value of this register should not be changed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

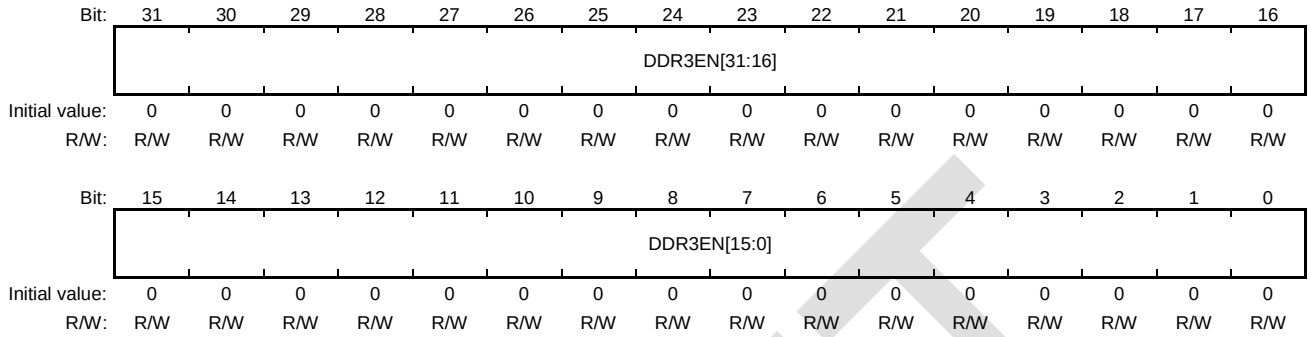
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	gpreg_msel03_p	—	—	—	—	conta_IIC3(DVFS)	contb_IIC3(DVFS)	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R/W	—
12	gpreg_msel03_p	0	R/W	Debug monitor function: 0: Use DU pins for debug monitor function. 1: Use SDHI pins for debug monitor function.
11 to 8	—	All 0	R/W	—
7	conta_IIC3(DVFS)	0	R/W	The setting value of these bits must be 00.
6	contb_IIC3(DVFS)	0	R/W	
5 to 0	—	All 0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.45 DDR3 General Port IO Enable Register (DDR3GPEN)

Function: DDR3GPEN is used to write values to enable DDR3 general port function.

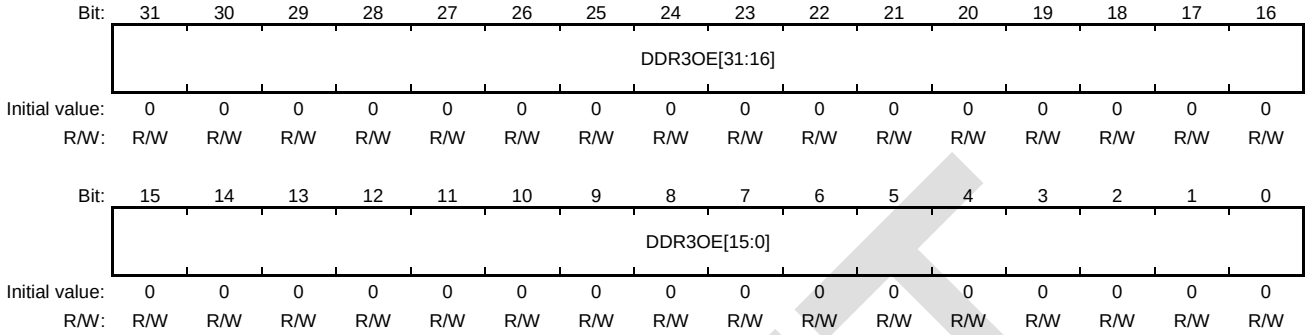


Bit	Bit Name	Initial Value	R/W	Description
31, 30	DDR3EN[31:30]	00	R/W	—
29 to 1	DDR3EN[29:1]	0	R/W	For enabling DDR3 general port function bit 29 to 1: 0: Disabled. 1: Enabled.
0	DDR3EN[0]	0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.46 DDR3 General Port Output Enable Register (DDR3GPOE)

Function: DDR3GPOE is use to enable output of DDR3 general port function.



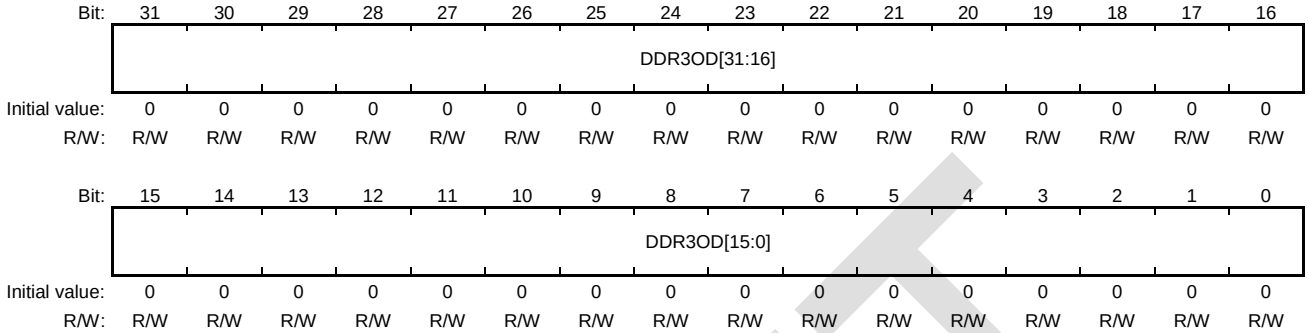
Bit	Bit Name	Initial Value	R/W	Description
31	DDR3OE[31]	0	R/W	—
30	DDR3OE[30]	0	R/W	—
29	DDR3OE[29]	0	R/W	Enabling output of DDR3 general port function bit 29 0: Disabled. 1: Enabled.
28	DDR3OE[28]	0	R/W	—
27	DDR3OE[27]	0	R/W	—
26	DDR3OE[26]	0	R/W	Enabling output of DDR3 general port function bit 26 0: Disabled. 1: Enabled.
25	DDR3OE[25]	0	R/W	—
24	DDR3OE[24]	0	R/W	Enabling output of DDR3 general port function bit 24 0: Disabled. 1: Enabled.
23	DDR3OE[23]	0	R/W	—
22	DDR3OE[22]	0	R/W	—
21	DDR3OE[21]	0	R/W	Enabling output of DDR3 general port function bit 21 0: Disabled. 1: Enabled.
20	DDR3OE[20]	0	R/W	Enabling output of DDR3 general port function bit 20 0: Disabled. 1: Enabled.
19	DDR3OE[19]	0	R/W	Enabling output of DDR3 general port function bit 19 0: Disabled. 1: Enabled.
18	DDR3OE[18]	0	R/W	—
17	DDR3OE[17]	0	R/W	Enabling output of DDR3 general port function bit 17 0: Disabled. 1: Enabled.

Bit	Bit Name	Initial Value	R/W	Description
16	DDR3OE[16]	0	R/W	Enabling output of DDR3 general port function bit 16 0: Disabled. 1: Enabled.
15	DDR3OE[15]	0	R/W	Enabling output of DDR3 general port function bit 15 0: Disabled. 1: Enabled.
14	DDR3OE[14]	0	R/W	—
13	DDR3OE[13]	0	R/W	—
12	DDR3OE[12]	0	R/W	Enabling output of DDR3 general port function bit 12 0: Disabled. 1: Enabled.
11	DDR3OE[11]	0	R/W	Enabling output of DDR3 general port function bit 11 0: Disabled. 1: Enabled.
10	DDR3OE[10]	0	R/W	—
9	DDR3OE[9]	0	R/W	Enabling output of DDR3 general port function bit 9 0: Disabled. 1: Enabled.
8	DDR3OE[8]	0	R/W	—
7	DDR3OE[7]	0	R/W	Enabling output of DDR3 general port function bit 7 0: Disabled. 1: Enabled.
6	DDR3OE[6]	0	R/W	—
5	DDR3OE[5]	0	R/W	—
4	DDR3OE[4]	0	R/W	—
3	DDR3OE[3]	0	R/W	Enabling output of DDR3 general port function bit 3 0: Disabled. 1: Enabled.
2	DDR3OE[2]	0	R/W	Enabling output of DDR3 general port function bit 2 0: Disabled. 1: Enabled.
1	DDR3OE[1]	0	R/W	Enabling output of DDR3 general port function bit 1 0: Disabled. 1: Enabled.
0	DDR3OE[0]	0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.47 DDR3 General Port Output Data Register (DDR3GPOD)

Function: DDR3GPOD is use to write data to DDR3 general port.



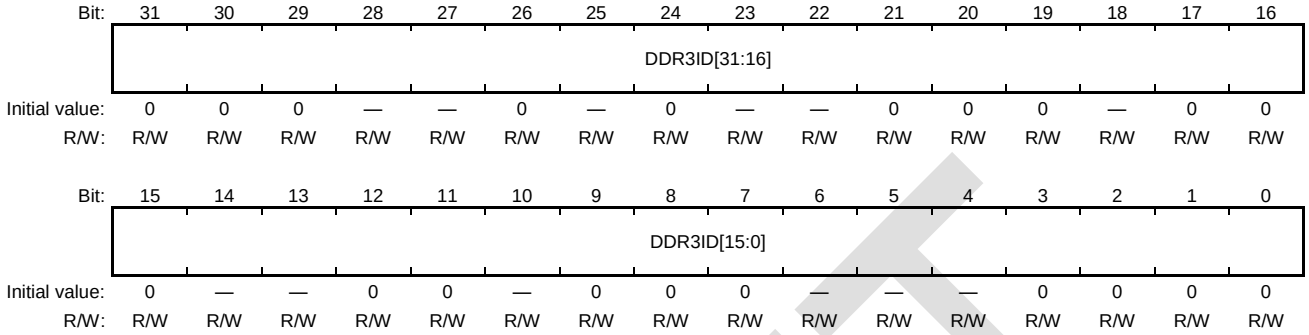
Bit	Bit Name	Initial Value	R/W	Description
31	DDR3OD[31]	0	R/W	—
30	DDR3OD[30]	0	R/W	—
29	DDR3OD[29]	0	R/W	For writing values to DDR3 general port bit 29
28	DDR3OD[28]	0	R/W	—
27	DDR3OD[27]	0	R/W	—
26	DDR3OD[26]	0	R/W	For writing values to DDR3 general port bit 26
25	DDR3OD[25]	0	R/W	—
24	DDR3OD[24]	0	R/W	For writing values to DDR3 general port bit 24
23	DDR3OD[23]	0	R/W	—
22	DDR3OD[22]	0	R/W	—
21	DDR3OD[21]	0	R/W	For writing values to DDR3 general port bit 21
20	DDR3OD[20]	0	R/W	For writing values to DDR3 general port bit 20
19	DDR3OD[19]	0	R/W	For writing values to DDR3 general port bit 19
18	DDR3OD[18]	0	R/W	—
17	DDR3OD[17]	0	R/W	For writing values to DDR3 general port bit 17
16	DDR3OD[16]	0	R/W	For writing values to DDR3 general port bit 16
15	DDR3OD[15]	0	R/W	For writing values to DDR3 general port bit 15
14	DDR3OD[14]	0	R/W	—
13	DDR3OD[13]	0	R/W	—
12	DDR3OD[12]	0	R/W	For writing values to DDR3 general port bit 12
11	DDR3OD[11]	0	R/W	For writing values to DDR3 general port bit 11
10	DDR3OD[10]	0	R/W	—
9	DDR3OD[9]	0	R/W	For writing values to DDR3 general port bit 9
8	DDR3OD[8]	0	R/W	—
7	DDR3OD[7]	0	R/W	For writing values to DDR3 general port bit 7
6	DDR3OD[6]	0	R/W	—
5	DDR3OD[5]	0	R/W	—
4	DDR3OD[4]	0	R/W	—
3	DDR3OD[3]	0	R/W	For writing values to DDR3 general port bit 3
2	DDR3OD[2]	0	R/W	For writing values to DDR3 general port bit 2

Bit	Bit Name	Initial Value	R/W	Description
1	DDR3OD[1]	0	R/W	For writing values to DDR3 general port bit 1
0	DDR3OD[0]	0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.48 DDR3 General Port Input Data Register (DDR3GPID)

Function: DDR3GPID is use to read input data from DDR3 general port.



Bit	Bit Name	Initial Value	R/W	Description
31	DDR3ID[31]	0	R	—
30	DDR3ID[30]	0	R	—
29	DDR3ID[29]	0	R	—
28	DDR3ID[28]	—	R	Indicating values from DDR3 general port bit 28
27	DDR3ID[27]	—	R	Indicating values from DDR3 general port bit 27
26	DDR3ID[26]	0	R	—
25	DDR3ID[25]	—	R	Indicating values from DDR3 general port bit 25
24	DDR3ID[24]	0	R	—
23	DDR3ID[23]	—	R	Indicating values from DDR3 general port bit 23
22	DDR3ID[22]	—	R	Indicating values from DDR3 general port bit 22
21	DDR3ID[21]	0	R	—
20	DDR3ID[20]	0	R	—
19	DDR3ID[19]	0	R	—
18	DDR3ID[18]	—	R	Indicating values from DDR3 general port bit 18
17	DDR3ID[17]	0	R	—
16	DDR3ID[16]	0	R	—
15	DDR3ID[15]	0	R	—
14	DDR3ID[14]	—	R	Indicating values from DDR3 general port bit 14
13	DDR3ID[13]	—	R	Indicating values from DDR3 general port bit 13
12	DDR3ID[12]	0	R	—
11	DDR3ID[11]	0	R	—
10	DDR3ID[10]	—	R	Indicating values from DDR3 general port bit 10
9	DDR3ID[9]	0	R	—
8	DDR3ID[8]	—	R	Indicating values from DDR3 general port bit 8
7	DDR3ID[7]	0	R	—
6	DDR3ID[6]	—	R	Indicating values from DDR3 general port bit 6
5	DDR3ID[5]	—	R	Indicating values from DDR3 general port bit 5
4	DDR3ID[4]	—	R	Indicating values from DDR3 general port bit 4
3	DDR3ID[3]	0	R	—
2	DDR3ID[2]	0	R	—
1	DDR3ID[1]	0	R	—

Bit	Bit Name	Initial Value	R/W	Description
0	DDR3ID[0]	0	R	—

5.4 Operation

5.4.1 Function Setting for Multiplexed Pins

Setting the LSI multiplexed pin setting mask register (PMMR) is necessary before setting each of the GPIO/peripheral function select registers 0 to 7 (GPSR0 to GPSR7) and peripheral function select registers 0 to 16 (IPSR0 to IPSR16). Specifically, the inverse of the value to be set in the select register must be written to the LSI multiplexed pin setting mask register. Otherwise, the GPIO/peripheral function select registers 0 to 7 (GPSR0 to GPSR7) and peripheral function select registers 0 to 16 (IPSR0 to IPSR16) cannot be set.

Note: When GPIO is selected by GPSRn for an LSI pin and one of the below pin functions is selected by IPSRn, make sure to disable data reception of SCIFA3/4/5.

LSI Pin	Pin Function
DU1_DB6	SCIFA3_RXD
ETH_REFCLK	SCIFA3_RXD_B
GPS_MAG	SCIFA4_RXD_C
GPS_SIGN	SCIFA3_RXD_C
SD0_WP	SCIFA5_RXD_B
SD3_WP	SCIFA5_RXD_C
VI0_FIELD	SCIFA4_RXD
VI0_VSYNC#	SCIFA5_RXD
VI1_VSYNC#	SCIFA4_RXD_B

(1) Procedure for changing pin function from GPIO to peripheral function

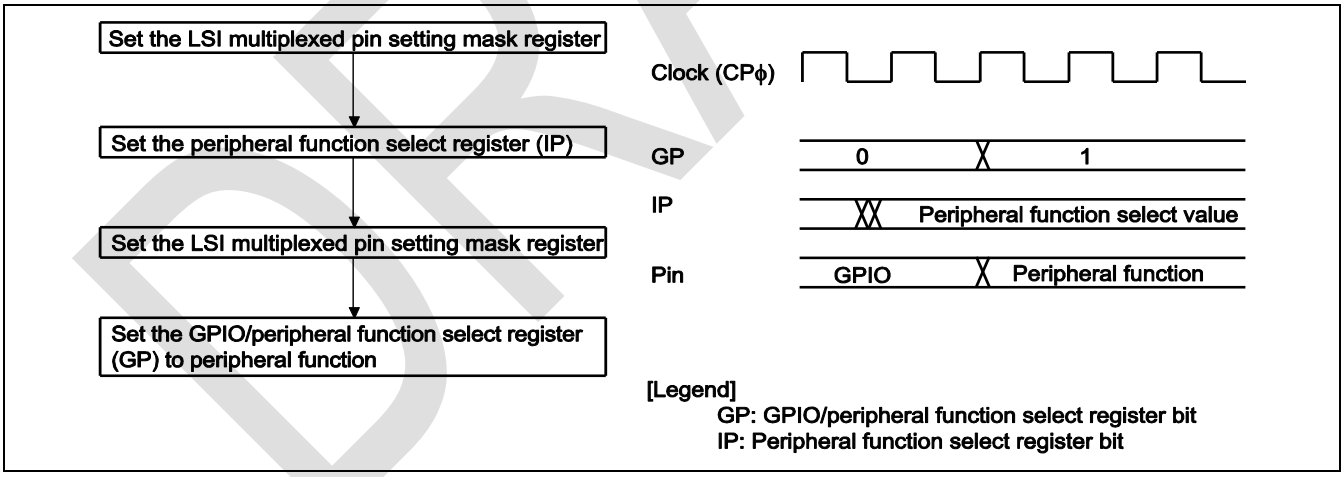


Figure 5.1 Procedure for Changing Pin Function from GPIO to Peripheral Function

(2) Procedure for changing pin function from peripheral function to GPIO

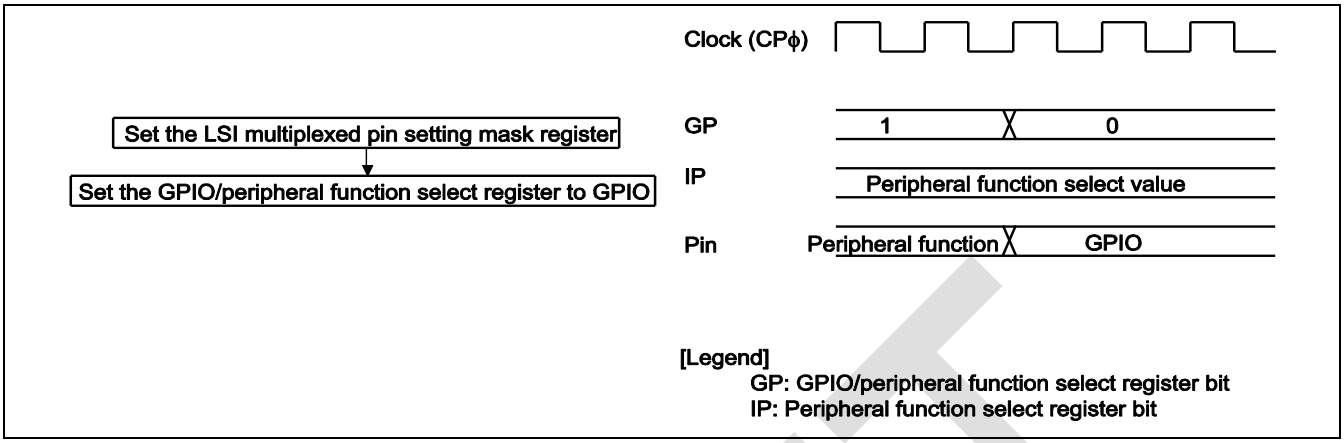


Figure 5.2 Procedure for Changing Pin Function from Peripheral function to GPIO

When changing pin function from peripheral function to GPIO of LSI pin in the below list, make sure to disable the data reception of corresponding SCIFAn channel before performing the sequence in the figure 5.2.

LSI Pin	Pin Function
DU1_DB6	SCIFA3_RXD
ETH_REFCLK	SCIFA3_RXD_B
GPS_MAG	SCIFA4_RXD_C
GPS_SIGN	SCIFA3_RXD_C
SD0_WP	SCIFA5_RXD_B
SD3_WP	SCIFA5_RXD_C
VI0_FIELD	SCIFA4_RXD_
VI0_VSYNC#	SCIFA5_RXD
VI1_VSYNC#	SCIFA4_RXD_B

(3) Procedure 1 for changing pin function from one peripheral function to another peripheral function

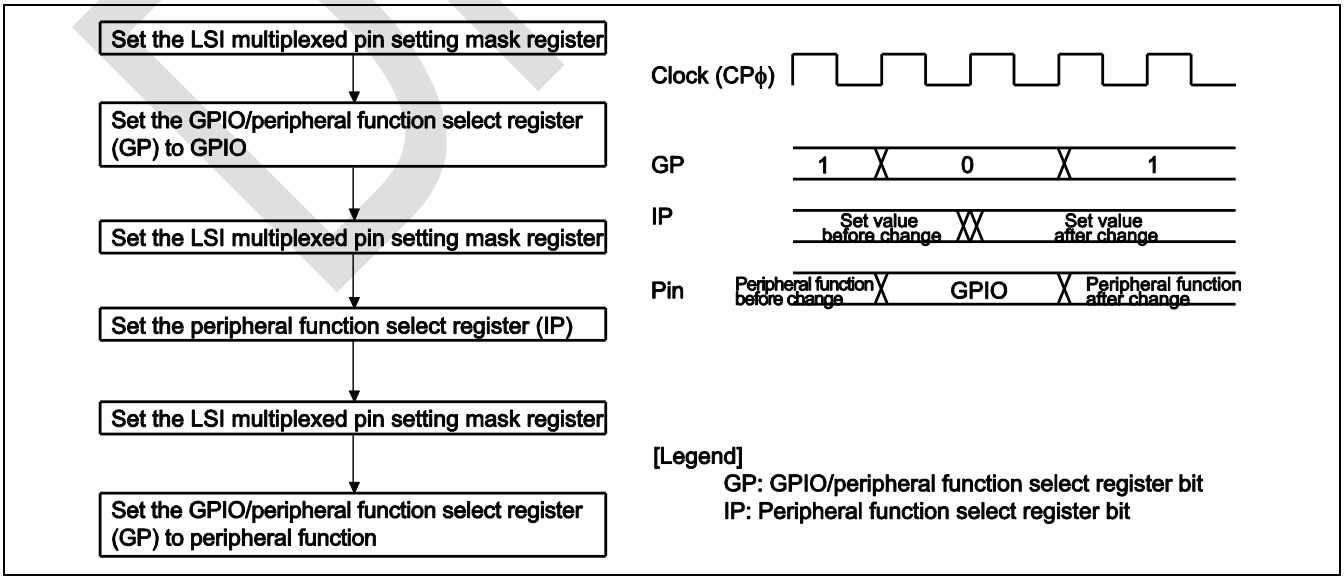


Figure 5.3 Procedure for Changing Pin Function from One Peripheral Function to Another Peripheral Function (with GPIO Setting)

In case that one of the pin function in the following list is selected, make sure to disable the data reception of corresponding SCIFAn channel before performing the sequence in the figure 5.3.

LSI Pin	Pin Function
DU1_DB6	SCIFA3_RXD
ETH_REFCLK	SCIFA3_RXD_B
GPS_MAG	SCIFA4_RXD_C
GPS_SIGN	SCIFA3_RXD_C
SD0_WP	SCIFA5_RXD_B
SD3_WP	SCIFA5_RXD_C
VI0_FIELD	SCIFA4_RXD
VI0_VSYNC#	SCIFA5_RXD
VI1_VSYNC#	SCIFA4_RXD_B

5.4.2 Setting Pull-Up/Down Resistors

The LSI pin pull-up/down control registers 0 to 7 (PUPR0 to PUPR7) are used to switch the pull-up/down resistors on and off.