# PFC Controller with Critical Conduction Mode

## General Description

The RT7313 is an active Power Factor Correction (PFC) controller with critical conduction mode (CRM) operation that is designed to meet line current harmonic regulations for the applications of AC/DC adapters, electronic ballasts and medium off-line power converters (<300W). The CRM and Feed-Forward schemes provide near unity power factor across a wide range of input voltages and output powers.

The totem-pole gate driver with 600mA sourcing current and 800mA sinking current provides powerful driving capability for power MOSFET to improve conversion efficiency. The RT7313 features an extra low start-up current (≤20μA) and supports a disable function to reduce power consumption in standby mode, which makes it easy to comply with energy saving regulations such as Blue Angel, Energy Star and Energy 2000.

This controller integrates comprehensive safety protection functions for robust designs including input under-voltage lockout, output over-voltage protection, under-voltage protection and cycle-by-cycle current limit.

The RT7313 is a cost-effective solution for PFC power converter with minimum external components. It is available in the SOP-8 package.
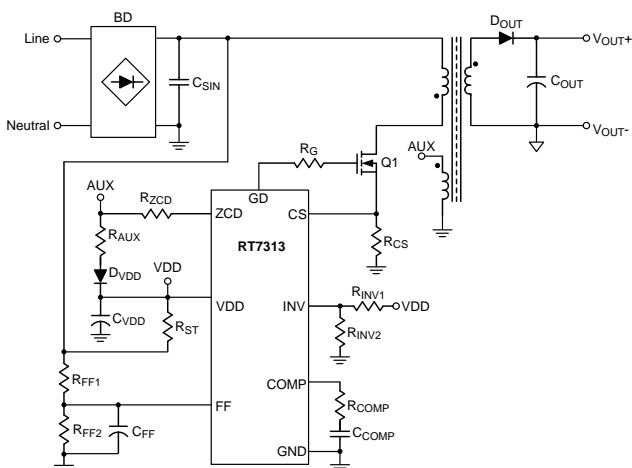
## Features

- **Critical Conduction Mode (CRM) Operation**
- **Constant On-Time Control (Voltage Mode)**
- **Near Unity Power Factor**
- **Ultra Low Start-up Current (≤20μA)**
- **Input Voltage Feed-Forward Compensation**
- **Wide Supply Voltage Range from 12V to 25V**
- **Totem Pole Gate Driver with 600mA−800mA**
- **Maximum Frequency Clamping (120kHz)**
- **DCM THD Optimization**
- **Fast Dynamic Response**
- **Light Load Burst Mode Operation**
- **Disable Function**
- **Maximum/Minimum On-Time Limit**
- **Cycle-by-Cycle Current Limit**
- **Output Over-Voltage Protection (OVP)**
- **Under-Voltage Lockout (UVLO)**
- **RoHS Compliant and Halogen Free**
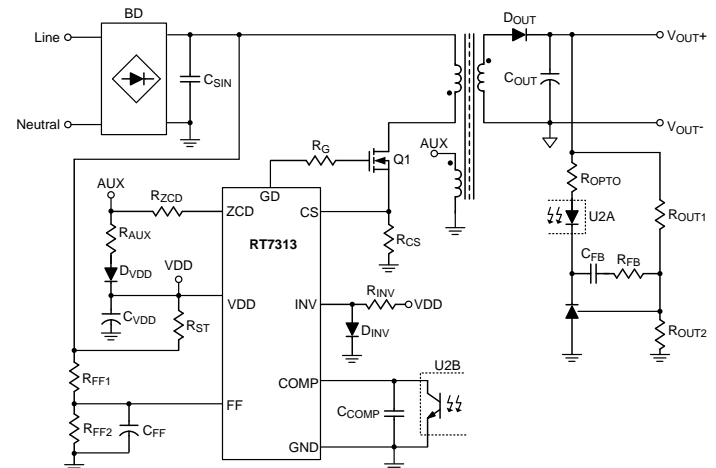
## Applications

- Electrical Lamp Ballast
- LED Lighting
- AC/DC Adapter/Charger for Desktop PC, NB, TV, Monitor, Etc.
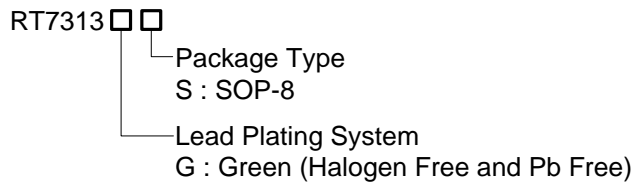- Entry-Level Server, Web Server
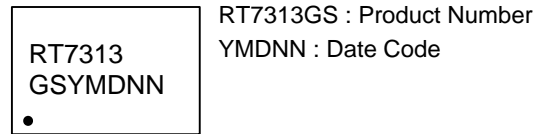
## Simplified Application Circuit

**PSR Converter**



**SSR Converter**

# RT7313

**RICHTEK**
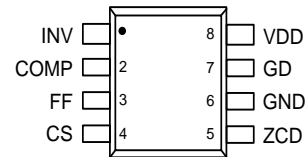
## Ordering Information

RT7313☐☐

  Package Type
  S : SOP-8

  Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

## Marking Information

RT7313
GSYMDNN
●

RT7313GS : Product Number
YMDNN : Date Code

## Pin Configuration

(TOP VIEW)

| INV | 1 | | 8 | VDD |
| COMP | 2 | | 7 | GD |
| FF | 3 | | 6 | GND |
| CS | 4 | | 5 | ZCD |

SOP-8

## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---------|----------|--------------|
| 1 | INV | Inverting input of the internal error amplifier. Connect a resistive divider from output voltage to this pin for voltage feedback. It also used for OVP and UVP detections. |
| 2 | COMP | Output of the internal error amplifier. Connect a compensation network between this pin and GND for dynamic load performance. |
| 3 | FF | Feed-forward input for line voltage. This pin senses the line input voltage via a resistive divider. Connect a suitable capacitor to filter out the line voltage ripple & noise. |
| 4 | CS | Current sense input. The current sense resistor between this pin and GND is used for current limit setting. |
| 5 | ZCD | Zero current detection input. Input from secondary winding of PFC choke for detecting demagnetization timing of PFC choke. This pin also can be used to enable/disable the controller. |
| 6 | GND | Ground of the controller. |
| 7 | GD | Gate driver output for external power MOSFET. |
| 8 | VDD | Supply voltage input. The controller will be enabled when VDD exceeds $V_{ON\_TH}$ (16V typ.) and disabled when VDD decreases lower than $V_{OFF\_TH}$ (9V typ.). |

## Functional Block Diagram

DS7313-01 July 2016
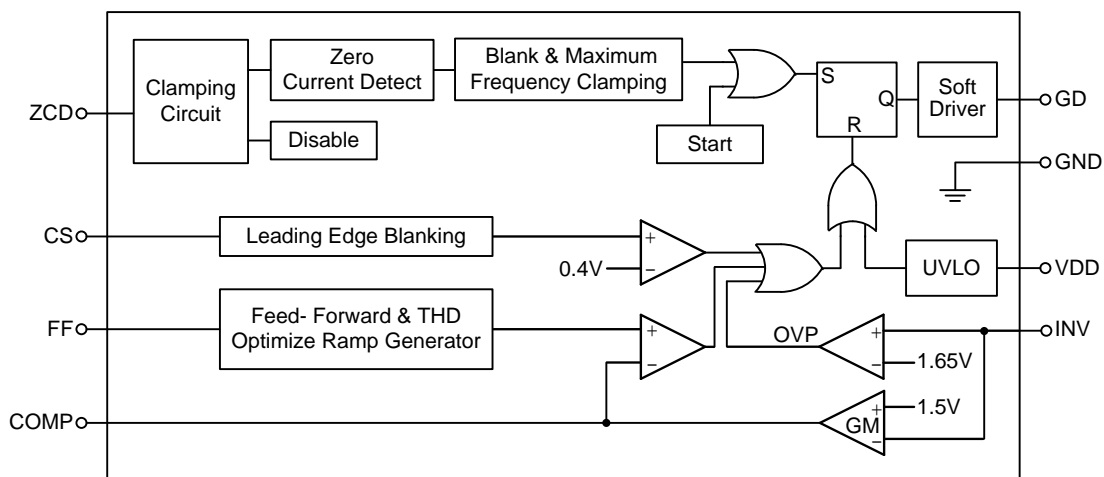
# Operation

## Critical Conduction Mode (CRM)

The Critical Conduction Mode is also called Transition Mode or Boundary Mode. Figure 1 shows the CRM operating at the boundary between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM).

In CRM, the power switch turns on immediately when the inductor current decreases to zero. The CRM is the preferred control method for medium power (<300W) applications due to the features of zero current switching and lower peak current than that in DCM.
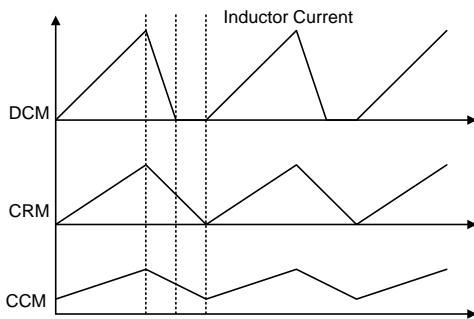


Figure 1. Inductor Current of DCM, CRM and CCM

## Constant On-Time Voltage Mode Control

Figure 2 shows a typical flyback converter. When the MOSFET turns on with a fixed on-time ($t_{ON}$), the inductor current can be calculated by the following equation (1).
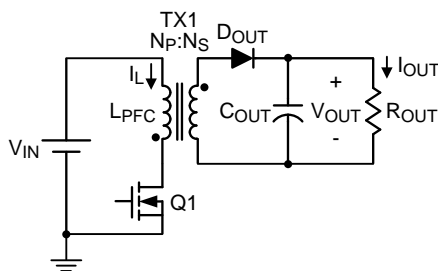


Figure 2. Typical flyback Converter

$$I_{L\_PK} = \frac{V_{IN}}{L_{PFC}} \times t_{ON} \qquad (1)$$

If the input voltage is a sinusoidal waveform and rectified by a bridge rectifier, the inductor current can be expressed with equation (2). When the converter operates in CRM with constant on-time voltage mode

control, the envelope of inductor peak current will follow the input voltage waveform with in-phase. The average inductor current will be half of the peak current shown as Figure 3. Therefore, the near unity power factor is easy to be achieved by this control scheme.

$$I_{L\_pk} \times |\sin\theta| = \frac{V_{IN\_pk} \times |\sin\theta| \times t_{ON}}{L_{PFC}} \qquad (2)$$



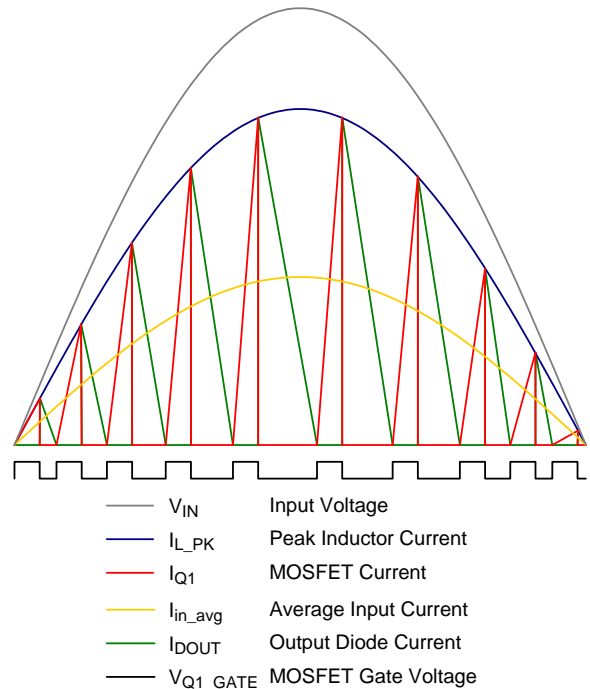| | | |
|---|---|---|
| $V_{IN}$ | Input Voltage |
| $I_{L\_PK}$ | Peak Inductor Current |
| $I_{Q1}$ | MOSFET Current |
| $I_{in\_avg}$ | Average Input Current |
| $I_{DOUT}$ | Output Diode Current |
| $V_{Q1\_GATE}$ | MOSFET Gate Voltage |

Figure 3. Inductor Current of CRM with Constant On-Time Voltage Mode Control

## Under-Voltage Lockout

The controller will be enabled when VDD exceeds $V_{ON\_TH}$ (16V typ.) and disabled when VDD decreases lower than $V_{OFF\_TH}$ (9V typ.).

The maximum VDD voltage is set at 27V typically for over-voltage protection shown as Figure 4. An internal 29V zener diode is also used to avoid over voltage stress for the internal circuits.

When the VDD is available, the precise reference is generated for internal circuitries such as Error Amplifier, Current Sense, OVP, UVP. The internal reference equips with excellent temperature coefficient performance so that the RT7313 can be operated in varied environments.
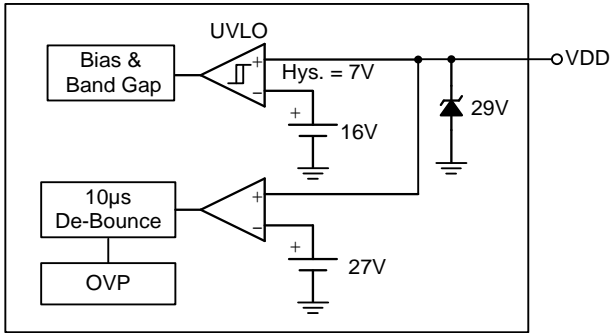
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Figure 4. VDD and UVLO

## Feedback Voltage Detection

Figure 5 shows the feedback voltage detection circuit. The INV pin is the inverting input of the Error Amplifier with 1.5V reference voltage. Over-voltage protection is provided with threshold voltage 1.65V. If the INV voltage is over 1.65V, the gate driver will be disabled to prevent output over voltage condition or feedback open condition. Although the INV is an input pin with high impedance, it is suggested that the bias current of the potential divider should be over 30μA for noise immunity.
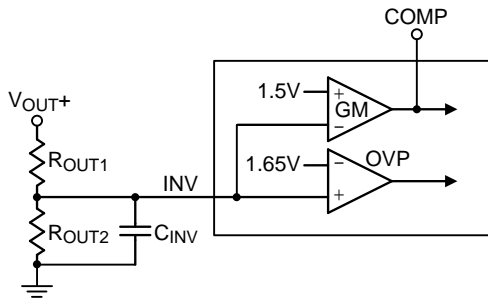


Figure 5. Feedback Voltage Detection

## Transconductance Error Amplifier

The RT7313 implements transconductance error amplifier with non-linear GM design to regulate the Flyback output voltage and provide fast dynamic response. The transconductance value is 100μA/V in normal operation. When the INV voltage increases over 1.65V or decreases under 1.35V, the output of error amplifier will source or sink 1.5mA (typ.) maximum current at COMP pin respectively shown as Figure 6. Thus, the non-linear GM design can provide fast response for the dynamic load of PFC converters even though the bandwidth of control loop is lower than line
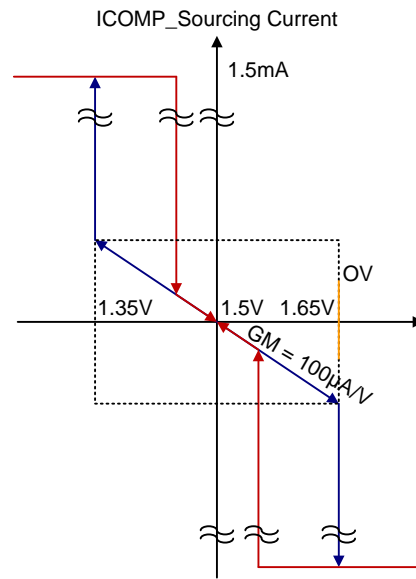
frequency.



Figure 6. Non-linear GM

## Feed-Forward Compensation

The FF pin is an input pin with high impedance to detect the line input voltage shown as Figure 7. A proper voltage divider should be applied to sense the line voltage after bridge diode rectifier. Since the FF voltage is proportional to the line input voltage, it provides a feed-forward signal to compensate the loop bandwidth for high line and low line input conditions.
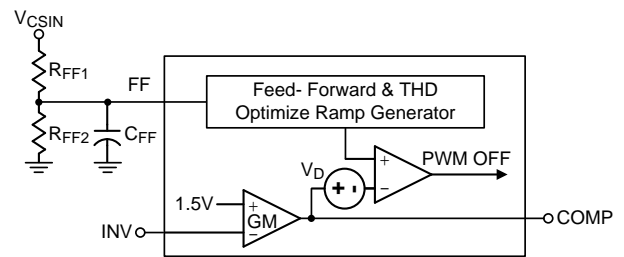


Figure 7. FF Detection Circuit

The constant on-time, $t_{ON}$, can be derived from the following equations.

$$P_{IN} = \frac{1}{4} \times V_{IN\_pk} \times I_{L\_pk} \times \frac{t_{ON}}{t_S} \qquad I_{L\_pk} = \frac{V_{IN\_pk}}{L_{PFC}} \times t_{ON}$$

$$P_{IN} = \frac{1}{4} \times V_{IN\_pk} \times \frac{V_{IN\_pk}}{L_{PFC}} \times t_{ON} \times \frac{t_{ON}}{t_S} = \frac{1}{4} \times \frac{(V_{IN\_pk})^2}{L_{PFC}} \times t_{ON} \times \frac{t_{ON}}{t_S}$$

$$\Rightarrow t_{ON} = \frac{4 \times P_{IN} \times L_{PFC}}{(V_{IN\_pk})^2 \times \left(\frac{t_{ON}}{t_S}\right)} \qquad (3)$$

In RT7313, the $t_{ON}$ is implemented by a constant current charging a capacitor till $V_{COMP}$ threshold voltage is reached. Therefore, the $t_{ON}$ is a function of $V_{COMP}$.

$$t_{ON} = \frac{C_{ramp} \times (V_{COMP} - V_D)}{I_{ramp}} \qquad (4)$$

Then, the $V_{COMP}$ can be derived from equation (3) and (4).

$$\frac{4 \times P_{IN} \times L_{PFC}}{(V_{IN\_pk})^2 \times \left(\frac{t_{ON}}{t_S}\right)} = \frac{C_{ramp} \times (V_{COMP} - V_D)}{I_{ramp}}$$

$$V_{COMP} = \frac{4 \times P_{IN} \times L_{PFC}}{(V_{IN\_pk})^2 \times \left(\frac{t_{ON}}{t_S}\right)} \times \frac{I_{ramp}}{C_{ramp}} + V_D \qquad (5)$$

According to equation (5), the $V_{COMP}$ is reversely proportional to the input voltage so that the $V_{COMP}$ has a large variation for the change of line voltage between high and low input voltages. This variation will impact $t_{ON}$, Burst mode entry level and loop bandwidth.

In order to compensate the variation, the $I_{ramp}$ is designed to be proportional to the input voltage shown as equation (6).

$$I_{ramp}(V_{IN\_pk}) = k \times (V_{FF})^2 \times gm_{ramp} \times \frac{t_{ON}}{t_S}$$

$$= k \times \left[ V_{IN\_RMS} \times \frac{2\sqrt{2}}{\pi} \times \left( \frac{R_{FF2}}{R_{FF1} + R_{FF2}} \right) \right]^2 \times gm_{ramp} \times \frac{t_{ON}}{t_S} \quad (6)$$

$$V_{Comp}(FF) = \frac{8 \times \left( \frac{V_{FF2}}{R_{FF1} + R_{FF2}} \right)^2 \times gm_{ramp} \times P_{IN} \times L_{PFC}}{\pi^2 \times C_{ramp}} + V_D \qquad (7)$$

in which k, $gm_{ramp}$, $C_{ramp}$, and $V_D$ are fixed parameters in the RT7313, and the typical values are : k = 0.5, $gm_{ramp}$ = 10μA/V, $C_{ramp}$ = 4.5pF, and $V_D$ = 1V.

## Ramp Generator

The RT7313 provides constant on-time voltage mode control to achieve near unity power factor for the CRM Flyback converters. Figure 8 shows the Ramp Generator with Feed-Forward compensation and THD optimization circuit for the constant on-time operation.
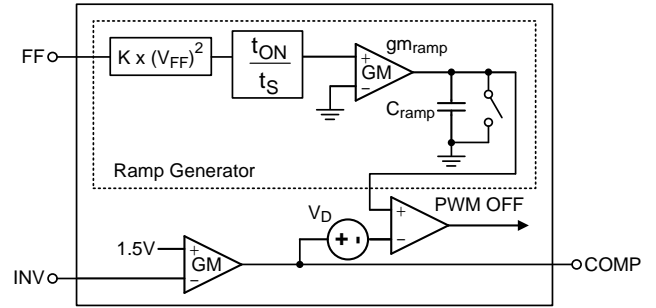


Figure 8. Ramp Generator

The charging current of ramp generator is modulated following the squared FF voltage with line voltage compensation and the THD optimization scheme is implemented to compensate the harmonic distortion.

## ZCD and Enable Function

In CRM operation, when the power switch turns on, the inductor current increases linearly to the peak value. When the power switch turns off, the inductor current decreases linearly to zero. The zero current can be detected by the ZCD pin with the auxiliary winding of Flyback inductor.

Figure 9 and Figure 10 show the ZCD block diagram and related waveforms. The ZCD block diagram provides zero current detection, voltage clamp and shutdown control functions. When the inductor current decreases to zero, the auxiliary winding voltage will turn from high to low. Once the ZCD voltage decreases to the threshold $V_{ZCDT}$ (1V, typ.), the controller will generate a signal for gate driver. The hysteresis voltage between the threshold $V_{ZCDA}$ (1.6V, typ.) and $V_{ZCDT}$ is designed to avoid mis-triggering. In order to prevent over voltage stress, the ZCD pin voltage is clamped at $V_{ZCDH}$ (4.8V, typ.) if the input voltage is too high from the auxiliary winding and the ZCD pin voltage is clamped at $V_{ZCDL}$ (0.6V, typ.) if the input voltage is lower than $V_{ZCDL}$.
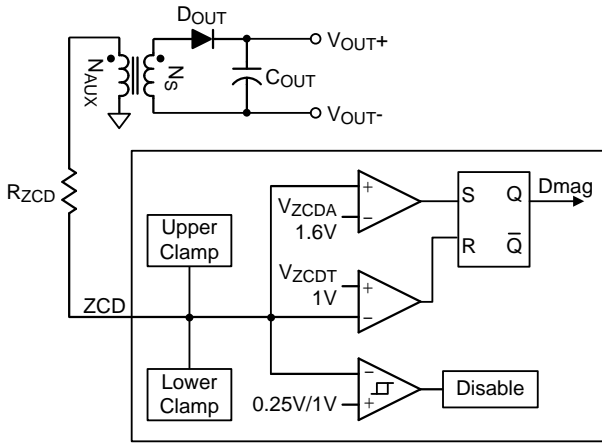
Figure 9.ZCD Block Diagram

The RT7313 provides shutdown function to save power consumption in standby mode. When the ZCD pin is pulled lower than 250mV, the gate driver will be turned off and operate in standby mode with low quiescent current less than 600$\mu$A. Once the ZCD pin is released, the controller will be activated.

The RT7313 also provides ZCD time-out detection function. If the controller runs at maximum frequency and there is no ZCD signal being detected after 4$\mu$s delay time, the PWM will be turned on for ZCD time-out detection.
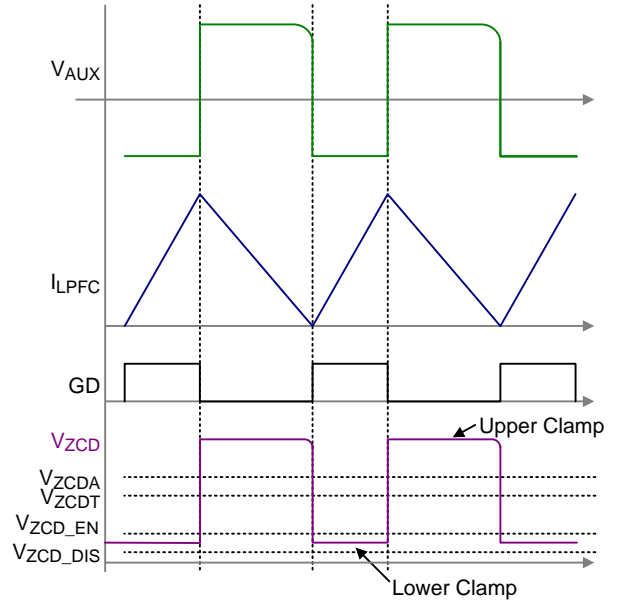


Figure 10. ZCD Related Waveforms.

# Absolute Maximum Ratings    (Note 1)

- Supply Voltage, VDD ------------------------------------------------------------------- −0.3 to 30V
- Gate Driver Output, GD ---------------------------------------------------------------- −0.3V to 20V
- Other Pins ------------------------------------------------------------------------------- −0.3V to 6V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  SOP-8 --------------------------------------------------------------------------------- 0.625W
- Package Thermal Resistance    (Note 2)
  SOP-8, $\theta_{JA}$ ---------------------------------------------------------------------- 160°C/W
- Junction Temperature    ------------------------------------------------------------------ 150°C
- Lead Temperature (Soldering, 10 sec.)------------------------------------------------------ 260°C
- Storage Temperature Range ------------------------------------------------------------ −65°C to 150°C
- ESD Susceptibility    (Note 3)
- HBM (Human Body Model) ------------------------------------------------------------------ 2kV

# Recommended Operating Conditions    (Note 4)

- Supply Voltage, VDD------------------------------------------------------------------------ 12V to 25V
- Junction Temperature Range ------------------------------------------------------------- −40°C to 125°C

# Electrical Characteristics

($V_{DD}$ = 15V, $T_A$ = 25°C, unless otherwise specification)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VDD Section** | | | | | | |
| VDD OVP Threshold Voltage | $V_{OVP}$ | | 25.5 | 27 | 28.5 | V |
| VDD OVP De-bounce Time | | | -- | 10 | -- | μs |
| VDD On Threshold Voltage | $V_{ON\_TH}$ | | 15 | 16 | 17 | V |
| VDD Off Threshold Voltage | $V_{OFF\_TH}$ | | 8 | 9 | 10 | V |
| Operating Supply Current | $I_{DD\_OP}$ | $I_{ZCD}$ = 0, and GD open | -- | -- | 2.5 | mA |
| Quiescent Current | $I_Q$ | At burst mode, and GD open | -- | -- | 1.7 | mA |
| Standby Current | | PFC is disabled | -- | -- | 0.6 | mA |
| Start-Up Current | $I_{DD\_ST}$ | Before $V_{ON\_TH}$ | -- | -- | 20 | μA |
| **ZCD Section** | | | | | | |
| Upper Clamp Voltage | $V_{ZCDH}$ | $I_{ZCD}$ = 2mA | 4.5 | 4.8 | 5.5 | V |
| Delay Time Between Trigger Point and Gate Turn On | | | -- | 100 | 170 | ns |
| Sourcing Current Capability | | | −2.5 | -- | −6.5 | mA |
| Sinking Current Capability | | | 2 | -- | -- | mA |
| Disable Voltage | $V_{ZCD\_DIS}$ | | 250 | 280 | -- | mV |
| Restart Voltage | $V_{ZCD\_EN}$ | | -- | 770 | 1000 | mV |
| Pull-High Current After Disable | | | 30 | 75 | 100 | μA |
| **FF Section** | | | | | | |
| Input Bias Current | $I_{BIAS}$ | Leakage Current of FF Pin | -- | -- | 1 | μA |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **GM Section** | | | | | | |
| Non-Inverting Input Reference | $V_{REF}$ | | 1.47 | 1.5 | 1.53 | V |
| INV Bias Current | | | -- | -- | −1 | μA |
| Transconduction | gm | $|V_{ERROR}| < 0.25V$ | 80 | 100 | 120 | μA/V |
| COMP Maximum Voltage | $V_{COMP\_OP}$ | | 4.25 | -- | -- | V |
| **PWM Section** | | | | | | |
| INV OVP Threshold Voltage | | | 1.55 | 1.65 | 1.75 | V |
| INV OVP De-bounce Time | | | -- | 20 | -- | μs |
| Burst Mode Threshold Voltage | $V_{BURST}$ | Measure at COMP Pin | 0.8 | 0.9 | 1 | V |
| Minimum On-Time | | $t_{ON(MIN)\_PFC}$ = 3pF x 2.5V / ($I_{ZCD}$ x 0.02), $I_{ZCD}$ = 75μA | 4.4 | 5.4 | 6.4 | μs |
| **Current Sense Section** | | | | | | |
| Leading Edge Blanking Time | $t_{LEB\_PFC}$ | LEB + Delay    (Note 6) | 240 | 400 | 570 | ns |
| Current Sense Threshold Voltage | $V_{CS\_PFC}$ | | 0.35 | 0.4 | 0.45 | V |
| **Gate Driver Section** | | | | | | |
| Rising Time | $t_R$ | $C_L$ = 1nF | -- | 40 | 80 | ns |
| Falling Time | $t_F$ | $C_L$ = 1nF | -- | 30 | 70 | ns |
| Gate Output Clamping Voltage | $V_{CLAMP}$ | $V_{DD}$ = 25V | -- | 13 | -- | V |
| Internal Pull Low Resistor | | | -- | 12 | -- | kΩ |
| **Oscillator Section** | | | | | | |
| Valley Mask Time | $t_{MASK}$ | | 7 | 8.5 | 10 | μs |
| Duration of Starter | $t_{START}$ | | 75 | 130 | 300 | μs |
| Maximum On-Time | $t_{ON(MAX)\_PFC}$ | | -- | 50 | -- | μs |

**Note 1.** Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability

**Note 2.** $\theta_{JA}$ is measured under natural convection (still air) at $T_A$ = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard. $\theta_{JC}$ is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended

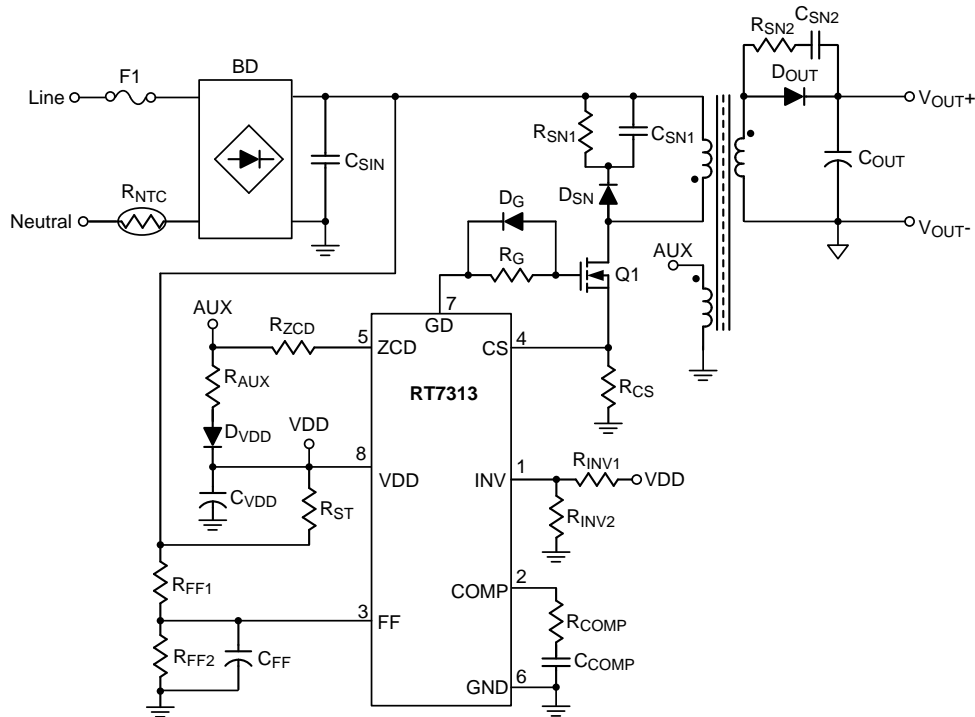**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** Guaranteed by Design.

**Note 6.** Leading edge blanking time and internal propagation delay time is guaranteed by design.
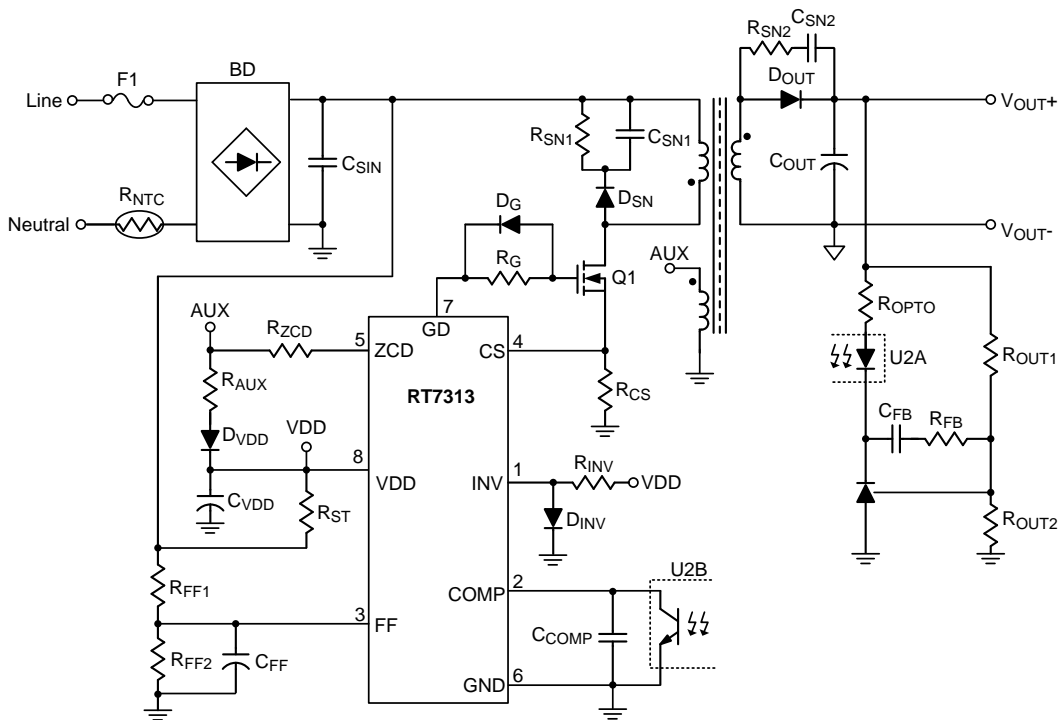
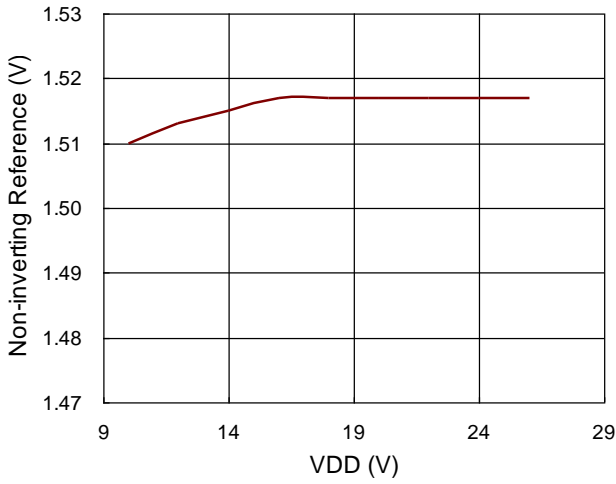## Typical Application Circuit

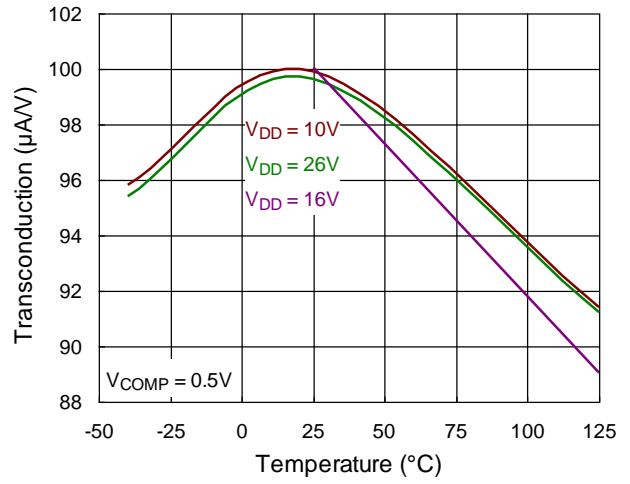**Typical PSR Application Circuit**



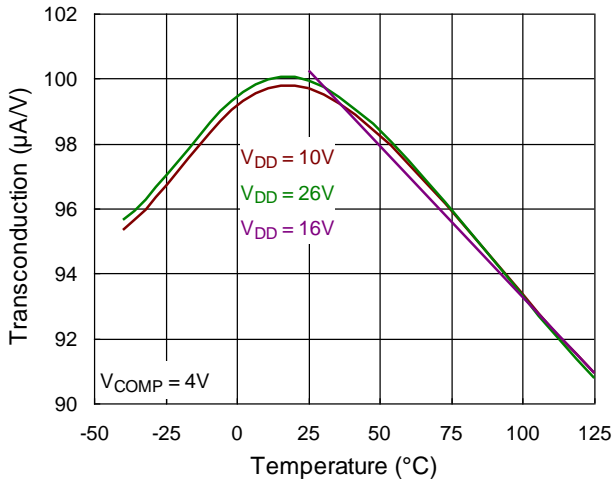**Typical SSR Application Circuit**

## Typical Operating Characteristics

**Non-inverting Input Reference vs. VDD**



**Transconduction vs. Temperature**



$V_{COMP}$ = 0.5V

$V_{DD}$ = 10V
$V_{DD}$ = 26V
$V_{DD}$ = 16V

**Transconduction vs. Temperature**



$V_{DD}$ = 10V
$V_{DD}$ = 26V
$V_{DD}$ = 16V

$V_{COMP}$ = 4V

**$I_{COMP}$ vs. $V_{COMP}$ (Sourcing)**



Non-linear Region

$V_{DD}$ = 26V, $T_A$ = 25°C
$V_{DD}$ = 10V, $T_A$ = 25°C
$V_{DD}$ = 26V, $T_A$ = 125°C
$V_{DD}$ = 10V, $T_A$ = 125°C
$V_{DD}$ = 26V, $T_A$ = −40°C
$V_{DD}$ = 10V, $T_A$ = −40°C

**$I_{COMP}$ vs. $V_{COMP}$ (Sinking)**



Non-linear Region

$V_{DD}$ = 26V, $T_A$ = 25°C
$V_{DD}$ = 10V, $T_A$ = 25°C
$V_{DD}$ = 26V, $T_A$ = 125°C
$V_{DD}$ = 10V, $T_A$ = 125°C
$V_{DD}$ = 26V, $T_A$ = −40°C
$V_{DD}$ = 10V, $T_A$ = −40°C
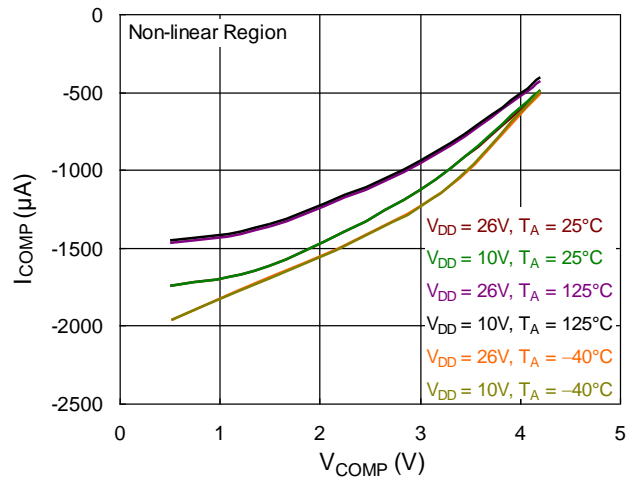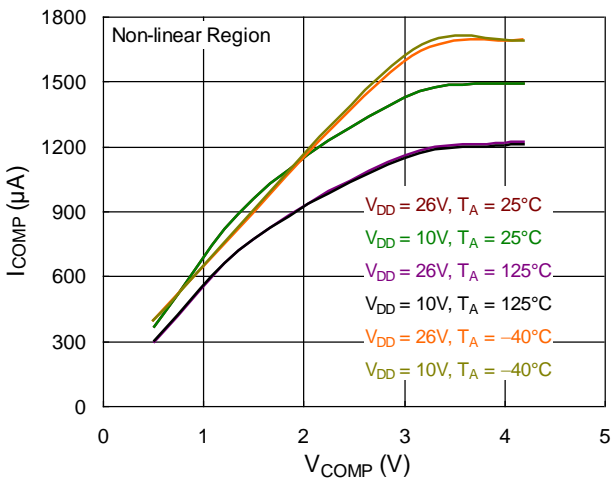
**Maximum COMP Voltage vs. VDD**
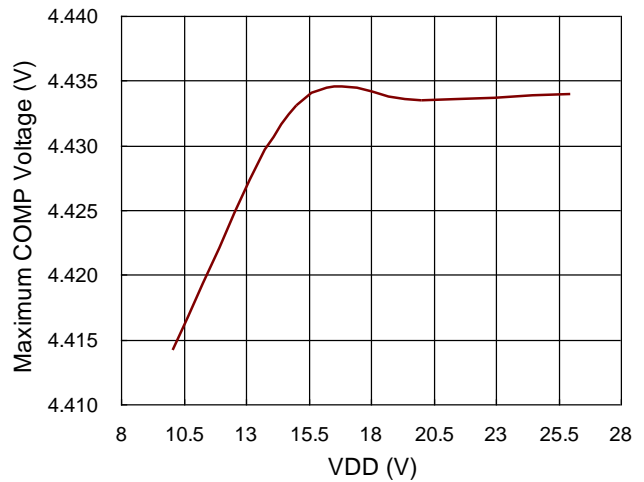
**Maximum COMP Voltage vs. Temperature**
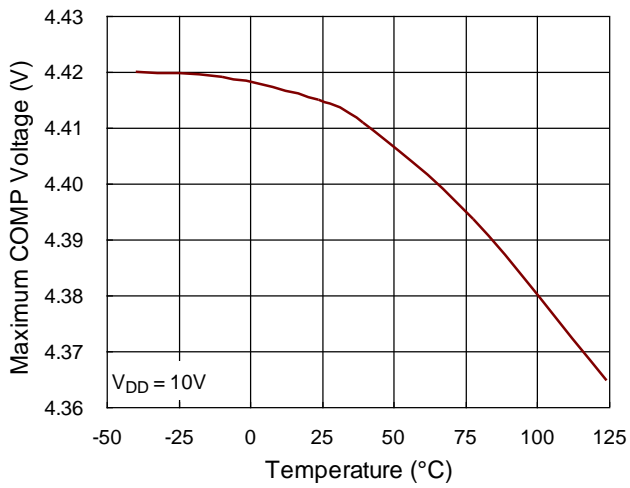
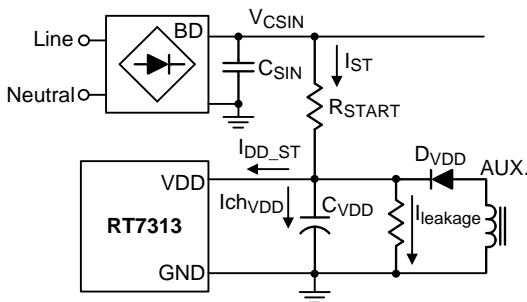## Application Information

### Start-Up Circuit Design
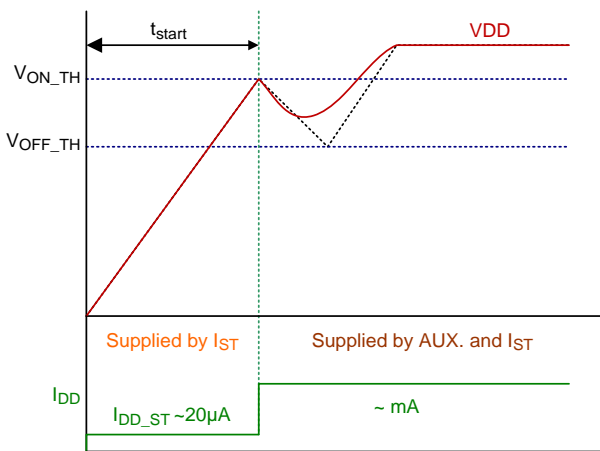


Figure 11. Start-Up Circuit



Figure 12. Start-Up Waveforms of VDD and $I_{DD}$

Figure 11 and Figure 12 show the equivalent start-up circuit and VDD waveform during start-up. In general, the start-up time ($t_{start}$) is required from system specification. The charging current ($Ich_{VDD}$) can be estimated by the following equation.

$$Ich_{VDD} = \frac{C_{VDD} \times V_{ON\_TH}}{t_{start}} \qquad (8)$$

where $C_{VDD}$ is the capacitor connected between VDD and GND, $V_{ON\_TH}$ is the power on threshold (16V typ.).

The start-up resistor ($R_{start}$) connected between $V_{CSIN}$ and VDD should be able to support the charging current ($Ich_{VDD}$), start-up current ($I_{DD\_ST}$) and leakage current ($I_{leakage}$) of $C_{VDD}$ before the VDD is supported by the auxiliary winding. The maximum start-up resistance can be calculated by the equation (9).

$$R_{Start} = \frac{\sqrt{2} \times Vin_{ac\_min}}{I_{DD\_ST} + Ich_{VDD} + I_{leakage}} \qquad (9)$$

where $V_{IN\ ac\_min}$ is the minimum input voltage. Note that the start-up resistor must have adequate voltage rating for reliability. 2 resistors in series can be applied for most of applications.

For example, the system required start-up time is 3sec, $V_{IN\ ac\_min}$ = 75V and maximum $I_{DD\_ST}$ = 20μA. If $C_{VDD}$ = 22μF is selected and the leakage current of $C_{VDD}$ can be ignored, the start-up resistor should be less than 772kΩ.

The capacitor $C_{FF}$ is applied to filter out the input ripple voltage. The corner frequency should be lower than line frequency ($f_{line}$). If the FF pin voltage is not flat, the PF and THD performance will be degraded.

$$\frac{1}{2\pi \times (R_{FF1} // R_{FF2}) \times C_{FF}} < 0.1 \times f_{line} \qquad (10)$$

### Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, $\theta_{JA}$, is layout dependent. For SOP-8 package, the thermal resistance, $\theta_{JA}$, is 160°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at $T_A$ = 25°C can be calculated by the following formula :

$P_{D(MAX)} = (125°C - 25°C) / (160°C/W) = 0.625W$ for SOP-8 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. The derating curve in Figure

13 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.
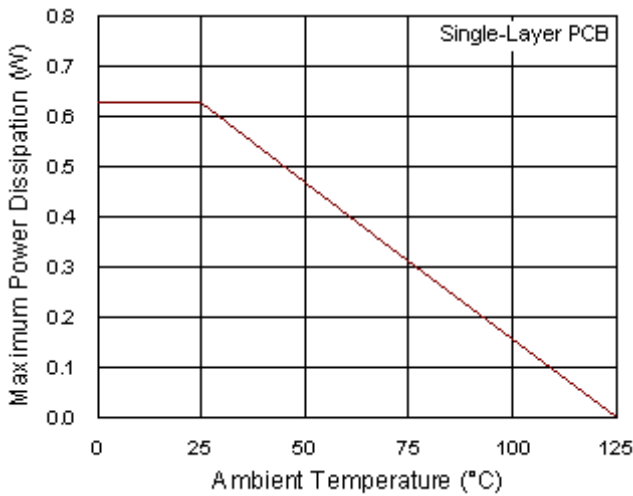


Figure 13. Derating Curve of Maximum Power Dissipation

**Layout Considerations**

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when designing a PCB layout for switching power supply.

▶ The current path(1) from input capacitor, transformer, MOSFET, $R_{CS}$ return to input capacitor is a high frequency current loop. The path(2) from GD pin,

MOSFET, $R_{CS}$ return to input capacitor is also a high frequency current loop. They must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially. Besides, the path(3) between MOSFET ground(b) and IC ground(d) is recommended to be as short as possible, too.

▶ It is good for reducing noise, output ripple and EMI issue to separate ground traces of input capacitor(a), MOSFET(b), auxiliary winding(c) and IC control circuit(d). Finally, connect them together on input capacitor ground(a). The areas of these ground traces should be kept large.

▶ Placing bypass capacitor for abating noise on IC is highly recommended. The capacitors $C_{INV}$ and $C_{CS}$ should be placed as close to controller as possible.

▶ In addition, apply sufficient copper area at the anode and cathode terminal of the diode for heat-sinking. It is recommended to apply a larger area at the quiet cathode terminal. A large anode area will induce high-frequency radiated EMI.
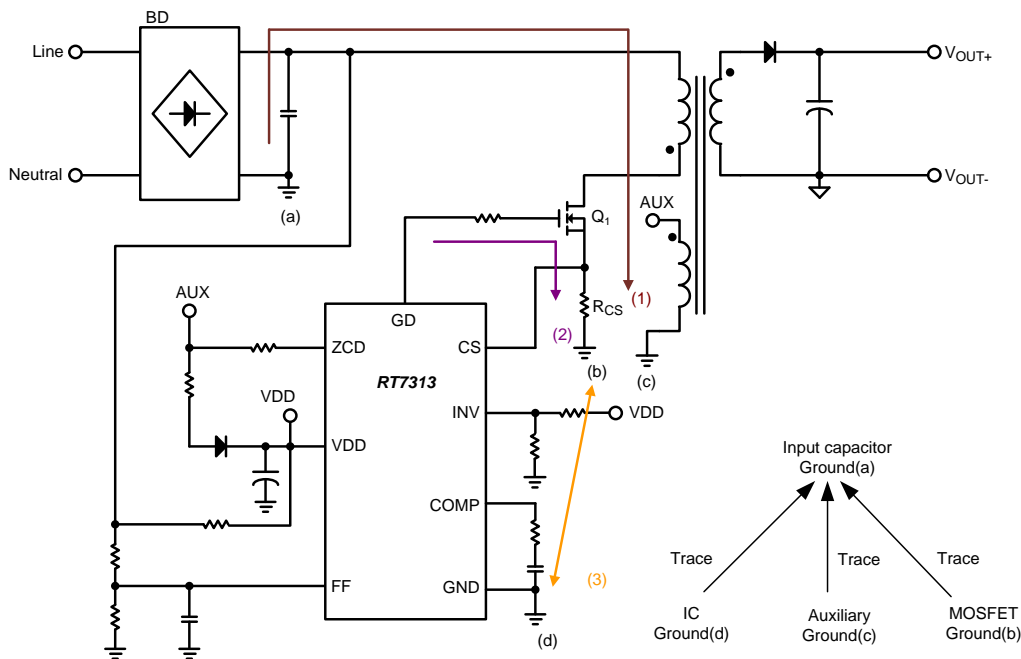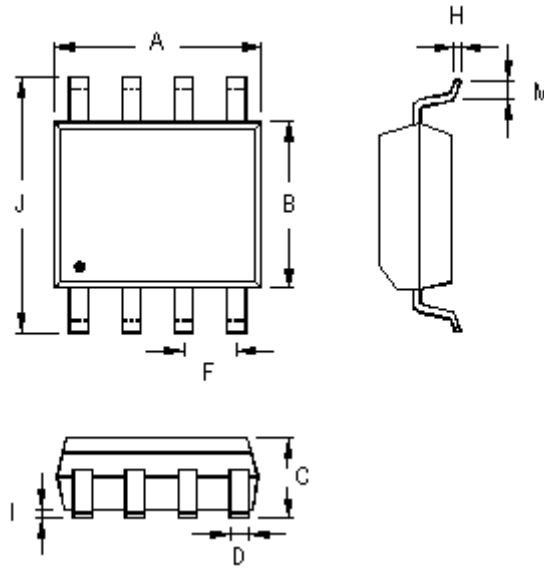


Figure 14. PCB Layout Guide

## Outline Dimension



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 4.801 | 5.004 | 0.189 | 0.197 |
| B | 3.810 | 3.988 | 0.150 | 0.157 |
| C | 1.346 | 1.753 | 0.053 | 0.069 |
| D | 0.330 | 0.508 | 0.013 | 0.020 |
| F | 1.194 | 1.346 | 0.047 | 0.053 |
| H | 0.170 | 0.254 | 0.007 | 0.010 |
| I | 0.050 | 0.254 | 0.002 | 0.010 |
| J | 5.791 | 6.200 | 0.228 | 0.244 |
| M | 0.400 | 1.270 | 0.016 | 0.050 |

**8-Lead SOP Plastic Package**

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