

FEATURES

- 10 MHz multiplying bandwidth
- On-chip 4-quadrant resistors allow flexible output ranges
- INL of ± 1 LSB
- 24-lead TSSOP package
- 2.5 V to 5.5 V supply operation
- ± 10 V reference input
- 50 MHz serial interface
- 2.47 MSPS update rate
- Extended temperature range: -40°C to 125°C
- 4-quadrant multiplication
- Power-on reset
- 0.5 μA typical current consumption
- Guaranteed monotonic
- Daisy-chain mode
- Readback function

APPLICATIONS

- Portable battery-powered applications
- Waveform generators
- Analog processing
- Instrumentation applications
- Programmable amplifiers and attenuators
- Digitally controlled calibration
- Programmable filters and oscillators
- Composite video
- Ultrasound
- Gain, offset, and voltage trimming

GENERAL DESCRIPTION

The AD5415¹ is a CMOS, 12-bit, dual-channel, current output digital-to-analog converter. This device operates from a 2.5 V to 5.5 V power supply, making it suited to battery-powered applications and other applications. As a result of being manufactured on a CMOS submicron process, this part offers excellent 4-quadrant multiplication characteristics, with large-signal multiplying bandwidths of 10 MHz.

The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full-scale voltage output when combined with an external current-to-voltage precision amplifier. In addition, this device contains the 4-quadrant resistors necessary for bipolar operation and other configuration modes.

This DAC uses a double-buffered, 3-wire serial interface that is compatible with SPI®, QSPI™, MICROWIRE™, and most DSP interface standards. In addition, a serial data out pin (SDO) allows daisy-chaining when multiple packages are used. Data readback allows the user to read the contents of the DAC register via the SDO pin. On power-up, the internal shift register and latches are filled with 0s, and the DAC outputs are at zero scale.

The AD5415 DAC is available in a 24-lead TSSOP package. The EV-AD5415/49SDZ evaluation board is available for evaluating DAC performance. For more information, see the UG-296 evaluation board user guide.

FUNCTIONAL BLOCK DIAGRAM

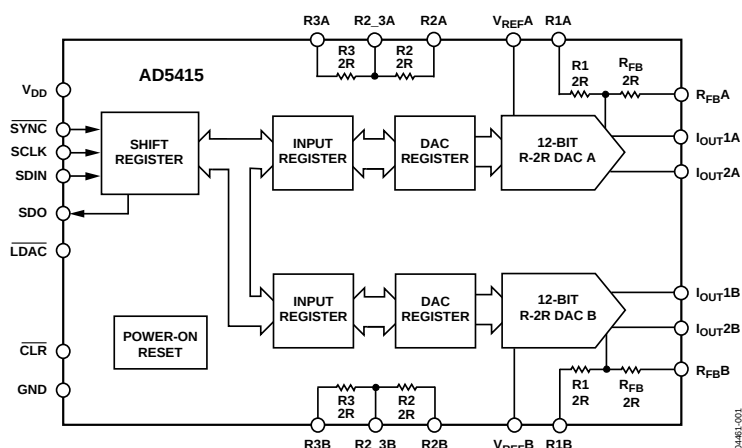


Figure 1.

¹ U.S. Patent Number 5,689,257.

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REVISION HISTORY

5/13—Rev. D to Rev. E

Changes to General Description	1
Change to Ordering Guide.....	26

5/12—Rev. C to Rev. D

Changes SDO Control (SDO1 and SDO2) Section	20
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6/11—Rev. B to Rev. C

Changes to General Description	1
Deleted Evaluation Board for the DAC Section and Power Supplies for the Evaluation Board Section	24
Changes to Ordering Guide	26

4/10—Rev. A to Rev. B

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7/05—Rev. 0 to Rev. A

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7/04—Revision 0: Initial Version

SPECIFICATIONS¹

$V_{DD} = 2.5\text{ V to }5.5\text{ V}$, $V_{REF} = 10\text{ V}$, $I_{OUT2} = 0\text{ V}$. Temperature range for Y version: $-40^{\circ}\text{C to }+125^{\circ}\text{C}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted. DC performance is measured with OP177, and ac performance is measured with AD8038, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
STATIC PERFORMANCE					
Resolution			12	Bits	Guaranteed monotonic
Relative Accuracy			±1	LSB	
Differential Nonlinearity			−1/+2	LSB	
Gain Error			±25	mV	
Gain Error Temperature Coefficient		±5		ppm FSR/°C	Data = 0x0000, T _A = 25°C, I _{OUT1} Data = 0x0000, T _A = −40°C to +125°C, I _{OUT1}
Bipolar Zero Code Error			±25	mV	
Output Leakage Current			±1	nA	
			±15	nA	
REFERENCE INPUT					
Reference Input Range		±10		V	Input resistance TC = −50 ppm/°C Typ = 25°C, max = 125°C
V _{REFA} , V _{REFB} Input Resistance	8	10	13	kΩ	
V _{REFA} -to-V _{REFB} Input Resistance Mismatch		1.6	2.5	%	
R1, R _{FB} Resistance	17	20	25	kΩ	
R2, R3 Resistance	17	20	25	kΩ	Input resistance TC = −50 ppm/°C Typ = 25°C, max = 125°C
R2-to-R3 Resistance Mismatch		0.06	0.18	%	
Input Capacitance					
Code 0		3.5		pF	
Code 4095		3.5		pF	
DIGITAL INPUTS/OUTPUT					
Input High Voltage, V _{IH}	1.7			V	V _{DD} = 3.6 V to 5.5 V V _{DD} = 2.5 V to 3.6 V
	1.7			V	
Input Low Voltage, V _{IL}			0.8	V	V _{DD} = 2.7 V to 5.5 V V _{DD} = 2.5 V to 2.7 V
			0.7	V	
Output High Voltage, V _{OH}	V _{DD} − 1			V	V _{DD} = 4.5 V to 5.5 V, I _{SOURCE} = 200 μA V _{DD} = 2.5 V to 3.6 V, I _{SOURCE} = 200 μA
	V _{DD} − 0.5			V	
Output Low Voltage, V _{OL}			0.4	V	V _{DD} = 4.5 V to 5.5 V, I _{SINK} = 200 μA V _{DD} = 2.5 V to 3.6 V, I _{SINK} = 200 μA
			0.4	V	
Input Leakage Current, I _{IL}			1	μA	
Input Capacitance		4	10	pF	
DYNAMIC PERFORMANCE					
Reference-Multiplying BW		10		MHz	V _{REF} = ±3.5 V p-p, DAC loaded all 1s R _{LOAD} = 100 Ω, C _{LOAD} = 15 pF, V _{REF} = 10 V DAC latch alternately loaded with 0s and 1s
Output Voltage Settling Time					
Measured to ±1 mV of FS		80	120	ns	
Measured to ±4 mV of FS		35	70	ns	
Measured to ±16 mV of FS		30	60	ns	Rise and fall times 1 LSB change around major carry, V _{REF} = 0 V DAC latches loaded with all 0s, V _{REF} = ±3.5 V
Digital Delay		20	40	ns	
10% to 90% Settling Time		15	30	ns	
Digital-to-Analog Glitch Impulse		3		nV-sec	
Multiplying Feedthrough Error			70	dB	1 MHz 10 MHz DAC latches loaded with all 0s DAC latches loaded with all 1s
			48	dB	
Output Capacitance		12	17	pF	
		25	30	pF	

Parameter	Min	Typ	Max	Unit	Conditions
Digital Feedthrough		3	5	nV-sec	Feedthrough to DAC output with $\overline{CS}$ high and alternate loading of all 0s and all 1s
Output Noise Spectral Density		25		nV/ $\sqrt{\text{Hz}}$	@ 1 kHz
Analog THD		81		dB	$V_{\text{REF}} = 3.5 \text{ V p-p}$, all 1s loaded, $f = 1 \text{ kHz}$
Digital THD					Clock = 10 MHz, $V_{\text{REF}} = 3.5 \text{ V}$
100 kHz f_{OUT}		61		dB	
50 kHz f_{OUT}		66		dB	
SFDR Performance (Wide Band)					$V_{\text{REF}} = 3.5 \text{ V}$
Clock = 10 MHz					
500 kHz f_{OUT}		55		dB	
100 kHz f_{OUT}		63		dB	
50 kHz f_{OUT}		65		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		50		dB	
100 kHz f_{OUT}		60		dB	
50 kHz f_{OUT}		62		dB	
SFDR Performance (Narrow Band)					$V_{\text{REF}} = 3.5 \text{ V}$
Clock = 10 MHz					
500 kHz f_{OUT}		73		dB	
100 kHz f_{OUT}		80		dB	
50 kHz f_{OUT}		87		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		70		dB	
100 kHz f_{OUT}		75		dB	
50 kHz f_{OUT}		80		dB	
Intermodulation Distortion					$V_{\text{REF}} = 3.5 \text{ V}$
$f_1 = 40 \text{ kHz}$, $f_2 = 50 \text{ kHz}$		72		dB	Clock = 10 MHz
$f_1 = 40 \text{ kHz}$, $f_2 = 50 \text{ kHz}$		65		dB	Clock = 25 MHz
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	$T_A = 25^\circ\text{C}$, logic inputs = 0 V or V_{DD} $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, logic inputs = 0 V or V_{DD} $\Delta V_{\text{DD}} = \pm 5\%$
I_{DD}			0.7	μA	
		0.5	10	μA	
Power Supply Sensitivity			0.001	%/%	

¹ Guaranteed by design and characterization, not subject to production test.

TIMING CHARACTERISTICS

All input signals are specified with $t_r = t_f = 1$ ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. $V_{DD} = 2.5$ V to 5.5 V, $V_{REF} = 10$ V, $I_{OUT2} = 0$ V, temperature range for Y version: -40°C to $+125^{\circ}\text{C}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

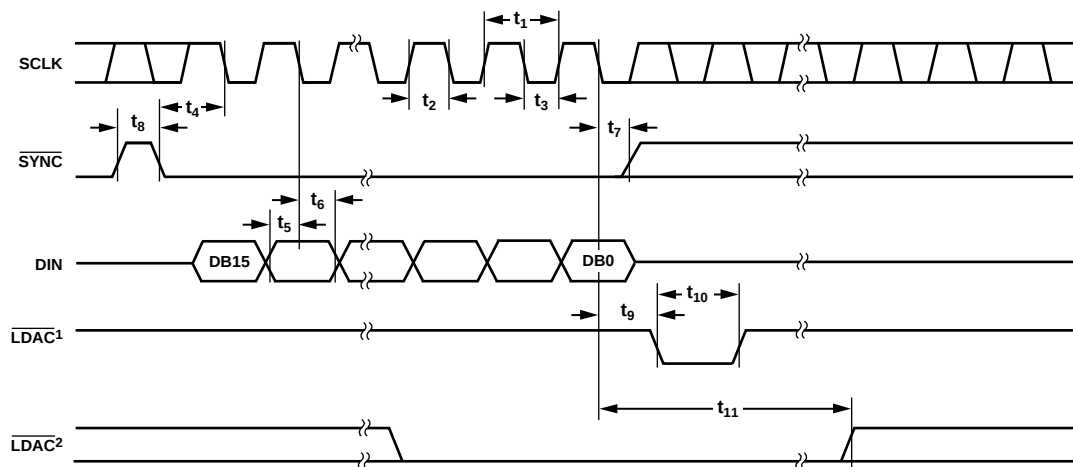
Table 2.

Parameter ¹	Limit at T_{MIN} , T_{MAX}	Unit	Conditions/Comments ²
f_{SCLK}	50	MHz max	Maximum clock frequency
t_1	20	ns min	SCLK cycle time
t_2	8	ns min	SCLK high time
t_3	8	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	4	ns min	Data hold time
t_7	5	ns min	$\overline{SYNC}$ rising edge to SCLK falling edge
t_8	30	ns min	Minimum $\overline{SYNC}$ high time
t_9	0	ns min	SCLK falling edge to $\overline{LDAC}$ falling edge
t_{10}	12	ns min	$\overline{LDAC}$ pulse width
t_{11}	10	ns min	SCLK falling edge to $\overline{LDAC}$ rising edge
t_{12}^3	25	ns min	SCLK active edge to SDO valid, strong SDO driver
	60	ns min	SCLK active edge to SDO valid, weak SDO driver
Update Rate	2.47	MSPS	Consists of cycle time, $\overline{SYNC}$ high time, data setup, and output voltage settling time

¹ Guaranteed by design and characterization, not subject to production test.

² Falling or rising edge as determined by the control bits of the serial word. Strong or weak SDO driver selected via the control register.

³ Daisy-chain and readback modes cannot operate at maximum clock frequency. SDO timing specifications measured with a load circuit, as shown in Figure 5.



¹ASYNCHRONOUS LDAC UPDATE MODE.

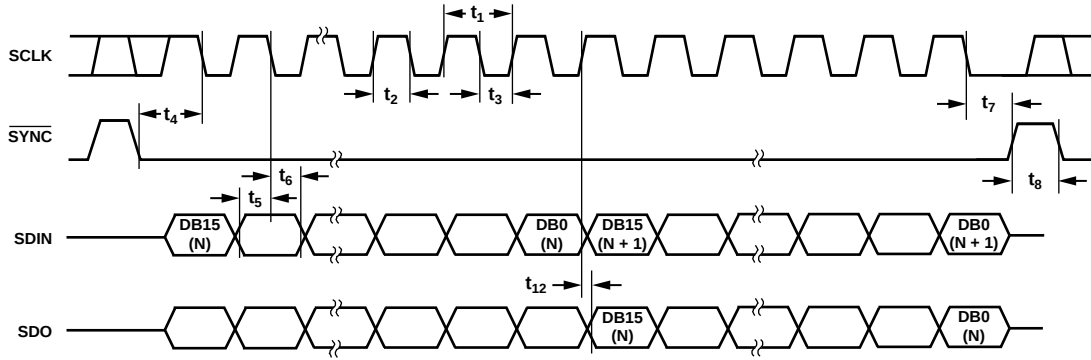
²SYNCHRONOUS LDAC UPDATE MODE.

NOTES

ALTERNATIVELY, DATA CAN BE CLOCKED INTO THE INPUT SHIFT REGISTER ON THE RISING EDGE OF SCLK AS DETERMINED BY THE CONTROL BITS. TIMING IS AS ABOVE, WITH SCLK INVERTED.

04481-002

Figure 2. Standalone Mode Timing Diagram

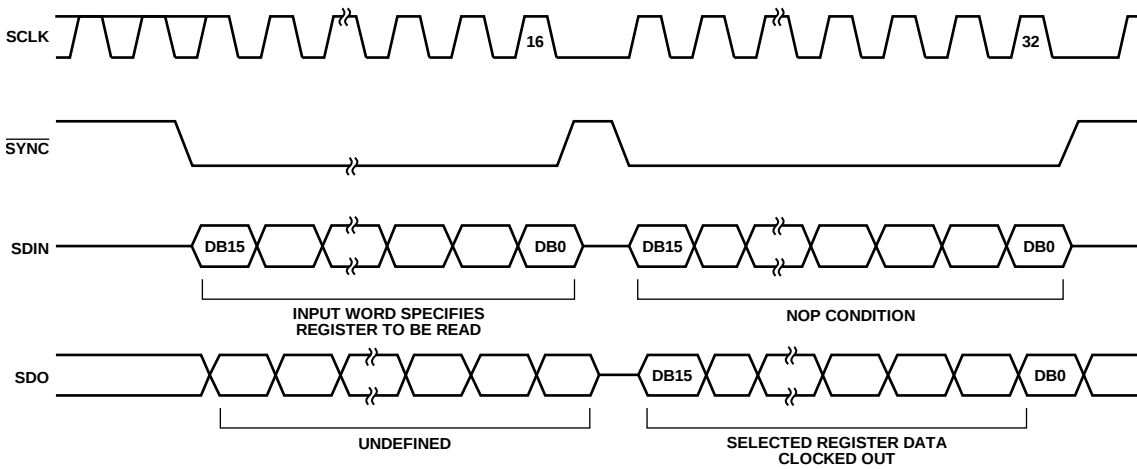


NOTES

1. ALTERNATIVELY, DATA CAN BE CLOCKED INTO THE INPUT SHIFT REGISTER ON THE RISING EDGE OF SCLK AS DETERMINED BY THE CONTROL BITS. IN THIS CASE, DATA IS CLOCKED OUT OF SDO ON THE FALLING EDGE OF SCLK. TIMING IS AS ABOVE, WITH SCLK INVERTED.

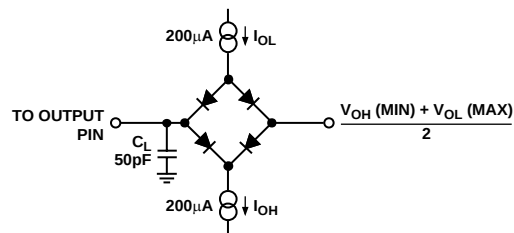
04461-003

Figure 3. Daisy-Chain Timing Diagram



04461-003

Figure 4. Readback Mode Timing Diagram



04461-004

Figure 5. Load Circuit for SDO Timing Specifications

ABSOLUTE MAXIMUM RATINGS

Transient currents of up to 100 mA do not cause SCR latch-up.

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	$-0.3\text{ V to }+7\text{ V}$
V_{REF} , R_{FB} to GND	$-12\text{ V to }+12\text{ V}$
I_{OUT1} , I_{OUT2} to GND	$-0.3\text{ V to }+7\text{ V}$
Input Current to Any Pin Except Supplies	$\pm 10\text{ mA}$
Logic Inputs and Output ¹	$-0.3\text{ V to }V_{DD} + 0.3\text{ V}$
Operating Temperature Range	
Extended (Y Version)	$-40^\circ\text{C to }+125^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Junction Temperature	150°C
24-Lead TSSOP, θ_{JA} Thermal Impedance	128°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

¹ Overvoltages at SCLK, $\overline{\text{SYNC}}$, and SDIN are clamped by internal diodes.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

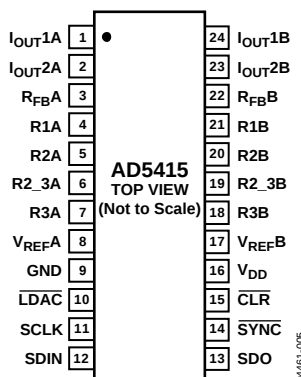


Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IOUT1A	DAC A Current Output.
2	IOUT2A	DAC A Analog Ground. This pin should normally be tied to the analog ground of the system, but can be biased to achieve single-supply operation.
3	RFB A	DAC Feedback Resistor Pin. This pin establishes voltage output for the DAC by connecting to an external amplifier output.
4 to 7	R1A, R2A, R2_3A, R3A	DAC A 4-Quadrant Resistors. These pins allow a number of configuration modes, including bipolar operation, with minimum external components.
8	VREF A	DAC A Reference Voltage Input Pin.
9	GND	Ground Pin.
10	LDAC	Load DAC Input. This pin allows asynchronous or synchronous updates to the DAC output. The DAC is asynchronously updated when this signal goes low. Alternatively, if this line is held permanently low, an automatic or synchronous update mode is selected, whereby the DAC is updated on the 16th clock falling edge when the device is in standalone mode, or on the rising edge of SYNC when in daisy-chain mode.
11	SCLK	Serial Clock Input. By default, data is clocked into the input shift register on the falling edge of the serial clock input. Alternatively, by means of the serial control bits, the device can be configured such that data is clocked into the shift register on the rising edge of SCLK.
12	SDIN	Serial Data Input. Data is clocked into the 16-bit input register on the active edge of the serial clock input. By default, on power-up data is clocked into the shift register on the falling edge of SCLK. The control bits allow the user to change the active edge to the rising edge.
13	SDO	Serial Data Output. This pin allows a number of parts to be daisy-chained. By default, data is clocked into the shift register on the falling edge and clocked out via SDO on the rising edge of SCLK. Data is always clocked out on the alternate edge to loading data to the shift register. Writing the readback control word to the shift register makes the DAC register contents available for readback on the SDO pin; they are clocked out on the next 16 opposite clock edges to the active clock edge.
14	SYNC	Active Low Control Input. This pin provides the frame synchronization signal for the input data. When SYNC goes low, it powers on the SCLK and SDIN buffers, and the input shift register is enabled. Data is loaded into the shift register on the active edge of the subsequent clocks. In standalone mode, the serial interface counts the clocks, and data is latched into the shift register on the 16th active clock edge.
15	CLR	Active Low Control Input. This pin clears the DAC output, input, and DAC registers. Configuration mode allows the user to enable the hardware CLR pin as a clear to zero scale or midscale as required.
16	VDD	Positive Power Supply Input. This part can be operated from a supply of 2.5 V to 5.5 V.
17	VREF B	DAC B Reference Voltage Input Pin.
18 to 21	R3B, R2_3B, R2B, R1B	DAC B 4-Quadrant Resistors. These pins allow a number of configuration modes, including bipolar operation, with a minimum of external components.
22	RFB B	DAC B Feedback Resistor Pin. This pin establishes voltage output for the DAC by connecting to the external amplifier output.
23	IOUT2B	DAC B Analog Ground. This pin should normally be tied to the analog ground of the system, but can be biased to achieve single-supply operation.
24	IOUT1B	DAC B Current Output.

TYPICAL PERFORMANCE CHARACTERISTICS

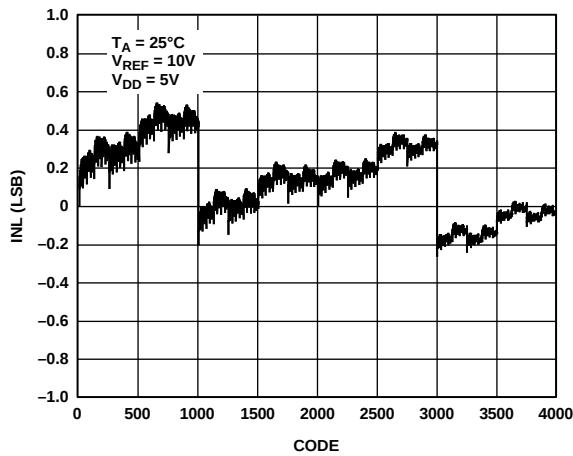


Figure 7. INL vs. Code (12-Bit DAC)

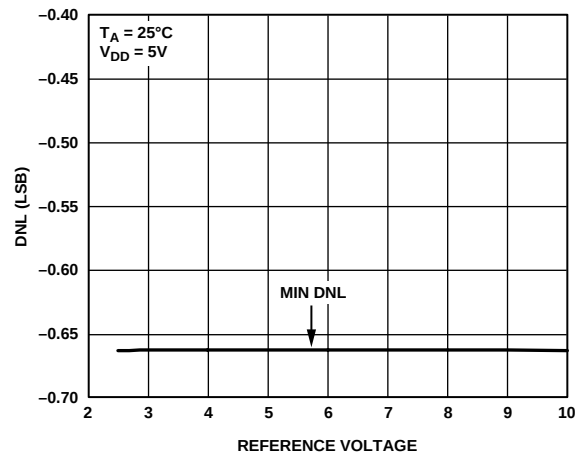


Figure 10. DNL vs. Reference Voltage

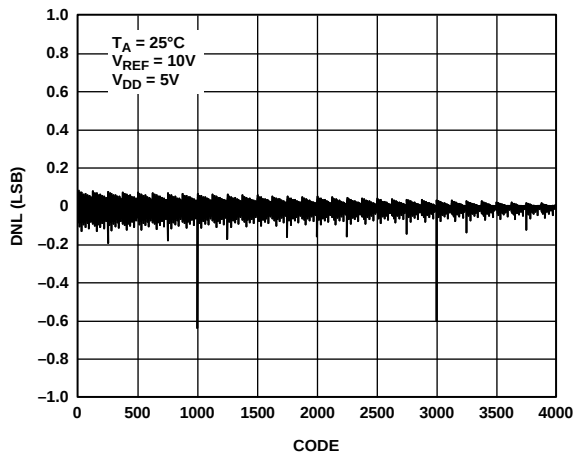


Figure 8. DNL vs. Code (12-Bit DAC)

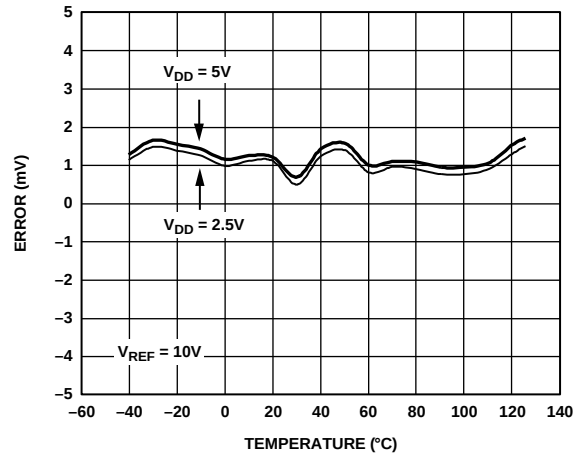


Figure 11. Gain Error vs. Temperature

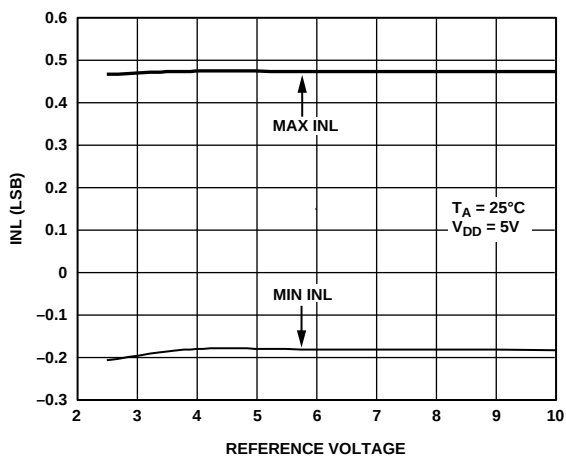


Figure 9. INL vs. Reference Voltage

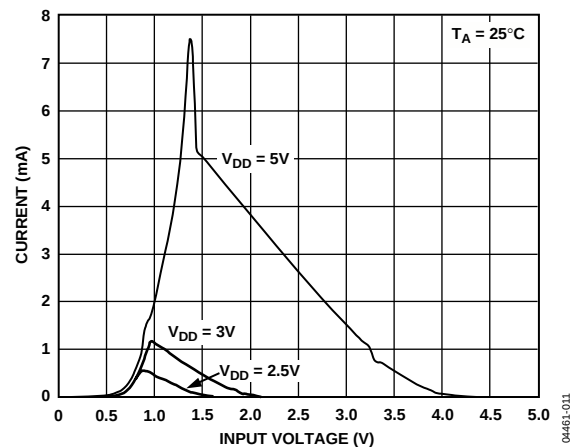


Figure 12. Supply Current vs. Logic Input Voltage

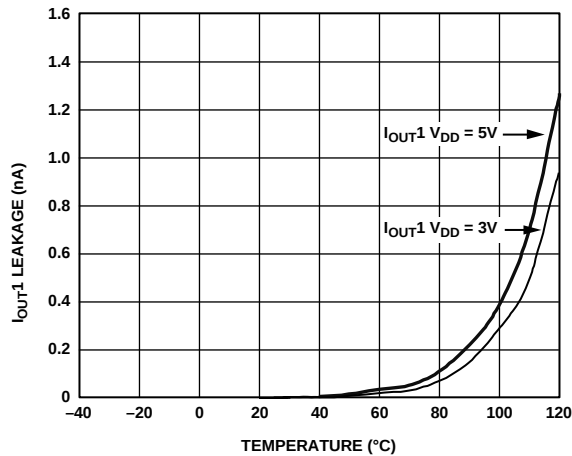
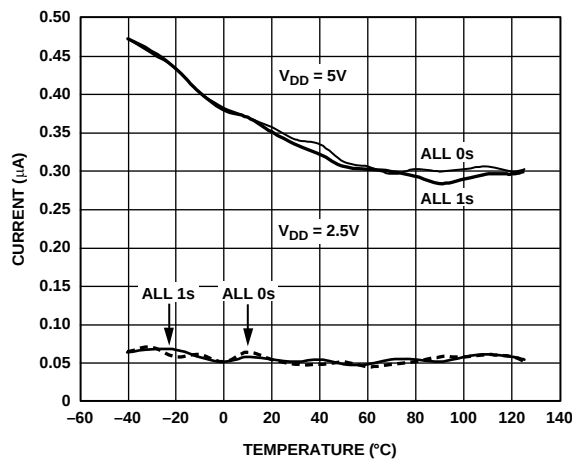
Figure 13. I_{OUT1} Leakage Current vs. Temperature

Figure 14. Supply Current vs. Temperature

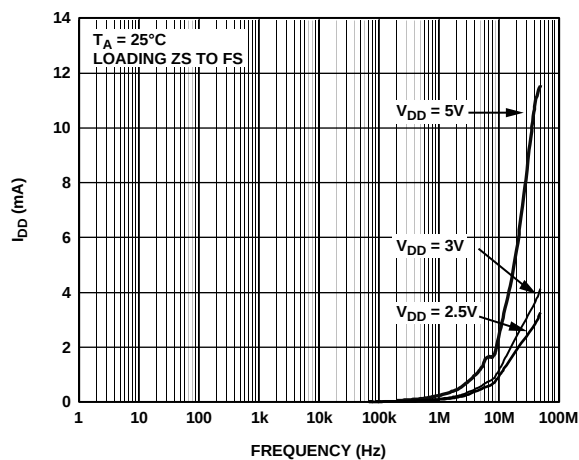


Figure 15. Supply Current vs. Update Rate

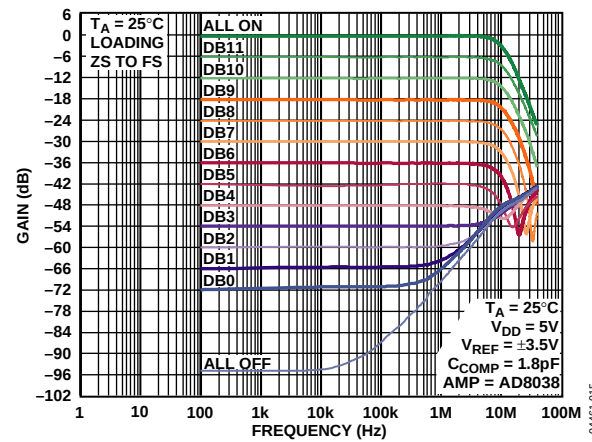


Figure 16. Reference Multiplying Bandwidth vs. Frequency and Code

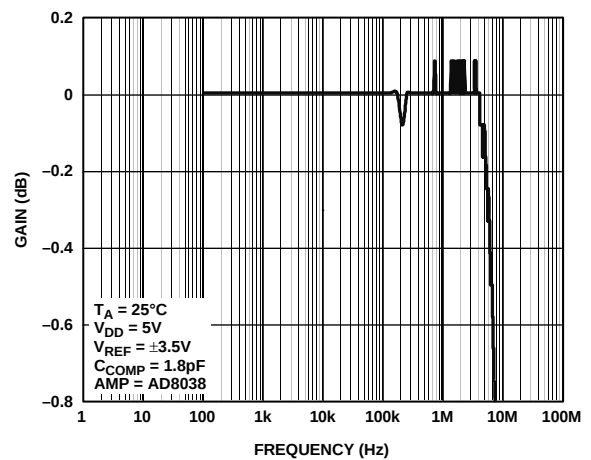


Figure 17. Reference Multiplying Bandwidth—All Ones Loaded

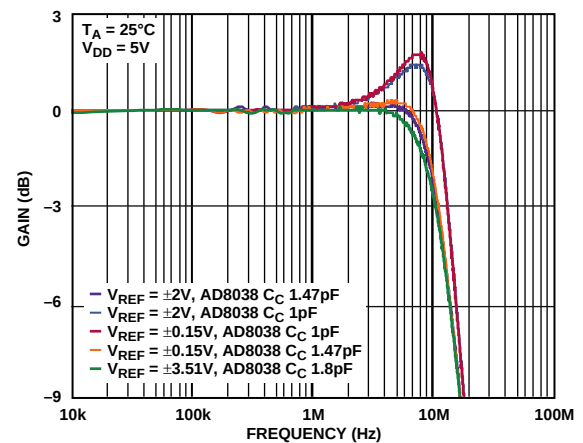


Figure 18. Reference Multiplying Bandwidth vs. Frequency and Compensation Capacitor

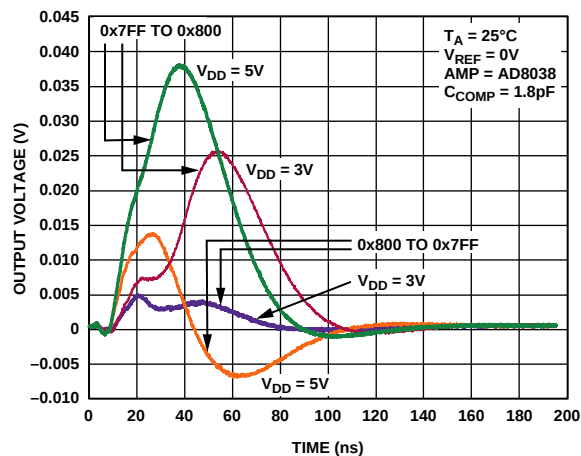
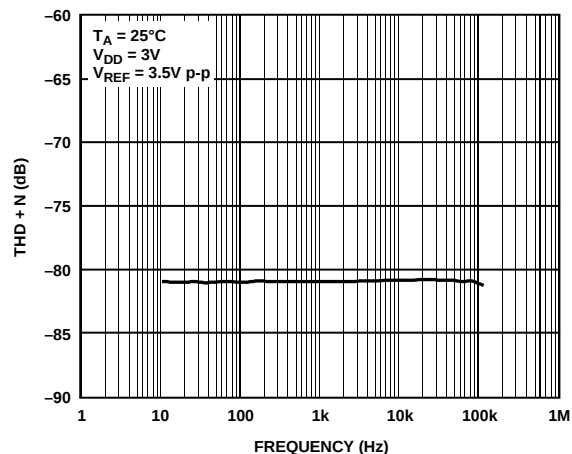
Figure 19. Midscale Transition, $V_{REF} = 0V$ 

Figure 22. THD and Noise vs. Frequency

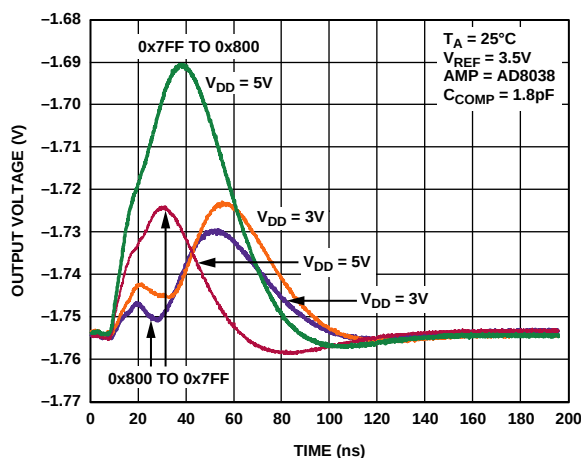
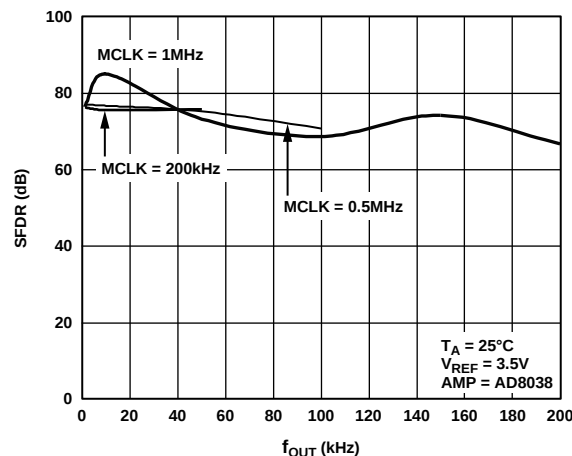
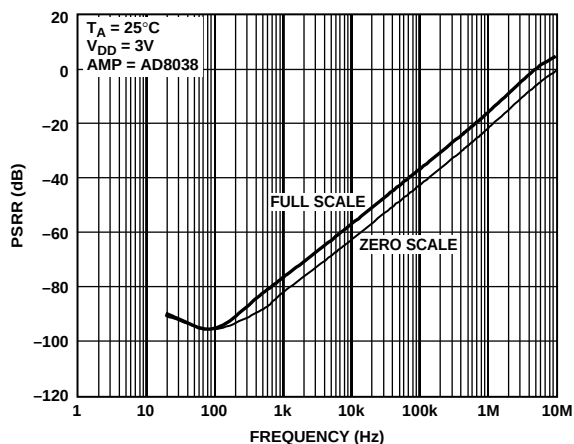
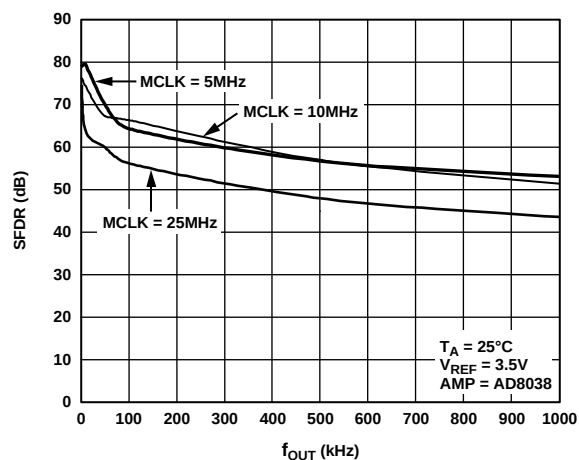
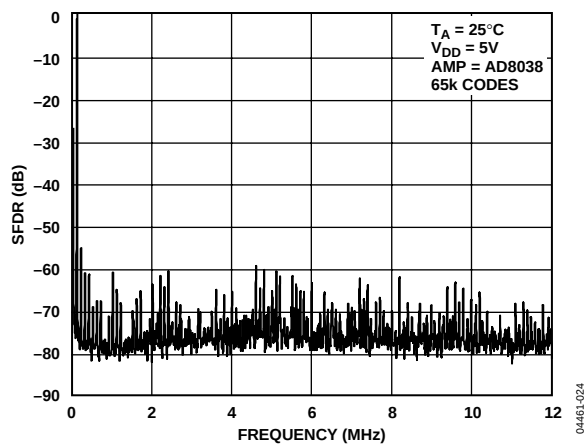
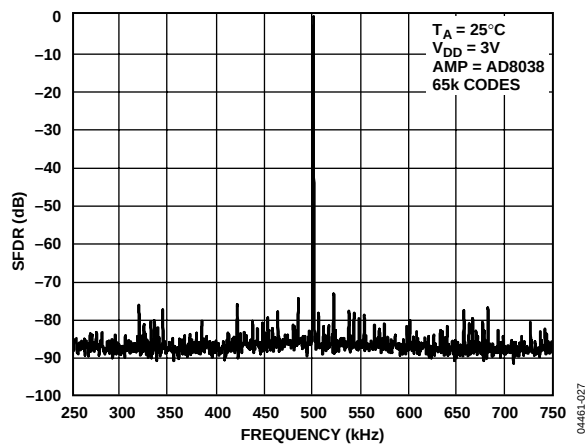
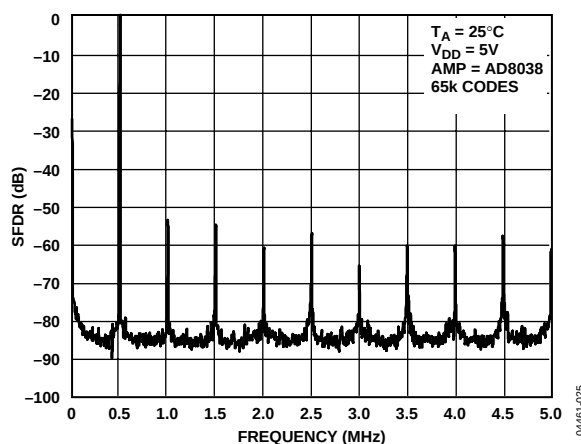
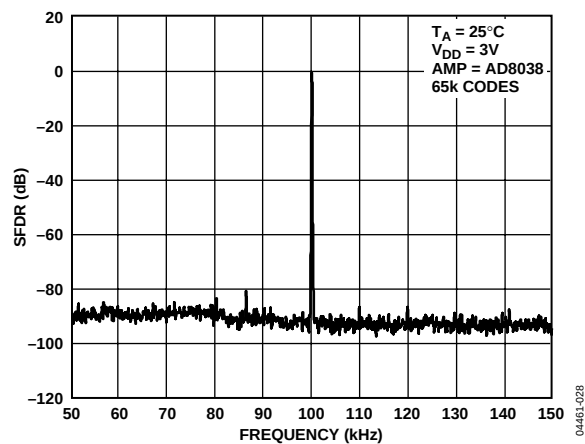
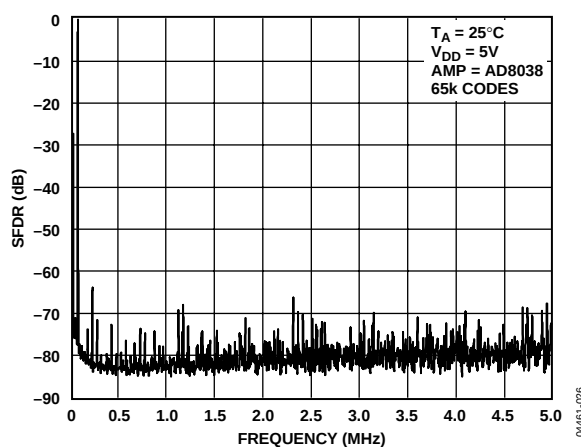
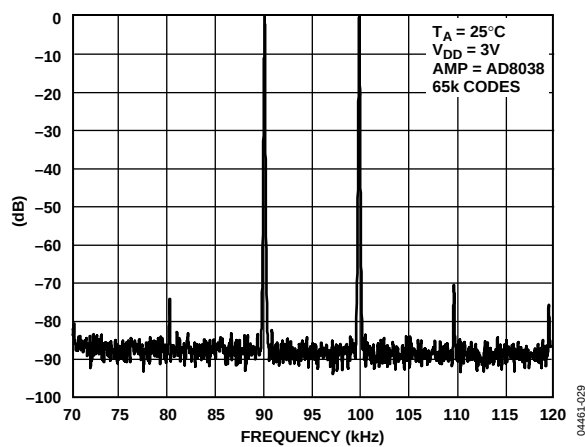
Figure 20. Midscale Transition, $V_{REF} = 3.5V$ Figure 23. Wideband SFDR vs. f_{OUT} Frequency

Figure 21. Power Supply Rejection Ratio vs. Frequency

Figure 24. Wideband SFDR vs. f_{OUT} Frequency

Figure 25. Wideband SFDR, $f_{OUT} = 100$ kHz, Clock = 25 MHzFigure 28. Narrow-Band Spectral Response, $f_{OUT} = 500$ kHz, Clock = 25 MHzFigure 26. Wideband SFDR, $f_{OUT} = 500$ kHz, Clock = 10 MHzFigure 29. Narrow-Band SFDR, $f_{OUT} = 100$ kHz, MCLK = 25 MHzFigure 27. Wideband SFDR, $f_{OUT} = 50$ kHz, Clock = 10 MHzFigure 30. Narrow-Band IMD, $f_{OUT} = 90$ kHz, 100 kHz, Clock = 10 MHz

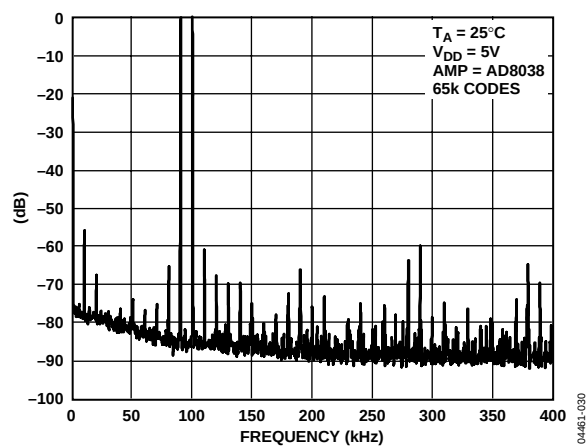


Figure 31. Wideband IMD, $f_{OUT} = 90\text{ kHz}$, 100 kHz, Clock = 25 MHz

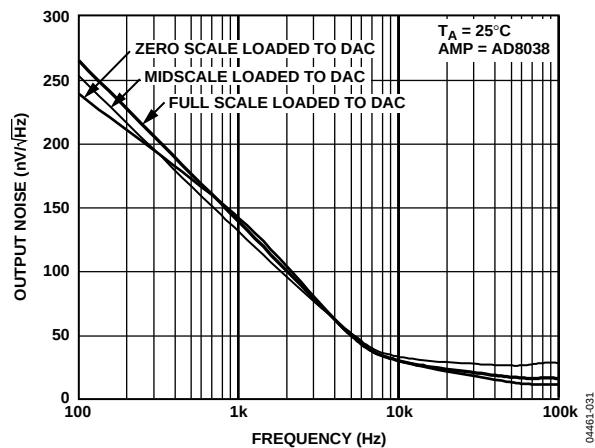


Figure 32. Output Noise Spectral Density

TERMINOLOGY

Relative Accuracy (Endpoint Nonlinearity)

A measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero scale and full scale and is normally expressed in LSB or as a percentage of the full-scale reading.

Differential Nonlinearity

The difference in the measured change and the ideal 1 LSB change between two adjacent codes. A specified differential nonlinearity of –1 LSB maximum over the operating temperature range ensures monotonicity.

Gain Error (Full-Scale Error)

A measure of the output error between an ideal DAC and the actual device output. For this DAC, ideal maximum output is $V_{REF} - 1$ LSB. The gain error of the DAC is adjustable to zero with an external resistance.

Output Leakage Current

The current that flows into the DAC ladder switches when they are turned off. For the I_{OUT1} terminal, it can be measured by loading all 0s to the DAC and measuring the I_{OUT1} current. Minimum current flows into the I_{OUT2} line when the DAC is loaded with all 1s.

Output Capacitance

Capacitance from I_{OUT1} or I_{OUT2} to AGND.

Output Current Settling Time

The amount of time for the output to settle to a specified level for a full-scale input change. For this device, it is specified with a 100 Ω resistor to ground.

Digital-to-Analog Glitch Impulse

The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-sec or nV-sec, depending on whether the glitch is measured as a current or voltage signal.

Digital Feedthrough

When the device is not selected, high frequency logic activity on the device's digital inputs is capacitively coupled through the device and produces noise on the I_{OUT} pins and, subsequently, on the following circuitry. This noise is digital feedthrough.

Multiplying Feedthrough Error

The error due to capacitive feedthrough from the DAC reference input to the DAC I_{OUT1} terminal when all 0s are loaded to the DAC.

Digital Crosstalk

The glitch impulse transferred to the outputs of one DAC in response to a full-scale code change (all 0s to all 1s, or vice versa) in the input register of the other DAC. It is expressed in nV-sec.

Analog Crosstalk

The glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s, or vice versa) while keeping $\overline{LDAC}$ high and then pulsing $\overline{LDAC}$ low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nV-sec.

Channel-to-Channel Isolation

The portion of input signal from a DAC reference input that appears at the output of another DAC. It is expressed in decibels.

Total Harmonic Distortion (THD)

The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower-order harmonics are included, such as the second to fifth harmonics.

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}$$

Intermodulation Distortion (IMD)

The DAC is driven by two combined sine wave references of frequencies f_a and f_b . Distortion products are produced at sum and difference frequencies of $m f_a \pm n f_b$, where $m, n = 0, 1, 2, 3 \dots$. Intermodulation terms are those for which m or n is not equal to 0. The second-order terms include $(f_a + f_b)$ and $(f_a - f_b)$, and the third-order terms are $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$. IMD is defined as

$$IMD = 20 \log \frac{\left(\text{rms sum of the sum and diff distortion products} \right)}{\text{rms amplitude of the fundamental}}$$

Compliance Voltage Range

The maximum range of (output) terminal voltage for which the device provides the specified characteristics.

Bipolar Operation

In some applications, it may be necessary to generate full 4-quadrant multiplying operation or a bipolar output swing. This can easily be accomplished by using another external amplifier and the on-chip 4-quadrant resistors, as shown in Figure 35.

When in bipolar mode, the output voltage is given by

V_{OUT} = (V_{REF} \times D/2^{n-1}) - V_{REF}

where:

D is the fractional representation, in the range of 0 to 4,095, of the digital word loaded to the DAC.
n is the number of bits.

When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication.

Table 6 shows the relationship between digital code and the expected output voltage for bipolar operation.

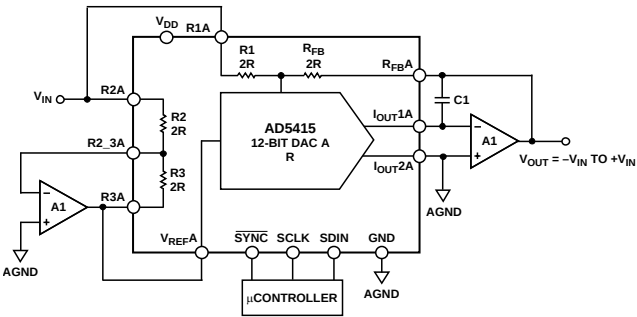
Table 6. Bipolar Code

Digital Input	Analog Output (V)
1111 1111 1111	+V_{REF} (4,095/4,096)
1000 0000 0000	0
0000 0000 0001	-V_{REF} (4,095/4,096)
0000 0000 0000	-V_{REF} (4,096/4,096)

Stability

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the op amp must be connected as close as possible, and proper PCB layout techniques must be used. Because every code change corresponds to a step function, gain peaking may occur if the op amp has limited gain bandwidth product (GBP) and there is excessive parasitic capacitance at the inverting node. This parasitic capacitance introduces a pole into the open-loop response, which can cause ringing or instability in the closed-loop applications circuit.

An optional compensation capacitor, C1, can be added in parallel with R_{FB}A for stability, as shown in Figure 34 and Figure 35. Too small a value of C1 can produce ringing at the output, whereas too large a value can adversely affect the settling time. C1 should be found empirically, but 1 pF to 2 pF is generally adequate for the compensation.



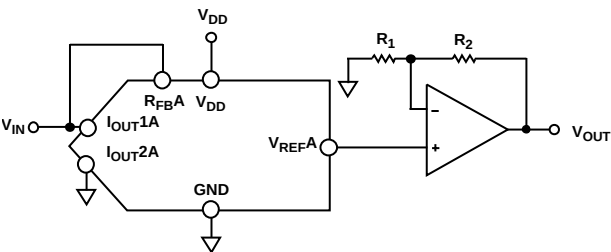
NOTES
1. DAC B OMITTED FOR CLARITY.
2. C1 PHASE COMPENSATION (1pF TO 2pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

Figure 35. Bipolar Operation

SINGLE-SUPPLY APPLICATIONS

Voltage-Switching Mode of Operation

Figure 36 shows the DAC operating in the voltage-switching mode. The reference voltage, V_{IN}, is applied to the I_{OUT1A} pin, I_{OUT2A} is connected to AGND, and the output voltage is available at the V_{REF}A terminal. In this configuration, a positive reference voltage results in a positive output voltage, making single-supply operation possible. The output from the DAC is voltage at a constant impedance (the DAC ladder resistance). Therefore, an op amp is necessary to buffer the output voltage. The reference input no longer sees a constant input impedance, but one that varies with code. Therefore, the voltage input should be driven from a low impedance source.



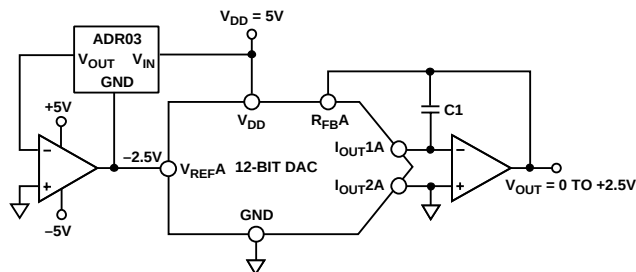
NOTES
1. SIMILAR CONFIGURATION FOR DACB
2. C1 PHASE COMPENSATION (1pF TO 2pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

Figure 36. Single-Supply Voltage-Switching Mode

Note that V_{IN} is limited to low voltages because the switches in the DAC ladder no longer have the same source-drain drive voltage. As a result, their on resistance differs and degrades the integral linearity of the DAC. Also, V_{IN} must not go negative by more than 0.3 V, or an internal diode turns on, causing the device to exceed the maximum ratings. In this type of application, the full range of multiplying capability of the DAC is lost.

Positive Output Voltage

The output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages. To achieve a positive voltage output, an applied negative reference to the input of the DAC is preferred over the output inversion through an inverting amplifier because of the resistors' tolerance errors. To generate a negative reference, the reference can be level-shifted by an op amp such that the V_{OUT} and GND pins of the reference become the virtual ground and -2.5 V, respectively, as shown in Figure 37.



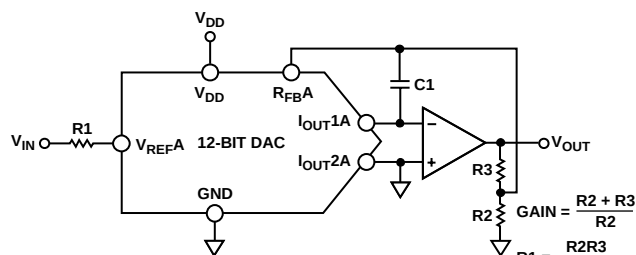
NOTES
1. ADDITIONAL PINS OMITTED FOR CLARITY.
2. C1 PHASE COMPENSATION (1pF TO 2pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

04461-036

Figure 37. Positive Voltage Output with Minimum of Components

ADDING GAIN

In applications where the output voltage must be greater than V_{IN} , gain can be added with an additional external amplifier, or it can be achieved in a single stage. Consider the effect of temperature coefficients of the thin film resistors of the DAC. Simply placing a resistor in series with the R_{FB} resistor causes mismatches in the temperature coefficients, resulting in larger gain temperature coefficient errors. Instead, the circuit in Figure 38 shows the recommended method for increasing the gain of the circuit. R_1 , R_2 , and R_3 should have similar temperature coefficients, but they need not match the temperature coefficients of the DAC. This approach is recommended in circuits where gains of greater than 1 are required.



NOTES
1. ADDITIONAL PINS OMITTED FOR CLARITY.
2. C1 PHASE COMPENSATION (1pF TO 2pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

04461-037

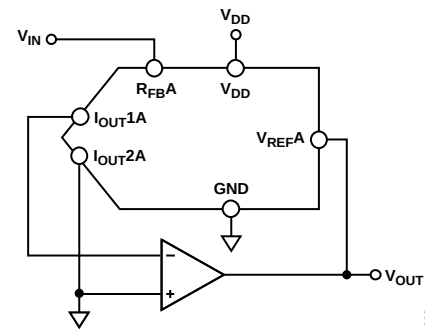
Figure 38. Increasing the Gain of the Current Output DAC

DIVIDER OR PROGRAMMABLE GAIN ELEMENT

Current-steering DACs are very flexible and lend themselves to many applications. If this type of DAC is connected as the feedback element of an op amp and R_{FB} is used as the input resistor, as shown in Figure 39, the output voltage is inversely proportional to the digital input fraction, D .

For D equal to $1 - 2^{-n}$, the output voltage is

$$V_{OUT} = -V_{IN}/D = -V_{IN}/(1 - 2^{-n})$$



NOTES
1. ADDITIONAL PINS OMITTED FOR CLARITY.

04461-038

Figure 39. Current-Steering DAC Used as a Divider or Programmable Gain Element

As D is reduced, the output voltage increases. For small values of the digital fraction, D , it is important to ensure that the amplifier does not saturate and that the required accuracy is met. For example, an 8-bit DAC driven with the binary code 0x10 (0001 0000)—that is, 16 decimal—in the circuit of Figure 39 should cause the output voltage to be 16 times V_{IN} . However, if the DAC has a linearity specification of ± 0.5 LSB, D can have a weight in the range of $15.5/256$ to $16.5/256$, so that the possible output voltage is in the range of $15.5 V_{IN}$ to $16.5 V_{IN}$ —an error of 3%, even though the DAC itself has a maximum error of 0.2%.

DAC leakage current is also a potential source of errors in divider circuits. The leakage current must be counterbalanced by an opposite current supplied from the op amp through the DAC. Because only a fraction, D , of the current into the V_{REFA} terminal is routed to the I_{OUT1A} terminal, the output voltage changes as follows:

$$\text{Output Error Voltage Due to DAC Leakage} = (\text{Leakage} \times R)/D$$

where R is the DAC resistance at the V_{REFA} terminal.

For a DAC leakage current of 10 nA, $R = 10$ k Ω , and a gain (that is, $1/D$) of 16, the error voltage is 1.6 mV.

REFERENCE SELECTION

When selecting a reference for use with the AD54xx series of current output DACs, pay attention to the reference's output voltage temperature coefficient specification. This parameter not only affects the full-scale error, but also can affect the linearity (INL and DNL) performance. The reference temperature coefficient should be consistent with the system accuracy specifications. For example, an 8-bit system required to hold its overall specification to within 1 LSB over the temperature range 0°C to 50°C dictates that the maximum system drift with temperature should be less than 78 ppm/°C. A 12-bit system with the same temperature range to overall specification within 2 LSB requires a maximum drift of 10 ppm/°C. Choosing a precision reference with a low output temperature coefficient minimizes this error source. Table 7 lists some of the references available from Analog Devices, Inc., that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. Because of the code-dependent output resistance of the DAC, the input offset voltage of an op amp is multiplied by the variable gain of the circuit. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the desired change in

output between the two codes and gives rise to a differential linearity error, which, if large enough, could cause the DAC to be nonmonotonic.

The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing in the feedback resistor, R_{FB} . Most op amps have input bias currents low enough to prevent significant errors in 12-bit applications.

Common-mode rejection of the op amp is important in voltage-switching circuits, because it produces a code-dependent error at the voltage output of the circuit. Most op amps have adequate common-mode rejection for use at 12-bit resolution.

Provided that the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew rate and settling time of a voltage-switching DAC circuit is largely determined by the output op amp. To obtain minimum settling time in this configuration, minimize capacitance at the V_{REF} node (the voltage output node in this application) of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design.

Most single-supply circuits include ground as part of the analog signal range, which in turn requires an amplifier that can handle rail-to-rail signals. Analog Devices offers a wide range of single-supply amplifiers, as listed in Table 8 and Table 9.

Table 7. Suitable ADI Precision References

Part No.	Output Voltage (V)	Initial Tolerance (%)	Temp Drift (ppm/°C)	I _{SS} (mA)	Output Noise (μV p-p)	Package
ADR01	10	0.05	3	1	20	SOIC-8
ADR01	10	0.05	9	1	20	TSOT-23, SC70
ADR02	5	0.06	3	1	10	SOIC-8
ADR02	5	0.06	9	1	10	TSOT-23, SC70
ADR03	2.5	0.10	3	1	6	SOIC-8
ADR03	2.5	0.10	9	1	6	TSOT-23, SC70
ADR06	3	0.10	3	1	10	SOIC-8
ADR06	3	0.10	9	1	10	TSOT-23, SC70
ADR431	2.5	0.04	3	0.8	3.5	SOIC-8
ADR435	5	0.04	3	0.8	8	SOIC-8
ADR391	2.5	0.16	9	0.12	5	TSOT-23
ADR395	5	0.10	9	0.12	8	TSOT-23

Table 8. Suitable ADI Precision Op Amps

Part No.	Supply Voltage (V)	V _{OS} (Max) (μV)	I _B (Max) (nA)	0.1 Hz to 10 Hz Noise (μV p-p)	Supply Current (μA)	Package
OP97	±2 to ±20	25	0.1	0.5	600	SOIC-8
OP1177	±2.5 to ±15	60	2	0.4	500	MSOP, SOIC-8
AD8551	2.7 to 5	5	0.05	1	975	MSOP, SOIC-8
AD8603	1.8 to 6	50	0.001	2.3	50	TSOT
AD8628	2.7 to 6	5	0.1	0.5	850	TSOT, SOIC-8

Table 9. Suitable ADI High Speed Op Amps

Part No.	Supply Voltage (V)	BW @ ACL (MHz)	Slew Rate (V/μs)	V _{OS} (Max) (μV)	I _B (Max) (nA)	Package
AD8065	5 to 24	145	180	1,500	6,000	SOIC-8, SOT-23, MSOP
AD8021	±2.5 to ±12	490	120	1,000	10,500	SOIC-8, MSOP
AD8038	3 to 12	350	425	3,000	750	SOIC-8, SC70-5
AD9631	±3 to ±6	320	1,300	10,000	7,000	SOIC-8

SERIAL INTERFACE

The AD5415 has an easy to use 3-wire interface that is compatible with SPI, QSPI, MICROWIRE, and most DSP interface standards. Data is written to the device in 16-bit words. Each 16-bit word consists of four control bits and 12 data bits, as shown in Figure 40.

Low Power Serial Interface

To minimize the power consumption of the device, the interface only powers up fully when the device is being written to, that is, on the falling edge of SYNC. The SCLK and DIN input buffers are powered down on the rising edge of SYNC.

DAC Control Bits C3 to C0

Control Bits C3 to C0 allow control of various functions of the DAC, as shown in Table 11. Default settings of the DAC at power on are as follows. Data is clocked into the shift register on falling clock edges, and daisy-chain mode is enabled. The device powers on with a zero-scale load to the DAC register and I_{OUT} lines. The DAC control bits allow the user to adjust certain features at power on. For example, daisy-chaining can be disabled when not in use, an active clock edge can be changed to a rising edge, and DAC output can be cleared to either zero scale or midscale. The user can also initiate a readback of the DAC register contents for verification purposes.

Control Register (Control Bits = 1101)

While maintaining software compatibility with single-channel current output DACs (AD5426/AD5433/AD5443), this DAC also features additional interface functionality. Simply set the control bits to 1101 to enter control register mode. Figure 41 shows the contents of the control register, the functions of which are described in the following sections.

SDO Control (SDO1 and SDO2)

The SDO bits enable the user to control the SDO output driver strength, disable the SDO output, or configure it as an open-drain driver. The strength of the SDO driver affects the timing of t_{12} and, when stronger, allows a faster clock cycle to be used. Note that when the SDO output is disabled the daisy-chain mode is also disabled.

Table 10. SDO Control Bits

SDO2	SDO1	Function
0	0	Full SDO driver
0	1	Weak SDO driver
1	0	SDO configured as open drain
1	1	Disable SDO output

Daisy-Chain Control (DSY)

DSY enables or disables daisy-chain mode. A 1 enables daisy-chain mode; a 0 disables it. When disabled, a readback request is accepted, SDO is automatically enabled, the DAC register contents of the relevant DAC are clocked out on SDO, and, when complete, SDO is disabled again.

Hardware CLR Bit (HCLR)

The default setting for the hardware CLR pin is to clear the registers and DAC output to zero code. A 1 in the HCLR bit clears the DAC outputs to midscale; a 0 clears them to zero scale.

Active Clock Edge (SCLK)

The default active clock edge is the falling edge. Write a 1 to this bit to clock data in on the rising edge; write a 0 to clock it in on the falling edge.

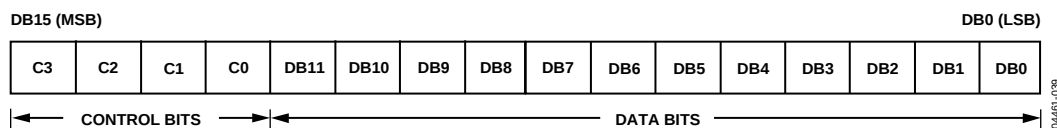


Figure 40. 12-Bit Input Shift Register Contents

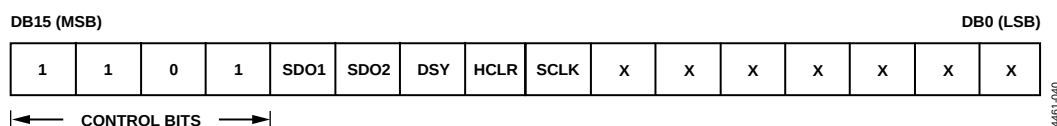


Figure 41. Control Register Loading Sequence

Table 11. DAC Control Bits

C3	C2	C1	C0	DAC	Function
0	0	0	0	A and B	No operation (power-on default)
0	0	0	1	A	Load and update
0	0	1	0	A	Initiate readback
0	0	1	1	A	Load input register
0	1	0	0	B	Load and update
0	1	0	1	B	Initiate readback
0	1	1	0	B	Load input register
0	1	1	1	A and B	Update DAC outputs
1	0	0	0	A and B	Load input registers
1	0	0	1	–	Disable daisy-chain
1	0	1	0	–	Clock data to shift register on rising edge
1	0	1	1	–	Clear DAC output to zero scale
1	1	0	0	–	Clear DAC output to midscale
1	1	0	1	–	Control word
1	1	1	0	–	Reserved
1	1	1	1	–	No operation

SYNC Function

SYNC is an edge-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device while SYNC is low. To start the serial data transfer, SYNC should be taken low, observing the minimum SYNC falling to SCLK falling edge setup time, t_4 .

Daisy-Chain Mode

Daisy-chain mode is the default mode at power on. To disable the daisy-chain function, write 1001 to the control word. In daisy-chain mode, the internal gating on SCLK is disabled. SCLK is continuously applied to the input shift register when SYNC is low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid for the next device on the falling edge of SCLK (default). By connecting this line to the SDIN input on the next device in the chain, a multidevice interface is constructed. For each device in the system, 16 clock pulses are required. Therefore, the total number of clock cycles must equal 16N, where N is the total number of devices in the chain. (See Figure 5.)

When the serial transfer to all devices is complete, SYNC should be taken high. This prevents additional data from being clocked into the input shift register. A burst clock containing the exact number of clock cycles can be used, after which SYNC is taken high. After the rising edge of SYNC, data is automatically transferred from each device's input shift register to the addressed DAC.

When control bits are 0000, the device is in no-operation mode. This might be useful in daisy-chain applications where the user does not want to change the settings of a particular DAC in the chain. Write 0000 to the control bits for that DAC, and subsequent data bits are ignored.

Standalone Mode

After power on, writing 1001 to the control word disables daisy-chain mode. The first falling edge of SYNC resets the serial clock counter to ensure that the correct number of bits are shifted in and out of the serial shift registers. A SYNC edge during the 16-bit write cycle causes the device to abort the current write cycle.

After the falling edge of the 16th SCLK pulse, data is automatically transferred from the input shift register to the DAC. For another serial transfer to take place, the counter must be reset by the falling edge of SYNC.

LDAC Function

The LDAC function allows asynchronous and synchronous updates to the DAC output. The DAC is asynchronously updated when this signal goes low. Alternatively, if this line is held permanently low, an automatic or synchronous update mode is selected, whereby the DAC is updated on the 16th clock falling edge when the device is in standalone mode, or on the rising edge of SYNC when the device is in daisy-chain mode.

Software LDAC Function

Load-and-update mode also functions as a software update function, irrespective of the voltage level on the LDAC pin.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5415 DAC is through a serial bus that uses standard protocol compatible with micro-controllers and DSP processors. The communication channel is a 3-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The AD5415 requires a 16-bit word, with the default being data valid on the falling edge of SCLK; however, this is changeable using the control bits in the data-word.

ADSP-21xx-to-AD5415 Interface

The ADSP-21xx family of DSPs is easily interfaced to the AD5415 DAC without the need for extra glue logic. Figure 42 is an example of an SPI interface between the DAC and the ADSP-2191. SCK of the DSP drives the serial data line, SDIN. SYNC is driven from a port line, in this case SPIxSEL.

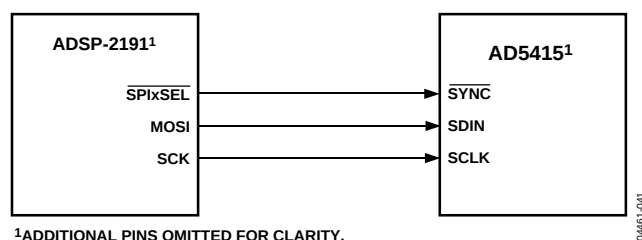


Figure 42. ADSP-2191 SPI-to-AD5415 Interface

A serial interface between the DAC and DSP SPORT is shown in Figure 43. In this interface example, SPORT0 is used to transfer data to the DAC shift register. Transmission is initiated by writing a word to the Tx register after SPORT is enabled. In a write sequence, data is clocked out on each rising edge of the DSP's serial clock and clocked into the DAC input shift register on the falling edge of its SCLK. The update of the DAC output takes place on the rising edge of the SYNC signal.

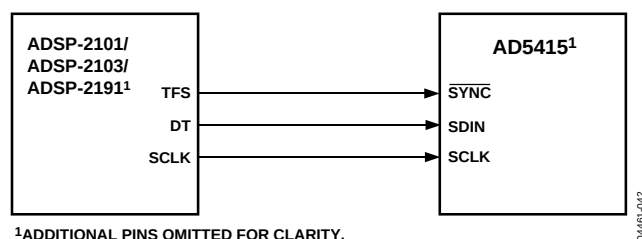


Figure 43. ADSP-2101/ADSP-2103/ADSP-2191 SPORT-to-AD5415 Interface

Communication between two devices at a given clock speed is possible when the following specifications are compatible: frame sync delay and frame sync setup-and-hold, data delay and data setup-and-hold, and SCLK width. The DAC interface expects a t_4 (SYNC falling edge to SCLK falling edge setup time) of 13 ns minimum. See the *ADSP-21xx User Manual* for information on clock and frame SYNC frequencies for the SPORT register.

Table 12 shows the setup for the SPORT control register.

Table 12. SPORT Control Register Setup

Name	Setting	Description
TFSW	1	Alternate framing
INVTFS	1	Active low frame signal
DTYPE	00	Right-justify data
ISCLK	1	Internal serial clock
TFSR	1	Frame every word
ITFS	1	Internal framing signal
SLEN	1111	16-bit data-word

ADSP-BF5xx-to-AD5415 Interface

The ADSP-BF5xx family of processors has an SPI-compatible port that enables the processor to communicate with SPI-compatible devices. A serial interface between the BlackFin® processor and the AD5415 DAC is shown in Figure 44. In this configuration, data is transferred through the MOSI (master output, slave input) pin. SYNC is driven by the SPIxSEL pin, which is a reconfigured programmable flag pin.

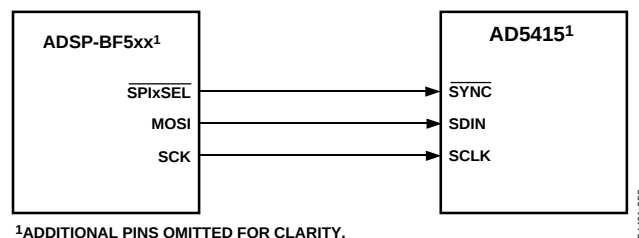


Figure 44. ADSP-BF5xx-to-AD5415 Interface

The ADSP-BF5xx processor incorporates channel synchronous serial ports (SPORT). A serial interface between the DAC and the DSP SPORT is shown in Figure 45. When SPORT is enabled, initiate transmission by writing a word to the Tx register. The data is clocked out on each rising edge of the DSP's serial clock and clocked into the DAC's input shift register on the falling edge of its SCLK. The DAC output is updated by using the transmit frame synchronization (TFS) line to provide a SYNC signal.

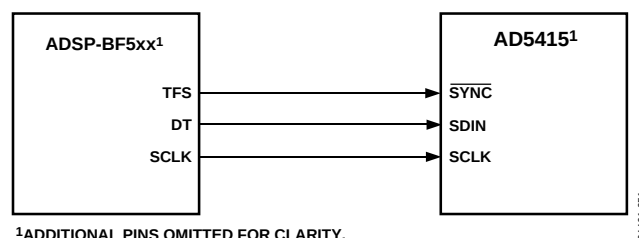


Figure 45. ADSP-BF5xx SPORT-to-AD5415 Interface

80C51/80L51-to-AD5415 Interface

A serial interface between the DAC and the 80C51 is shown in Figure 46. TxD of the 80C51 drives SCLK of the DAC serial interface, and RxD drives the serial data line, SDIN. P1.1 is a bit-programmable pin on the serial port and is used to drive SYNC. When data is to be transmitted to the switch, P1.1 is taken low. The 80C51/80L51 only transmits data in 8-bit bytes; therefore, only eight falling clock edges occur in the transmit cycle. To load data correctly to the DAC, P1.1 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. Data on RxD is clocked out of the microcontroller on the rising edge of TxD and is valid on the falling edge of TxD. As a result, no glue logic is required between the DAC and microcontroller interface. P1.1 is taken high following the completion of this cycle. The 80C51 provides the LSB of its SBUF register as the first bit in the data stream. The DAC input register requires its data with the MSB as the first bit received. The transmit routine should take this into account.

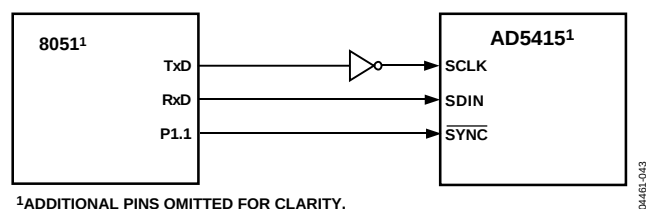


Figure 46. 80C51/80L51-to-AD5415 Interface

MC68HC11-to-AD5415 Interface

Figure 47 is an example of a serial interface between the DAC and the MC68HC11 microcontroller. The serial peripheral interface (SPI) on the MC68HC11 is configured for master mode (MSTR) = 1, clock polarity bit (CPOL) = 0, and the clock phase bit (CPHA) = 1. The SPI is configured by writing to the SPI control register (SPCR); see the *68HC11 User Manual*. SCK of the 68HC11 drives the SCLK of the DAC interface; the MOSI output drives the serial data line (SDIN) of the DAC.

The SYNC signal is derived from a port line (PC7). When data is being transmitted to the AD5415, the SYNC line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the DAC, leave PC7 low after the first eight bits are transferred and perform a second serial write operation to the DAC. PC7 is taken high at the end of this procedure.

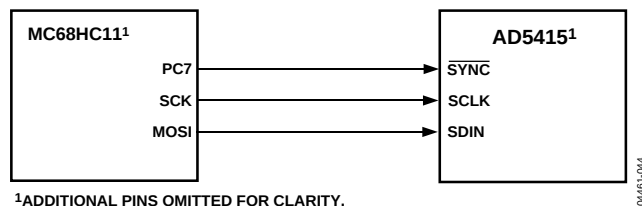


Figure 47. MC68HC11-to-AD5415 Interface

If the user wants to verify the data previously written to the input shift register, the SDO line can be connected to MISO of the MC68HC11, and, with SYNC low, the shift register clocks data out on the rising edges of SCLK.

MICROWIRE-to-AD5415 Interface

Figure 48 shows an interface between the DAC and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock, SK, and is clocked into the DAC input shift register on the rising edge of SK, which corresponds to the falling edge of the DAC's SCLK.

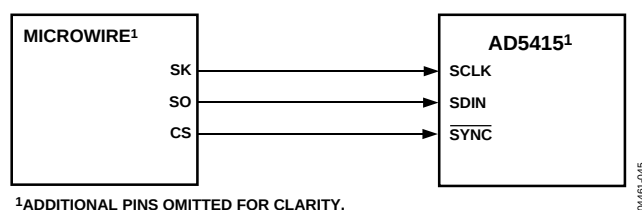


Figure 48. MICROWIRE-to-AD5415 Interface

PIC16C6x/7x-to-AD5415 Interface

The PIC16C6x/7x synchronous serial port (SSP) is configured as an SPI master with the clock polarity bit (CKP) = 0. This is done by writing to the synchronous serial port control register (SSPCON); see the *PIC16/17 Microcontroller User Manual*. In this example, I/O port RA1 is used to provide a SYNC signal and enable the serial port of the DAC. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, two consecutive write operations are required. Figure 49 shows the connection diagram.

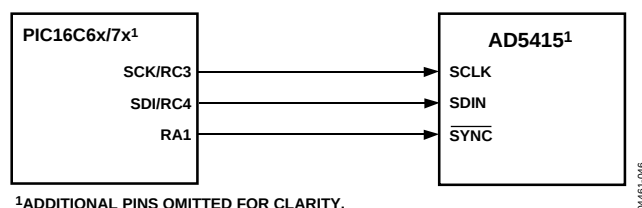


Figure 49. PIC16C6x/7x-to-AD5415 Interface

PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5415 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the DAC is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

The DAC should have ample supply bypassing of 10 μF in parallel with 0.1 μF on the supply located as close as possible to the package, ideally right up against the device. The 0.1 μF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), like the common ceramic types of capacitors that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching. Low ESR 1 μF to 10 μF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

Components, such as clocks, that produce fast-switching signals should be shielded with digital ground to avoid radiating noise to other parts of the board, and they should never be run near the reference inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is by far the best, but its use is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the soldered side.

It is good practice to use compact, minimum lead length PCB layout design. Leads to the input should be as short as possible to minimize IR drops and stray inductance.

The PCB metal traces between V_{REF} and R_{FB} should also be matched to minimize gain error. To maximize high frequency performance, the I-to-V amplifier should be located as close as possible to the device.

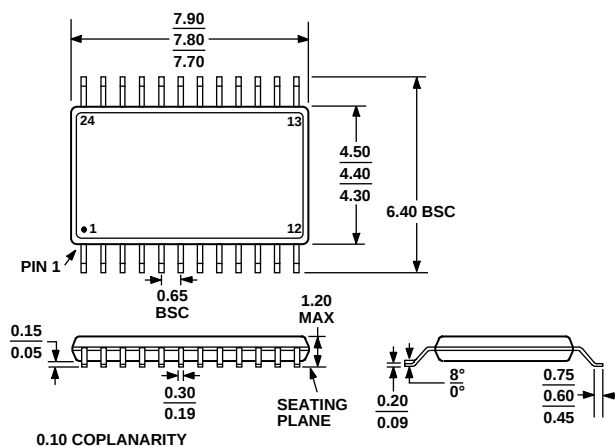
OVERVIEW OF AD54XX DEVICES

Table 13.

Part No.	Resolution	No. DACs	INL (LSB)	Interface	Package ¹	Features
AD5424	8	1	±0.25	Parallel	RU-16, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5426	8	1	±0.25	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5428	8	2	±0.25	Parallel	RU-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5429	8	2	±0.25	Serial	RU-10	10 MHz BW, 50 MHz serial
AD5450	8	1	±0.25	Serial	UJ-8	10 MHz BW, 50 MHz serial
AD5432	10	1	±0.5	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5433	10	1	±0.5	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5439	10	2	±0.5	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5440	10	2	±0.5	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5451	10	1	±0.25	Serial	UJ-8	10 MHz BW, 50 MHz serial
AD5443	12	1	±1	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5444	12	1	±0.5	Serial	RM-8	10 MHz BW, 50 MHz serial
AD5415	12	2	±1	Serial	RU-24	10 MHz BW, 50 MHz serial
AD5405	12	2	±1	Parallel	CP-40	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5445	12	2	±1	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5447	12	2	±1	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5449	12	2	±1	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5452	12	1	±0.5	Serial	UJ-8, RM-8	10 MHz BW, 50 MHz serial
AD5446	14	1	±1	Serial	RM-8	10 MHz BW, 50 MHz serial
AD5453	14	1	±2	Serial	UJ-8, RM-8	10 MHz BW, 50 MHz serial
AD5553	14	1	±1	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5556	14	1	±1	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5555	14	2	±1	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5557	14	2	±1	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5543	16	1	±2	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5546	16	1	±2	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5545	16	2	±2	Serial	RU-16	4 MHz BW, 50 MHz serial clock
AD5547	16	2	±2	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ pulse width

¹ RU = TSSOP, CP = LFCSP, RM = MSOP, UJ = TSOT.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 50. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Resolution	INL (LSB)	Temperature Range	Package Description	Package Option
AD5415YRU	12	±1	−40°C to +125°C	24-Lead TSSOP	RU-24
AD5415YRU-REEL7	12	±1	−40°C to +125°C	24-Lead TSSOP	RU-24
AD5415YRUZ	12	±1	−40°C to +125°C	24-Lead TSSOP	RU-24
AD5415YRUZ-REEL	12	±1	−40°C to +125°C	24-Lead TSSOP	RU-24
AD5415YRUZ-REEL7	12	±1	−40°C to +125°C	24-Lead TSSOP	RU-24
EV-AD5415/49SDZ				Evaluation Board	

¹ Z = RoHS Compliant Part.

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