

**FEATURES**
**Single +5 V Supply**
**On-Chip  $\pi/4$  DQPSK Modulator**
**Modulator Bypass Analog Mode**
**Root-Raised Cosine Tx Filters,  $\alpha = 0.35$** 
**Two 10-Bit D/A Converters**
**4th Order Reconstruction Filters**
**Differential Analog Outputs**
**On-Chip Ramp Up/Down Power Control**
**On-Chip Tx Offset Calibration**
**Dual Mode Operation, Analog and Digital**
**Very Low Power Dissipation, 30 mW typical**
**Power Down Mode < 10  $\mu$ A**
**On-Chip Voltage Reference**
**24-Pin SSOP**
**APPLICATIONS**
**American Digital Cellular Telephony**
**American Analog Cellular Telephony**
**GENERAL DESCRIPTION**

The AD7011 is a complete low power, CMOS,  $\pi/4$  DQPSK modulator with single +5 V power supply. The part is designed to perform the baseband conversion of I and Q transmit waveforms in accordance with the American Digital Cellular Telephone system (TIA IS-54).

The on-chip  $\pi/4$  Differential Quadrature Phase Shift Keying (DQPSK) digital modulator, which includes the root raised cosine filters, generates I and Q data in response to the transmit data stream. The AD7011 also contains ramp control envelope logic to shape the I and Q output waveforms when ramping up or down at the beginning or end of a transmit burst.

Besides providing all the necessary logic to perform  $\pi/4$  DQPSK modulation, the part also provides reconstruction filters to

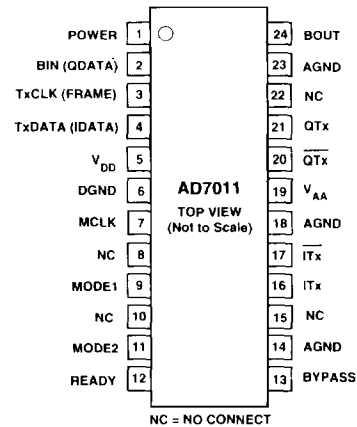
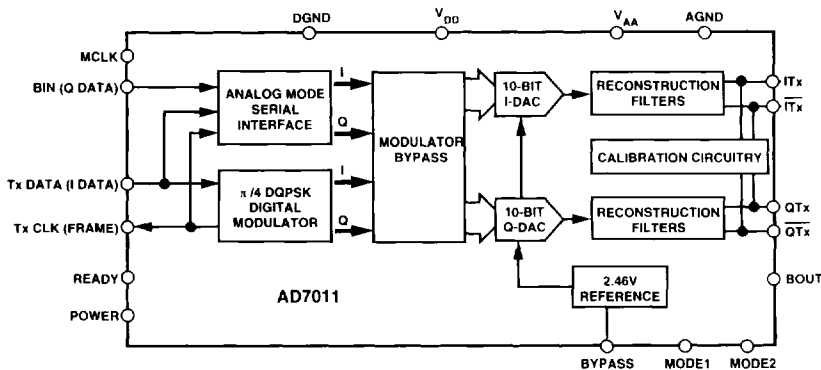
smooth the DAC outputs, providing continuous time analog outputs. The AD7011 generates differential analog outputs for both the I and Q signals.

As it is a necessity for all digital mobile systems to use the lowest possible power, the device has transmit and receive power-down options. The AD7011 is housed in a space efficient 24-pin SSOP (Shrink Small Outline Package).

**ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option*
AD7011ARS	-40°C to +85°C	Shrink Small Outline Package	RS-24

\*For outline information see Package Information section.

**SSOP PIN CONFIGURATION**

**FUNCTIONAL BLOCK DIAGRAM**


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COMMUNICATIONS (WIRELESS, DDS &amp; RF) CIRCUITS 17-17

# AD7011—SPECIFICATIONS<sup>1</sup>

( $V_{AA} = V_{DD} = +5\text{ V} \pm 10\%$ ; Test = AGND = DGND = 0 V; Digital Mode,  $f_{MCLK} = 3.1104\text{ MHz}$ ; Analog Mode,  $f_{MCLK} = 2.56\text{ MHz}$ , POWER =  $V_{DD}$ . All specifications are  $T_{MIN}$  to  $T_{MAX}$  unless otherwise noted.)

Parameter	AD7011ARS	Units	Test Conditions/Comments
<b>DIGITAL MODE TRANSMIT SPECIFICATIONS</b>			
Number of Channels	2		(ITx $\overline{\text{ITx}}$ ) and (QTx $\overline{\text{QTx}}$ )
Output Signal Range	$V_{REF} \pm V_{REF}/4$	Volts	For Each Analog Output
Differential Output Range	$\pm V_{REF}/2$	Volts	I Channel = (ITx $\overline{\text{ITx}}$ ) and Q Channel = (QTx $\overline{\text{QTx}}$ )
Signal Vector Magnitude <sup>2</sup>	$0.875 \pm 7.5\%$	Volts max	Measured Differentially
Error Vector Magnitude <sup>2</sup>	1	% rms typ	
	2.5	% rms max	
Offset Vector Magnitude <sup>2</sup>	0.5	% typ	
	2.5	% max	
IS-54 Spurious Power <sup>2, 3</sup>			
@ 30 kHz	35	dB typ	
	-30	dB max	
@ 60 kHz	70	dB typ	
	65	dB max	
@ 90 kHz, 120 kHz	75	dB typ	
	70	dB max	
<b>ANALOG MODE SPECIFICATIONS</b>			
No. of Channels	2		(ITx $\overline{\text{Tx}}$ ) and (QTx $\overline{\text{QTx}}$ )
Resolution	10	Bits	
Output Signal Range	$V_{REF} \pm V_{REF}/3$	Volts	For Each Analog Output
Differential Output Range	$\pm 2V_{REF}/3$	Volts	I Channel = (ITx $\overline{\text{ITx}}$ ) and Q Channel = (QTx $\overline{\text{QTx}}$ )
DAC Update Rate	160	kHz	MCLK/16; $f_{MCLK} = 2.56\text{ MHz}$ Generating a 10 kHz Sine Wave
SNR	60	dB typ	
	55	dB min	
Differential Offset Error	$\pm 15$	mV max	Post Calibration
Group Delay Matching Between I & Q Outputs	30	ns typ	
Coding	Twos Complement		
Maximum and Minimum DAC Codes <sup>4</sup>	+450/-450	max/min	
<b>REFERENCE &amp; CHANNEL SPECIFICATIONS</b>			
Reference, $V_{REF}$	2.46	Volts	
Reference Accuracy	$\pm 5$	%	
I and Q Gain Matching	$\pm 0.2$	dB max	Measured @ 10 kHz
Power-Down Option	Yes		Power = 0 V
<b>LOGIC INPUTS</b>			
$V_{INH}$ , Input High Voltage	$V_{DD} - 0.9$	V min	
$V_{INL}$ , Input Low Voltage	0.9	V max	
$I_{INH}$ , Input Current	10	$\mu\text{A}$ max	
$C_{IN}$ , Input Capacitance	10	pF max	
<b>LOGIC OUTPUTS</b>			
$V_{OH}$ , Output High Voltage	$V_{DD} - 0.4$	V min	$ I_{OUT}  \leq 40\ \mu\text{A}$
$V_{OL}$ , Output Low Voltage	0.4	V max	$ I_{OUT}  \leq 1.6\ \text{mA}$
<b>POWER SUPPLIES</b>			
$V_{DD}$	4.5/5.5	V min/V max	
$I_{DD}$			
Transmit Section Active	8	mA max	POWER = $V_{DD}$
	6	mA typ	
Transmit Section Powered Down <sup>5</sup>	35	$\mu\text{A}$ max	MCLK Active
	5	$\mu\text{A}$ max	MCLK Inactive

## NOTES

<sup>1</sup>Operating temperature ranges as follows: A Version:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup>See terminology.

<sup>3</sup>Measured in continuous transmission and Burst Mode with the I and Q channels ramping up and down at the beginning and end of a burst.

<sup>4</sup>Headroom must be allowed for the transmit DACs such that offsets in I & Q transmit channels can be calibrated out. Therefore, the full range of the I and Q DACs are not available to the user. The user should ensure that binary codes greater than or less than the maximum or minimum are not loaded into the I or Q DACs.

<sup>5</sup>Measured while the digital inputs to the transmit interface are static and equal to 0 V or  $V_{DD}$ .

Specifications subject to change without notice.