Four Channel, Simultaneous Sampling, Fast, 14-Bit ADC

Preliminary Technical Data — AD7865

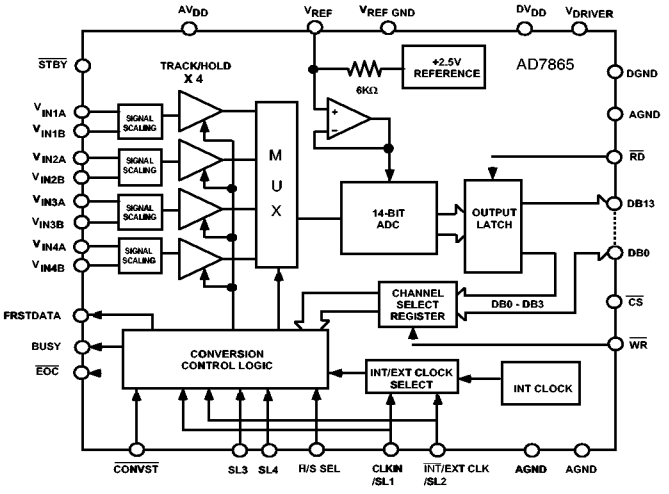
FEATURES

Fast (2.5 µs) 14-Bit ADC
Four Simultaneously Sampled Inputs
Four Track/Hold Amplifiers
0.35 µs Track/Hold Acquisition Time
2.5 µs Conversion Time per Channel
HW/SW Select of Channel Sequence for conversion
Single Supply Operation
Selection of Input Ranges: ±10 V, ±5 V
High Speed Parallel Interface
which also allows Interfacing to 3V processors
Low Power, 90mW typ
Power Saving Mode, 5 µA typ
Overvoltage Protection on Analog Inputs

APPLICATIONS

AC Motor Control
Uninterruptible Power Supplies
Industrial Power Meters/Monitors
Data Acquisition Systems
Communications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7865 is a fast, low power, four-channel simultaneous sampling 14-bit A/D converter that operates from a single +5 V supply. The part contains a 2.5µs successive approximation ADC, four track/hold amplifiers, 2.5V reference, on chip clock oscillator, signal conditioning circuitry and a high speed parallel interface. The input signals on four channels are sampled simultaneously thus preserving the relative phase information of the signals on the four analog inputs. The part accepts analog input ranges of ±10 V or ±5V. Overvoltage protection on the analog inputs for the part allows the input voltage to go to ±20 V without damaging the parts or affecting a conversion in progress.

The part allows any subset of the 4 channels to be converted in order to maximize the throughput rate on the selected sequence. The channels to be converted can be selected either via hardware (channel select input pins) or via software (programming the channel select register).

A single conversion start signal ($\overline{\text{CONVST}}$) places all the track/holds into hold simultaneously and initiates conversion sequence for the selected channels. The $\overline{\text{EOC}}$ signal indicates the end of each individual conversion in the selected conversion sequence. The BUSY signal indicates the end of the conversion sequence.

Data is read from the part via a 14-bit parallel data bus using the standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals. Maximum throughput for a single channel is 350 ksps. For all four channels the maximum throughput is 100 ksps.

The AD7865 is available in a small (0.3 sq.inch area) 44-pin PQFP.

PRODUCT HIGHLIGHTS

1. The AD7865 features four Track/Hold amplifiers and a fast (2.5µs) ADC allowing simultaneous sampling and then conversion of any subset of the four channels.
2. The AD7865 operates from a single +5 V supply and consumes only 90 mW typ making it ideal for low power and portable applications.
3. The part offers a high speed parallel interface for easy connection to microprocessors, microcontrollers and digital signal processors.
4. The part can be hardwired for either ±10V or ±5V input ranges.
5. The part features very tight aperture delay matching between the four input sample & hold amplifiers.

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AD7865–SPECIFICATIONS[1] (V_{DD}= +5 V ±5%, AGND=DGND= 0V, V_{REF} = Internal. Clock = Internal, All Specifications T_{MIN} to T_{MAX} unless otherwise noted).

Parameter	A[1] Version[1]	B Version	Units	Test Conditions/Comments
SAMPLE AND HOLD				
-3dB Full Power Bandwidth	3	3	MHz typ	
Aperture Delay	20	20	ns max	
Aperture Jitter	50	50	ps typ	
Aperture Delay Matching	4	4	ns max	
DYNAMIC PERFORMANCE[2]				f_{IN} = 100 kHz, f_S = 350 ksps
Signal to (Noise+Distortion) Ratio[3]				
@ 25°C	80	80	dB min	
Tmin to Tmax	78	80	dB min	
Total Harmonic Distortion[3]	-86	-90	dB max	
Peak Harmonic or Spurious Noise[3]	-86	-90	dB max	
Intermodulation Distortion[3]				fa = 49kHz, fb = 50kHz
2nd Order Terms	-86	-90	dB typ	
3rd Order Terms	-86	-90	dB typ	
Channel to Channel Isolation[3]	-86	-90	dB max	f_{IN} = 50kHz Sine Wave
DC ACCURACY				Any Channel
Resolution	14	14	Bits	
Relative Accuracy (INL)[3]	±2	±1.5	LSB max	
Differential Nonlinearity (DNL)[3]	±0.9	±0.9	LSB max	No missing codes guaranteed
Positive Gain Error[3]	±4	±4	LSB max	
Positive Gain Error Match[3]	2	2	LSB max	
Negative Gain Error[3]	±4	±4	LSB max	
Negative Gain Error Match[3]	2	2	LSB max	
Bipolar Zero Error	±4	±4	LSB max	
Bipolar Zero Error Match	2	2	LSB max	
ANALOG INPUTS				
Input Voltage Range	±5, ±10	±5, ±10	Volts	
Input Resistance	9, 18	9, 18	kΩ min	
REFERENCE INPUT/OUTPUT				
V_{REF} IN Input Voltage Range	2.375/2.625	2.375/2.625	Vmin/Vmax	2.5V ± 5%
V_{REF} IN Input Capacitance[4]	10	10	pF max	
V_{REF} OUT Output Voltage	2.5	2.5	V nom	
V_{REF} OUT Error @ 25°C	±10	±10	mV max	
V_{REF} OUT Error Tmin to Tmax	±20	±20	mV max	
V_{REF} OUT Temperature Coefficient	25	25	ppm/°C typ	
V_{REF} OUT Output Impedance	6	6	kΩ typ	See Reference Section
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5V±5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5V±5%
Input Current, I_{IN}	±10	±10	µA max	
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	4.0	4.0	V min	I_{SOURCE} = 400µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6mA
DB11 - DB0				
High Impedance				
Leakage Current	±10	±10	µA max	
Capacitance[4]	10	10	pF max	
Output Coding	Two's Complement			

AD7865–SPECIFICATIONS ($V_{D=}$ = +5 V ±5%, AGND=DGND= 0V, V_{REF} = Internal, Clock = Internal. All Specifications T_{MIN} to T_{MAX} unless otherwise noted).

Parameter	A Version[1]	B Version	Units	Test Conditions/Comments
CONVERSION RATE				
Conversion Time	2.5	2.5	µs max	For Single Channel
Track/Hold Acquisition Time[2,3]	0.35	0.35	µs max	
Throughput Time	350	350	ksps max	For Single Channel
Throughput Time	100	100	ksps max	For All Four Channels
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for specified performance
I_{DD}				(5 µA typ) Logic Inputs = 0V or V_{DD}
Normal Mode	24	24	mA max	
Standby Mode	20	20	µA max	
Power Dissipation				
Normal Mode	120	120	mW max	Typically 90 mW. V_{DD} =+5V
Standby Mode	100	100	µW max	Typically 20 µW

NOTES
[1]Temperature Ranges are as follows : A,B Versions: -40°C to +85°C.
[2] Performance measured through full channel (SHA and ADC)
[3] See Terminology
[4] Sample tested @ 25°C to ensure compliance.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Input Ranges	Relative Accuracy	Temperature Range	Package Option *
AD7865AS	±5V, ±10V	±2 LSB	-40°C to +85°C[1]	S-44
AD7865BS	±5V, ±10V	±1.5 LSB	-40°C to +85°C	S-44

*S = PQFP

TIMING CHARACTERISTICS[1,2]

($V_{D=}$ = +5 V ±5%, AGND=DGND= 0V, V_{REF} = Internal, Clock = Internal, All Specifications T_{MIN} to T_{MAX} unless otherwise noted).

Parameter	A, B Versions	Units	Test Conditions/Comments
t_{CONV}	2.5	µs max	Conversion Time, Internal Clock
	15	clock cycles	Conversion Time, External Clock
	3	µs max	CLKIN = 5MHz
t_{ACQ}	0.35	µs max	Acquisition Time
t_{BUSY}	No. of Channels		Selected number of channels multiplied by
	x (t_{CONV} + t_9) - t_9	µs max	(t_{CONV} + $\overline{EOC}$ pulse width) - $\overline{EOC}$ pulse width
$t_{WAKE-UP}$ - External Vref	2	µs max	$\overline{STBY}$ rising edge to $\overline{CONVST}$ rising edge
$t_{WAKE-UP}$ - InternalVref [5]	6	ms max	$\overline{STBY}$ rising edge to $\overline{CONVST}$ rising edge
t_1	35	ns min	$\overline{CONVST}$ Pulse Width
t_2	70	ns min	$\overline{CONVST}$ rising edge to BUSY rising edge
Read Operation			
t_3	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_4	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_5	35	ns min	Read Pulse Width
t_6 [3]	35	ns max	Data Access Time After Falling Edge of $\overline{RD}$, V_{DRIVE} = 5V
	40	ns max	Data Access Time After Falling Edge of $\overline{RD}$, V_{DRIVE} = 3V
t_7 [4]	5	ns min	Bus Relinquish Time After Rising Edge of $\overline{RD}$
	30	ns max	
t_8	10	ns min	Time between consecutive reads
t_9	75	ns min	$\overline{EOC}$ Pulse Width
	180	ns max	
t_{10}	70	ns max	$\overline{RD}$ rising edge to FRSTDATA edge (rising or falling)
t_{11}	15	ns max	$\overline{EOC}$ falling edge to FRSTDATA falling delay
t_{12}	0	ns min	$\overline{EOC}$ to $\overline{RD}$ delay
Write Operation			
t_{13}	20	ns min	$\overline{WR}$ Pulse Width
t_{14}	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_{15}	0	ns min	$\overline{WR}$ to $\overline{CS}$ Hold Time
t_{16}	5	ns min	Input data Set up Time ot Rising edge of $\overline{WR}$
t_{17}	5	ns min	Input data Hold Time

NOTES

[1] Sample tested at 25°C to ensure compliance. All input signals are measured with tr = tf = 1ns (10% to 90% of +5V) and timed from a voltage level of +1.6 V.

[2] See Figures 7, 8 and 9.

[3] Measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8 V or 2.0 V.

[4] These times are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

[5] Refer to the section, "Standby Mode Operation". The MAX specification of 6ms is valid when using a 0.1µF decoupling capacitor on the V_{REF} pin.

Specifications subject to change without notice.

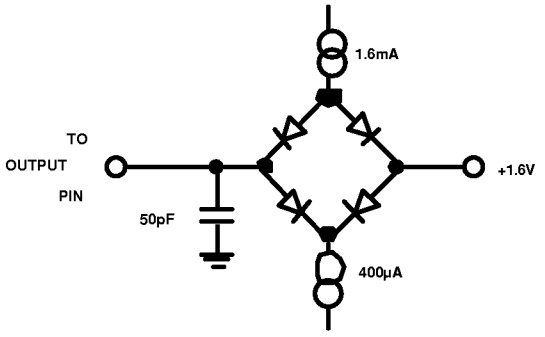


Figure 2. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

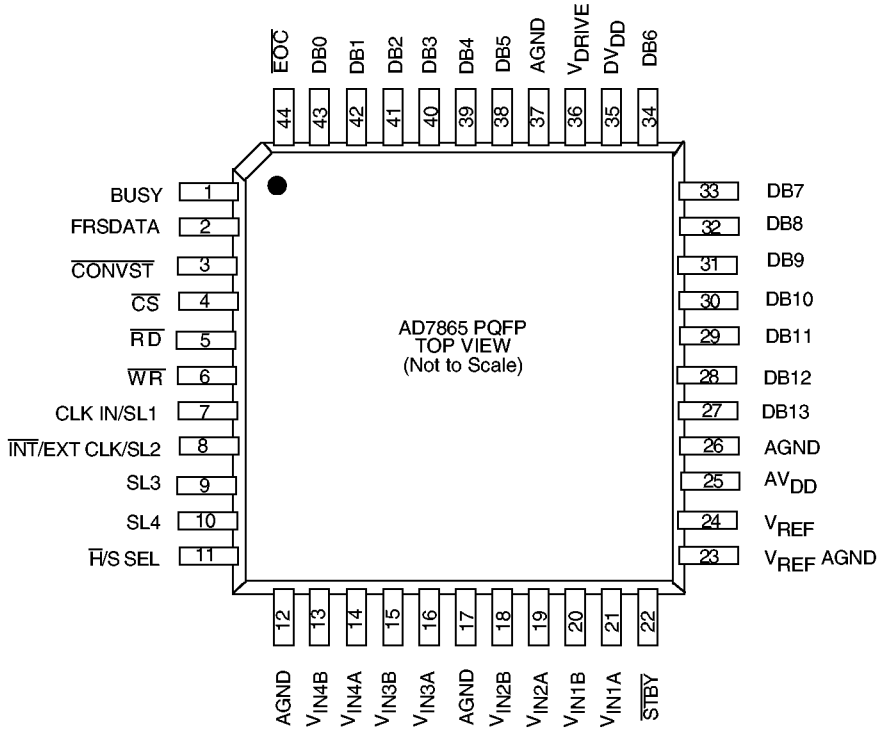
V_{DD} to AGND ..... -0.3 V to +7V
V_{DD} to DGND ..... -0.3 V to +7V
Analog Input Voltage to AGND.....±20V
Reference Input Voltage to AGND .....-0.3V to V_{DD}+0.3V
Digital Input Voltage to DGND .....-0.3V to V_{DD}+0.3V
Digital Output Voltage to DGND .....-0.3V to V_{DD}+0.3V
Operating Temperature Range
Commercial (A, B Version) ..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....+150°C
PQFP Package, Power Dissipation.....450mW
θ_{JA} Thermal Impedance.....95°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec).....+215°C
Infared (15 sec)..... .....+220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7864 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
PQFP



PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	BUSY	Busy Output. The busy output is triggered high by the rising edge of $\overline{\text{CONVST}}$ and remains high until conversion is completed on all selected channels.
2	FRSTDATA	First Data Output. FRSTDATA is a logic output which, when high, indicates that the Output Data Register Pointer is addressing Register 1 - See Accessing the Output Data Registers
3	$\overline{\text{CONVST}}$	Convert Start Input. Logic Input. A low to high transition on this input puts all track/hold's into their hold mode and starts conversion on the selected channels. In addition, the state of the Channel Sequence Selection is also latched on the rising edge of $\overline{\text{CONVST}}$.
4	$\overline{\text{CS}}$	Chip Select Input. Active low logic input. The device is selected when this input is active.
5	$\overline{\text{RD}}$	Read Input. Active low logic input which is used in conjunction with $\overline{\text{CS}}$ low to enable the data outputs. Ensure the $\overline{\text{WR}}$ pin is at logic high while performing a read operation.
6	$\overline{\text{WR}}$	Write Input. A rising edge on the $\overline{\text{WR}}$ input, with $\overline{\text{CS}}$ low and $\overline{\text{RD}}$ high, latches the logic state on DB0 to DB3 into the channel select register.
7	CLK IN/SL1	Conversion Clock Input/Hardware Channel Select. The function of this pin depends upon the $\overline{\text{H}}$/S SEL input. When the $\overline{\text{H}}$/S SEL input is high (choosing software control of the channel selection sequence), this pin assumes its CLK IN function. CLK IN is an externally applied clock which allows the user to control the conversion rate of the AD7865. Each conversion needs fifteen clock cycles in order for the conversion to be completed. The clock should have a duty cycle which is no worse than 60/40. See Using an External Clock. When the $\overline{\text{H}}$/S SEL input is low (choosing hardware control of the channel conversion sequence), this pin assumes its Hardware Channel Select function. The SL1 input determines whether Channel 1 is included in the channel conversion sequence. The selection is latched on the rising edge of $\overline{\text{CONVST}}$. See Selecting a conversion sequence.
8	$\overline{\text{INT}}$/EXT CLK/SL2	Internal/External Clock/Hardware Channel Select. The function of this pin depends upon the $\overline{\text{H}}$/S SEL input. When the $\overline{\text{H}}$/S SEL input is high (choosing software control of the channel selection sequence), this pin assumes its $\overline{\text{INT}}$/EXT CLK function. When $\overline{\text{INT}}$/EXT CLK is at a logic 0, the AD7865 uses its internally generated master clock. When $\overline{\text{INT}}$/EXT CLK is at logic 1, the master clock is generated externally to the device and applied to CLK IN. When the $\overline{\text{H}}$/S SEL input is low (choosing hardware control of the channel conversion sequence), this pin assumes its Hardware Channel Select function. The SL2 input determines whether Channel 2 is included in the channel conversion sequence. The selection is latched on the rising edge of $\overline{\text{CONVST}}$. See Selecting a conversion sequence.
9 -10	SL3 - SL4	Hardware Channel Select. The SL3 input determines whether Channel 3 is included in the channel conversion sequence while SL4 determines whether Channel 4 is included in the channel conversion sequence. The selection is latched on the rising edge of $\overline{\text{CONVST}}$. See Selecting a conversion sequence.
11	$\overline{\text{H}}$/S SEL	Hardware/Software Select Input. When this pin is at a logic 0, the AD7865 conversion sequence selection is controlled via the SL1 - SL4 input pins. When this pin is at logic 1, the sequence is controlled via the channel select register. See Selecting a conversion sequence.

12	AGND	Analog Ground. General analog ground. This AGND pin should be connected to the system's AGND plane.
13-16	V_{IN4X}, V_{IN3X}	Analog Inputs. Each input can be configured for ±5 V or ±10 V operation. For ±5 V operation, the V_{INXA} and V_{INXB} inputs are tied together and the input voltage is applied to both. For ±10V operation, the V_{INXB} input is tied to AGND and the input voltage is applied to the V_{INXA} input. The V_{INXA} and V_{INXB} inputs are symmetrical and fully interchangeable. See Analog Input Section.
17	AGND	Analog Ground. Analog Ground reference for the attenuator circuitry. This AGND pin should be connected to the system's AGND plane.
18-21	V_{IN2X}, V_{IN1X}	Analog Inputs. Each input can be configured for ±5 V or ±10 V operation. For ±5 V operation, the V_{INXA} and V_{INXB} inputs are tied together and the input voltage is applied to both. For ±10V operation, the V_{INXB} input is tied to AGND and the input voltage is applied to the V_{INXA} input. The V_{INXA} and V_{INXB} inputs are symmetrical and fully interchangeable. See Analog Input Section.
22	$\overline{STBY}$	Standby Mode Input. TTL-compatible input which is used to put the device into the power save or standby mode. The $\overline{STBY}$ input is high for normal operation and low for standby operation.
23	V_{REF} AGND	Reference Ground. Ground reference for the part's on-chip reference buffer. The V_{REF}AGND pin should be connected to the system's AGND plane.
24	V_{REF}	Reference Input/Output. This pin is provides access to the internal reference (2.5V ± 20mV) and also allows the internal reference to be overdriven by an external reference source (2.5V ± 5%) . A 0.1µF decoupling capacitor should be connected between this pin and AGND.
25	AV_{DD}	Analog Positive Supply Voltage, +5.0 V ±5%.
26	AGND	Analog Ground. Analog Ground reference for the DAC circuitry.
27 - 34	DB13- DB6	Data Bit 13 is the MSB, followed by Data Bit 12 to Data Bit 6. Three-state TTL outputs. Output coding is 2's complement.
35	DV_{DD}	Positive Supply Voltage for Digital section, +5.0V ±5%. A 0.1µF decoupling capacitor should be connected between this pin and AGND. Both DV_{DD} and AV_{DD} should be externally tied together.
36	V_{DRIVE}	This pin provides the positive supply voltage for the output drivers (DB0 to DB11), BUSY, $\overline{EOC}$ and FRSTDATA. It is normally tied to DV_{DD}. V_{DRIVE} should be decoupled with a 0.1µF capacitor. It allows improved performance when reading during the conversion sequence. Also, the output data drivers may be powered by a 3V±10% supply to facilitate interfacing to 3V processors and DSPs.
37	DGND	Digital Ground. Ground reference for Digital circuitry. This DGND pin should be connected to the system's AGND plane at the AGND pin.
38, 39	DB5, DB4	Data Bit 5 to Data Bit 4. Three-state TTL outputs.
40 - 43	DB3 - DB0	Data Bit 3 to Data Bit 0. Bidirectional data pins. When a read operation takes place, these pins are Three-state TTL outputs. The channel select register is programmed with the data on the DB0 - DB3 pins with standard $\overline{CS}$ and $\overline{WR}$ signals. DB0 represents channel 1 and DB3 represents channel 4.
44	$\overline{EOC}$	End-of-Conversion. Active low logic output indicating conversion status. The end of each conversion in a conversion sequence is indicated by a low-going pulse on this line.