Ultralow Distortion, Wide Bandwidth Voltage Feedback Op Amps

AD9631/AD9632

FEATURES

Wide Bandwidth
- AD9631, G = +1
- AD9632, G = +2
- Small Signal
  - 320 MHz
  - 250 MHz
- Large Signal (4 V p-p)
  - 175 MHz
  - 180 MHz

Ultralow Distortion (SFDR), Low Noise
- –113 dBc Typ @ 1 MHz
- –95 dBc Typ @ 5 MHz
- –72 dBc Typ @ 20 MHz
- 46 dBm Third Order Intercept @ 25 MHz
- 7.0 nV/$\sqrt{Hz}$ Spectral Noise Density

High Speed
- Slew Rate 1300 V/μs
- Settling 16 ns to 0.01%, 2 V Step
- ±3 V to ±5 V Supply Operation
- 17 mA Supply Current

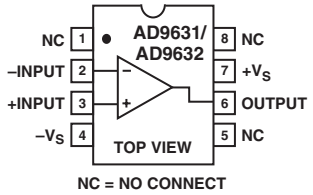
APPLICATIONS

- ADC Input Driver
- Differential Amplifiers
- IF/RF Amplifiers
- Pulse Amplifiers
- Professional Video
- DAC Current to Voltage
- Baseband and Video Communications
- Pin Diode Receivers
- Active Filters/Integrators/Log Amps

GENERAL DESCRIPTION

The AD9631 and AD9632 are very high speed and wide bandwidth amplifiers. They are an improved performance alternative to the AD9621 and AD9622. The AD9631 is unity gain stable. The AD9632 is stable at gains of 2 or greater. Using a voltage feedback architecture, the AD9631/AD9632's exceptional settling time, bandwidth, and low distortion meet the requirements of many applications that previously depended on current feedback amplifiers. Its classical op amp structure works much more predictably in many designs.

PIN CONFIGURATION
8-Lead PDIP (N) and SOIC (R) Packages



A proprietary design architecture has produced an amplifier that combines many of the best characteristics of both current feedback and voltage feedback amplifiers. The AD9631 and AD9632 exhibit exceptionally fast and accurate pulse response (16 ns to 0.01%) as well as extremely wide small signal and large signal bandwidth and ultralow distortion. The AD9631 achieves –72 dBc at 20 MHz, and 320 MHz small signal and 175 MHz large signal bandwidths.

These characteristics position the AD9631/AD9632 ideally for driving flash as well as high resolution ADCs. Additionally, the balanced high impedance inputs of the voltage feedback architecture allow maximum flexibility when designing active filters.

The AD9631/AD9632 are offered in the industrial (–40°C to +85°C) temperature range. They are available in PDIP and SOIC.

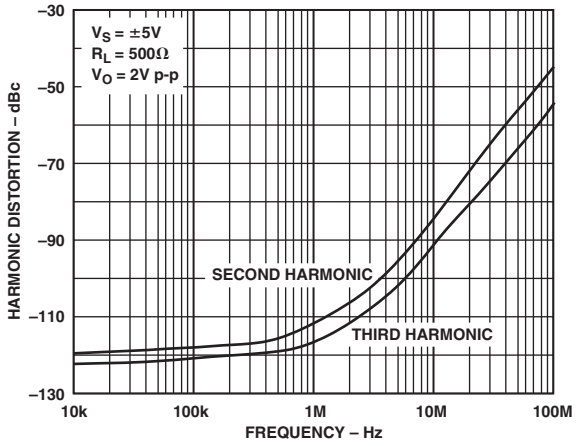


Figure 1. AD9631 Harmonic Distortion vs. Frequency, G = +1

REV. C

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AD9631/AD9632–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5$ V; $R_{LOAD} = 100\ \Omega$; $A_V = 1$ (AD9631); $A_V = 2$ (AD9632), unless otherwise noted.)

Parameter	Conditions	AD9631A Min	AD9631A Typ	AD9631A Max	AD9632A Min	AD9632A Typ	AD9632A Max	Unit
DYNAMIC PERFORMANCE								
Bandwidth (–3 dB)								
Small Signal	$V_{OUT} \leq 0.4$ V p-p	220	320		180	250		MHz
Large Signal[1]	V_{OUT} = 4 V p-p	150	175		155	180		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 300 mV p-p							
	AD9631, $R_F = 140\ \Omega$;		130			130		MHz
	AD9632, $R_F = 425\ \Omega$							
Slew Rate, Average ±	V_{OUT} = 4 V Step	1000	1300		1200	1500		V/µs
Rise/Fall Time	V_{OUT} = 0.5 V Step		1.2			1.4		ns
	V_{OUT} = 4 V Step		2.5			2.1		ns
Settling Time								
To 0.1%	V_{OUT} = 2 V Step		11			11		ns
To 0.01%	V_{OUT} = 2 V Step		16			16		ns
HARMONIC/NOISE PERFORMANCE								
Second Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		–64	–57		–54	–47	dBc
	$R_L = 500\ \Omega$		–72	–65		–72	–65	dBc
Third Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		–76	–69		–74	–67	dBc
	$R_L = 500\ \Omega$		–81	–74		–81	–74	dBc
Third Order Intercept	25 MHz		46			41		dBm
Noise Figure	$R_S = 50\ \Omega$		18			14		dB
Input Voltage Noise	1 MHz to 200 MHz		7.0			4.3		nV/√Hz
Input Current Noise	1 MHz to 200 MHz		2.5			2.0		pA/√Hz
Average Equivalent Integrated								
Input Noise Voltage	0.1 MHz to 200 MHz		100			60		µV rms
Differential Gain Error (3.58 MHz)	$R_L = 150\ \Omega$		0.03	0.06		0.02	0.04	%
Differential Phase Error (3.58 MHz)	$R_L = 150\ \Omega$		0.02	0.04		0.02	0.04	Degree
Phase Nonlinearity	DC to 100 MHz		1.1			1.1		Degree
DC PERFORMANCE[2], $R_L = 150\ \Omega$								
Input Offset Voltage[3]			3	10		2	5	mV
	T_{MIN}–T_{MAX}			13			8	mV
Offset Voltage Drift			±10			±10		µV/°C
Input Bias Current			2	7		2	7	µA
	T_{MIN}–T_{MAX}			10			10	µA
Input Offset Current			0.1	3		0.1	3	µA
	T_{MIN}–T_{MAX}			5			5	µA
Common-Mode Rejection Ratio	$V_{CM} = \pm 2.5$ V	70	90		70	90		dB
Open-Loop Gain	$V_{OUT} = \pm 2.5$ V	46	52		46	52		dB
	T_{MIN}–T_{MAX}	40			40			dB
INPUT CHARACTERISTICS								
Input Resistance			500			500		kΩ
Input Capacitance			1.2			1.2		pF
Input Common-Mode Voltage Range			±3.4			±3.4		V
OUTPUT CHARACTERISTICS								
Output Voltage Range, $R_L = 150\ \Omega$		±3.2	±3.9		±3.2	±3.9		V
Output Current			70			70		mA
Output Resistance			0.3			0.3		Ω
Short Circuit Current			240			240		mA
POWER SUPPLY								
Operating Range		±3.0	±5.0	±6.0	±3.0	±5.0	±6.0	V
Quiescent Current			17	18		16	17	mA
	T_{MIN}–T_{MAX}			21			20	mA
Power Supply Rejection Ratio	T_{MIN}–T_{MAX}	50	60		56	66		dB

NOTES

[1]See Absolute Maximum Ratings and Theory of Operation sections of this data sheet.

[2]Measured at $A_V = 50$.

[3]Measured with respect to the inverting input.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S$ to $-V_S$) . . . . . 12.6 V
Voltage Swing × Bandwidth Product . . . . . 550 V-MHz
Internal Power Dissipation[2]
Plastic Package (N) . . . . . 1.3 W
Small Outline Package (R) . . . . . 0.9 W
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±1.2 V
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range N, R . . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

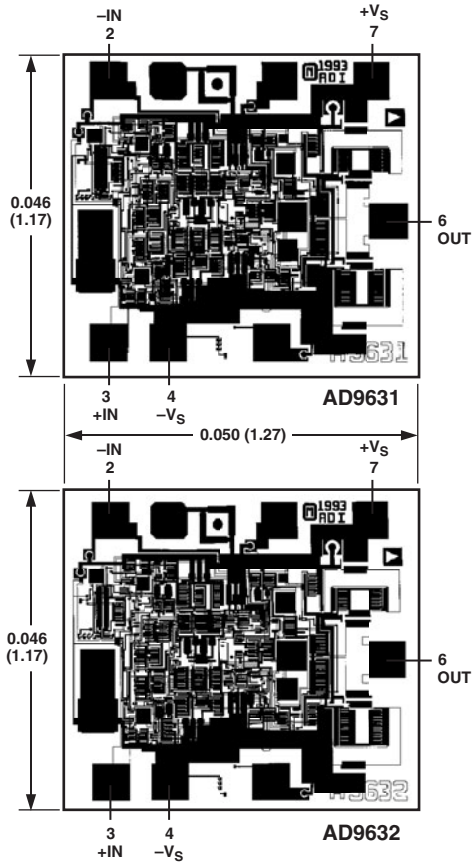
NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Specification is for device in free air:
8-Lead PDIP Package: θ_{JA} = 90°C/W
8-Lead SOIC Package: θ_{JA} = 140°C/W

METALLIZATION PHOTO

Dimensions shown in inches and (millimeters)
Connect Substrate to $-V_S$



MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by these devices is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD9631 and AD9632 are internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

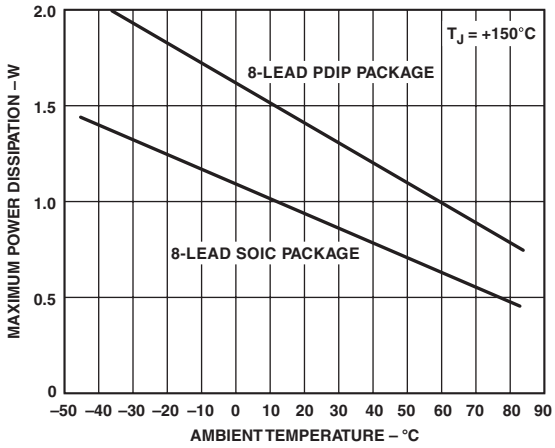


Figure 2. Maximum Power Dissipation vs. Temperature

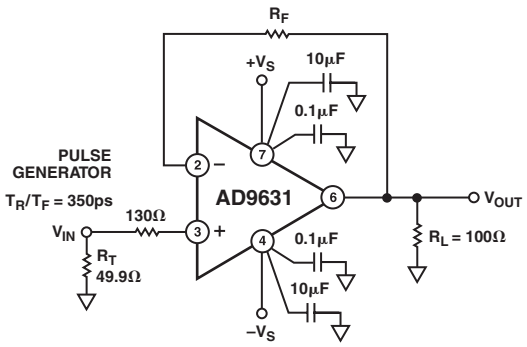
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9631AN	–40°C to +85°C	PDIP	N-8
AD9631AR	–40°C to +85°C	SOIC	R-8
AD9631AR-REEL	–40°C to +85°C	SOIC	R-8
AD9631AR-REEL7	–40°C to +85°C	SOIC	R-8
AD9631CHIPS		Die	
AD9632AN	–40°C to +85°C	PDIP	N-8
AD9632AR	–40°C to +85°C	SOIC	R-8
AD9632AR-REEL	–40°C to +85°C	SOIC	R-8
AD9632AR-REEL7	–40°C to +85°C	SOIC	R-8

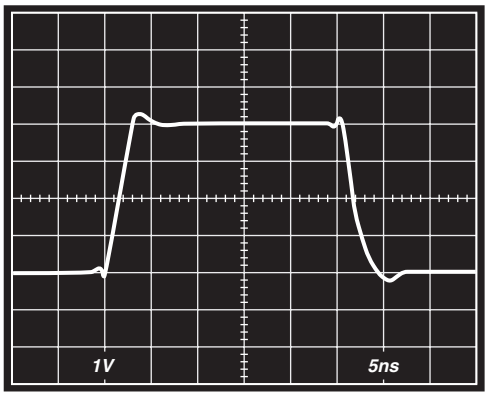
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9631/AD9632 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

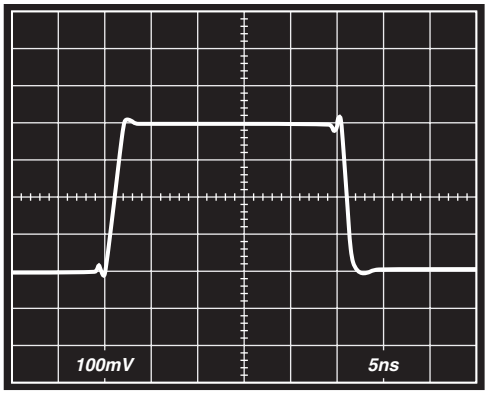
AD9631/AD9632–Typical Performance Characteristics



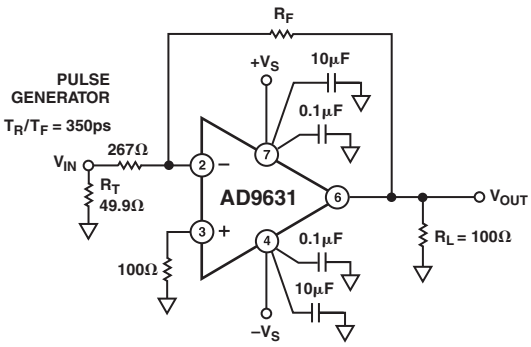
TPC 1. AD9631 Noninverting Configuration, G = +1



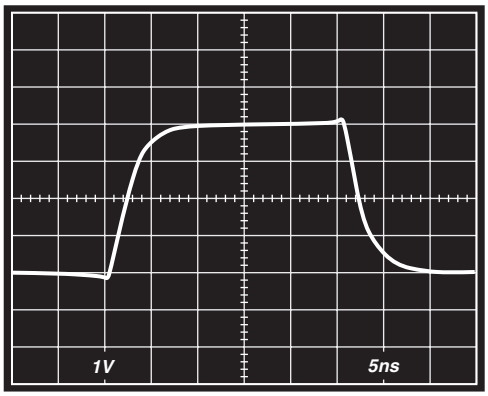
TPC 2. AD9631 Large Signal Transient Response; V_O = 4 V p-p, G = +1, R_F = 250 Ω



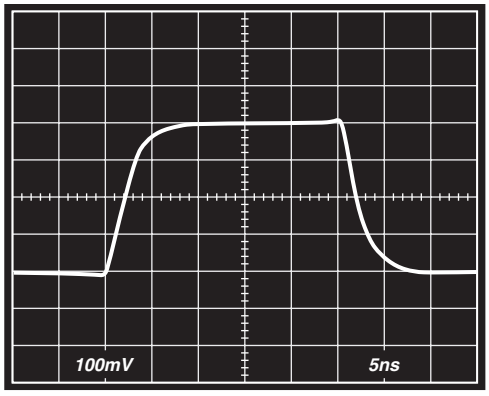
TPC 3. AD9631 Small Signal Transient Response; V_O = 400 mV p-p, G = +1, R_F = 140 Ω



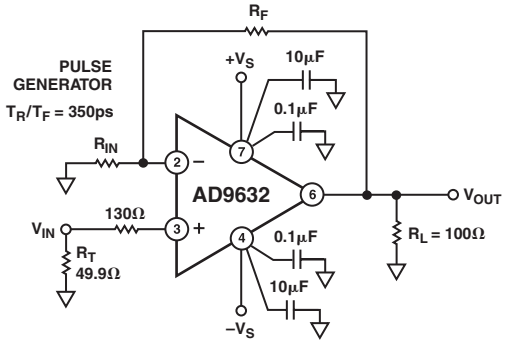
TPC 4. AD9631 Inverting Configuration, G = –1



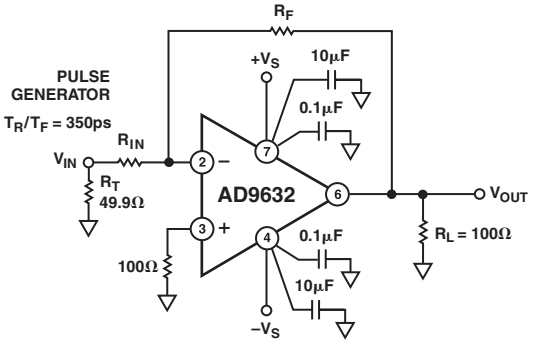
TPC 5. AD9631 Large Signal Transient Response; V_O = 4 V p-p, G = –1, R_F = R_{IN} = 267 Ω



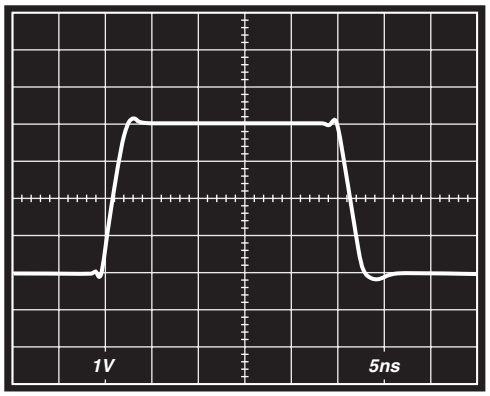
TPC 6. AD9631 Small Signal Transient Response; V_O = 400 mV p-p, G = –1, R_F = R_{IN} = 267 Ω



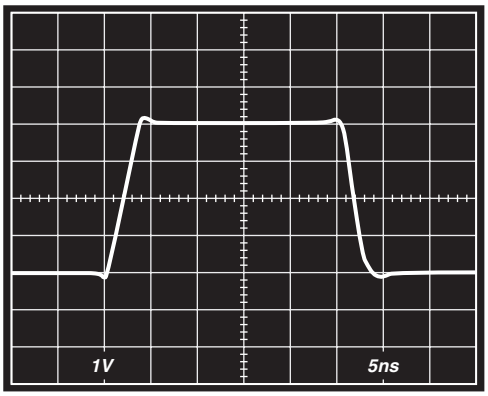
TPC 7. AD9632 Noninverting Configuration, G = +2



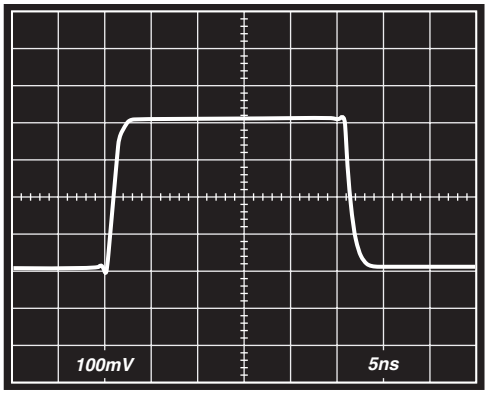
TPC 10. AD9632 Inverting Configuration, G = –1



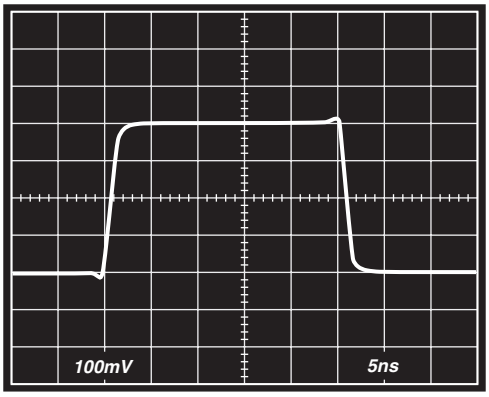
TPC 8. AD9632 Large Signal Transient Response; V_O = 4 V p-p, G = +2, $R_F = R_{IN}$ = 422 Ω



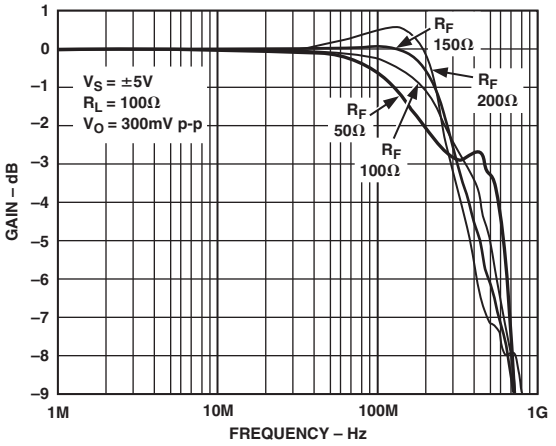
TPC 11. AD9632 Large Signal Transient Response; V_O = 4 V p-p, G = –1, $R_F = R_{IN}$ = 422 Ω, R_T = 56.2 Ω



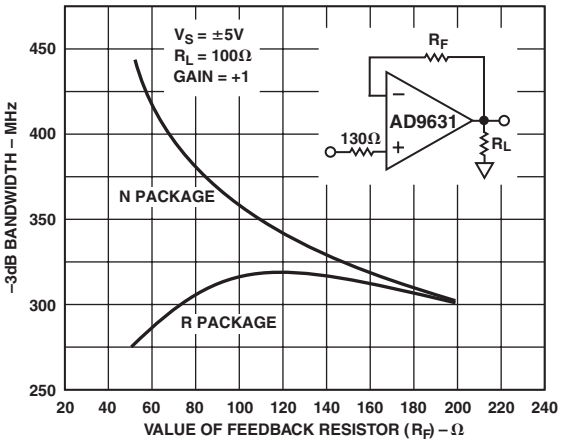
TPC 9. AD9632 Small Signal Transient Response; V_O = 400 mV p-p, G = +2, $R_F = R_{IN}$ = 274 Ω



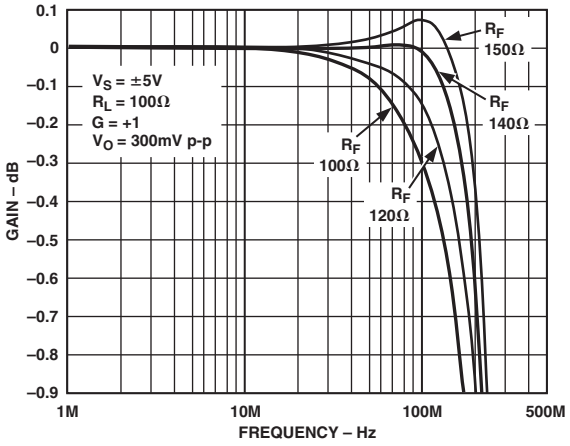
TPC 12. AD9632 Small Signal Transient Response; V_O = 400 mV p-p, G = –1, $R_F = R_{IN}$ = 267 Ω, R_T = 61.9 Ω



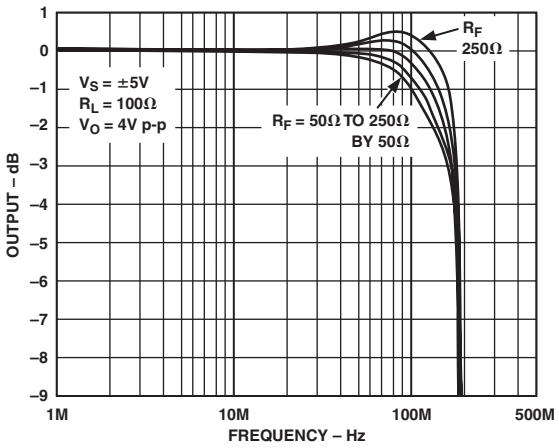
TPC 13. AD9631 Small Signal Frequency Response, G = +1



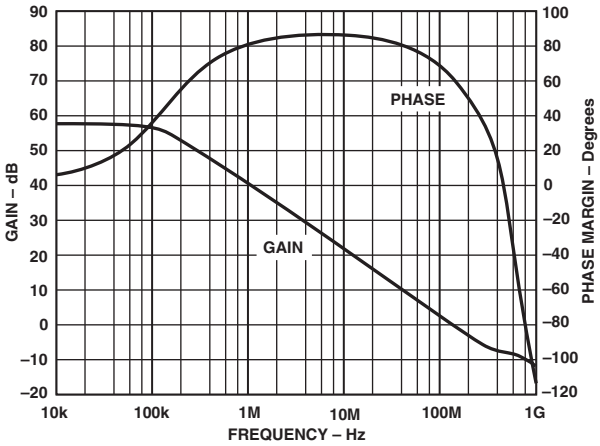
TPC 16. AD9631 Small Signal –3 dB Bandwidth vs. R_F



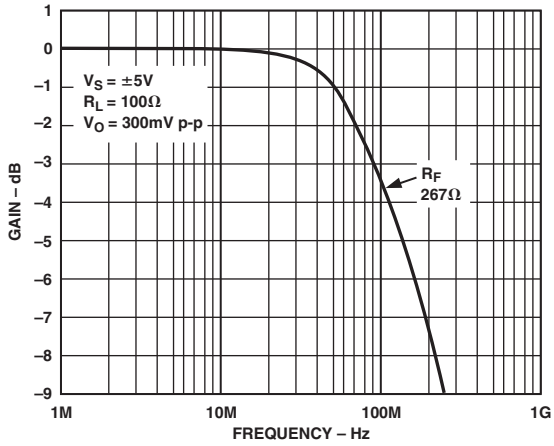
TPC 14. AD9631 0.1 dB Flatness, N Package (for R Package Add 20 Ω to R_F)



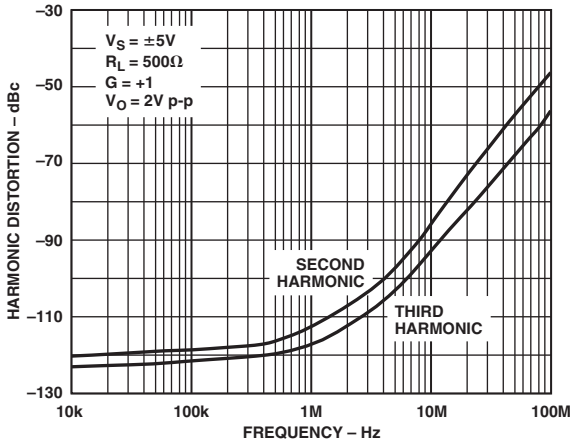
TPC 17. AD9631 Large Signal Frequency Response, G = +1



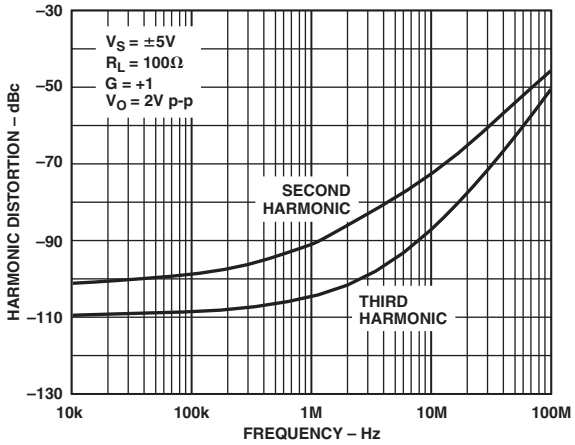
TPC 15. AD9631 Open-Loop Gain and Phase Margin vs. Frequency, R_L = 100 Ω



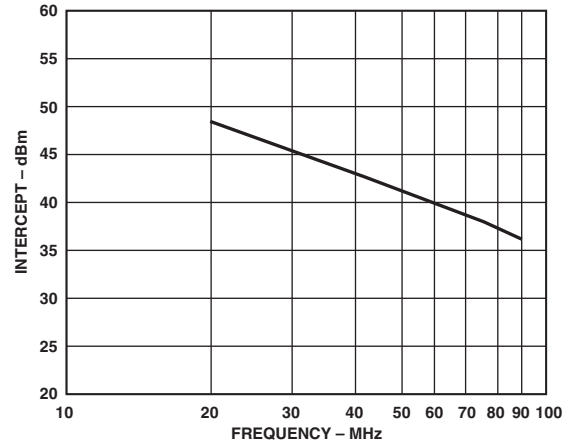
TPC 18. AD9631 Small Signal Frequency Response, G = –1



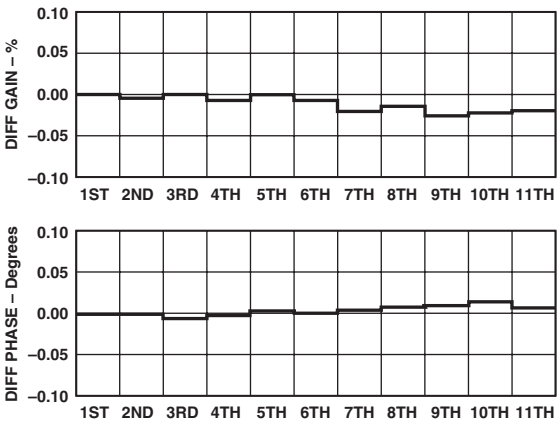
TPC 19. AD9631 Harmonic Distortion vs. Frequency, R_L = 500 Ω



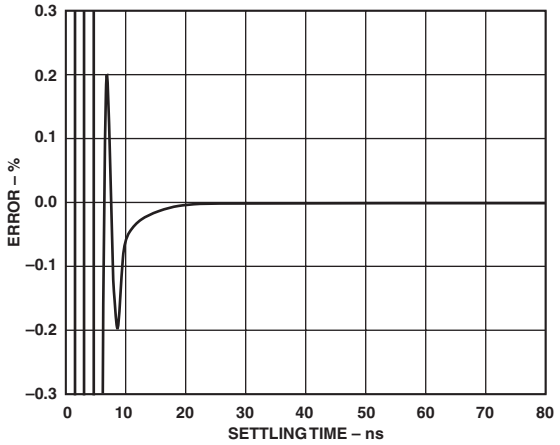
TPC 20. AD9631 Harmonic Distortion vs. Frequency, R_L = 100 Ω



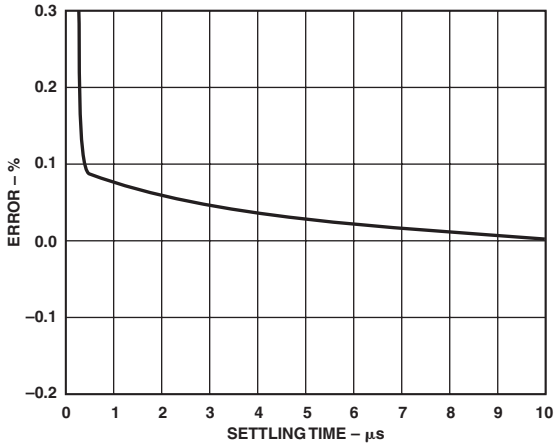
TPC 21. AD9631 Third Order Intercept vs. Frequency



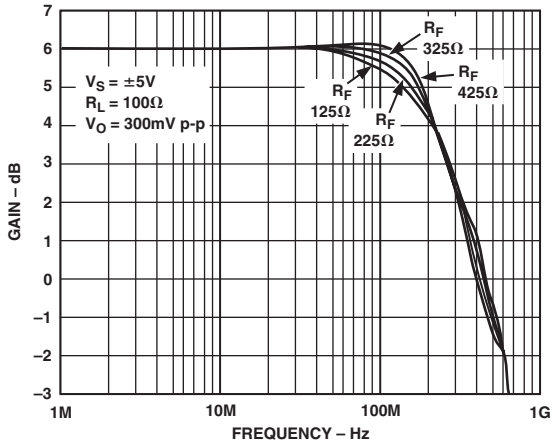
TPC 22. AD9631 Differential Gain and Phase Error, G = +2, R_L = 150 Ω



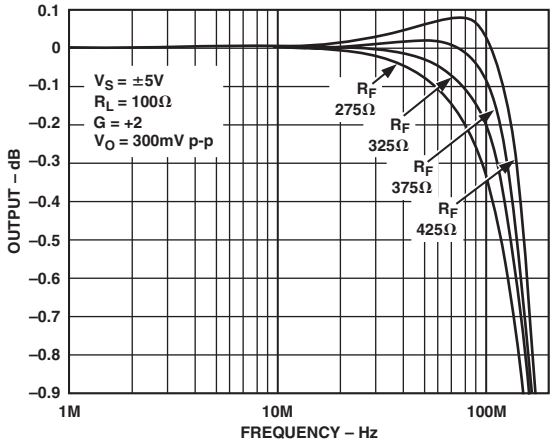
TPC 23. AD9631 Short-Term Settling Time, 2 V Step, R_L = 100 Ω



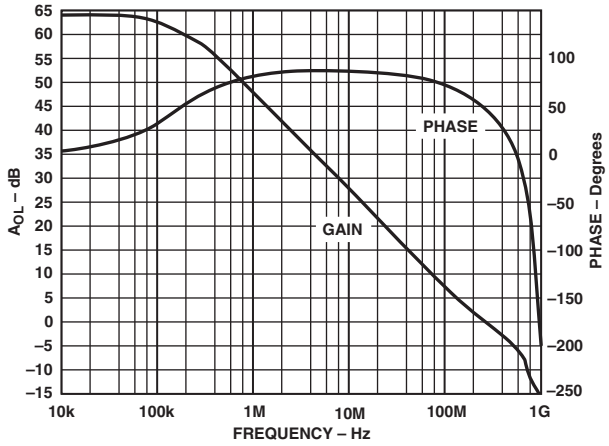
TPC 24. AD9631 Long-Term Settling Time, 2 V Step, R_L = 100 Ω



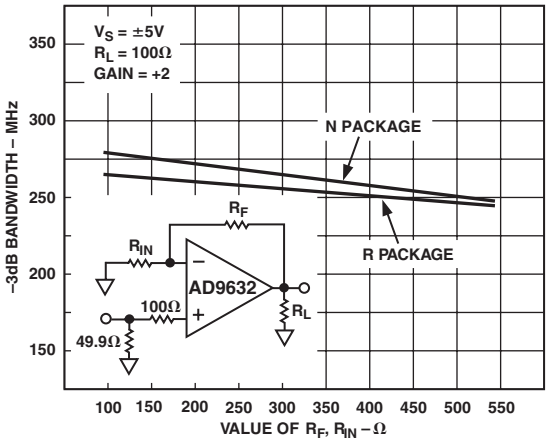
TPC 25. AD9632 Small Signal Frequency Response, G = +2



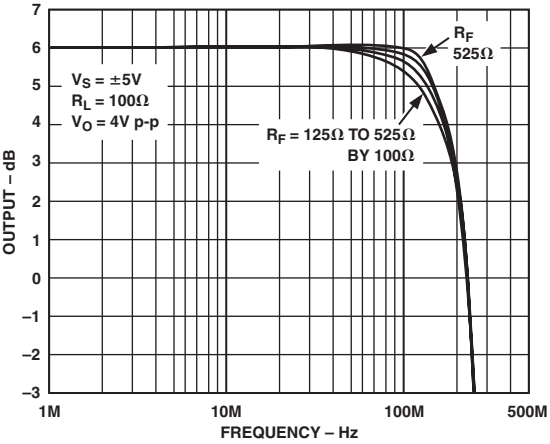
TPC 26. AD9632 0.1 dB Flatness, N Package (for R Package Add 20 Ω to R_F)



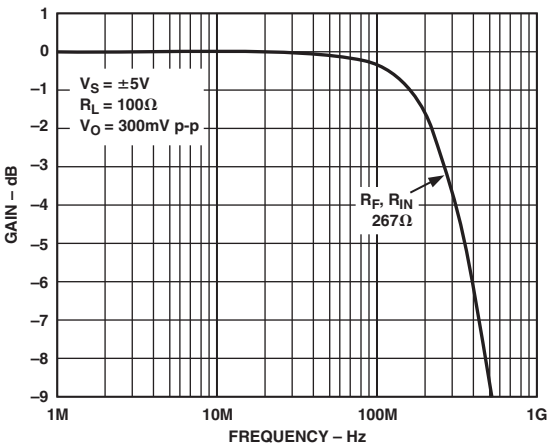
TPC 27. AD9632 Open-Loop Gain and Phase Margin vs. Frequency, R_L = 100 Ω



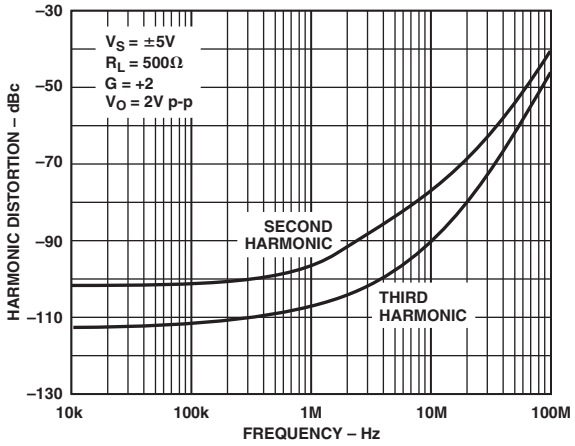
TPC 28. AD9632 Small Signal –3 dB Bandwidth vs. R_F, R_{IN}



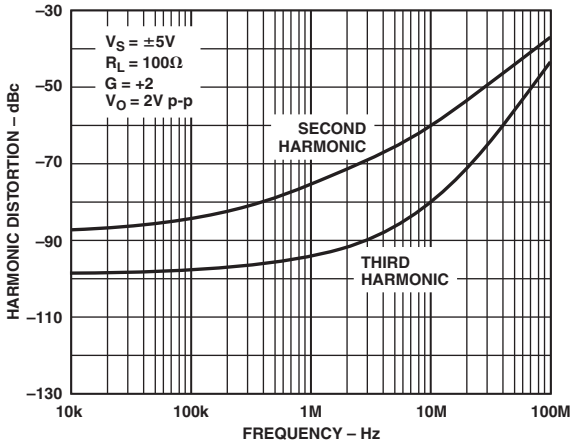
TPC 29. AD9632 Large Signal Frequency Response, G = +2



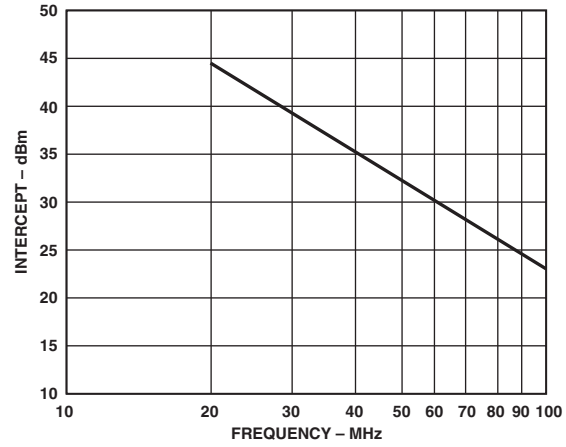
TPC 30. AD9632 Small Signal Frequency Response, G = –1



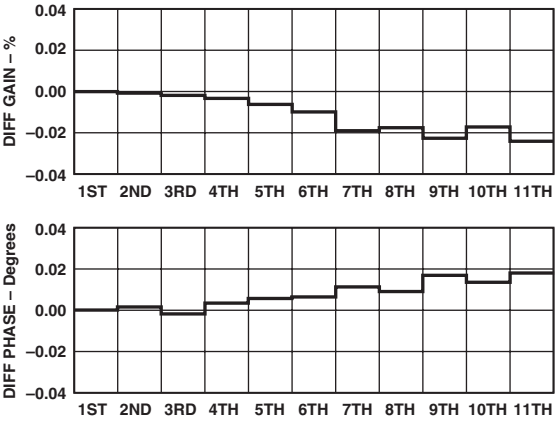
TPC 31. AD9632 Harmonic Distortion vs. Frequency, R_L = 500 Ω



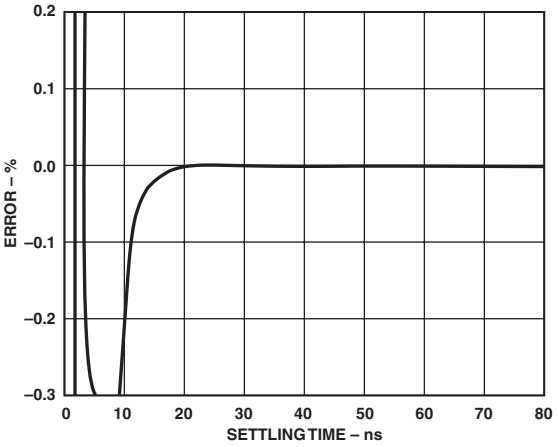
TPC 32. AD9632 Harmonic Distortion vs. Frequency, R_L = 100 Ω



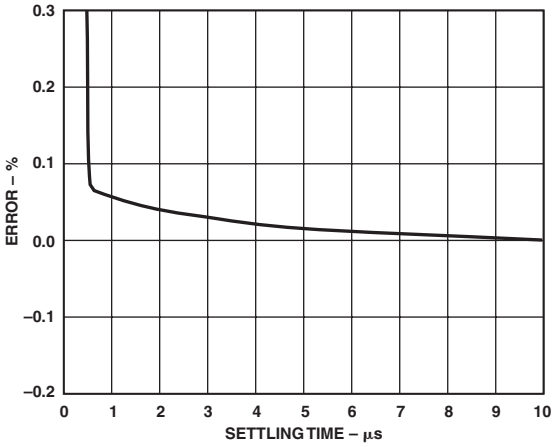
TPC 33. AD9632 Third Order Intercept vs. Frequency



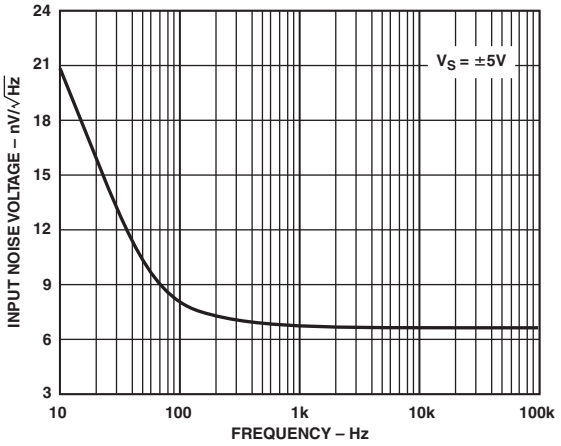
TPC 34. AD9632 Differential Gain and Phase Error G = +2, R_L = 150 Ω



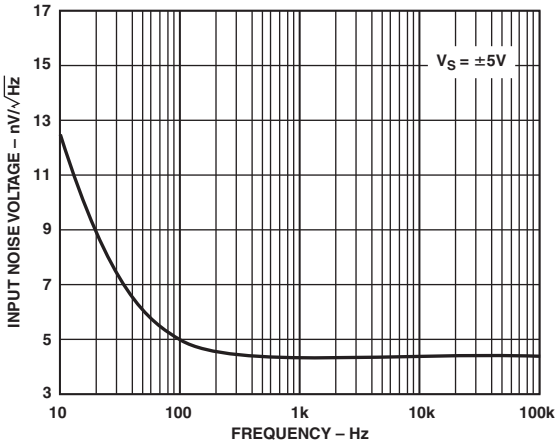
TPC 35. AD9632 Short-Term Settling Time, 2 V Step, R_L = 100 Ω



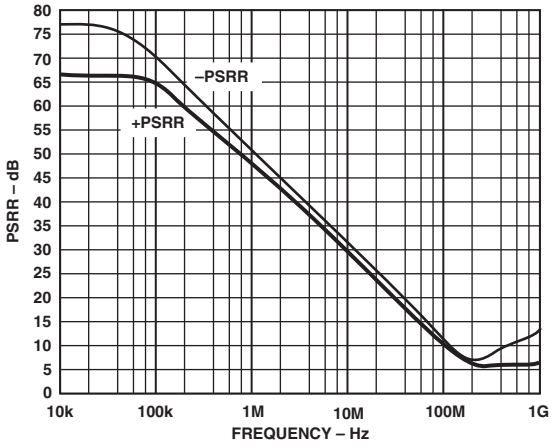
TPC 36. AD9632 Long-Term Settling Time, 2 V Step, R_L = 100 Ω



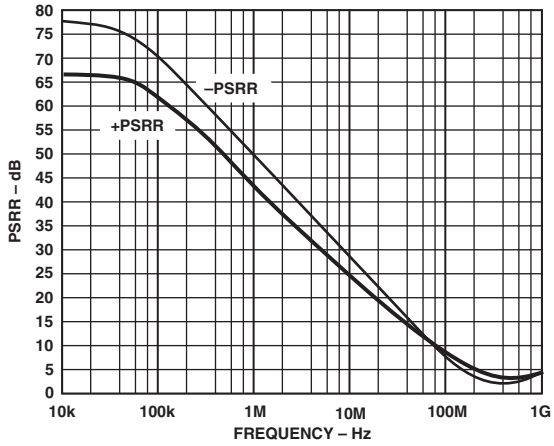
TPC 37. AD9631 Noise vs. Frequency



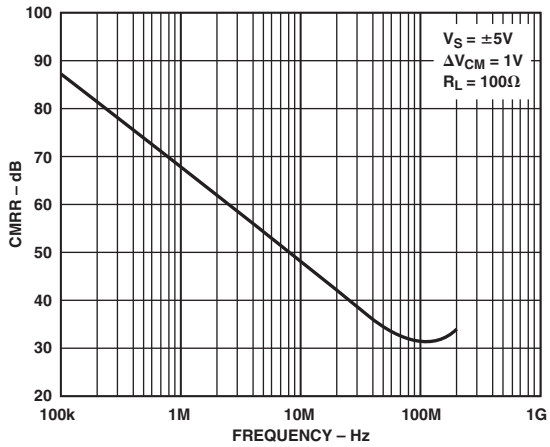
TPC 40. AD9632 Noise vs. Frequency



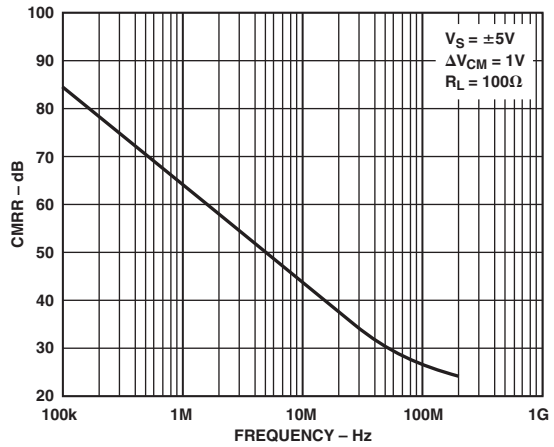
TPC 38. AD9631 PSRR vs. Frequency



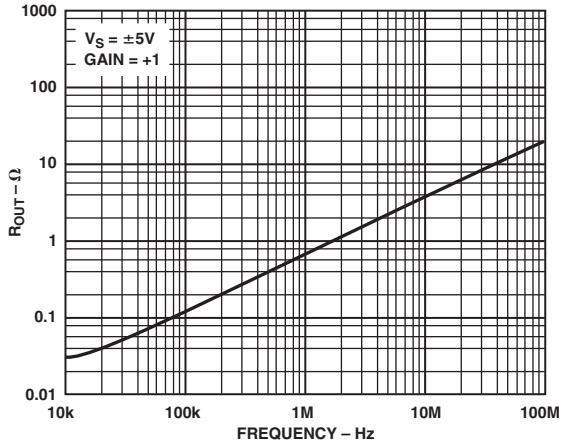
TPC 41. AD9632 PSRR vs. Frequency



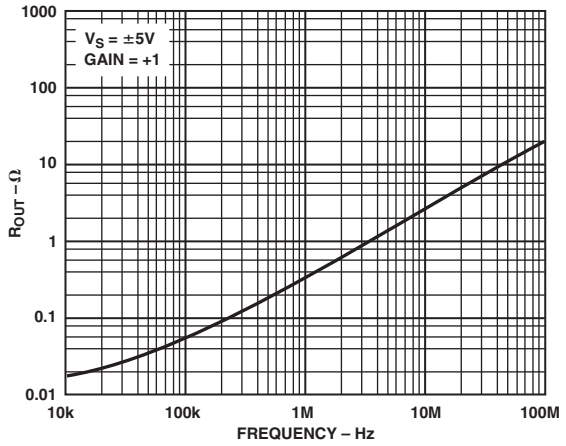
TPC 39. AD9631 CMRR vs. Frequency



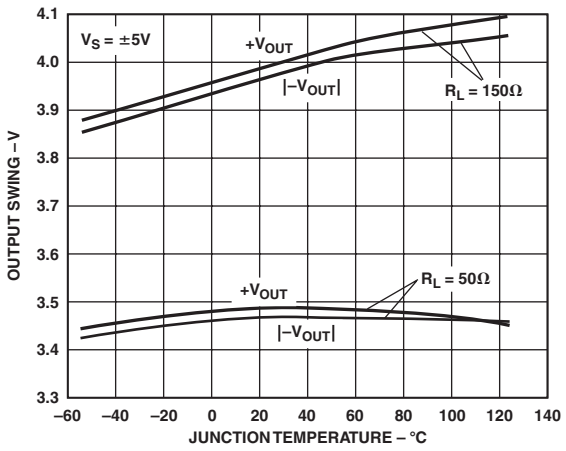
TPC 42. AD9632 CMRR vs. Frequency



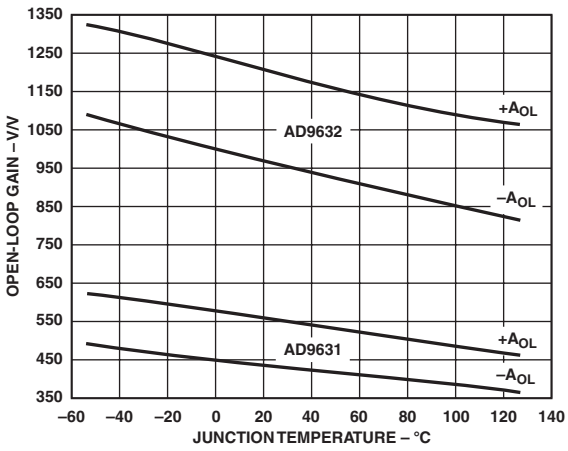
TPC 43. AD9631 Output Resistance vs. Frequency



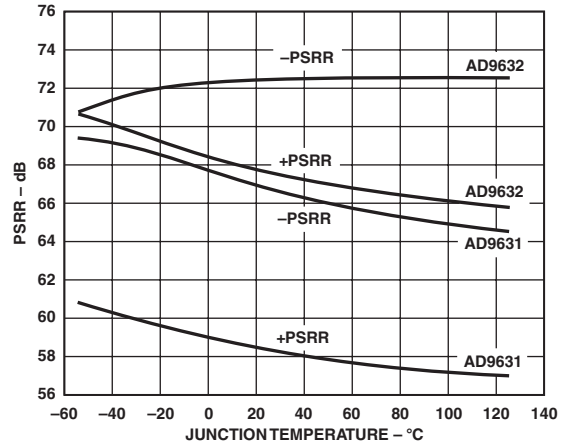
TPC 44. AD9632 Output Resistance vs. Frequency



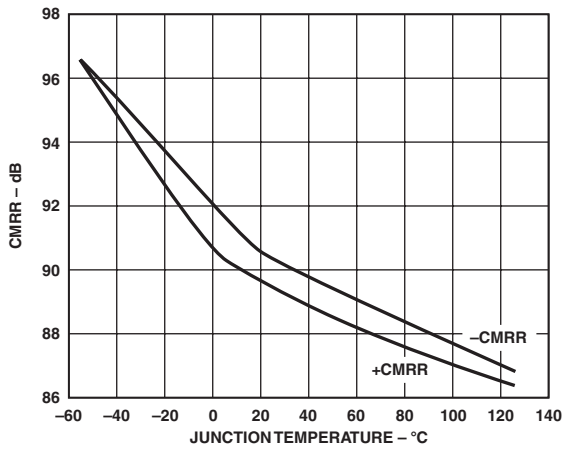
TPC 45. AD9631/AD9632 Output Swing vs. Temperature



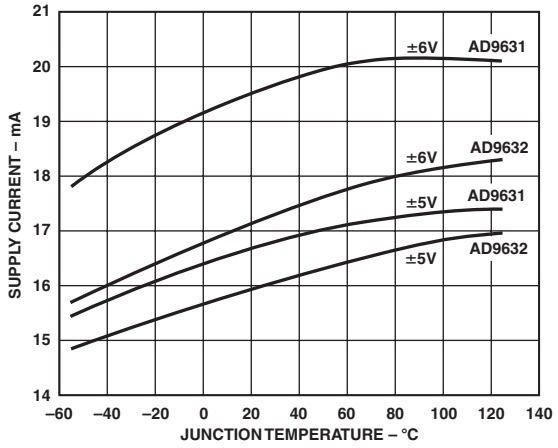
TPC 46. Open-Loop Gain vs. Temperature



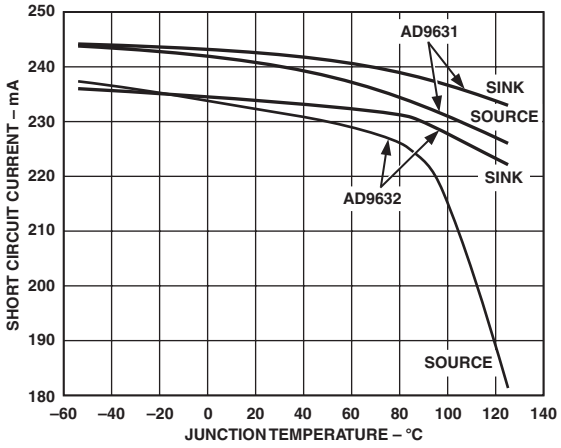
TPC 47. PSRR vs. Temperature



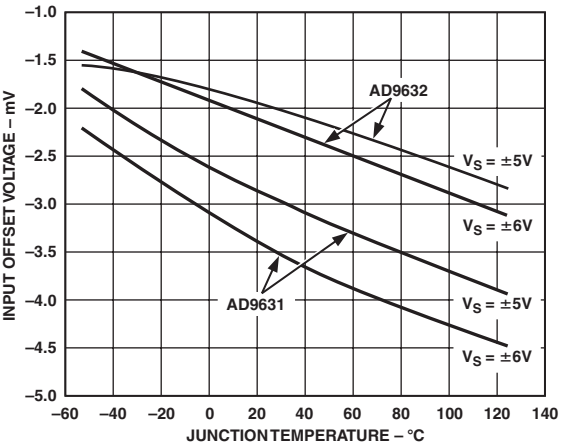
TPC 48. AD9631/AD9632 CMRR vs. Temperature



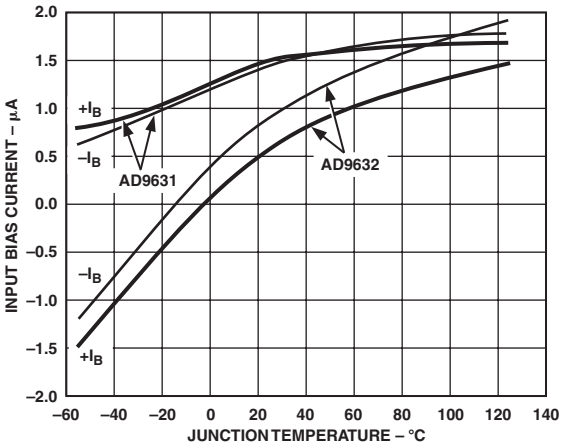
TPC 49. Supply Current vs. Temperature



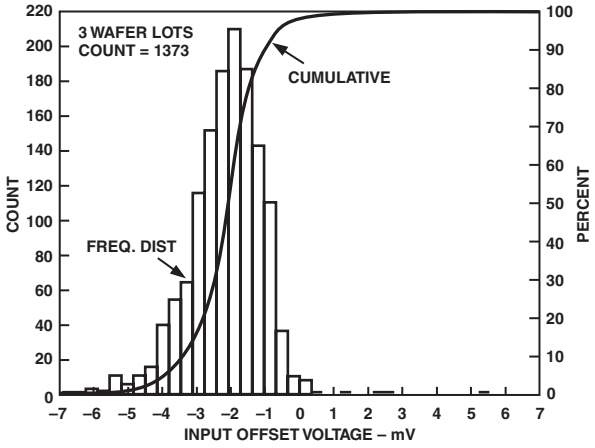
TPC 52. Short Circuit Current vs. Temperature



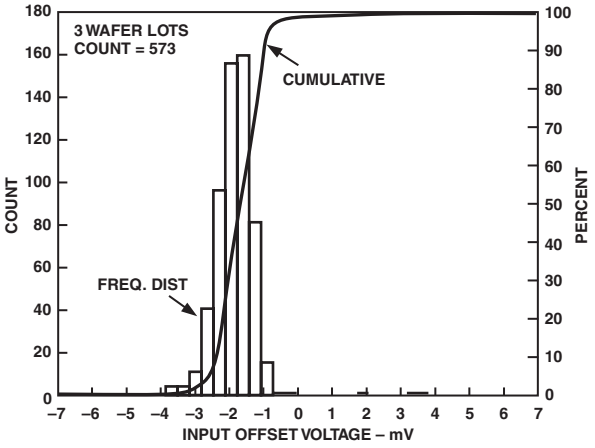
TPC 50. Input Offset Voltage vs. Temperature



TPC 53. Input Bias Current vs. Temperature



TPC 51. AD9631 Input Offset Voltage Distribution



TPC 54. AD9632 Input Offset Voltage Distribution

THEORY OF OPERATION

General

The AD9631 and AD9632 are wide bandwidth, voltage feedback amplifiers. Since their open-loop frequency response follows the conventional 6 dB/octave roll-off, their gain bandwidth product is basically constant. Increasing their closed-loop gain results in a corresponding decrease in small signal bandwidth. This can be observed by noting the bandwidth specification between the AD9631 (gain of +1) and AD9632 (gain of +2). The AD9631/AD9632 typically maintain 65 degrees of phase margin. This high margin minimizes the effects of signal and noise peaking.

Feedback Resistor Choice

The value of the feedback resistor is critical for optimum performance on the AD9631 (gain of +1) and less critical as the gain increases. Therefore, this section is specifically targeted at the AD9631.

At minimum stable gain (+1), the AD9631 provides optimum dynamic performance with R_F = 140 Ω. This resistor acts as a parasitic suppressor only against damped RF oscillations that can occur due to lead (input, feedback) inductance and parasitic capacitance. This value of R_F provides the best combination of wide bandwidth, low parasitic peaking, and fast settling time.

In fact, for the same reasons, a 100 Ω–130 Ω resistor should be placed in series with the positive input for other AD9631 noninverting and all AD9631 inverting configurations. The correct connection is shown in Figures 3 and 4.

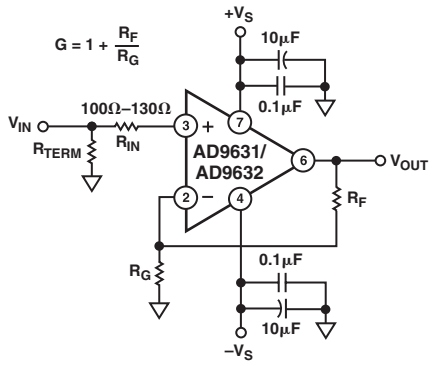


Figure 3. Noninverting Operation

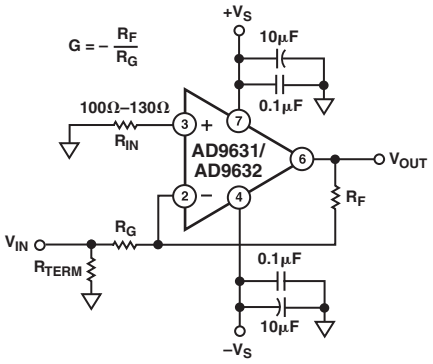


Figure 4. Inverting Operation

When the AD9631 is used in the transimpedance (I to V) mode, such as in photodiode detection, the value of R_F and diode capacitance (C_I) are usually known. Generally, the value of R_F selected will be in the kΩ range, and a shunt capacitor (C_F) across R_F will be required to maintain good amplifier stability. The value of C_F required to maintain optimal flatness (<1 dB peaking) and settling time can be estimated as

$$C_F \cong \left[\left(2\omega_O C_I R_F - 1\right) / \omega_O{}^2 R_F{}^2\right]^{\frac{1}{2}}$$

where ω_O is equal to the unity gain bandwidth product of the amplifier in rad/sec, and C_I is the equivalent total input capacitance at the inverting input. Typically $\omega_O = 800 \times 10^6$ rad/sec (see TPC 15).

As an example, choosing R_F = 10 kΩ and C_I = 5 pF requires C_F to be 1.1 pF (Note: C_I includes both source and parasitic circuit capacitance). The bandwidth of the amplifier can be estimated using the C_F calculated as

$$f_{3dB} \cong \frac{1.6}{2\pi R_F C_F}$$

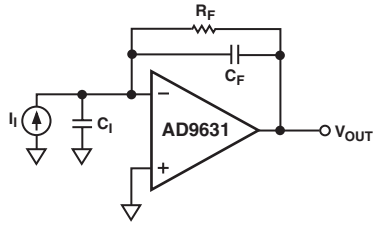


Figure 5. Transimpedance Configuration

For general voltage gain applications, the amplifier bandwidth can be closely estimated as

$$f_{3dB} \cong \frac{\omega_O}{2\pi\left(1 + R_F/R_G\right)}$$

This estimation loses accuracy for gains of +2/–1 or lower due to the amplifier's damping factor. For these "low gain" cases, the bandwidth will actually extend beyond the calculated value (see TPCs 13 and 25).

As a general rule, capacitor C_F will not be required if

$$\left(R_F \| R_G\right) \times C_I \leq \frac{NG}{4\,\omega_O}$$

where NG is the noise gain $(1 + R_F/R_G)$ of the circuit. For most voltage gain applications, this should be the case.

Pulse Response
Unlike a traditional voltage feedback amplifier, where the slew speed is dictated by its front end dc quiescent current and gain bandwidth product, the AD9631 and AD9632 provide "on-demand" current that increases proportionally to the input "step" signal amplitude. This results in slew rates (1300 V/μs) comparable to wideband current feedback designs. This, combined with relatively low input noise current (2.0 pA/√Hz), gives the AD9631 and AD9632 the best attributes of both voltage and current feedback amplifiers.

Large Signal Performance
The outstanding large signal operation of the AD9631 and AD9632 is due to a unique, proprietary design architecture. In order to maintain this level of performance, the maximum 550 V-MHz product must be observed (e.g., @ 100 MHz, $V_O \leq 5.5$ V p-p).

Power Supply Bypassing
Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 μF) will be required to provide the best settling time and lowest distortion. A parallel combination of at least 4.7 μF, and between 0.1 μF and 0.01 μF, is recommended. Some brands of electrolytic capacitors will require a small series damping resistor ≈4.7 Ω for optimum results.

Driving Capacitive Loads
The AD9631 and AD9632 were designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, the best frequency response is obtained by the addition of a small series resistance as shown in Figure 6. The accompanying graph shows the optimum value for R_{SERIES} versus capacitive load. It is worth noting that the frequency response of the circuit when driving large capacitive loads will be dominated by the passive roll-off of R_{SERIES} and C_L.

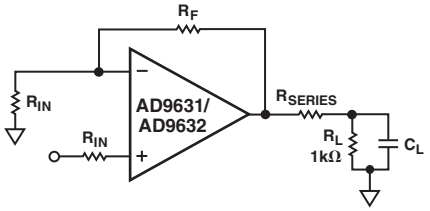


Figure 6. Driving Capacitive Loads

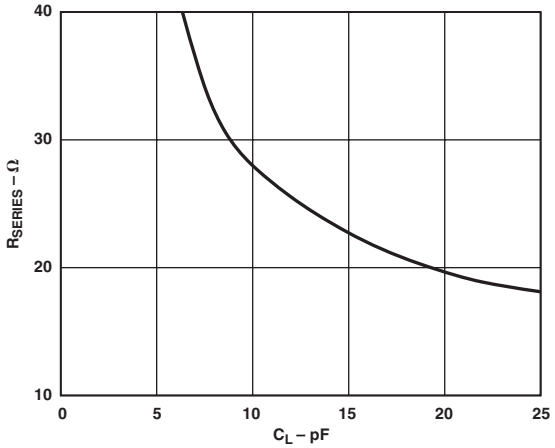


Figure 7. Recommended R_{SERIES} vs. Capacitive Load

APPLICATIONS
The AD9631 and AD9632 are voltage feedback amplifiers well suited for applications such as photodetectors, active filters, and log amplifiers. The devices' wide bandwidth (320 MHz), phase margin (65°), low current noise (2.0 pA/√Hz), and slew rate (1300 V/μs) give higher performance capabilities to these applications over previous voltage feedback designs.

With a settling time of 16 ns to 0.01% and 11 ns to 0.1%, the devices are an excellent choice for DAC I/V conversion. The same characteristics along with low harmonic distortion make them a good choice for ADC buffering/amplification. With superb linearity at relatively high signal frequencies, the AD9631 and AD9632 are ideal drivers for ADCs up to 12 bits.

Operation as a Video Line Driver
The AD9631 and AD9632 have been designed to offer outstanding performance as video line drivers. The important specifications of differential gain (0.02%) and differential phase (0.02°) meet the most exacting HDTV demands for driving video loads.

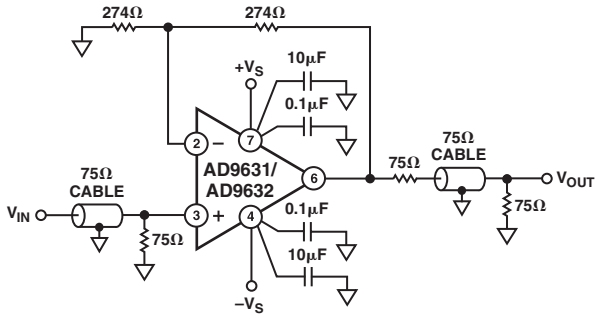


Figure 8. Video Line Driver

Active Filters

The wide bandwidth and low distortion of the AD9631 and AD9632 are ideal for the realization of higher bandwidth active filters. These characteristics, while being more common in many current feedback op amps, are offered in the AD9631 and AD9632 in a voltage feedback configuration. Many active filter configurations are not realizable with current feedback amplifiers.

A multiple feedback active filter requires a voltage feedback amplifier and is more demanding of op amp performance than other active filter configurations, such as the Sallen-Key. In general, the amplifier should have a bandwidth that is at least 10 times the bandwidth of the filter if problems due to phase shift of the amplifier are to be avoided.

Figure 9 is an example of a 20 MHz low-pass multiple feedback active filter using an AD9632.

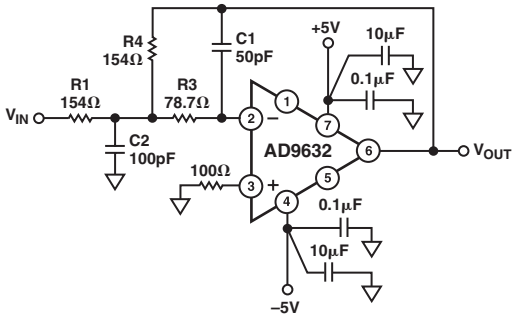


Figure 9. Active Filter Circuit

Choose

F_O = Cutoff Frequency = 20 MHz

α = Damping Ratio = $1/Q$ = 2

H = Absolute Value of Circuit Gain = $\left|\frac{-R4}{R1}\right|$ = 1

Then

$$k = 2\pi F_O C1$$

$$C2 = \frac{4C1(H+1)}{\alpha^2}$$

$$R1 = \frac{\alpha}{2HK}$$

$$R3 = \frac{\alpha}{2K(H+1)}$$

$$R4 = H(R1)$$

A/D Converter Driver

As A/D converters move toward higher speeds with higher resolutions, there becomes a need for high performance drivers that will not degrade the analog signal to the converter. It is desirable from a system's standpoint that the A/D be the element in the signal chain that ultimately limits overall distortion. This places new demands on the amplifiers that are used to drive fast, high resolution A/Ds.

With high bandwidth, low distortion, and fast settling time, the AD9631 and AD9632 make high performance A/D drivers for advanced converters. Figure 10 is an example of an AD9631 used as an input driver for an AD872, a 12-bit, 10 MSPS A/D converter.

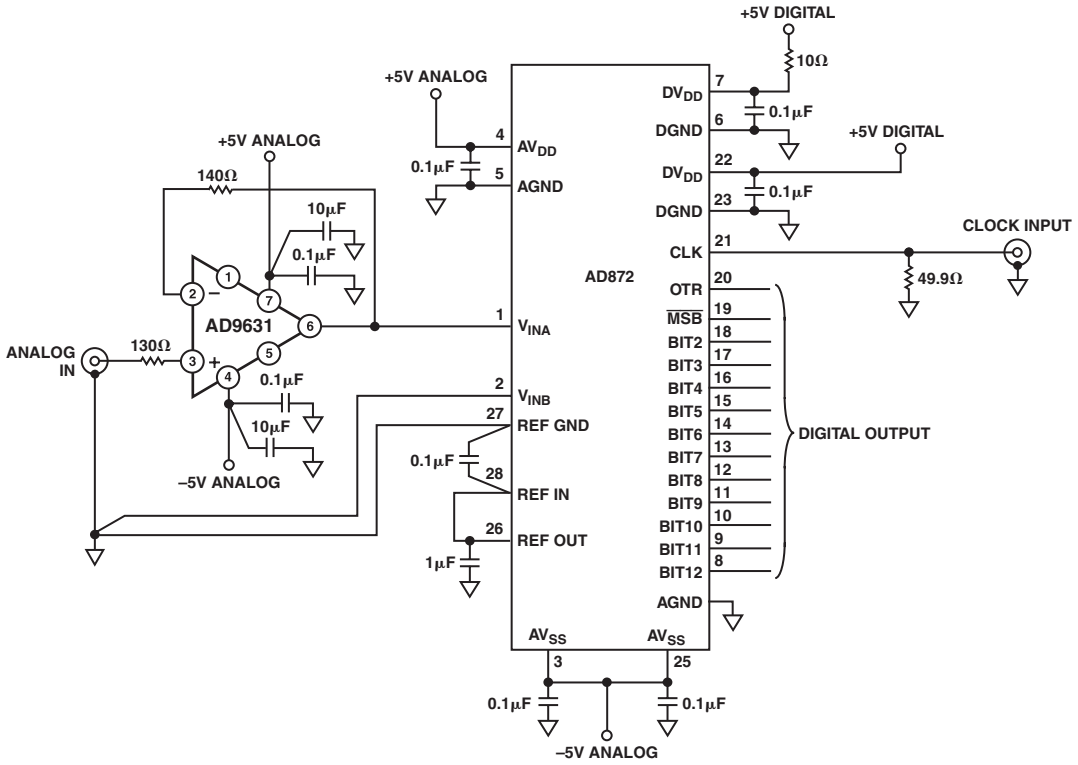


Figure 10. AD9631 Used as Driver for an AD872, a 12-Bit, 10 MSPS A/D Converter

Layout Considerations

The specified high speed performance of the AD9631 and AD9632 requires careful attention to board layout and component selection. Proper RF design techniques and low-pass parasitic component selection are mandatory.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

Chip capacitors should be used for supply bypassing (see Figure 10). One end should be connected to the ground plane, and the other within 1/8 inch of each power pin. An additional large (0.47 μF–10 μF) tantalum electrolytic capacitor should be connected in parallel, though not necessarily so close, to supply current for fast, large signal changes at the output.

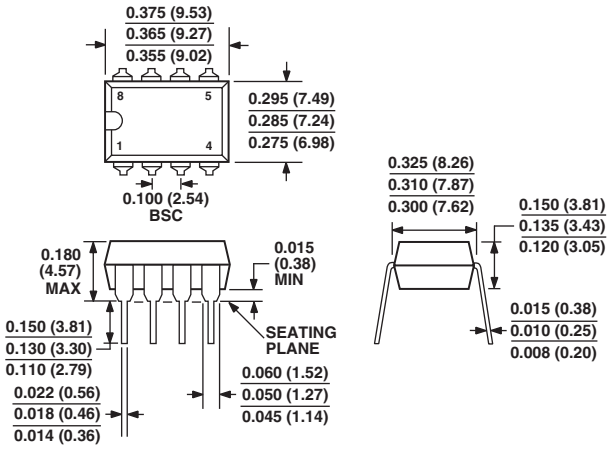
The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will significantly affect high speed performance.

Stripline design techniques should be used for long signal traces (greater than about 1 inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)

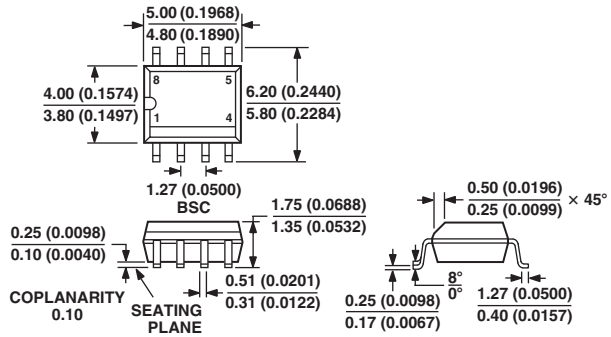
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)



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CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
7/03—Data Sheet changed from REV. B to REV. C.	
Deleted Evaluation Boards information	Universal
Deleted military CERDIP version	Universal
Change to ABSOLUTE MAXIMUM RATINGS	3
Change to TPC 4	4
Change to TPC 10	5
Change to Figure 6	14
Updated OUTLINE DIMENSIONS	17
1/03—Data Sheet changed from REV. A to REV. B.	
Deleted DIP (N) Inverter, SOIC (R) Inverter, and DIP (N) Noninverter Evaluation Boards in Figures 12–14	17
Updated OUTLINE DIMENSIONS	18