36-Mbit (1M × 36) Pipelined SRAM with NoBL™ Architecture

Features

- Pin compatible and functionally equivalent to ZBT™
- Supports 200 MHz bus operations with zero wait states
  - Available speed grade is 200 MHz
- Internally self-timed output buffer control to eliminate the need to use asynchronous $\overline{OE}$
- Fully registered (inputs and outputs) for pipelined operation
- Byte write capability
- 3.3 V power supply
- 3.3 V/2.5 V I/O power supply
- Fast clock-to-output times
  - 3.2 ns (for 200 MHz device)
- Clock Enable ($\overline{CEN}$) pin to suspend operation
- Synchronous self-timed writes
- CY7C1460SV33 available in JEDEC-standard Pb-Free 100-pin TQFP
- Burst capability – linear or interleaved burst order
- “ZZ” Sleep Mode option and Stop Clock option

Functional Description

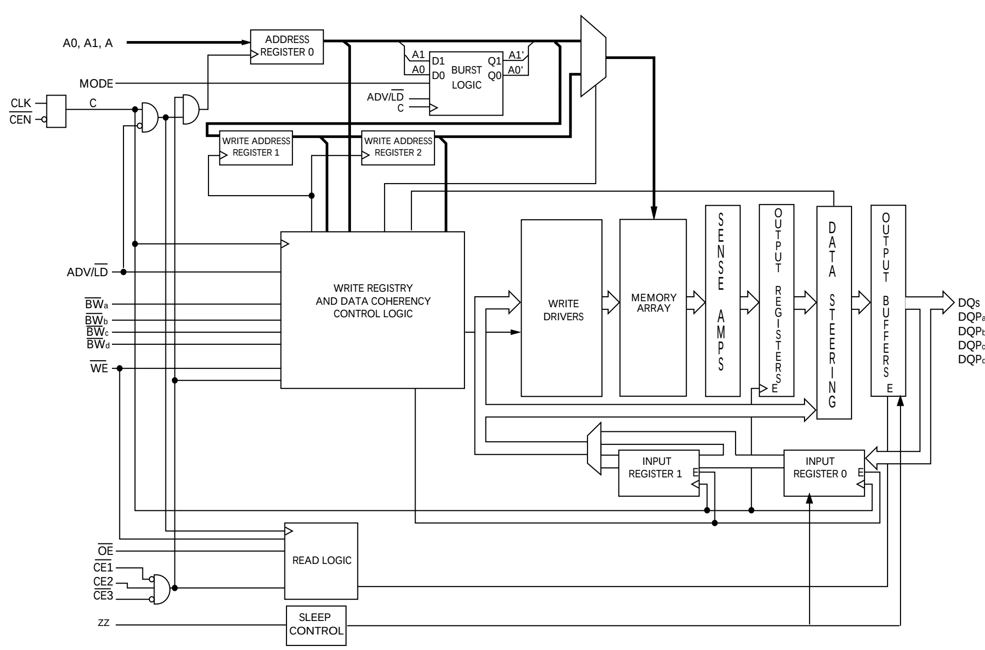
The CY7C1460SV33 is a 3.3 V, 1M × 36 synchronous pipelined burst SRAM with No Bus Latency™ (NoBL™) logic, respectively. They are designed to support unlimited true back to back Read/Write operations with no wait states. The CY7C1460SV33 are equipped with the advanced (NoBL) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data in systems that require frequent Write/Read transitions. CY7C1460SV33 is pin compatible and functionally equivalent to ZBT devices.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle.

Write operations are controlled by the Byte Write Selects ($\overline{BW}_a$–$\overline{BW}_d$ for CY7C1460SV33) and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tristate control. To avoid bus contention, the output drivers are synchronously tristated during the data portion of a write sequence.

Logic Block Diagram – CY7C1460SV33



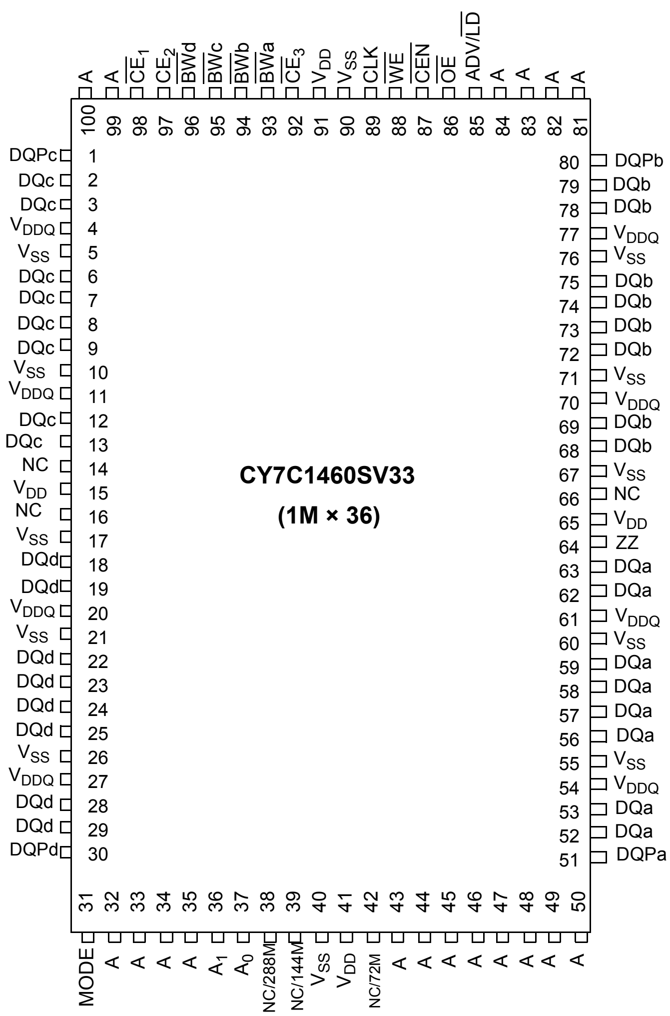
Contents

Selection Guide

Description	200 MHz	Unit
Maximum Access Time	3.2	ns
Maximum Operating Current	425	mA
Maximum CMOS Standby Current	120	mA

Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout



Pin Definitions

Pin Name	I/O Type	Pin Description
A_0, A_1, A	Input-Synchronous	**Address Inputs Used to Select One of the Address Locations**. Sampled at the rising edge of the CLK.
$\overline{BW}_a$, $\overline{BW}_b$, $\overline{BW}_c$, $\overline{BW}_d$	Input-Synchronous	**Byte Write Select Inputs, Active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BW}_a$ controls DQ_a and DQP_a, $\overline{BW}_b$ controls DQ_b and DQP_b, $\overline{BW}_c$ controls DQ_c and DQP_c, $\overline{BW}_d$ controls DQ_d and DQP_d.
$\overline{WE}$	Input-Synchronous	**Write Enable Input, Active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance/Load Input Used to Advance the On Chip Address Counter or Load a New Address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW to load a new address.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, Active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
DQ_a, DQ_b, DQ_c, DQ_d	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A_X during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_a–DQ_d are placed in a tristate condition. The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_a, DQP_b, DQP_c, DQP_d	I/O-Synchronous	**Bidirectional Data Parity I/O Lines**. Functionally, these signals are identical to $DQ_{[31:0]}$. During write sequences, DQP_a is controlled by $\overline{BW}_a$, DQP_b is controlled by $\overline{BW}_b$, DQP_c is controlled by $\overline{BW}_c$, and DQP_d is controlled by $\overline{BW}_d$.
MODE	Input Strap Pin	**Mode Input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE defaults HIGH, to an interleaved burst order.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{DDQ}	I/O Power Supply	**Power Supply for the I/O Circuitry**.
V_{SS}	Ground	**Ground for the Device**. Should be connected to ground of the system.
NC	N/A	**No Connects**. This pin is not connected to the die.
NC/72M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/144M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.

Pin Definitions (continued)

Pin Name	I/O Type	Pin Description
NC/288M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/576M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/1G	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
ZZ	Input-Asynchronous	**ZZ "sleep" Input**. This active HIGH input places the device in a non time critical "sleep" condition with data integrity preserved. During normal operation, this pin can be connected to V_{SS} or left floating. ZZ pin has an internal pull down.

Functional Overview

The CY7C1460SV33 are synchronous pipelined Burst NoBL SRAMs designed specifically to eliminate wait states during Write/Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.2 ns (200 MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) active at the rising edge of the clock. If Clock Enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the Write Enable ($\overline{WE}$). $\overline{BW}_{[x]}$ can be used to conduct byte write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/$\overline{LD}$ should be driven LOW after the device has been deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active, (3) the Write Enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the Address Register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 3.2 ns (200 MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (Read/Write/Deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output tristates following the next clock rise.

Burst Read Accesses

The CY7C1460SV33 have an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load a new address into the SRAM, as described in the Single Read Access section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A_0 and A_1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ increments the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active, and (3) the write signal $\overline{WE}$ is asserted LOW. The address presented to the address inputs is loaded into the Address Register. The write signals are latched into the Control Logic block.

On the subsequent clock rise the data lines are automatically tristated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1460SV33). In addition, the address for the subsequent access (Read/Write/Deselect) is latched into the Address Register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1460SV33) (or a subset for byte write operations; see Write Cycle Description table for details) inputs is latched into the device and the write is complete.

The data written during the Write operation is controlled by $\overline{BW}$ ($\overline{BW}_{a,b,c,d}$ for CY7C1460SV33) provides byte write capability that is described in the Write Cycle Description table. Asserting the Write Enable input ($\overline{WE}$) with the selected Byte Write Select ($\overline{BW}$) input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1460SV33 is a common I/O device, data should not be driven into the device while the outputs are active. The Output Enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for

CY7C1460SV33) inputs. Doing so tristates the output drivers. As a safety precaution, DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1460SV33) are automatically tristated during the data portion of a write cycle, regardless of the state of OE.

Burst Write Accesses

The CY7C1460SV33 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four WRITE operations without reasserting the address inputs. ADV/LD must be driven LOW to load the initial address, as described in the Single Write Access section. When ADV/LD is driven HIGH on the subsequent clock rise, the chip enables (CE_1, CE_2, and CE_3) and WE inputs are ignored and the burst counter is incremented. The correct BW ($BW_{a,b,c,d}$ for CY7C1460SV33) inputs must be driven in each cycle of the burst write to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. CE_1, CE_2, and CE_3, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2$ V	–	100	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2$ V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1460SV33 follows. [1, 2, 3, 4, 5, 6, 7]

Operation	Address Used	CE	ZZ	ADV/LD	WE	BW_x	OE	CEN	CLK	DQ
Deselect Cycle	None	H	L	L	X	X	X	L	L–H	Tristate
Continue Deselect Cycle	None	X	L	H	X	X	X	L	L–H	Tristate
Read Cycle (Begin Burst)	External	L	L	L	H	X	L	L	L–H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	L	H	X	X	L	L	L–H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	L	L	H	X	H	L	L–H	Tristate
Dummy Read (Continue Burst)	Next	X	L	H	X	X	H	L	L–H	Tristate
Write Cycle (Begin Burst)	External	L	L	L	L	L	X	L	L–H	Data In (D)
Write Cycle (Continue Burst)	Next	X	L	H	X	L	X	L	L–H	Data In (D)
NOP/WRITE ABORT (Begin Burst)	None	L	L	L	L	H	X	L	L–H	Tristate
WRITE ABORT (Continue Burst)	Next	X	L	H	X	H	X	L	L–H	Tristate
IGNORE CLOCK EDGE (Stall)	Current	X	L	X	X	X	X	H	L–H	–
SLEEP MODE	None	X	H	X	X	X	X	X	X	Tristate

Notes
1. X = “Don't Care”, H = Logic HIGH, L = Logic LOW, CE stands for ALL Chip Enables active. BWx = L signifies at least one Byte Write Select is active, BWx = Valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
2. Write is defined by WE and BW_X. See Write Cycle Description table for details.
3. When a write cycle is detected, all I/Os are tristated, even during byte writes.
4. The DQ and DQP pins are controlled by the current cycle and the OE signal.
5. CEN = H inserts wait states.
6. Device powers up deselected and the I/Os in a tristate condition, regardless of OE.
7. OE is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles.During a read cycle DQ_s and DQP_X = Tristate when OE is inactive or when the device is deselected, and DQ_s=data when OE is active.

Partial Write Cycle Description

Partial Write Cycle Description for CY7C1460SV33 follows. [8, 9, 10, 11]

Function (CY7C1460SV33)	$\overline{WE}$	$\overline{BW}_d$	$\overline{BW}_c$	$\overline{BW}_b$	$\overline{BW}_a$
Read	H	X	X	X	X
Write – No bytes written	L	H	H	H	H
Write Byte a – (DQ_a and DQP_a)	L	H	H	H	L
Write Byte b – (DQ_b and DQP_b)	L	H	H	L	H
Write Bytes b, a	L	H	H	L	L
Write Byte c – (DQ_c and DQP_c)	L	H	L	H	H
Write Bytes c, a	L	H	L	H	L
Write Bytes c, b	L	H	LL	L	H
Write Bytes c, b, a	L	H	L	L	L
Write Byte d – (DQ_d and DQP_d)	L	L	H	H	H
Write Bytes d, a	L	L	H	H	L
Write Bytes d, b	L	L	H	L	H
Write Bytes d, b, a	L	L	H	L	L
Write Bytes d, c	L	L	L	H	H
Write Bytes d, c, a	L	L	L	H	L
Write Bytes d, c, b	L	L	L	L	H
Write All Bytes	L	L	L	L	L

Notes

8. X = "Don't Care", H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for ALL Chip Enables active. $\overline{BW}x$ = L signifies at least one Byte Write Select is active, $\overline{BW}x$ = Valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
9. Write is defined by $\overline{WE}$ and $\overline{BW}_X$. See Write Cycle Description table for details.
10. When a write cycle is detected, all I/Os are tristated, even during byte writes.
11. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW}_{[a:d]}$ is valid. Appropriate write is done based on which byte write is active.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with
Power Applied .... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.5 V to $+V_{DD}$

DC to Outputs in Tristate ....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage ....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage
(per MIL-STD-883, Method 3015) .... > 2001 V

Latch up current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}

Electrical Characteristics

Over the Operating Range

Parameter [12, 13]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	for 3.3 V I/O		3.135	V_{DD}	V
		for 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW Voltage	for 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage [12]	for 3.3 V I/O		2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage [12]	for 3.3 V I/O		–0.3	0.8	V
		for 2.5 V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND $\le V_I \le V_{DDQ}$		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input Current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output Leakage Current	GND $\le V_I \le V_{DDQ}$, Output Disabled		–5	5	µA
I_{DD} [14]	V_{DD} Operating Supply	V_{DD} = Max, I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{CYC}$	5-ns cycle, 200 MHz	–	425	mA
I_{SB1}	Automatic CE Power down Current – TTL Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, $f = f_{MAX} = 1/t_{CYC}$	5-ns cycle, 200 MHz	–	225	mA
I_{SB2}	Automatic CE Power down Current – CMOS Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \le$ 0.3 V or $V_{IN} \ge V_{DDQ}$ – 0.3 V, f = 0	5-ns cycle, 200 MHz	–	120	mA

Notes

12. Overshoot: $V_{IH(AC)} < V_{DD}$ + 1.5 V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL(AC)} >$ –2 V (Pulse width less than $t_{CYC}/2$).
13. $T_{Powe\ up}$: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.
14. The operation current is calculated with 50% read cycle and 50% write cycle.

Electrical Characteristics (continued)

Over the Operating Range

Parameter [12, 13]	Description	Test Conditions		Min	Max	Unit
I_{SB3}	Automatic CE Power down Current – CMOS Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, $f = f_{MAX} = 1/t_{CYC}$	5-ns cycle, 200 MHz	–	200	mA
I_{SB4}	Automatic CE Power down Current – TTL Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0	5-ns cycle, 200 MHz	–	135	mA

Capacitance

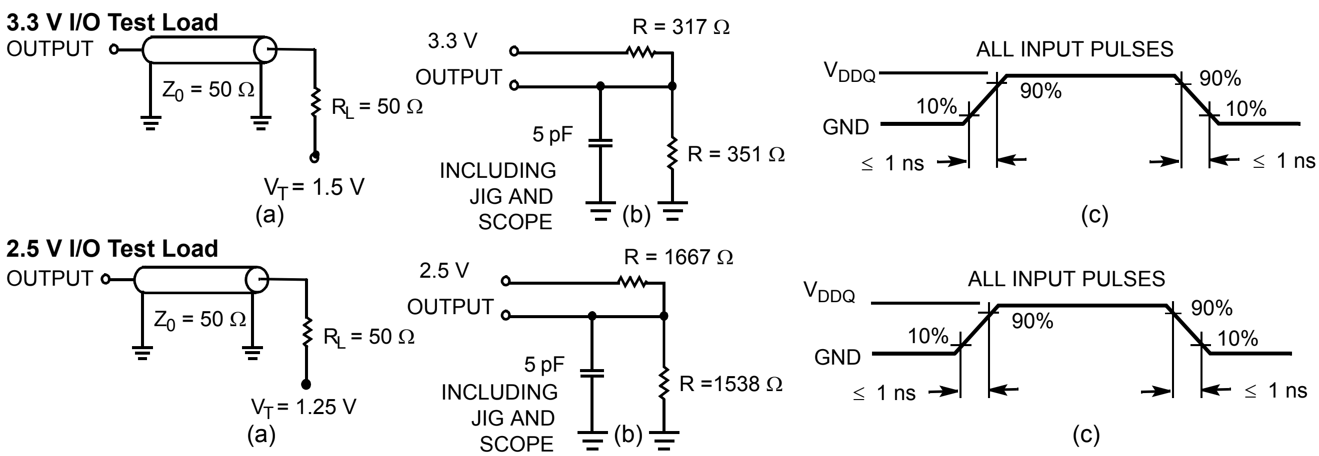
Parameter [15]	Description	Test Conditions	100-pin TQFP Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 2.5 V V_{DDQ} = 2.5 V	6.5	pF
C_{CLK}	Clock input capacitance		3	pF
C_{IO}	Input/Output capacitance		5.5	pF

Thermal Resistance

Parameter [15]	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	25.21	°C/W
Θ_{JC}	Thermal resistance (junction to case)		2.28	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Note

15. Tested initially and after any design or process changes that may affect these parameters

Switching Characteristics

Over the Operating Range

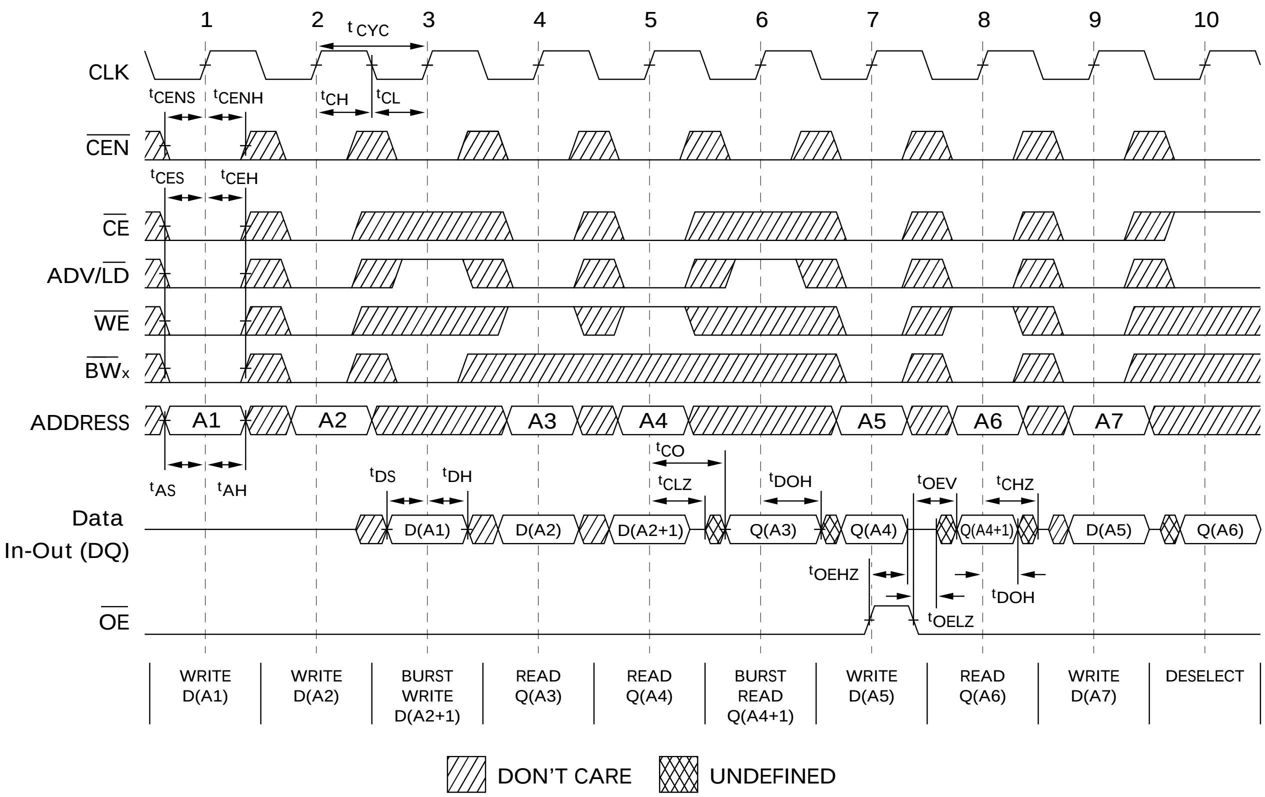
Parameter [16, 17]	Description	-200		Unit
		Min	Max	
t_{Power}[18]	V_{CC}(typical) to the first access read or write	1	–	ms
Clock				
t_{CYC}	Clock Cycle Time	5.0	–	ns
F_{MAX}	Maximum Operating Frequency	–	200	MHz
t_{CH}	Clock HIGH	2.0	–	ns
t_{CL}	Clock LOW	2.0	–	ns
Output Times				
t_{CO}	Data Output Valid After CLK Rise	–	3.2	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid	–	3.0	ns
t_{DOH}	Data Output Hold After CLK Rise	1.5	–	ns
t_{CHZ}	Clock to High Z[19, 20, 21]	–	3.0	ns
t_{CLZ}	Clock to Low Z[19, 20, 21]	1.3	–	ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High Z[19, 20, 21]	–	3.0	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low Z[19, 20, 21]	0	–	ns
Set up Times				
t_{AS}	Address Set up Before CLK Rise	1.4	–	ns
t_{DS}	Data Input Set up Before CLK Rise	1.4	–	ns
t_{CENS}	$\overline{CEN}$ Set up Before CLK Rise	1.4	–	ns
t_{WES}	$\overline{WE}$, $\overline{BW}_x$ Set up Before CLK Rise	1.4	–	ns
t_{ALS}	ADV/$\overline{LD}$ Set up Before CLK Rise	1.4	–	ns
t_{CES}	Chip Select Set up	1.4	–	ns
Hold Times				
t_{AH}	Address Hold After CLK Rise	0.4	–	ns
t_{DH}	Data Input Hold After CLK Rise	0.4	–	ns
t_{CENH}	$\overline{CEN}$ Hold After CLK Rise	0.4	–	ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_x$ Hold After CLK Rise	0.4	–	ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.4	–	ns
t_{CEH}	Chip Select Hold After CLK Rise	0.4	–	ns

Notes

16. Timing reference is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
17. Test conditions shown in (a) of Figure 2 on page 10 unless otherwise noted.
18. This part has a voltage regulator internally; tpower is the time power is supplied above $V_{DD(minimum)}$ initially, before a Read or Write operation can be initiated.
19. t_{CHZ}, t_{CLZ}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in (b) of Figure 2 on page 10. Transition is measured ±200 mV from steady state voltage.
20. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.
21. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 3. Read/Write/Timing [22, 23, 24]



Notes

22. For this waveform ZZ is tied low.
23. When CE is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When CE is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
24. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved).Burst operations are optional.

Switching Waveforms (continued)

Figure 4. NOP, STALL and DESELECT Cycles [25, 26, 27]

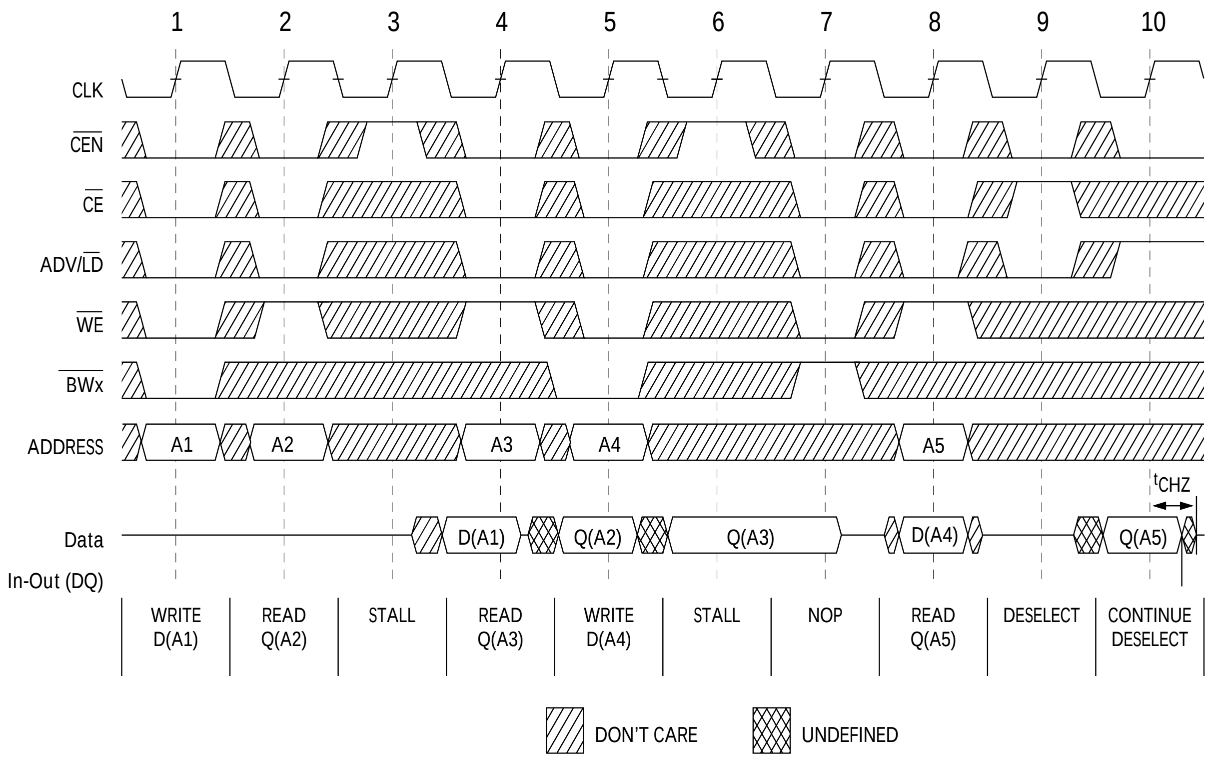
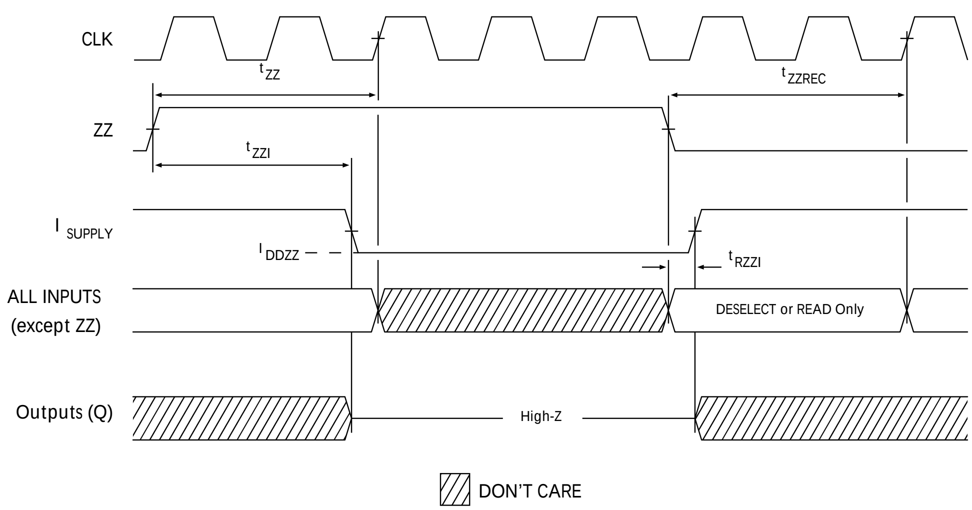


Figure 5. ZZ Mode Timing [28, 29]



Notes

25. For this waveform ZZ is tied low.
26. When CE is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When CE is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
27. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrated CEN being used to create a pause. A write is not performed during this cycle.
28. Device must be deselected when entering ZZ mode. See cycle description table for all possible signal conditions to deselect the device.
29. I/Os are in High Z when exiting ZZ sleep mode.

Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
200	CY7C1460SV33-200AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial

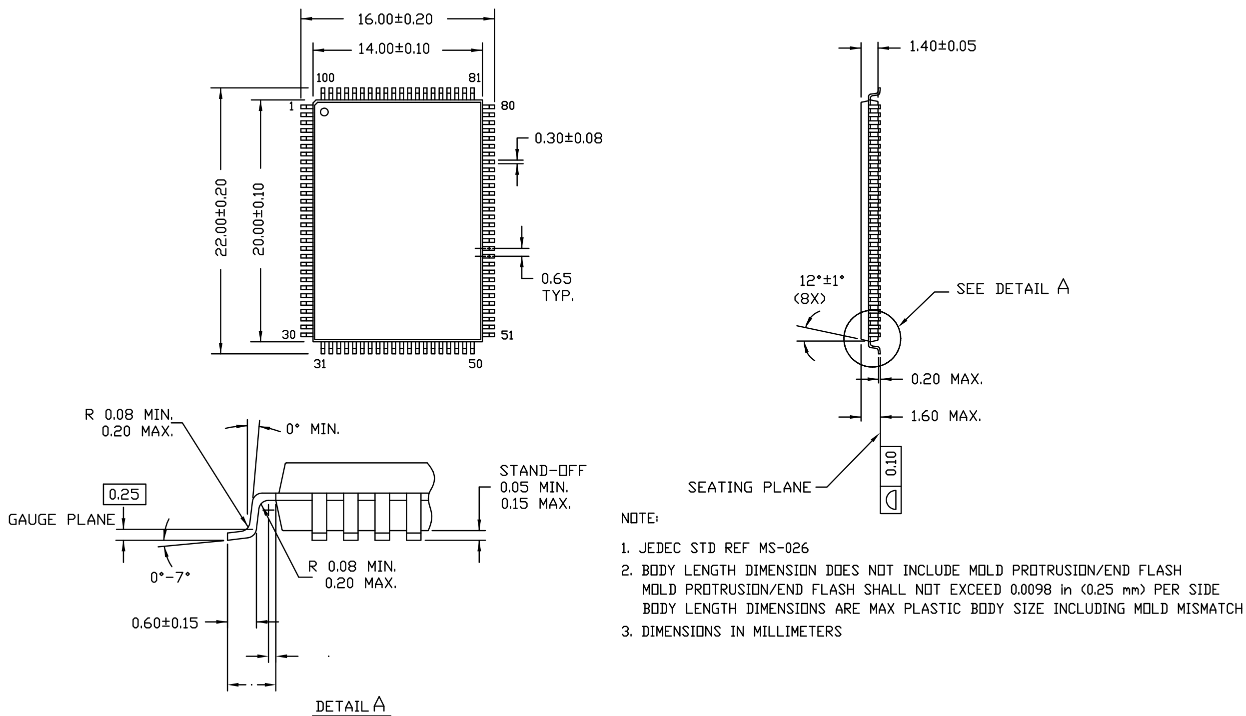
Ordering Code Definitions

CY 7 C 1460 S V33 - 200 A X C

- Temperature Range: C = Commercial
- Pb-free
- Package Type: A = 100-pin TQFP
- Frequency Range: 200 MHz
- V33 = 3.3 V
- Die Revision
- Part Identifier: 1460 = PL, 1Mb × 36 (36 Mb)
- Technology Code: C = CMOS
- Marketing Code: 7 = SRAM
- Company ID: CY = Cypress

Package Diagrams

Figure 6. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



51-85050 *E

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
Document Title: CY7C1460SV33, 36-Mbit (1M × 36) Pipelined SRAM with NoBL™ Architecture Document Number: 001-43803				
**	1897686	See ECN	VKN / AESA	New data sheet.
*A	2082846	See ECN	VKN	Changed status from Preliminary to Final.
*B	2950609	06/11/2010	NJY	Updated Functional Description (Removed CY7C1462SV33, and CY7C1464SV33 related information). Removed Logic Block Diagram – CY7C1462SV33. Removed Logic Block Diagram – CY7C1464SV33. Updated Pin Configurations (Removed CY7C1462SV33, and CY7C1464SV33 related information). Updated Functional Overview (Removed CY7C1462SV33, and CY7C1464SV33 related information). Updated Truth Table (Removed CY7C1462SV33, and CY7C1464SV33 related information). Removed Partial Write Cycle Description (Corresponding to CY7C1462SV33, and CY7C1464SV33). Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Removed CY7C1462SV33, and CY7C1464SV33 related information). Updated Identification Register Definitions (Removed CY7C1462SV33, and CY7C1464SV33 related information). Updated Boundary Scan Order (Removed CY7C1462SV33, and CY7C1464SV33 related information). Updated Ordering Information (Updated part numbers). Updated Package Diagrams. Added Sales, Solutions, and Legal Information.
*C	3221156	04/10/2011	NJY	Added Ordering Code Definitions. Updated Package Diagrams. Added Acronyms and Units of Measure. Updated to new template.
*D	3569737	04/02/2012	PRIT	Updated Features (Removed CY7C1462SV33, and CY7C1464SV33 related information). Updated Selection Guide (Removed 250 MHz, and 167 MHz frequencies related information). Updated Pin Configurations (Removed 165-ball FBGA package related information). Updated Pin Definitions (Removed JTAG related information). Removed IEEE 1149.1 Serial Boundary Scan (JTAG). Removed TAP Controller State Diagram. Removed TAP Controller Block Diagram. Removed TAP Timing. Removed TAP AC Switching Characteristics. Removed 3.3 V TAP AC Test Conditions. Removed 3.3 V TAP AC Output Load Equivalent. Removed 2.5 V TAP AC Test Conditions. Removed 2.5 V TAP AC Output Load Equivalent. Removed TAP DC Electrical Characteristics and Operating Conditions. Removed Identification Register Definitions. Removed Scan Register Sizes. Removed Identification Codes. Removed Boundary Scan Order (corresponding to 165-ball FBGA and 209-ball BGA).

Document History Page (continued)

Document Title: CY7C1460SV33, 36-Mbit (1M × 36) Pipelined SRAM with NoBL™ Architecture Document Number: 001-43803				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*D (cont.)	3569737	04/02/2012	PRIT	Updated Operating Range (Removed Industrial Range). Updated Electrical Characteristics (Removed 250 MHz, and 167 MHz frequencies related information). Updated Capacitance (Removed 165-ball FBGA, and 209-ball FBGA package related information). Updated Thermal Resistance (Removed 165-ball FBGA, and 209-ball FBGA package related information). Updated Switching Characteristics (Removed 250 MHz, and 167 MHz frequencies related information). Updated Package Diagrams (Removed 165-ball FBGA, and 209-ball FBGA package related information).
*E	3957732	04/08/2013	PRIT	No technical updates. Completing Sunset Review.
*F	5181018	03/18/2016	PRIT	Updated Package Diagrams: spec 51-85050 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

cypress.com/psoc

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/support