

NTP45N06, NTB45N06

Power MOSFET 45 Amps, 60 Volts N-Channel TO-220 and D²PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Higher Current Rating
- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Tighter V_{SD} Specification
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge
- Pb-Free Packages are Available

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	60	Vdc
Drain-to-Gate Voltage ($R_{GS} = 10\text{ M}\Omega$)	V_{DGR}	60	Vdc
Gate-to-Source Voltage	V_{GS}	± 20	Vdc
– Continuous	V_{GS}	± 30	
– Non-Repetitive ($t_p \leq 10\text{ ms}$)			
Drain Current	I_D	45	Adc
– Continuous @ $T_A = 25^\circ\text{C}$	I_D	30	
– Continuous @ $T_A = 100^\circ\text{C}$	I_{DM}	150	Apk
– Single Pulse ($t_p \leq 10\text{ }\mu\text{s}$)			
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	125	W
Derate above 25°C		0.83	W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)		3.2	W
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2)		2.4	W
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to $+175$	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50\text{ Vdc}$, $V_{GS} = 10\text{ Vdc}$, $R_G = 25\text{ }\Omega$, $I_{L(pk)} = 40\text{ A}$, $L = 0.3\text{ mH}$, $V_{DS} = 60\text{ Vdc}$)	E_{AS}	240	mJ
Thermal Resistance	$R_{\theta JC}$	1.2	$^\circ\text{C/W}$
– Junction-to-Case	$R_{\theta JA}$	46.8	
– Junction-to-Ambient (Note 1)	$R_{\theta JA}$	63.2	
– Junction-to-Ambient (Note 2)			
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1 in pad size, (Cu Area 1.127 in²).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in²).

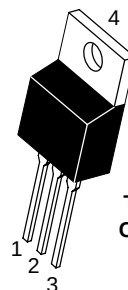
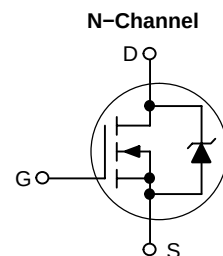


ON Semiconductor®

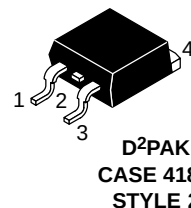
<http://onsemi.com>

45 AMPERES, 60 VOLTS

$R_{DS(on)} = 26\text{ m}\Omega$

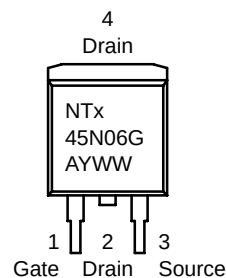
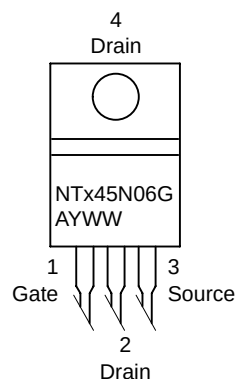


**TO-220AB
CASE 221A
STYLE 5**



**D²PAK
CASE 418B
STYLE 2**

MARKING DIAGRAMS & PIN ASSIGNMENTS



NTx45N06 = Device Code
x = B or P
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NTP45N06, NTB45N06

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	60 –	70 57	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	±100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	2.0 –	2.8 7.2	4.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 10 Vdc, I _D = 22.5 Adc)	R _{DS(on)}	–	21	26	mΩ
Static Drain-to-Source On-Voltage (Note 3) (V _{GS} = 10 Vdc, I _D = 45 Adc) (V _{GS} = 10 Vdc, I _D = 22.5 Adc, T _J = 150°C)	V _{DS(on)}	– –	0.93 0.93	1.4 –	Vdc
Forward Transconductance (Note 3) (V _{DS} = 8.0 Vdc, I _D = 12 Adc)	g _{FS}	–	16.6	–	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	1224	1725	pF
Output Capacitance		C _{oss}	–	345	485	
Transfer Capacitance		C _{rss}	–	76	160	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{DD} = 30 Vdc, I _D = 45 Adc, V _{GS} = 10 Vdc, R _G = 9.1 Ω) (Note 3)	t _{d(on)}	–	10	25	ns
Rise Time		t _r	–	101	200	
Turn-Off Delay Time		t _{d(off)}	–	33	70	
Fall Time		t _f	–	106	220	
Gate Charge	(V _{DS} = 48 Vdc, I _D = 45 Adc, V _{GS} = 10 Vdc) (Note 3)	Q _T	–	33	46	nC
		Q ₁	–	6.4	–	
		Q ₂	–	15	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 45 Adc, V _{GS} = 0 Vdc) (Note 3) (I _S = 45 Adc, V _{GS} = 0 Vdc, T _J = 150°C)	V _{SD}	– –	1.08 0.93	1.2 –	Vdc
Reverse Recovery Time	(I _S = 45 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs) (Note 3)	t _{rr}	–	53.1	–	ns
		t _a	–	36	–	
		t _b	–	16.9	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.087	–	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping [†]
NTP45N06	TO-220AB	50 Units / Rail
NTP45N06G	TO-220AB (Pb-Free)	50 Units / Rail
NTB45N06	D ² PAK	50 Units / Rail
NTB45N06G	D ² PAK (Pb-Free)	50 Units / Rail
NTB45N06T4	D ² PAK	800 Units / Tape & Reel
NTB45N06T4G	D ² PAK (Pb-Free)	800 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTP45N06, NTB45N06

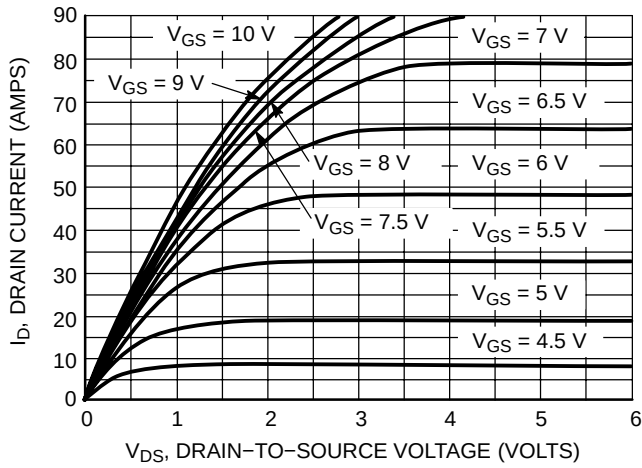


Figure 1. On-Region Characteristics

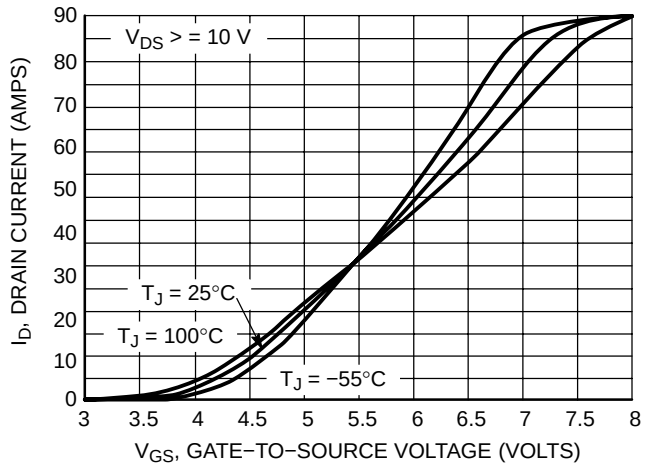


Figure 2. Transfer Characteristics

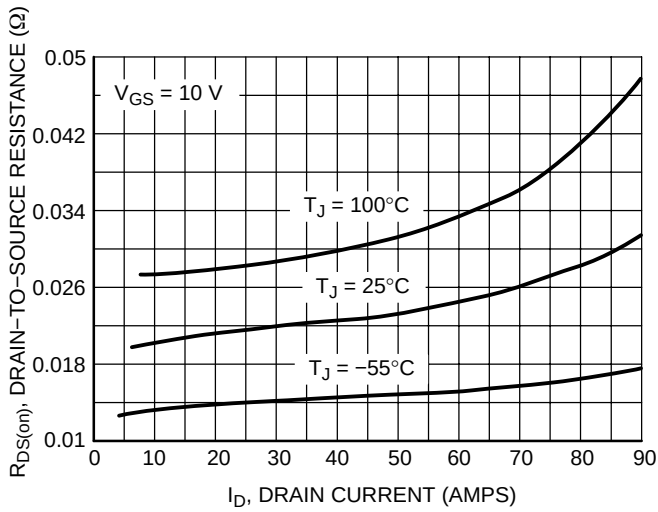


Figure 3. On-Resistance vs. Gate-to-Source Voltage

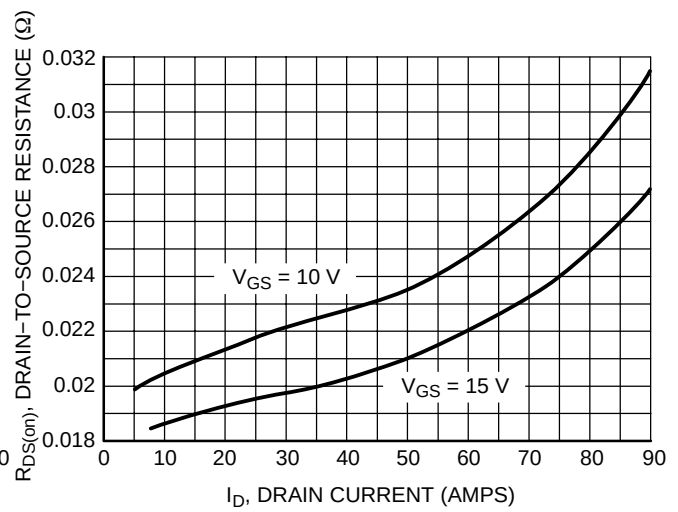


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

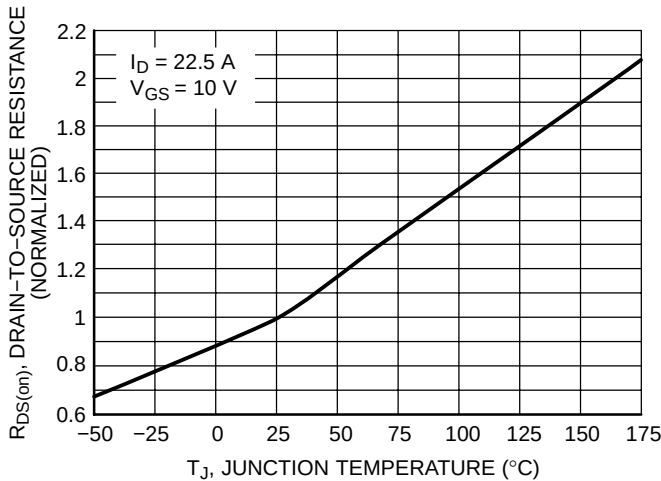


Figure 5. On-Resistance Variation with Temperature

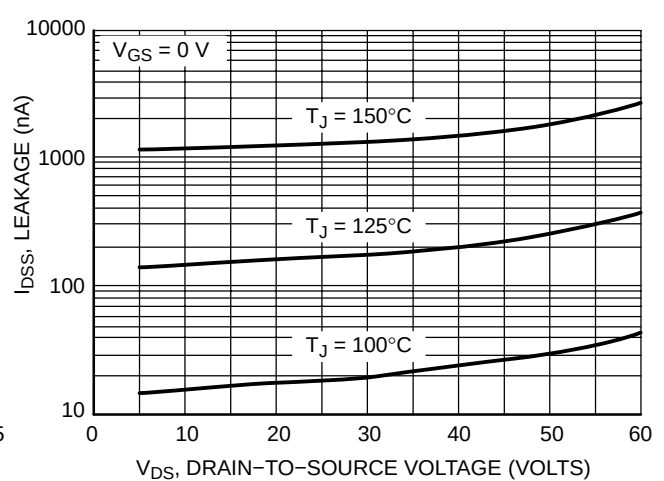


Figure 6. Drain-to-Source Leakage Current vs. Voltage

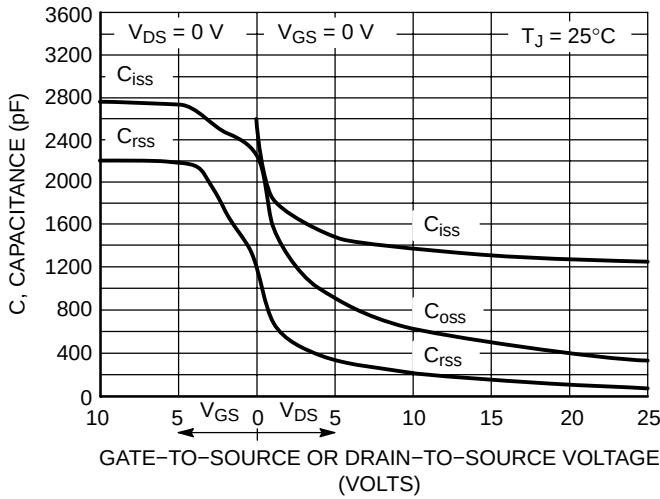


Figure 7. Capacitance Variation

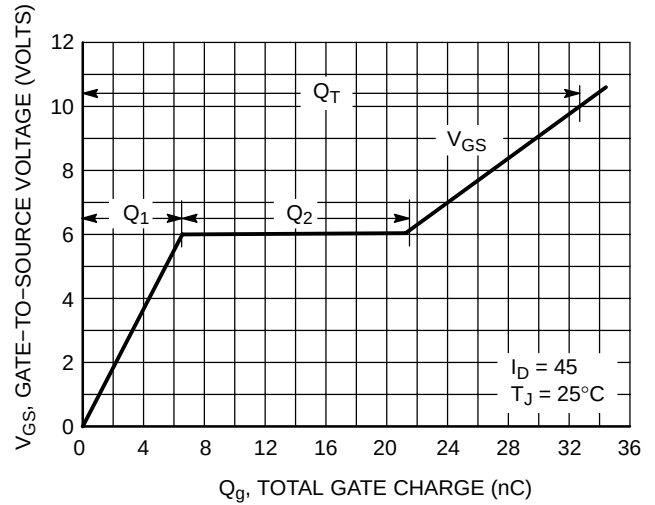


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

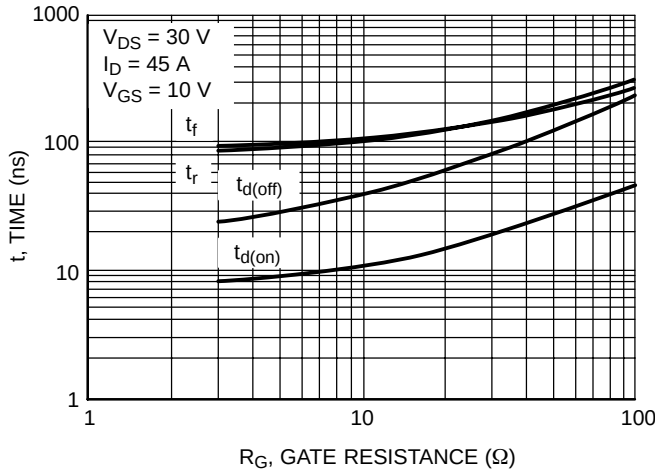


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

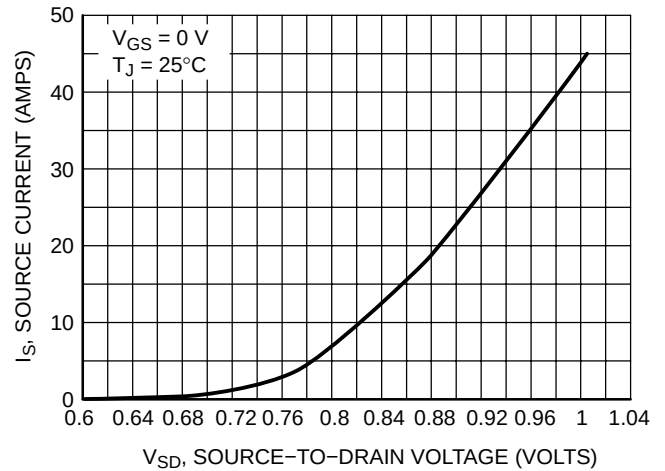


Figure 10. Diode Forward Voltage vs. Current

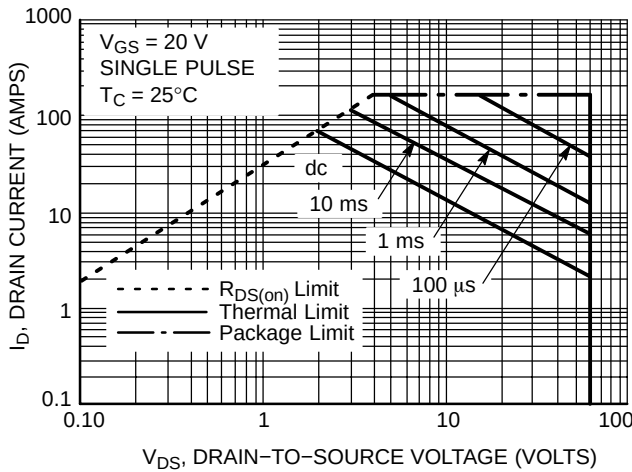


Figure 11. Maximum Rated Forward Biased Safe Operating Area

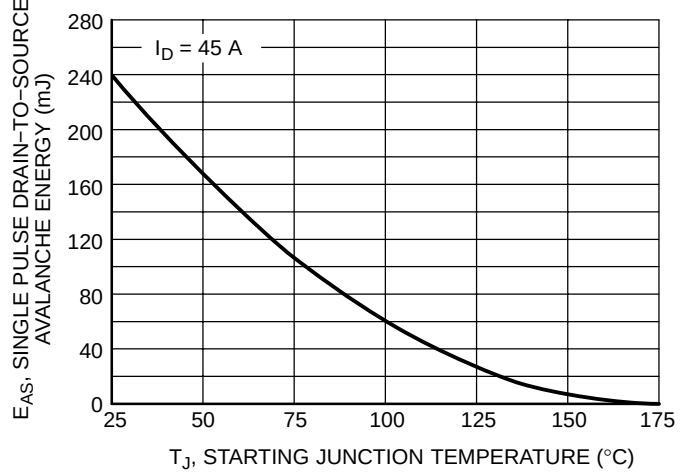


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTP45N06, NTB45N06

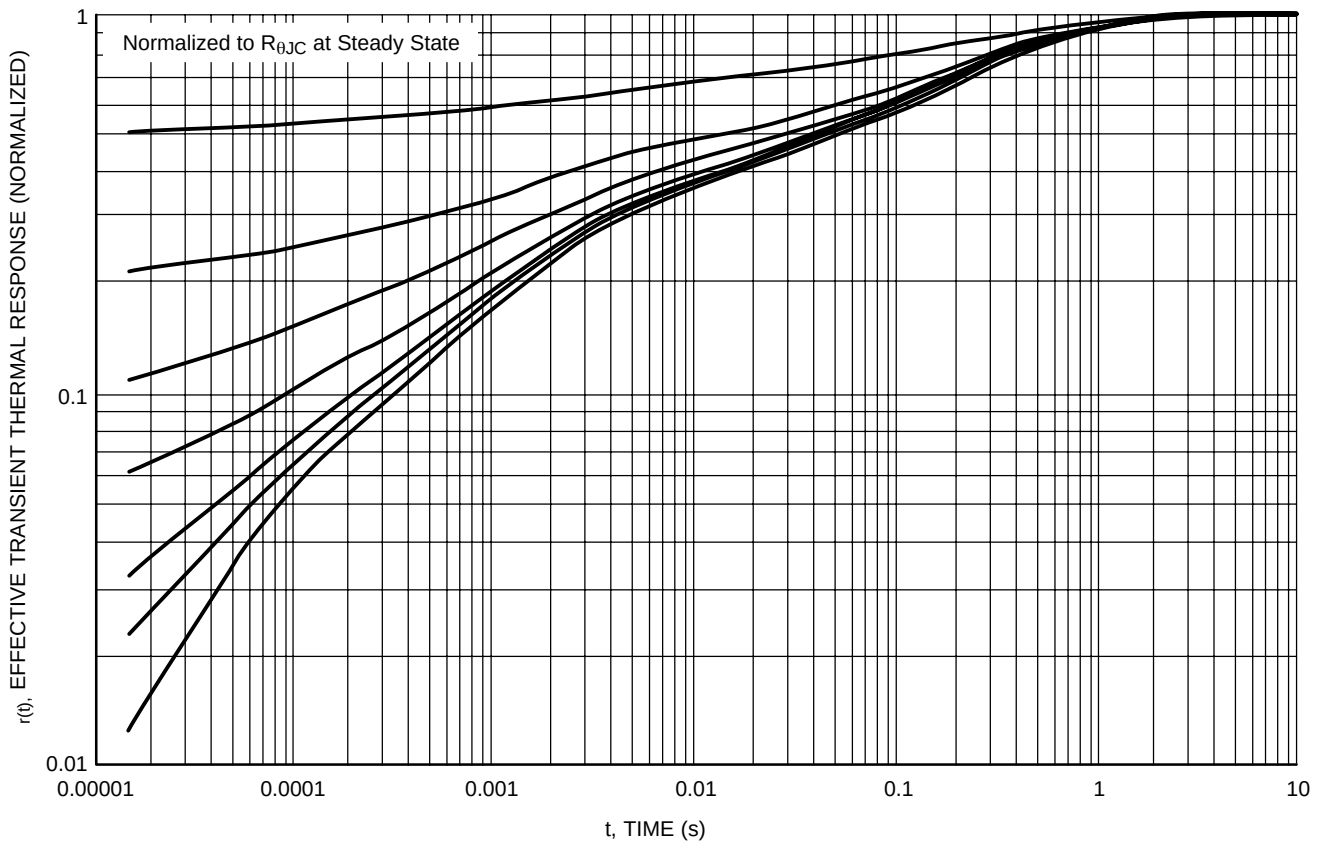


Figure 13. Thermal Response

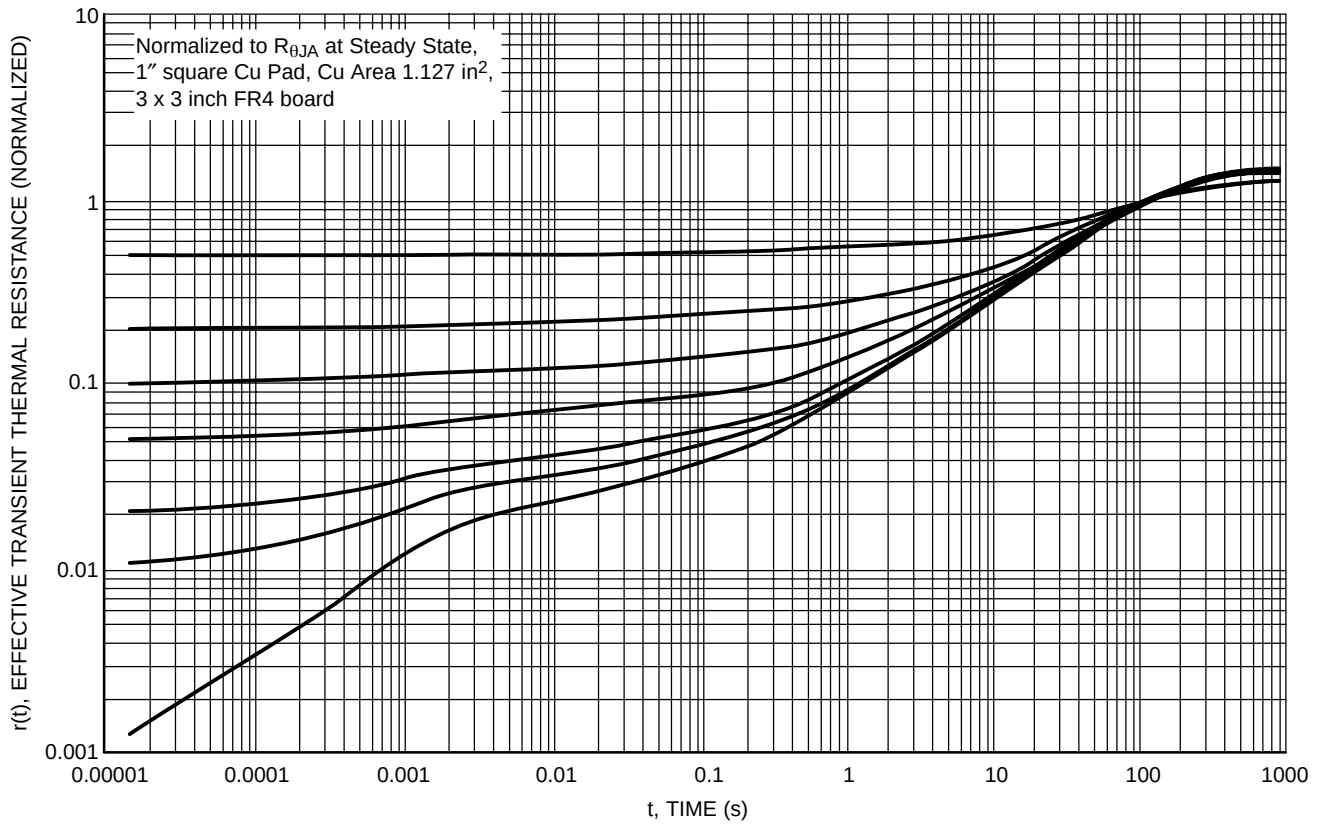
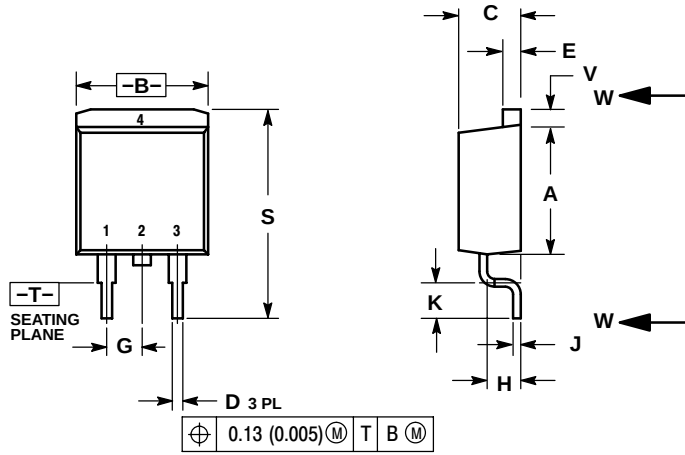


Figure 14. Thermal Response

NTP45N06, NTB45N06

PACKAGE DIMENSIONS

D²PAK
CASE 418B-04
ISSUE J



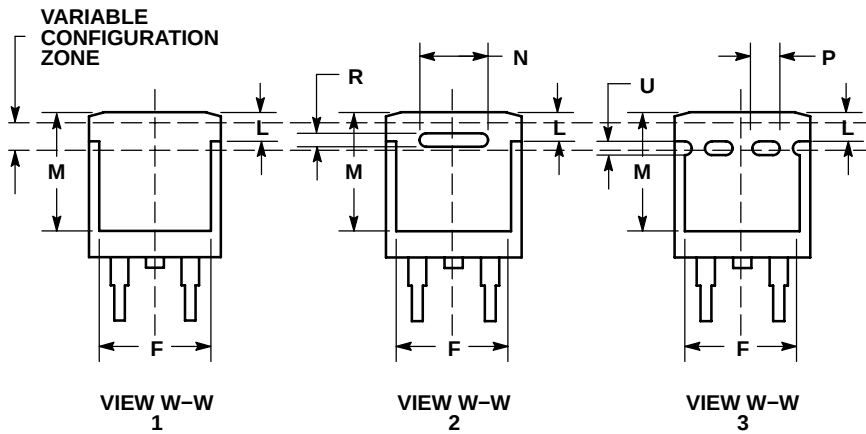
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

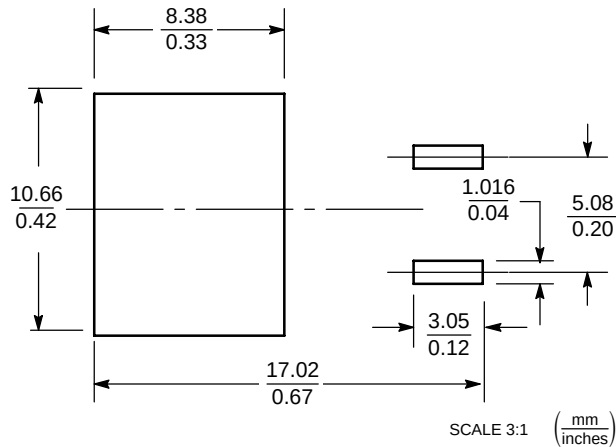
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:

- PIN 1: GATE
2: DRAIN
3: SOURCE
4: DRAIN



SOLDERING FOOTPRINT*

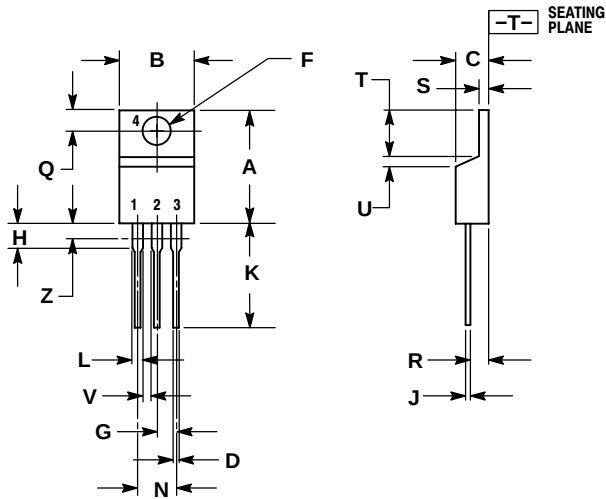


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTP45N06, NTB45N06

PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.

NTP45N06/D